

Bipolar Modelling for ESD Circuits Design

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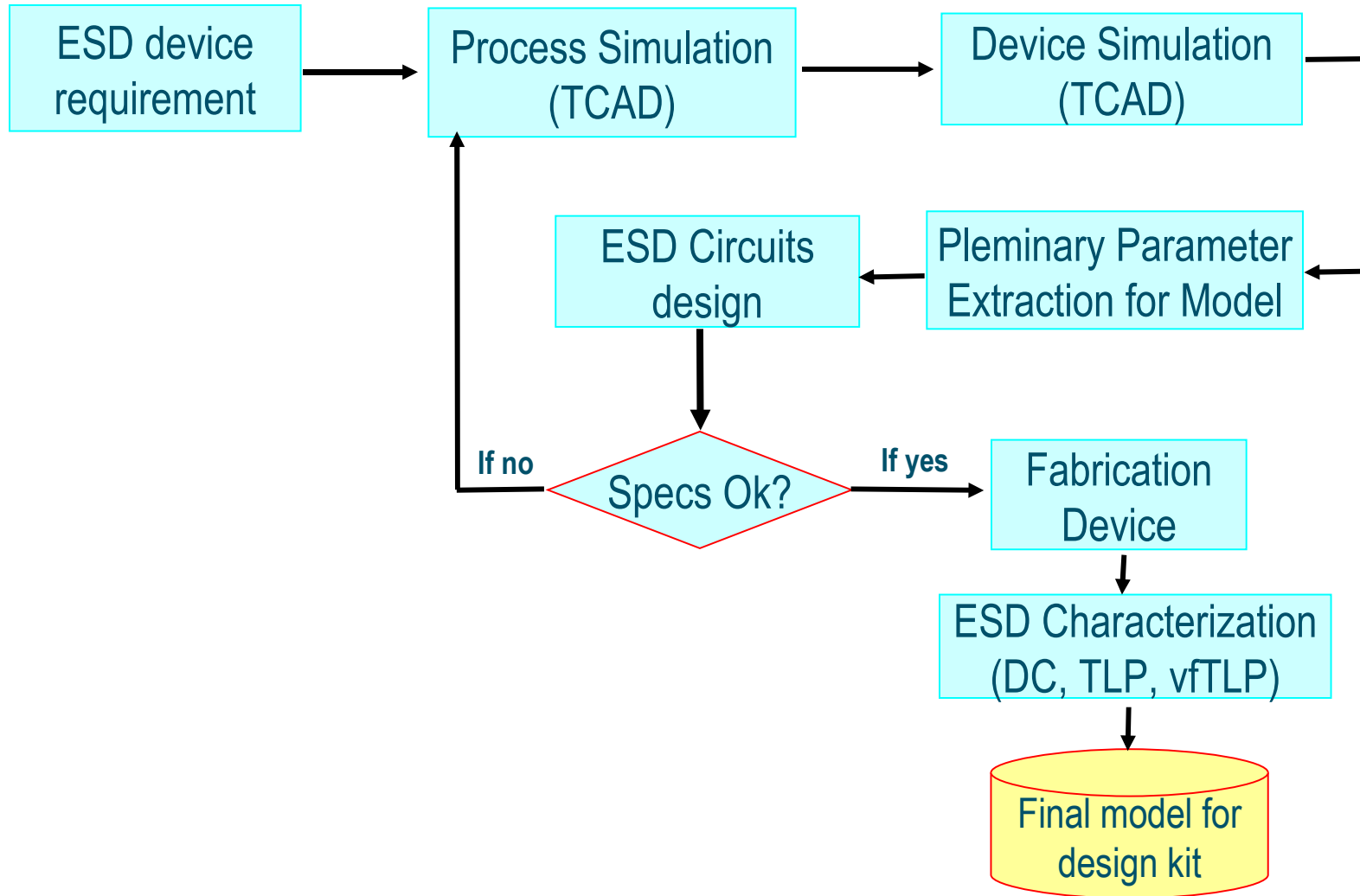
Bipolar Arbeitskreis, 30 October 2008, Hamburg, Germany

a leap ahead

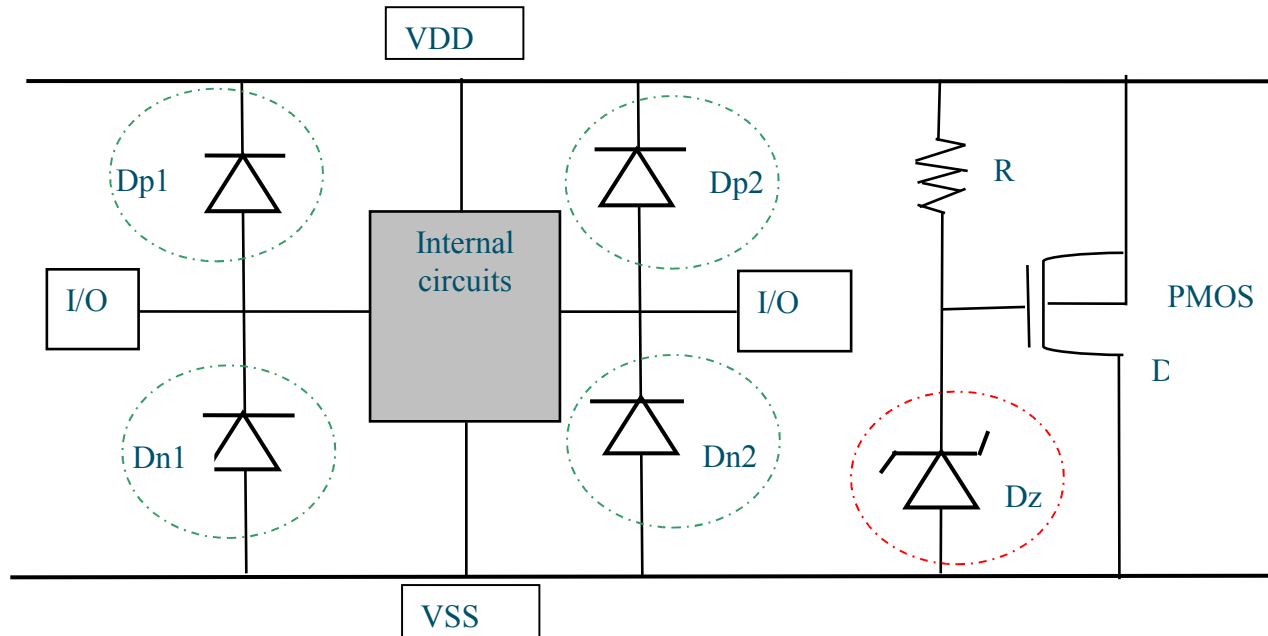
Outline

- Flow of ESD device optimization and modelling
- Diode/Bipolar used as ESD Protection Device
- Diode Overshoot Measurements
- Bipolar B-E Breakdown Model
- Snapback phenomena of NMOS MOSFETs
- Summary

Flow of ESD Device Optimization and Modelling



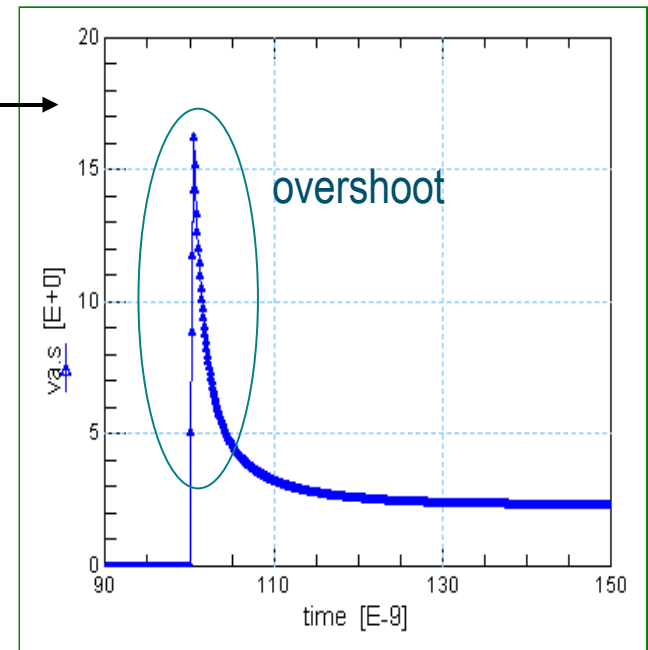
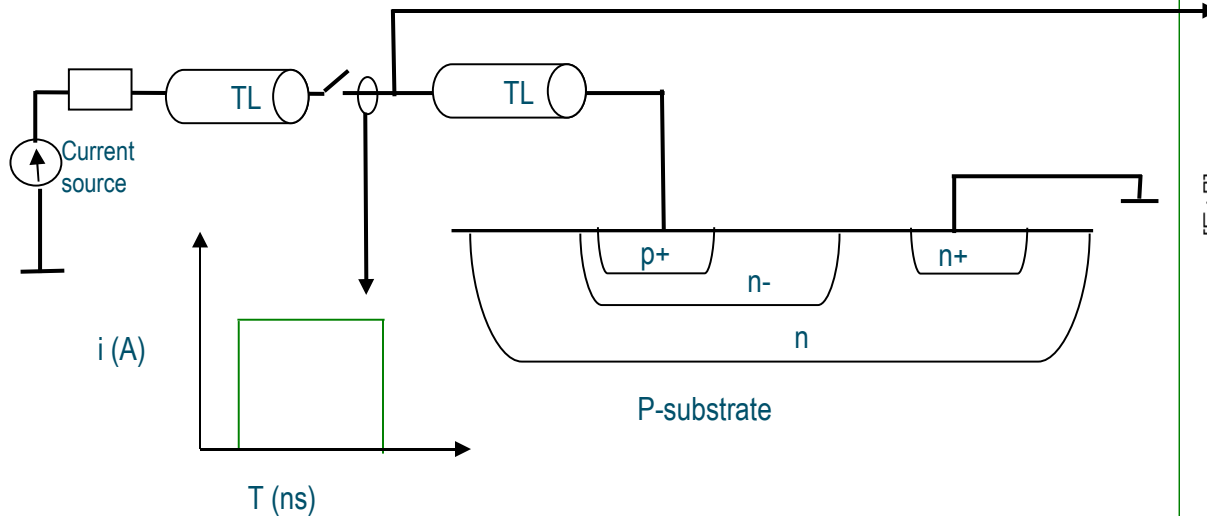
Diode or Bipolar Used in ESD Protection Circuits



- Diode Dp1, Dn1 and Dp2, Dn2 are used as ESD protection, and used in the forward operation
- Diode Dz is used as trigger device for MOSFETs for ESD protection, and used in reverse operation

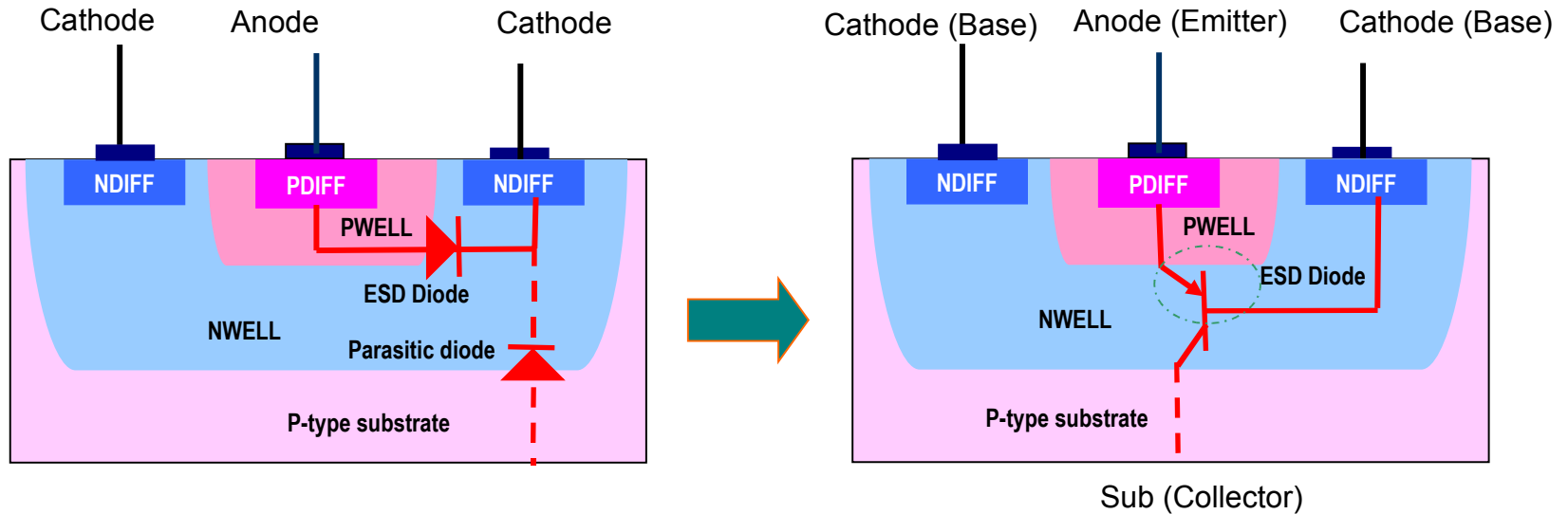
Forward Diode Measurement

Transmission Line Pulsing (TLP) Measurement



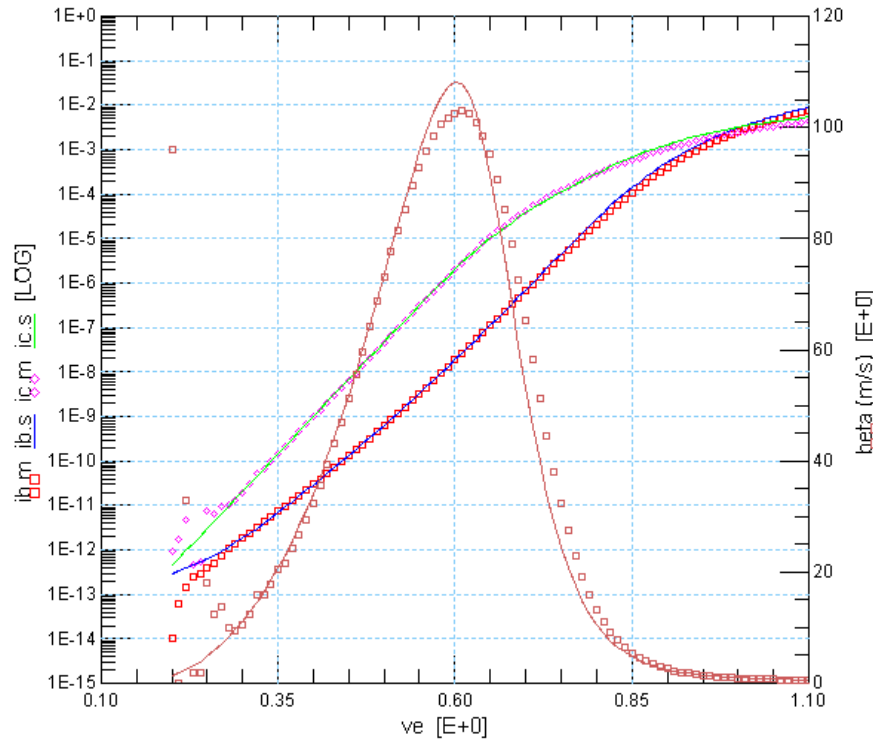
- Forward diode measurement in TLP instrument
- Measurement accuracy for Overshoot ?
- How to calibrate the systems ?
- How to get a precise fast current ramp ?

Modeling Reverse Diode, Dz



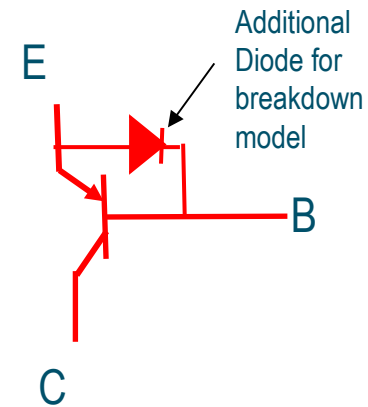
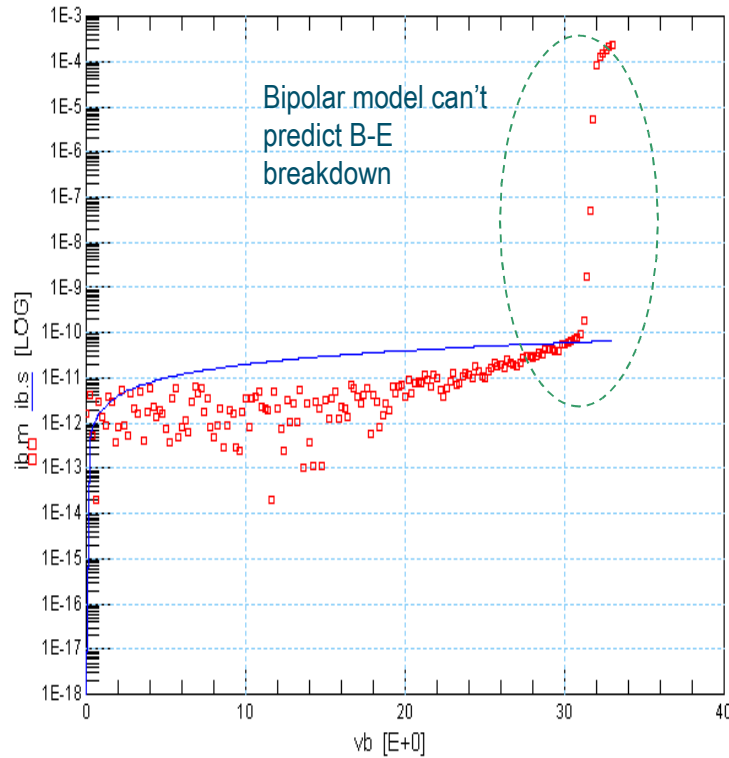
- Device cross section shows a actual diode and a parasitic diode at substrate
- Consider as a bipolar device to model both actual diode and parasitic diode

Forward Model



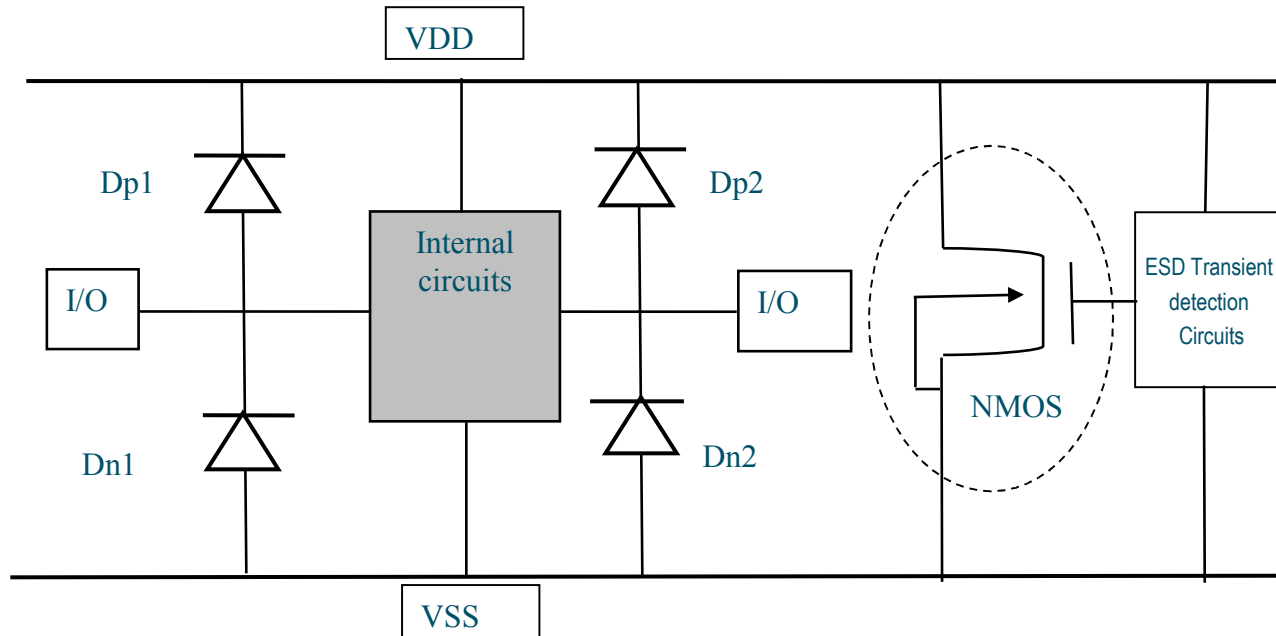
- Forward characteristics shows very good Bipolar action instead of diode.
- Measurement data has very good fit with a Bipolar Model

Base-Emitter Breakdown Modelling



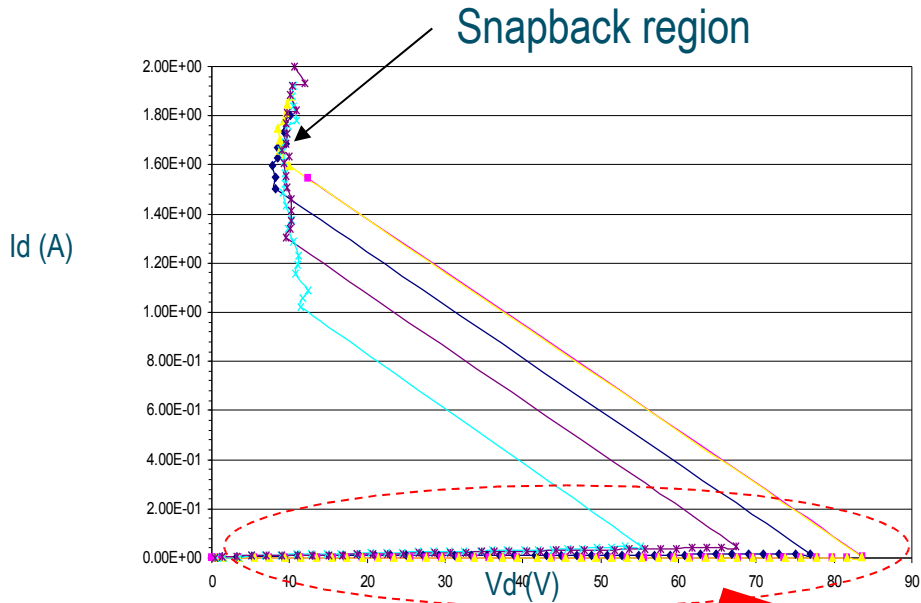
- Bipolar model is not suitable for B-E breakdown model required for ESD Model
- Required B-E avalanche effect inside the Bipolar Model
- Alternatively, an extra diode in parallel between B-E may necessary to model breakdown

MOSFET Used in ESD Protection

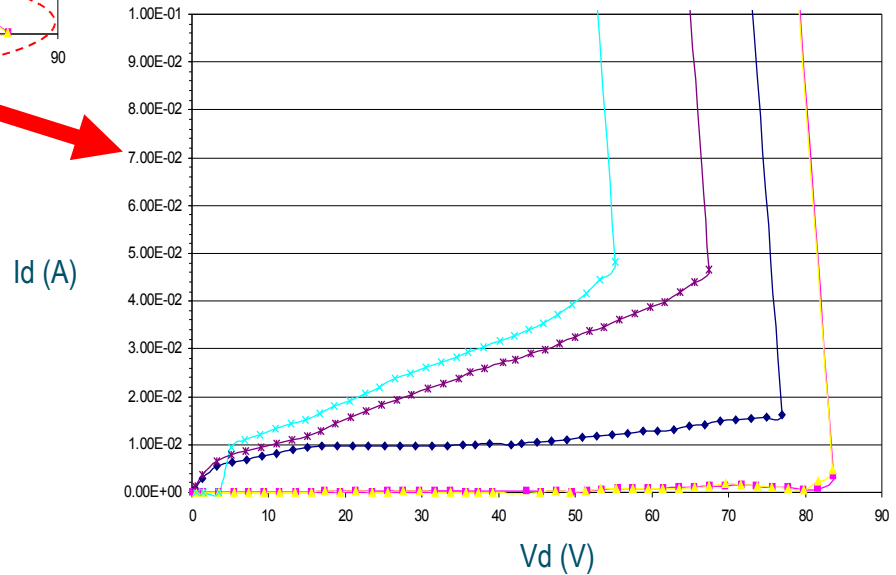


- MOSFET used as central clamp ESD protection
- Parasitic Bipolar in MOSFET play the role during ESD event

Snapback Drain Current in HVNMOS50T

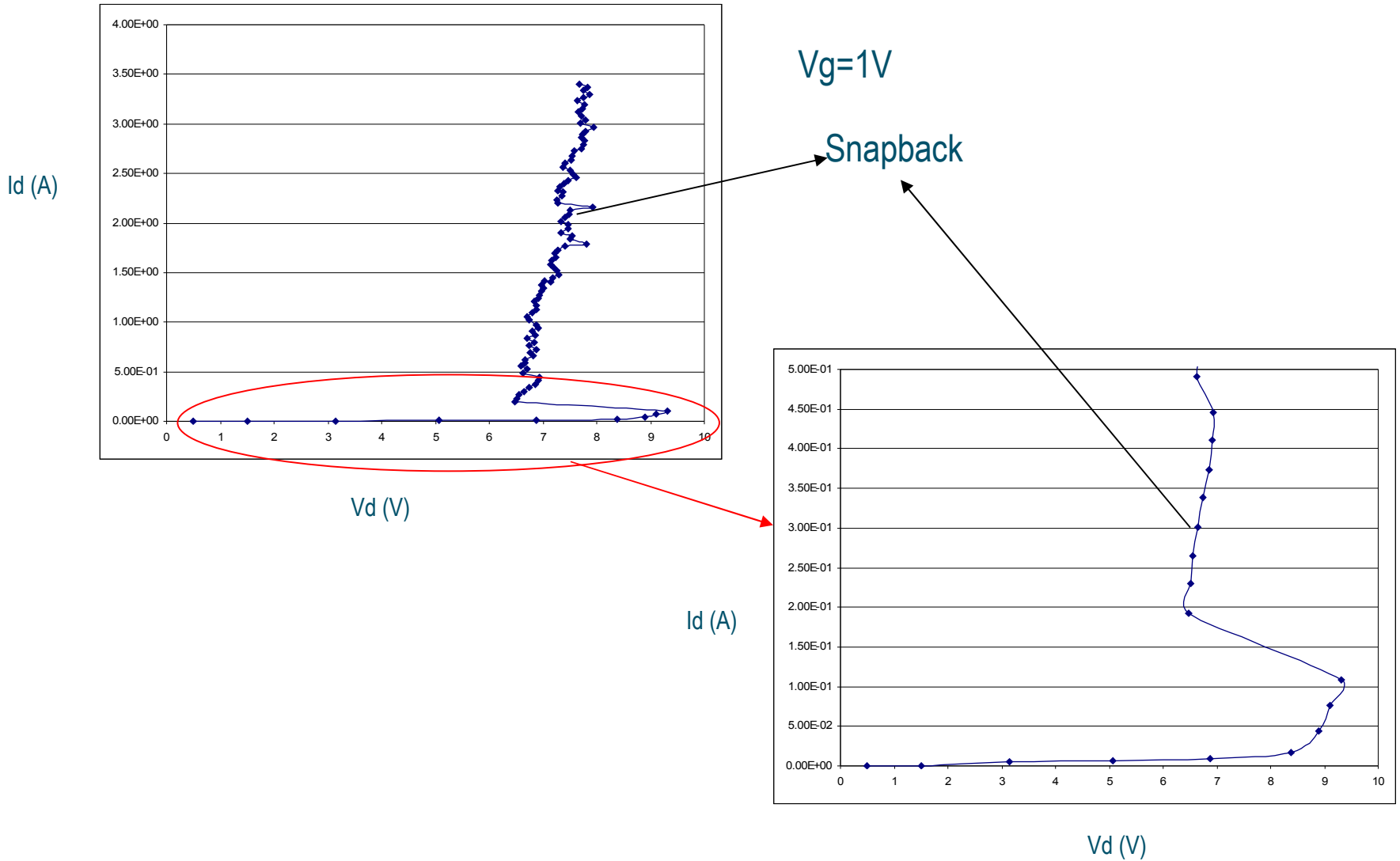


- ▲— Gate open
- Gate shorted to source
- ◆— $V_g=1.5V$
- *— $V_g=3V$
- ×— $V_g=6V$



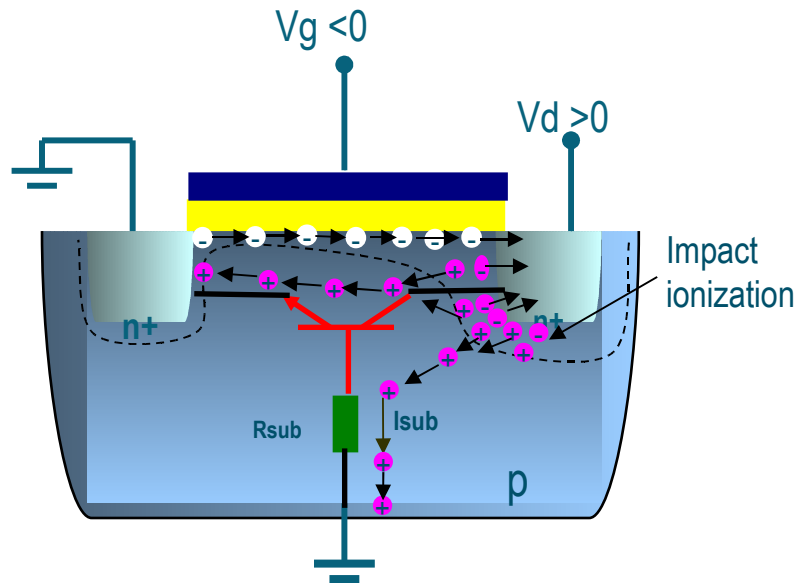
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Snapback Drain Current in NMOS5



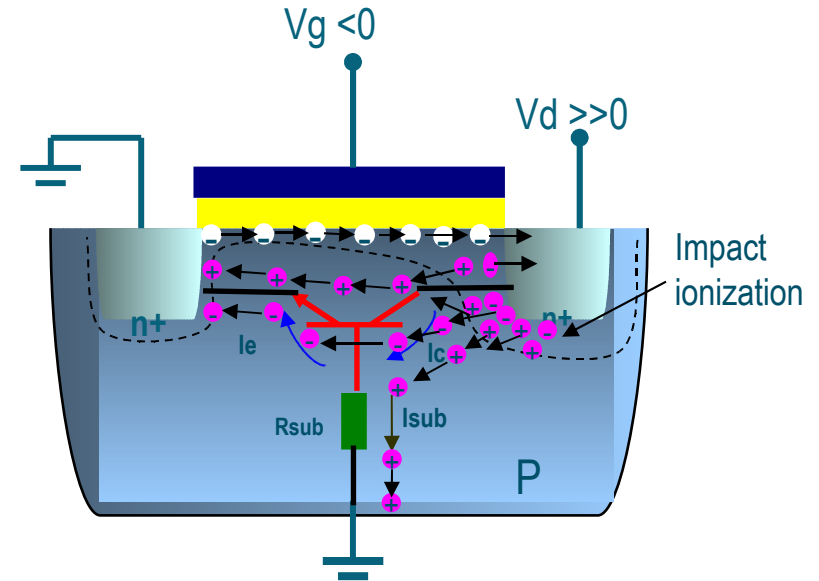
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Why Snapback ?



Parasitic NPN transistor turns off

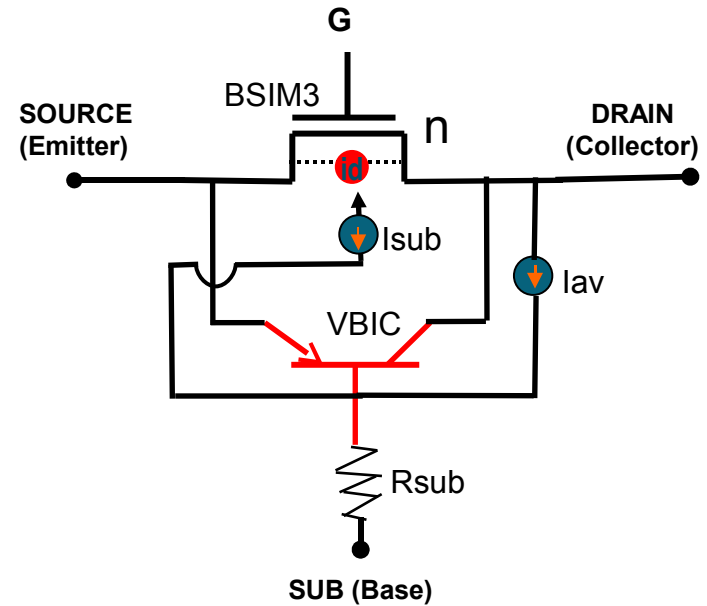
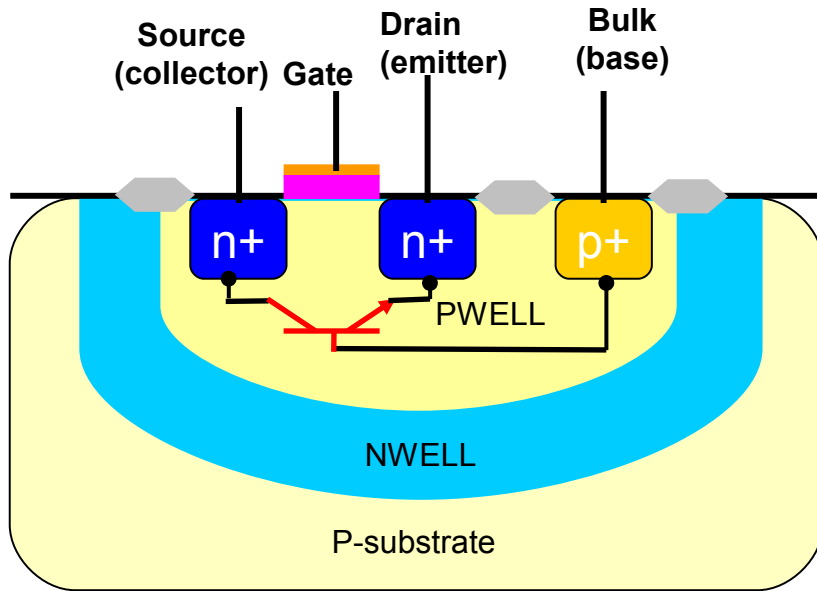
- Holes created by Impact Ionization in Drain-to-Bulk depletion layer are injected into substrate



Parasitic NPN transistor turns on

- Parasitic NPN transistor turns on when the voltage drop cross R_{sub} ($I_{sub} \times R_{sub}$) reaches $\sim 0.7V$
- Electrons emitted when S-B junction is forward biased

Composite Model NMOSFET and Lateral Bipolar



BSIM:
$$I_{sub} = \left[\alpha_{11} + \frac{\alpha_{10}}{L_{eff}} \right] * [V_{ds} - V_{dseff}] \exp\left(-\frac{\beta_{00}}{v_{ds} - V_{dseff}} \right) * I_d$$

VBIC:
$$I_{av} = I_c * AVC1 * (PC - V_{bci}) * \exp^{-AVC2(PC - V_{bci})^{(MC-1)}}$$

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Summary

- Details flow of ESD device to model generation
- Basic application of Diode and Bipolar used in ESD circuits
- Forward overshoot measurement problem
- Forward diode needs a B-E avalanche breakdown model
- Snapback results of MOSFETs in ESD events