Thermal impedance measurement and modeling including thermal coupling

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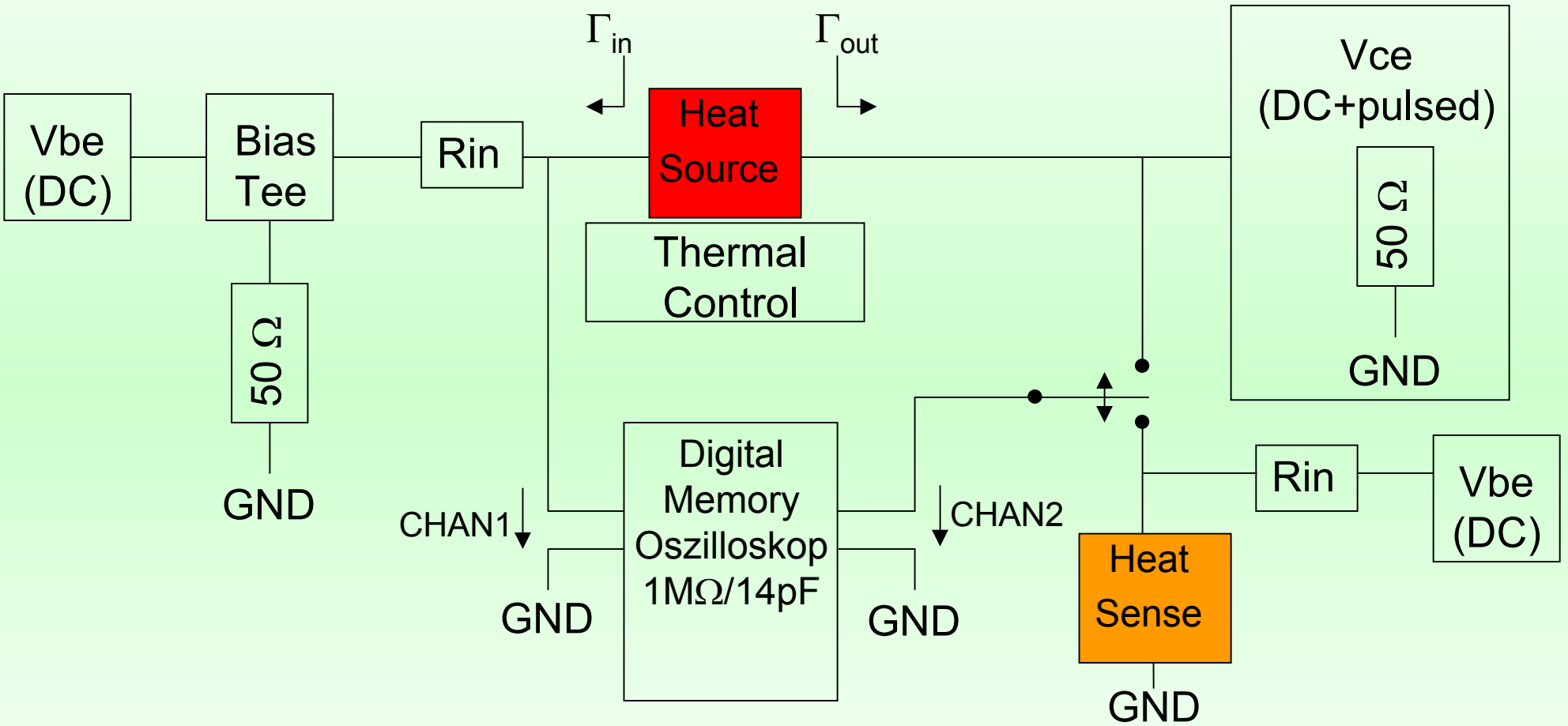
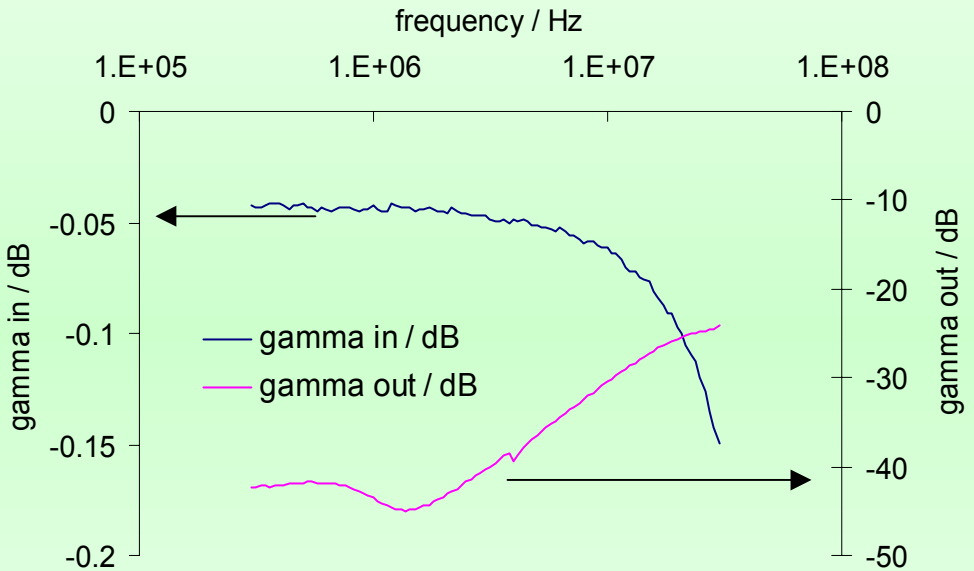
- pulsed measurement setup
- on wafer test-structure
- modeling of thermal network
- parameter extraction of thermal network
- influence and modeling of a thermal shunt

measurement setup



measured Γ_{in} / Γ_{out}

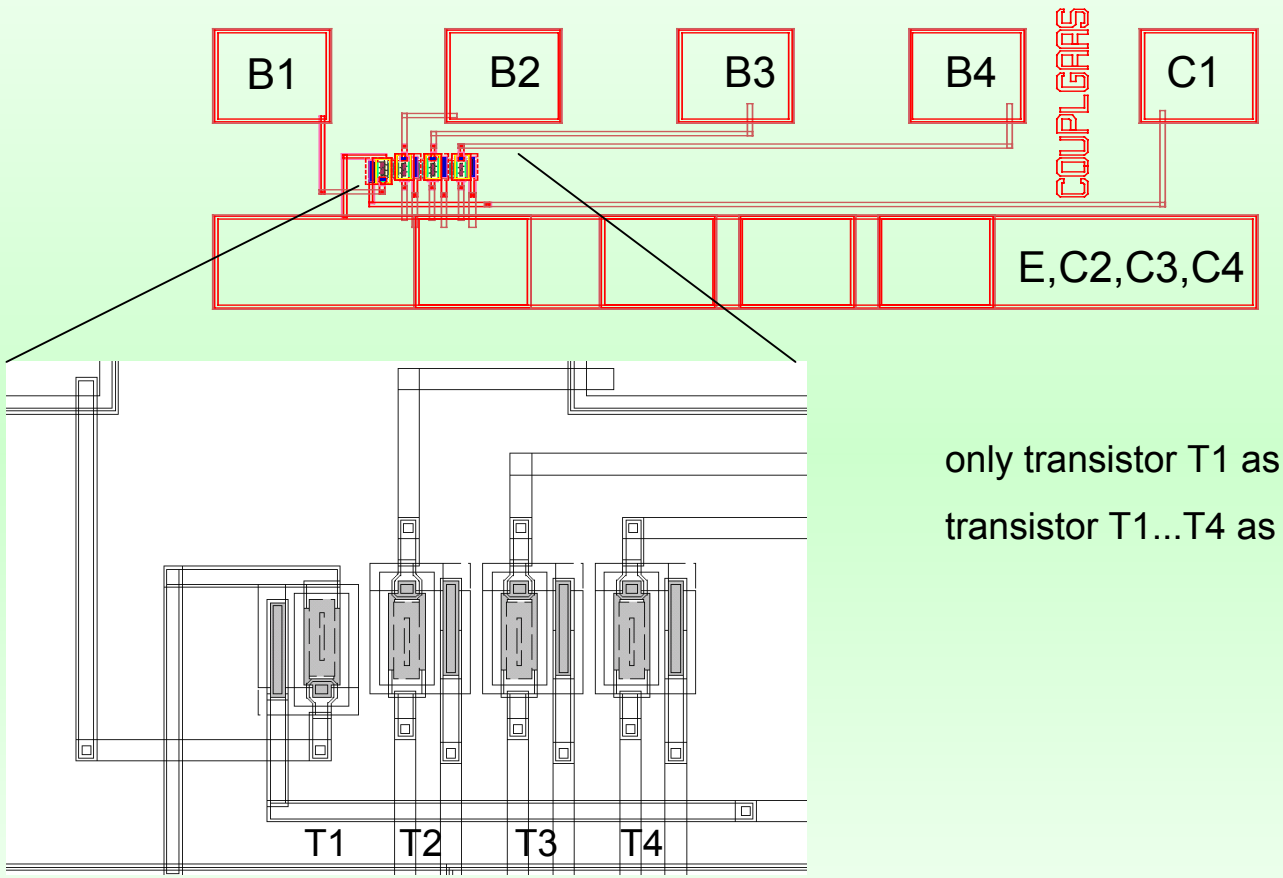


-input as high impedance current source

-output with 50 Ohm to calculate

time dependent collector current from Vce

on wafer test structure



only transistor T1 as heat source

transistor T1...T4 as heat sense

measured pulsed waveforms of the heat source

pulsed operating conditions for GaAs HBT at T_1=15°C and T_2=30°C

Vbe(DC)=4.09 V

Ib=80 µA

Vcedc=1.5 V

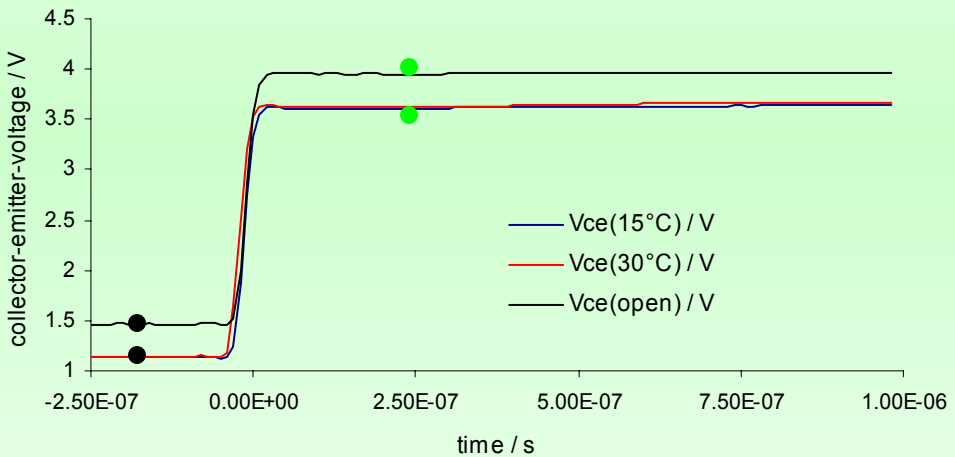
Vcestep=2.5 V

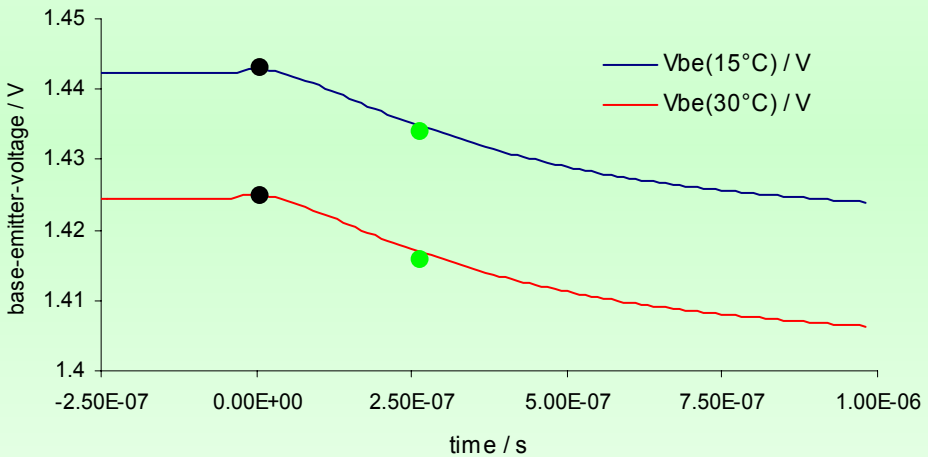
Three measurements:

-DUT at T1

-DUT at T2

-measurement setup without DUT (open)





- steady state
- after the pulse as function of time

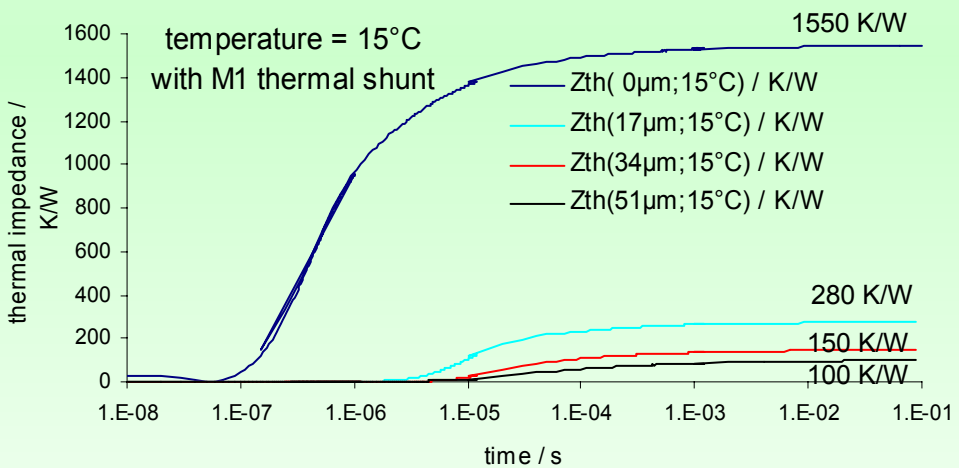
thermal impedance calculation

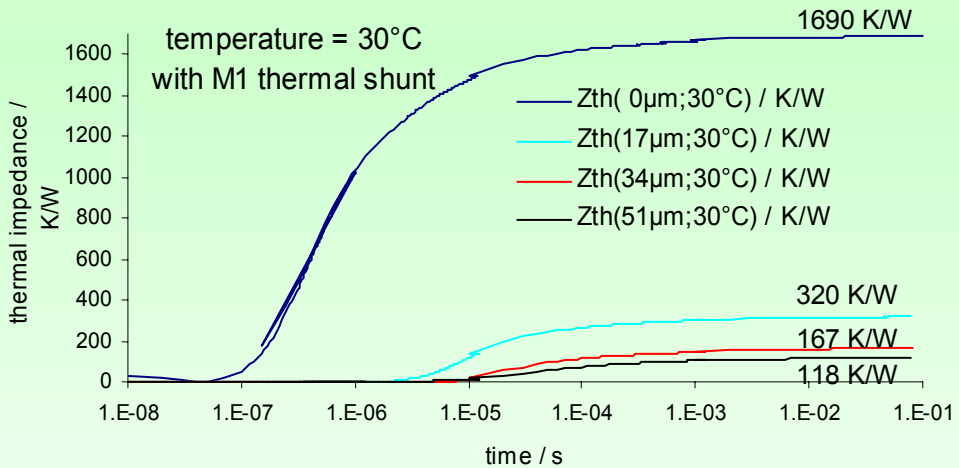
$$Z_{th}(T,t) = \frac{\Delta T(T,t)}{\Delta P_{diss}(T,t)}$$

$$\Delta T(T_1,t) = \frac{V_{be}(T_1,0ns) - V_{be}(T_1,t)}{V_{be}(T_1,t) - V_{be}(T_2,t)} \cdot (T_2 - T_1)$$

$$\Delta T(T_2,t) = \frac{V_{be}(T_2,0ns) - V_{be}(T_2,t)}{V_{be}(T_1;t) - V_{be}(T_2;t)} \cdot (T_2 - T_1)$$

$$\Delta P_{diss}(T,t) = \frac{V_{ce}(T,t)\cdot(V_{ce}(open,t) - V_{ce}(T,t)) - V_{ce}(T,-200ns)\cdot(V_{ce}(open,-200ns) - V_{ce}(T,-200ns))}{50\Omega}$$





thermal impedance modeling - 4 finger FET

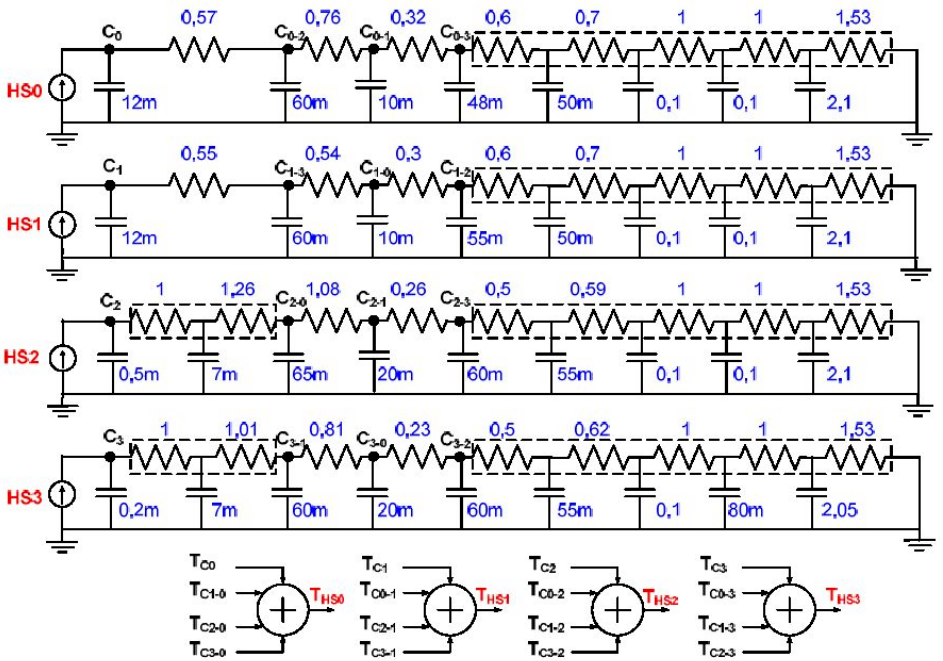


Fig. 9. Accurate dynamic CTM for four heat sources.

From W.Habra, et. Al., "New electro-thermal modeling tools for automotive power circuits design optimization", pp. 86.89, BCTM2007

some open questions:

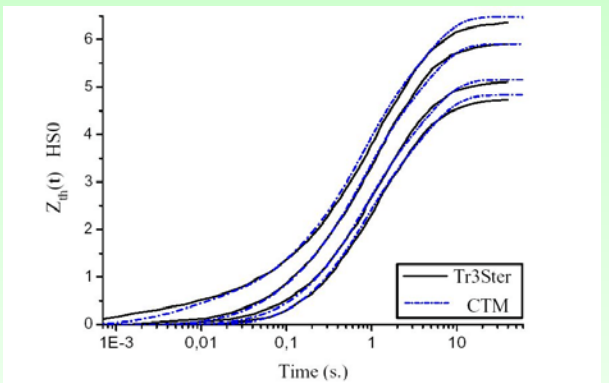
parameter extraction?

physical meaning of the parameters?

where is the thermal coupling?

extension strategy if applying new heat sources?

after "global" optimization excellent results comparing measured and simulated data



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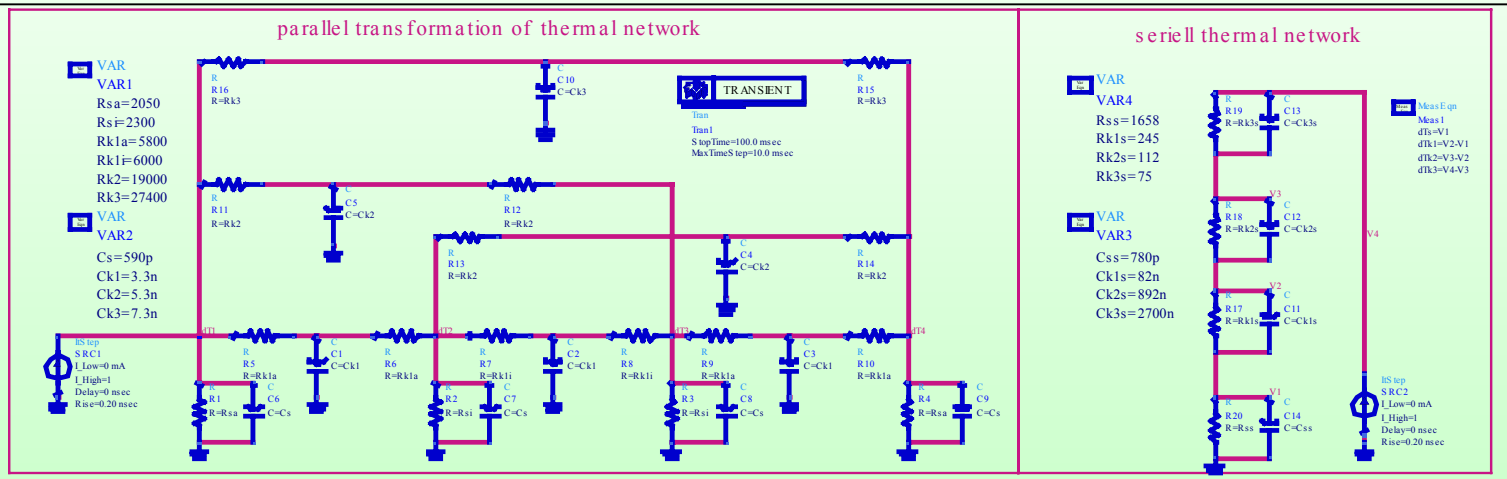
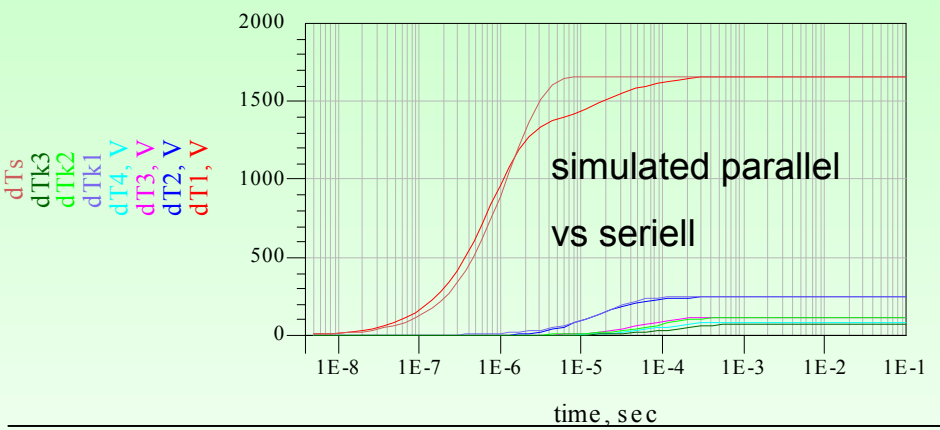
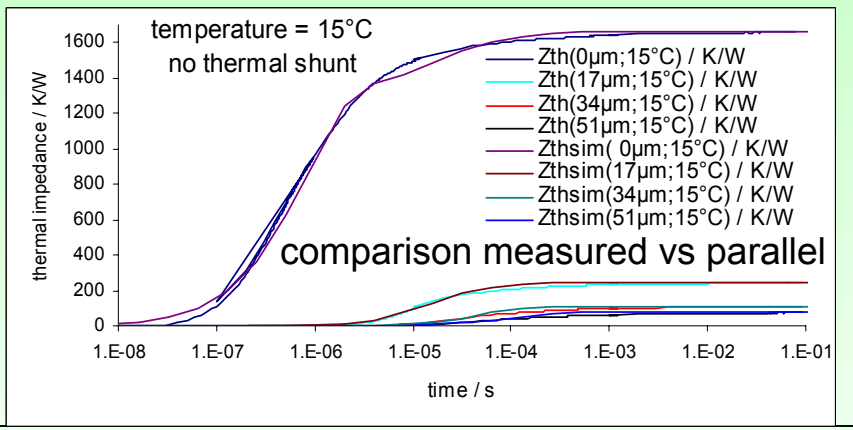
thermal equivalent circuit
parallel vs seriell

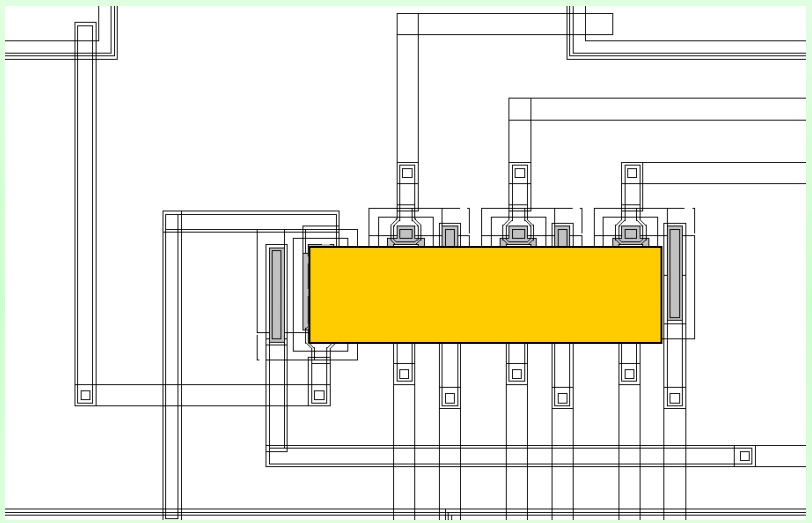


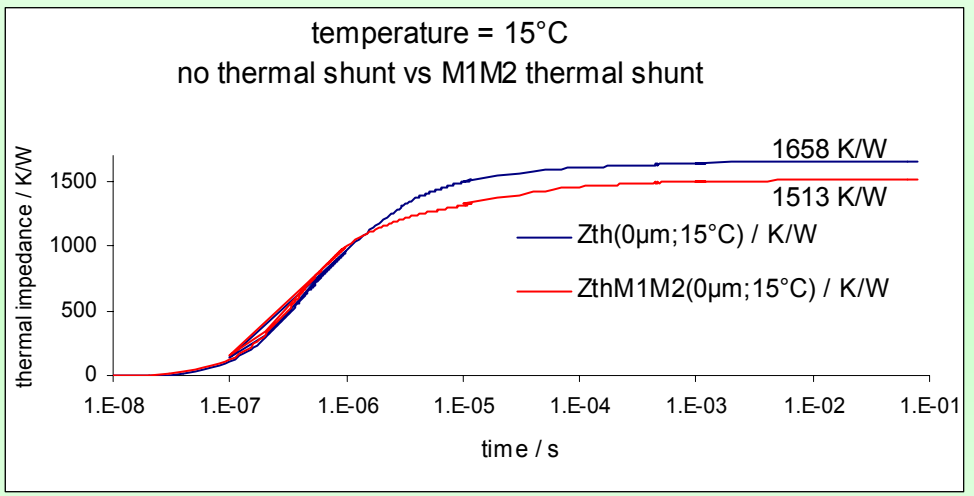




measured result with thermal shunt from metal1+metal2

51 µm*12 µm* 2 µm Au



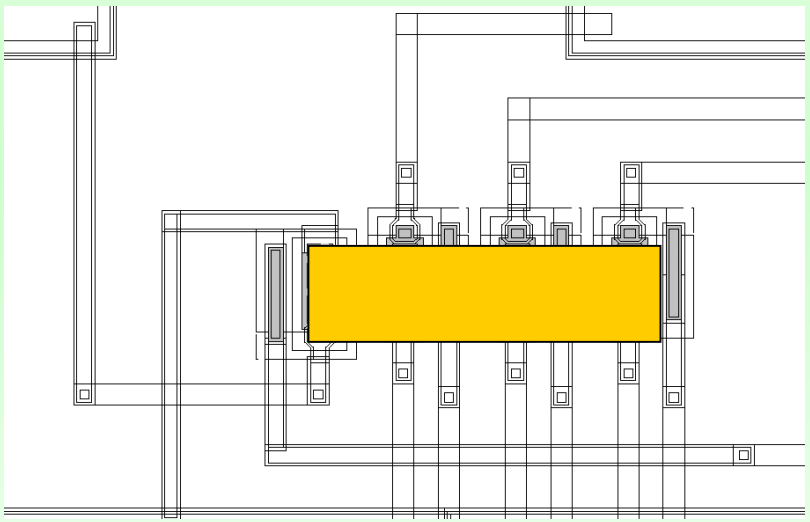


Rth reduction from 1658 K/W to 1513 K/W

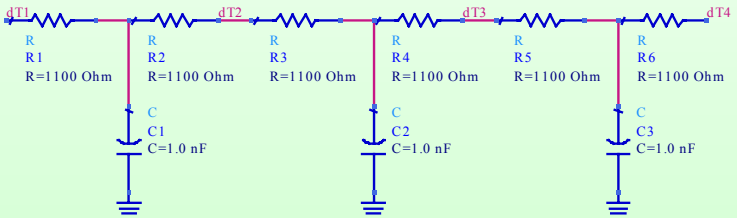
simulation with thermal shunt from metal1+metal2 failed

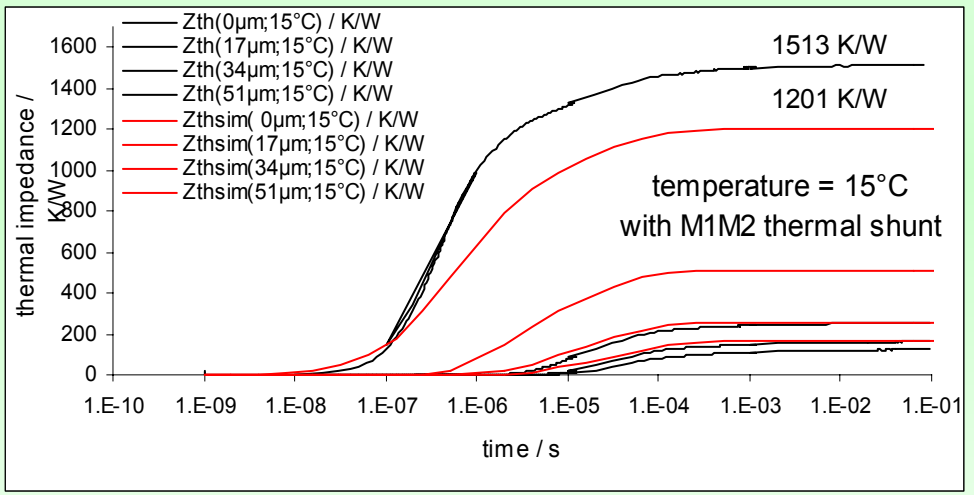
The geometry of the Au shunt allows to calculate the thermal parameters of the thermal shunt:

R_{th}=6600 K/W; C_{th}=3 nJ/K



Additional thermal network for simulation:



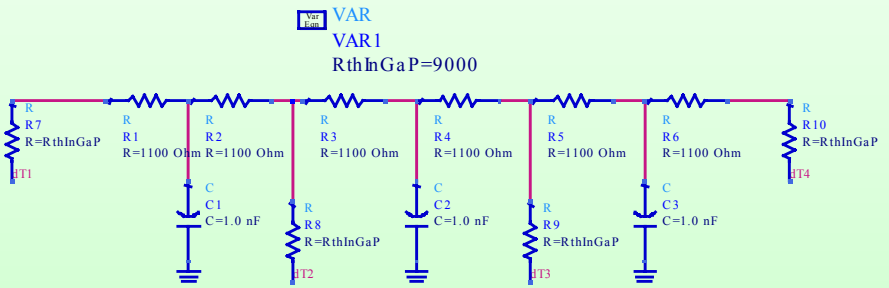


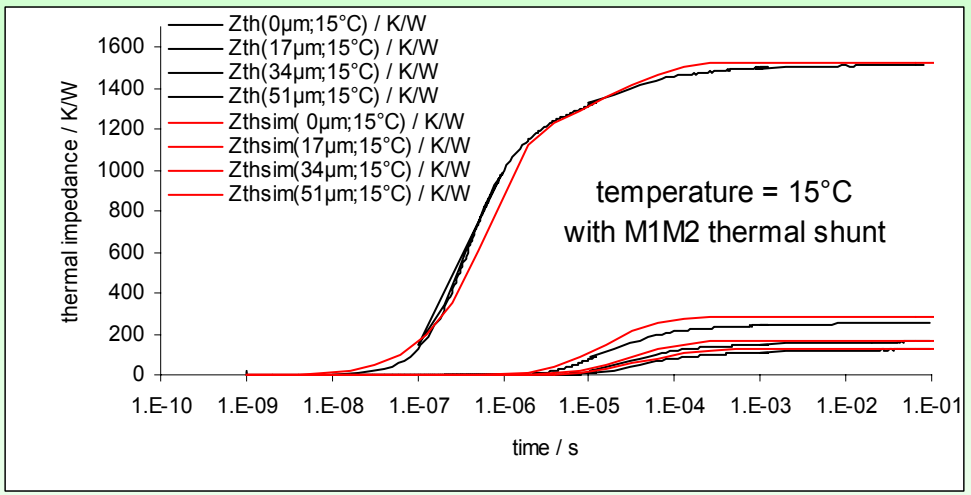
measured Rth =1512 K/W vs simulated Rth=1201 K/W

improved simulation with thermal shunt from metal1+metal2

InGaP Emitter with low thermal conductivity (~10 times lower than GaAs) is the problem

Therefore each finger has an additional thermal resistance to model the heatflow from collector to emitter





conclusions

- one pole parallel connected thermal impedances can implement thermal effects into electrical circuit simulators

- parameter extraction using appropriate test-structures is straight forward

- model extensions for optimization of the model based on test-structures are possible (e.g. thermal shunt)

- are there other experiences for structural thermal modeling?

The paper is now open for discussion!!

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