Darlington transistors

Two ways of modelling

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General Application Discretes
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Motivation

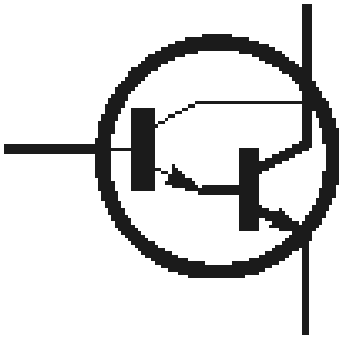
- Revision of Spice-models, new extractions
- Quantity: Some millions per year
- Examples: BCV26/27, BSP50/60

- Applications:

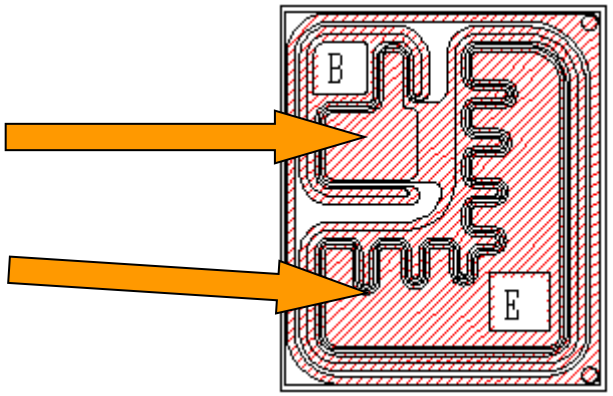
  - Circuits requiring very high DC current gain (about 20.000)
  - Relay driver

Darlington transistor: design

- 2 transistors processed in a very similar way, same diffusion



- Active area of transistors different
  - 1 small transistor for providing the base current
  - 1 big one as “main” transistor



Modelling strategies (1)

First possibility:

- Separate measuring and modelling of each transistor

- Result: Two independent models, combined to a subcircuit model

```
.SUBCKT Darlington 1 2 3
*
Q1 1 2 22 Transistor1
Q2 1 22 3 Transistor2
*
.MODEL Transistor1 PNP
+ IS = 1.593E-14
+ NF = 0.9855
+ ISE = 7E-15
+ NE = 1.5
.
.
. .MODEL Transistor2 PNP
+ IS = 1.623E-14
+ NF = 0.9725
+ ISE = 1.6E-15
+ NE = 1.27
.
.
.ENDS
```

Modelling strategies (2)

Second possibility:

- Using the AREA-variable

  (for reproducing the different silicon area of transistors similar to MOSFET)

- Result: subcircuit model with the same parameter set for both transistors

```
.SUBCKT Darlington 1 2 3
*
Q1 1 2 22 Transistor AREA = 1
Q2 1 22 3 Transistor AREA = 4.68
*
.MODEL Transistor PNP
+ IS = 1.593E-14
+ NF = 0.9855
+ ISE = 7E-15
+ NE = 1.5
.
.
.
.ENDS
```

Questions:

- “Mis”use of AREA-variable allowed?

  - Value of AREA referring to the proportions of the transistors or adjusted? ➔ Extraction strategy?

  - Which plots are affected by this? (gummel, output etc.)

- Advantages/disadvantages of described modelling strategies?

- Possibility of measuring/extracting the “whole” transistor to avoid a special wafer treatment for “open” base of Q2 (without covering layer) ?

Thank you for your attention!