

On the feasibility of single touch
on wafer calibration using HBT
(on wafer ECAL)

- advantages of ecal
- methodology description
- results
- discussion

- complete calibration with only one contact (compared to four with SOLT)
- improved repeatability
- simpler wafer handling and recalibration of the VNA
- reduced probe head contacts
- coaxial calibration with on wafer standards is also possible

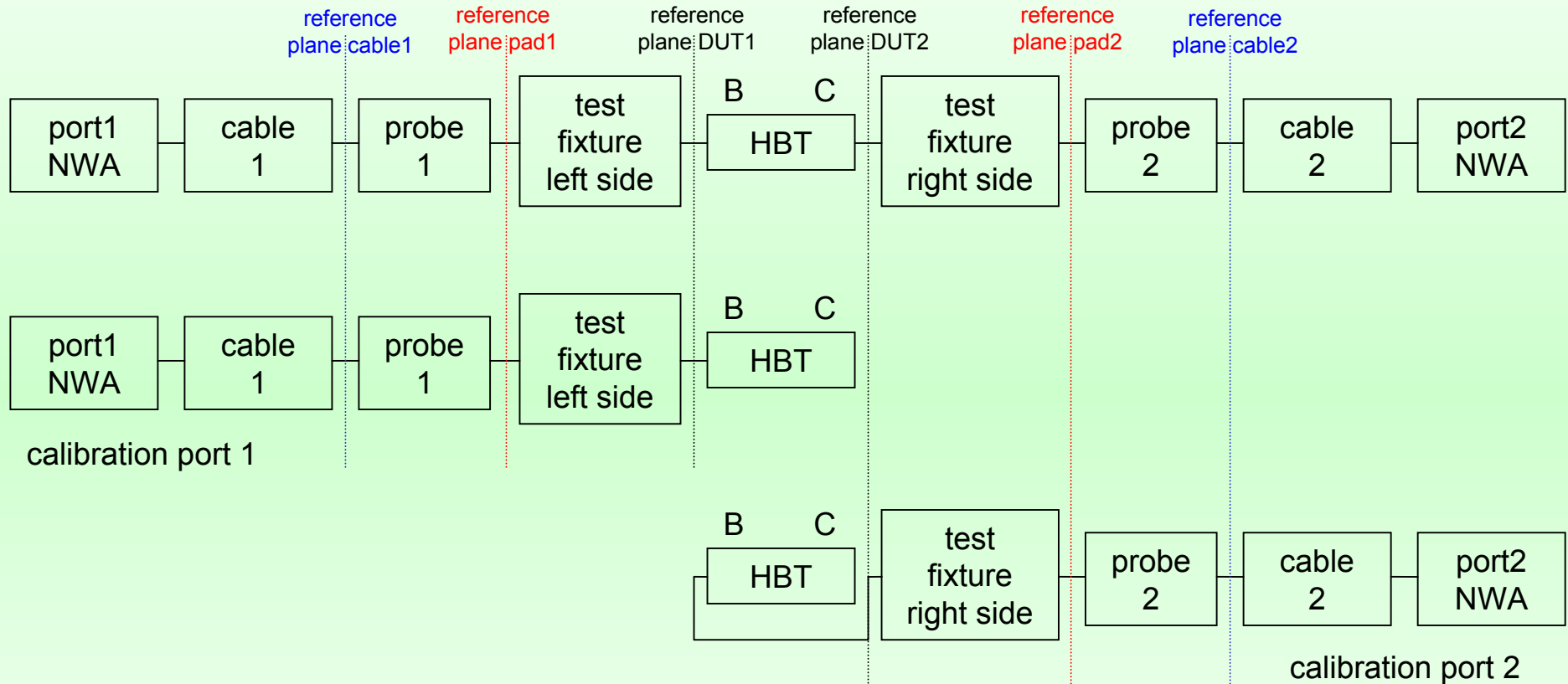
- 1 two-port self calibration procedure using ISS standards (e.g. TRL)
- 2 measurement and deembedding of the DUT (e.g. Transistor) test fixture e.g. [1]
- 3 one-port measurement with port1 of the base-emitter diode at three different operating points to have three different “non overlapping“ reflection coefficients.
- 4 repeat the reflection measurements with port 2 (same device and operating points, second contact)
- 5 calculation of the calibrated reflection coefficients

[1] K.H.Yau, et al., “A Transmission-Line Based Technique for De-Embedding Noise Parameters“, 2007 IEEE ICMTS, pp.237-243.

- 6 perform uncalibrated measurements of steps 3 and 4
- 7 contacting an arbitrary DUT with the same test fixture as in 2 and measure a reciprocal operating point (unknown thru)
- 8 calculating 12-Term error coefficients with data from 6 and 7 with models from 5 (SOLR-Method [2])
- 9 measure the calibrated S-parameters of the DUT at the desired operating points.
- 10 for recalibration repeat only steps 6 to 8

[2] A.Ferrero, U. Pisani, "Two-Port Network Analyzer Calibration Using an Unknown "Thru"", 1992 IEEE MGWL, Vol.2, No 12, pp.505-506.

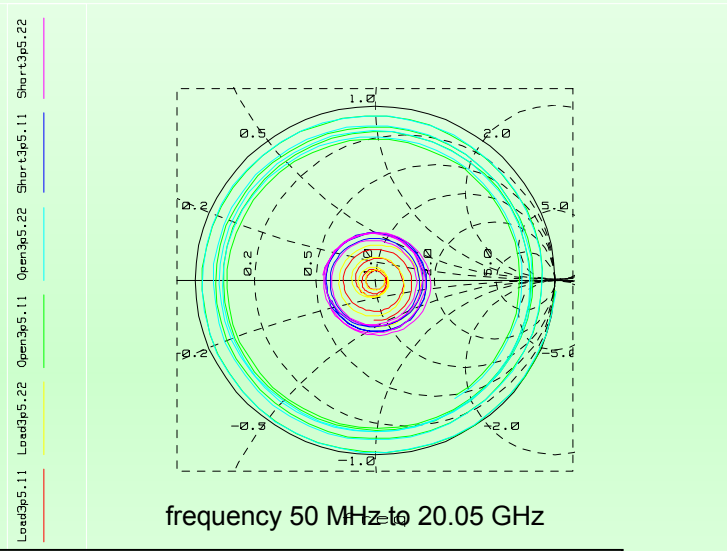
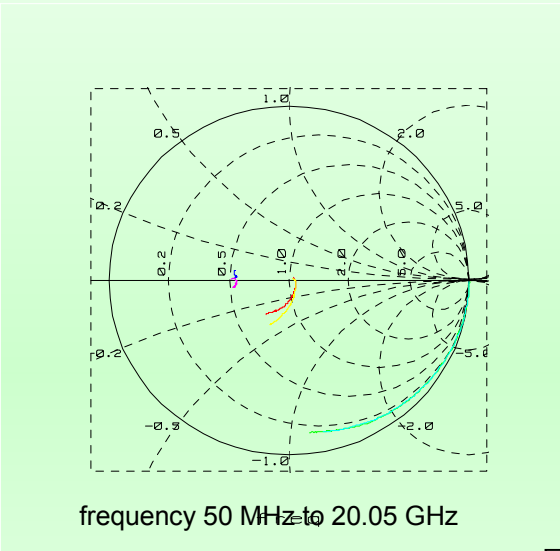
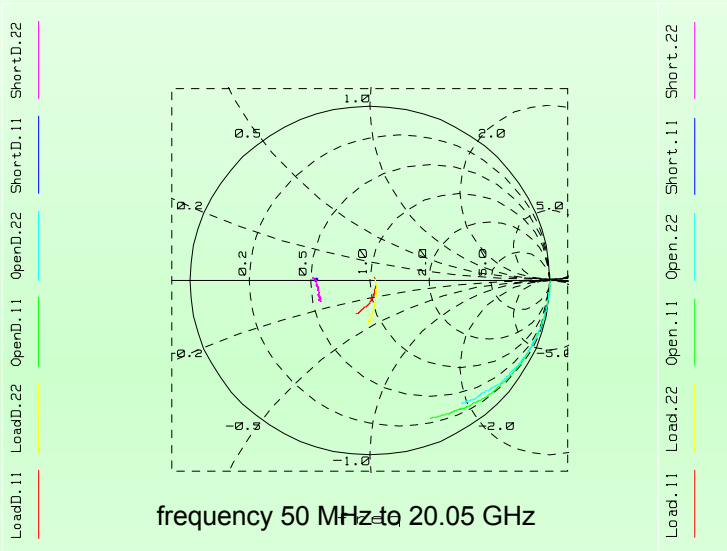
signal flow charts two port and one port measurements



reference plane DUT

reference plane pad

reference plane cable



GaAs HBT 8x1.5x1.5 μm^2 emitterarea

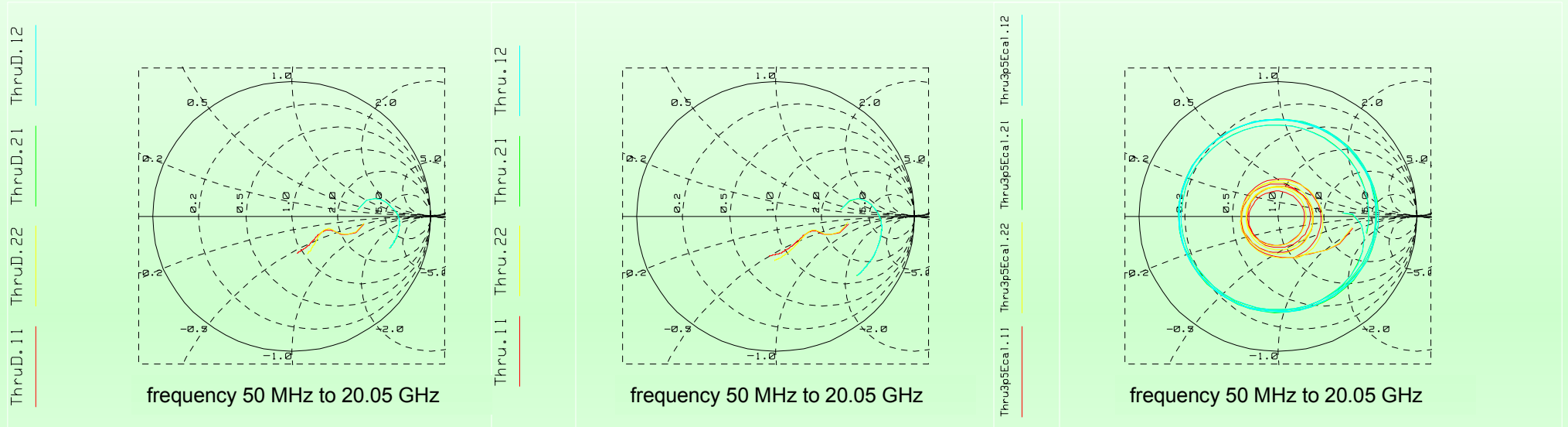
operating points: I (Open)=0 mA , I (Load)= 1 mA, I (Short)=6 mA

problem: difference between port1 and port2 calibration
reason: -probe positioning error?
-different coupling of the probe to the substrate?

reference plane DUT

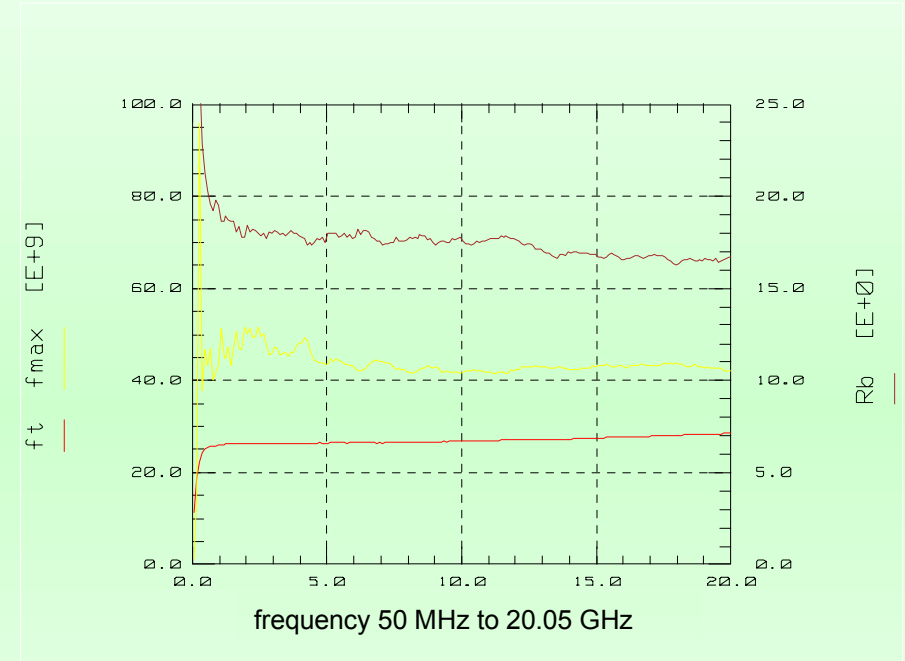
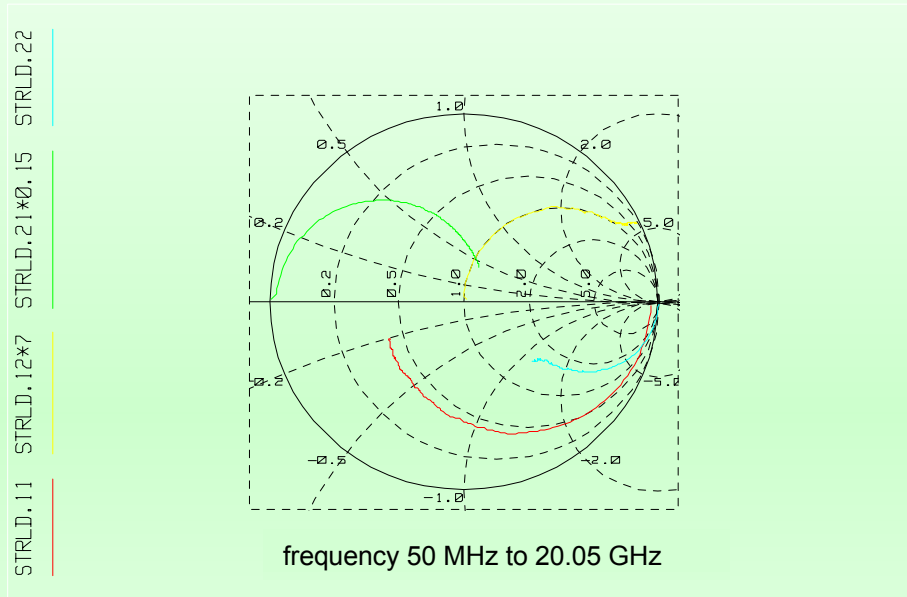
reference plane pad

reference plane cable



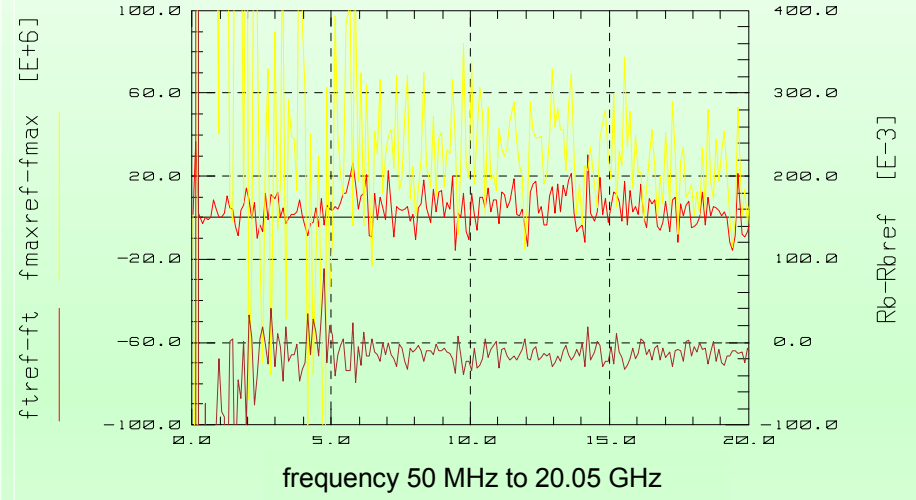
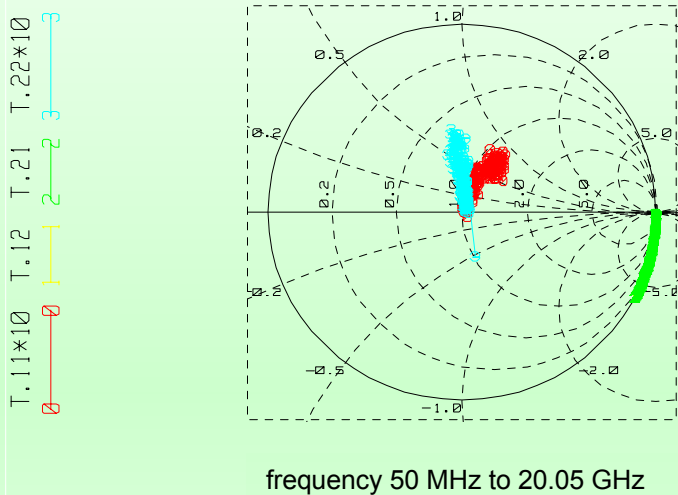
GaAs HBT 8x1.5x1.5 μm^2 emitterarea
 operating point: $I(\text{port1}) = -I(\text{port2}) = 0.5 \text{ mA}$

reference plane DUT



GaAs HBT 8x1.5x1.5 μm^2 emitterarea

operating point: I (port1)=50 μA , V (port2)=3 V



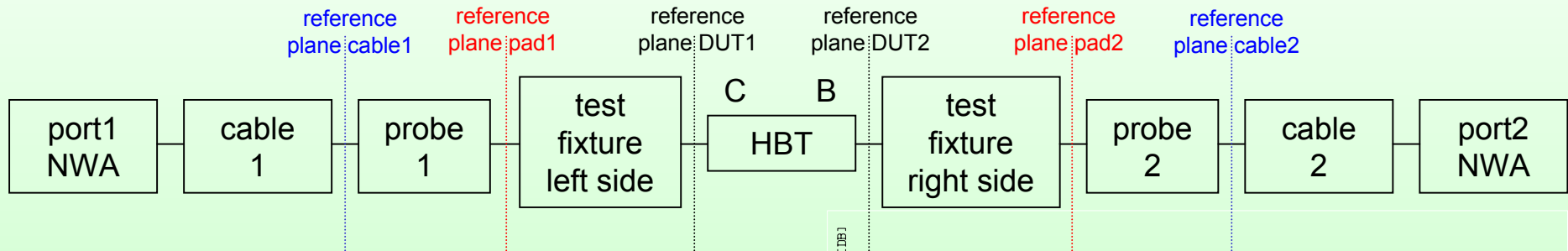
3.7 ps transmission line as reciprocal standard for SOLR

reference plane DUT

GaAs HBT 8x1.5x1.5 μm^2 emitterarea

operating point:

I (port1)=50 μA , V (port2)=3 V



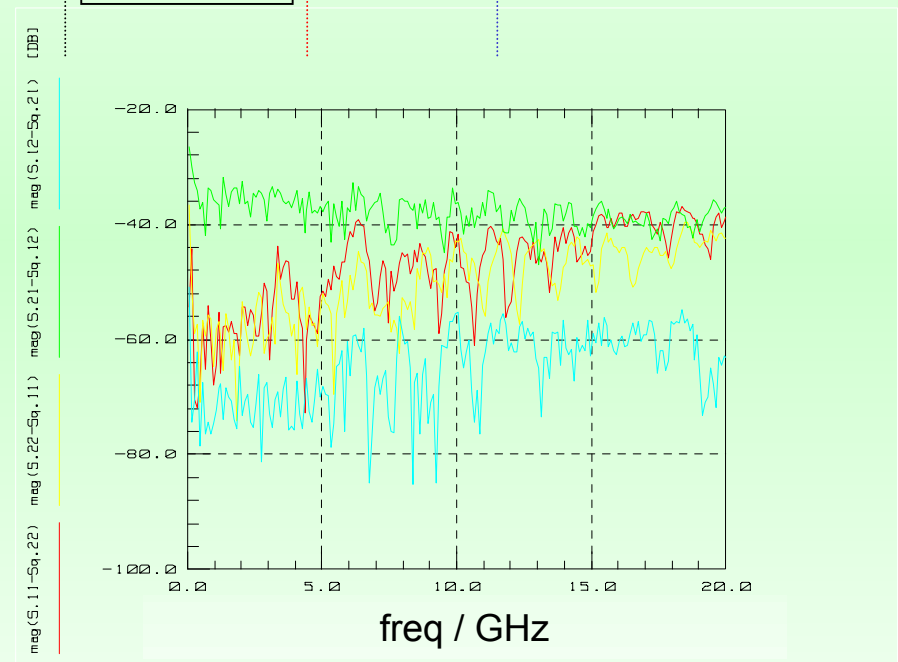
reference plane DUT

GaAs HBT 8x1.5x1.5 μm² emitterarea

operating points:

S: I (port1)=50 μA, V (port2)=3 V

Sq: I (port2)=50 μA, V (port1)=3 V



reference plane DUT

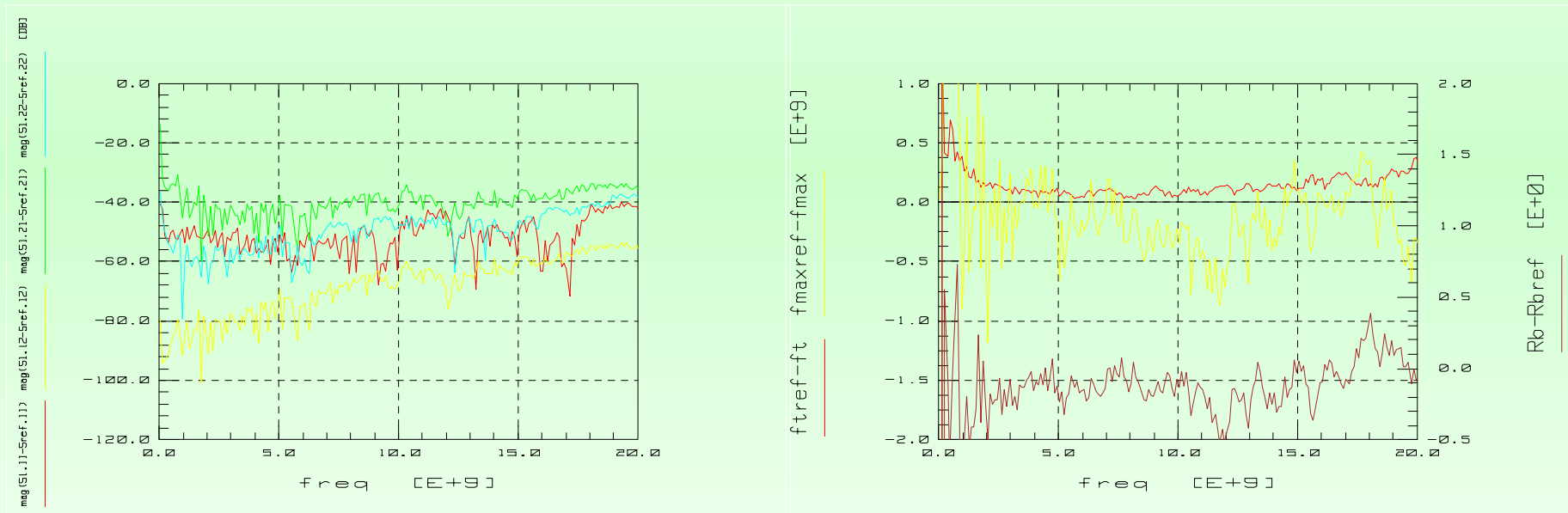
GaAs HBT 8x1.5x1.5 μm^2 emitterarea

operating point:

I (port1)=50 μA , V (port2)=3 V

Sref: reference measurement

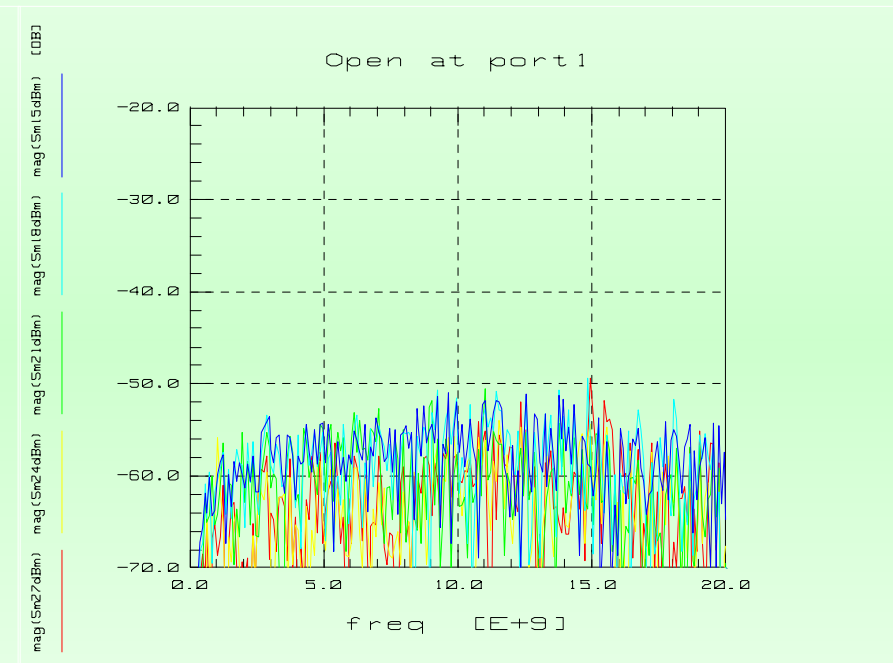
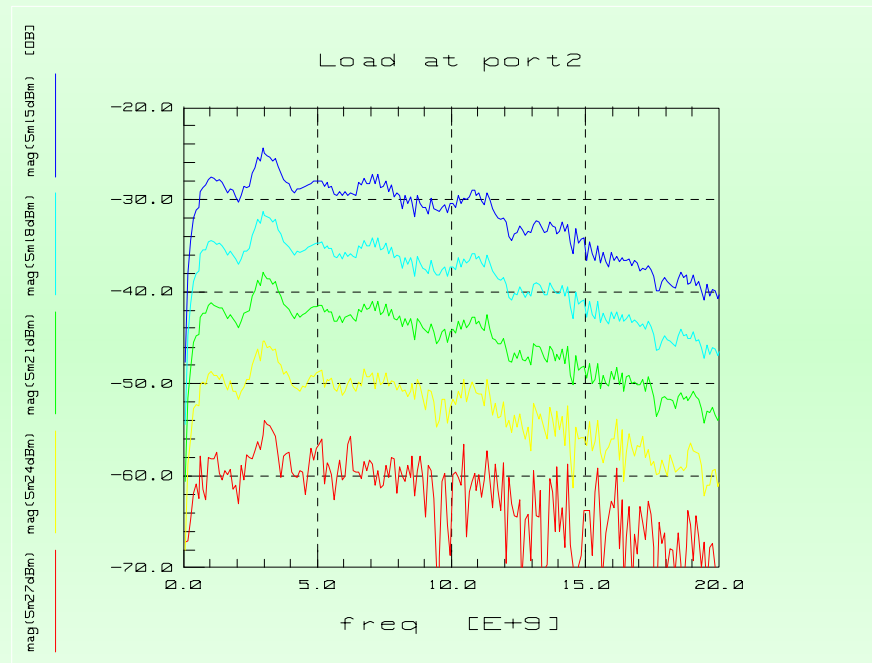
S1:repeating steps 1-9 three weeks later



reference plane DUT

GaAs HBT 8x1.5x1.5 μm^2 emitterarea

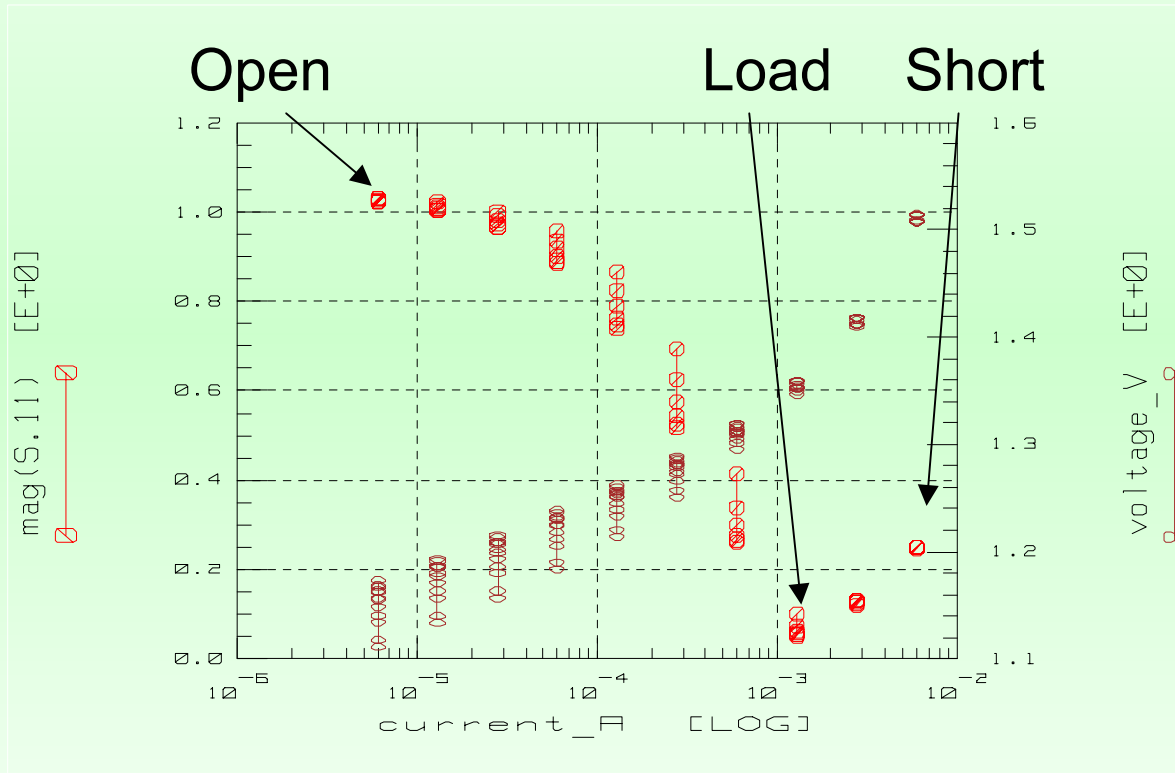
vector difference of data from -27 dBm to
-15 dBm in 3dB steps with data at -30 dBm



reference plane DUT

GaAs HBT 8x1.5x1.5 μm^2 emitterarea

Reflection factor at 3 GHz from -30 dBm to -15 dBm source power in 3dB steps together with resulting voltage (right axis)



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- calibration using HBT as calibration standard is possible
 - one touch calibration should be possible if using appropriate test- structure with two transistors
 - the method can be equally used deembedding other test fixtures (coaxial calibration (e.g. 3.5 mm...1mm) with on wafer standards, or different on wafer test fixtures)
 - further developments (remove ISS, improve “load“ standards linearity, comparing FET and Bipolar as calibration standard, extending frequency range)
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