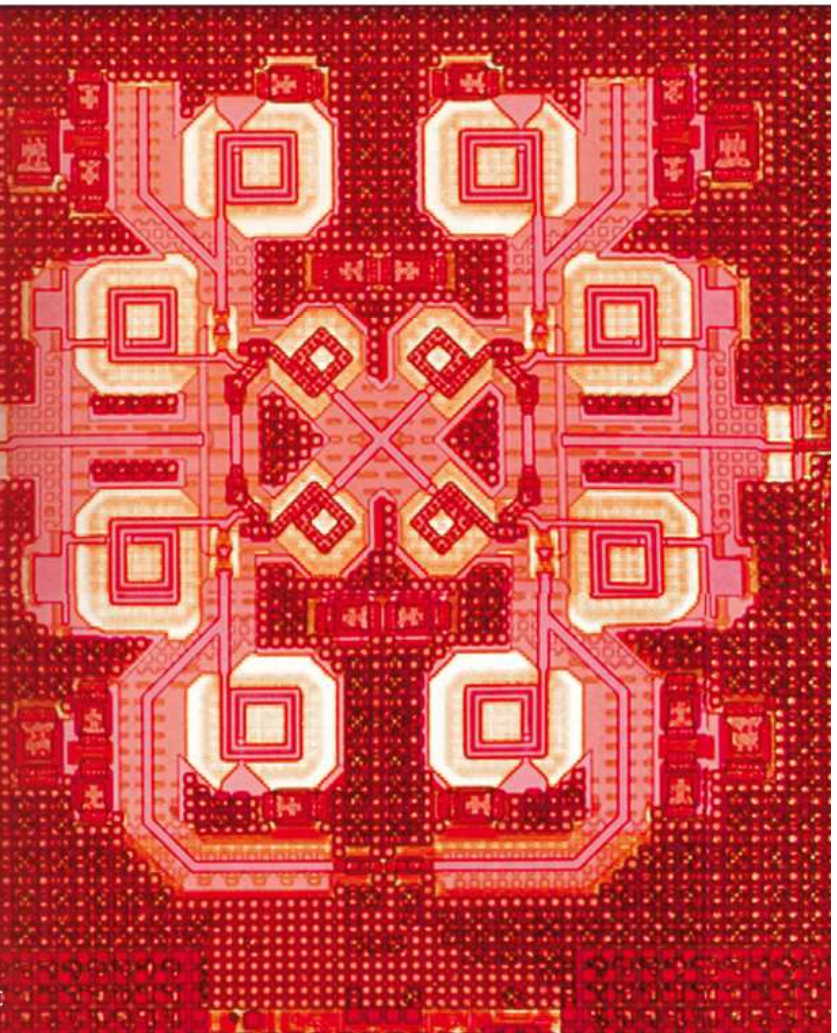




On-Si calibration vs ISS calibration

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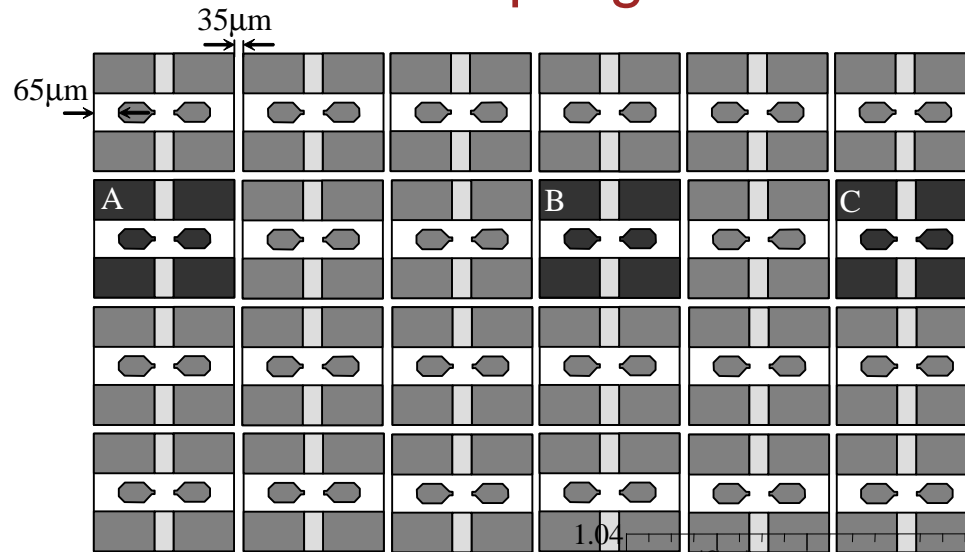
Outline

- Motivation
- EM Simulation
- Calibration ISS (SOLT)
- On Si-Calibration (TRL)
 - Test-structures
 - Pros and Cons of On Si-Calibration
- Results: SOLT (ISS) vs TRL (On Si-calibration)
- Perspectives

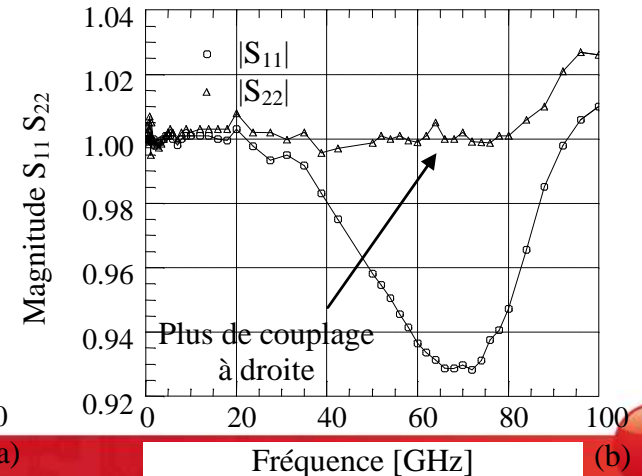
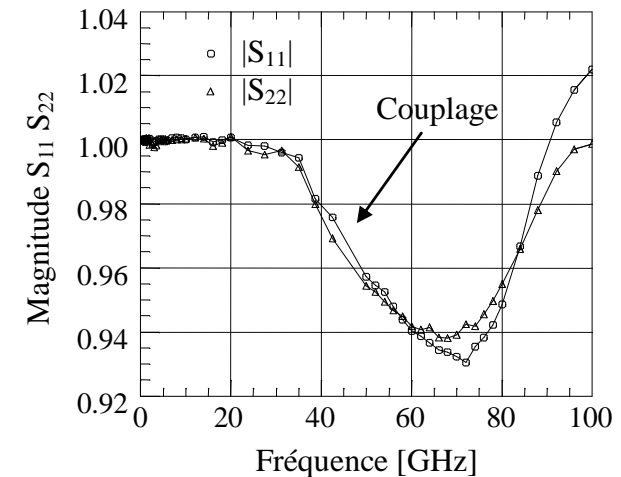
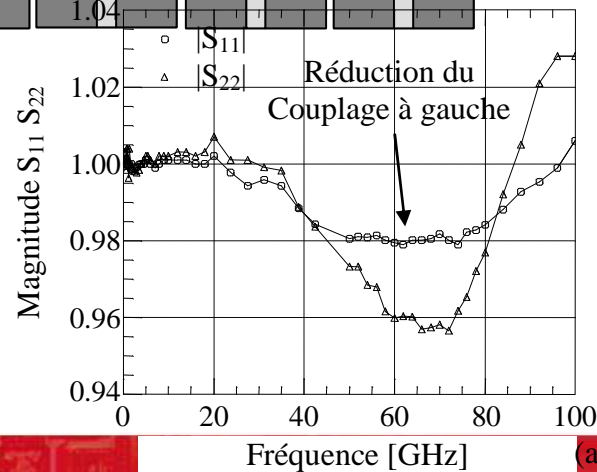


Motivation

- Reminder: Coupling of HF structures observed



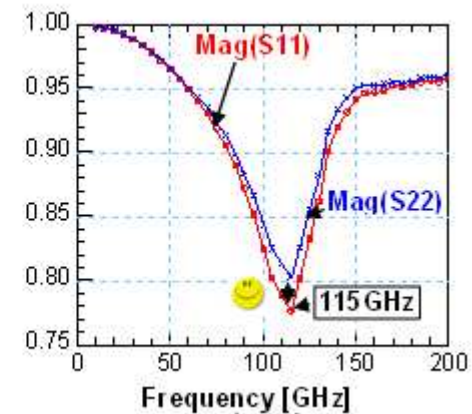
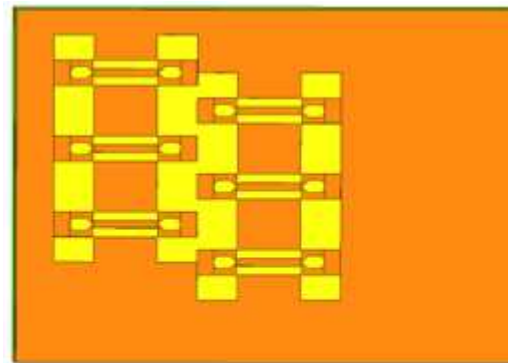
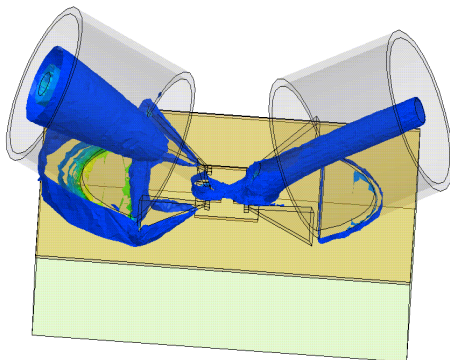
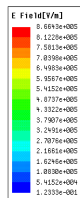
- Environment dependence
- Physical origin ?





EM simulation

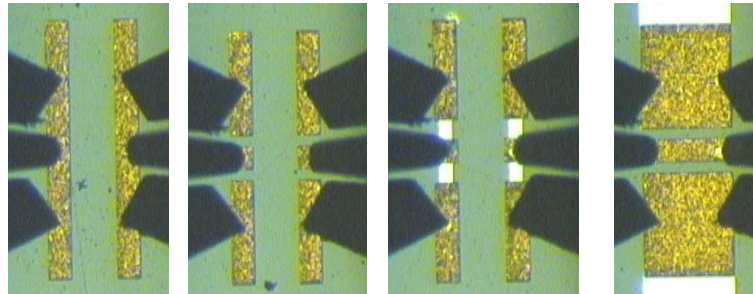
- **Investigation of coupling between wafer surface and probe tips through EM simulation**
 - Different test-structure layouts have been investigated.
 - Using metal layers (top metal or bottom metal) helps making the results reproducible, i.e. less sensitive to the adjacent test structures.
 - In fact, reproducible results can be corrected using appropriate de-embedding techniques.
 - Improved Si Test-structures have been designed where the coupling is wafer location-independent.





Calibration (SOLT)

- Specific chip (ISS)



short

open

load

thru

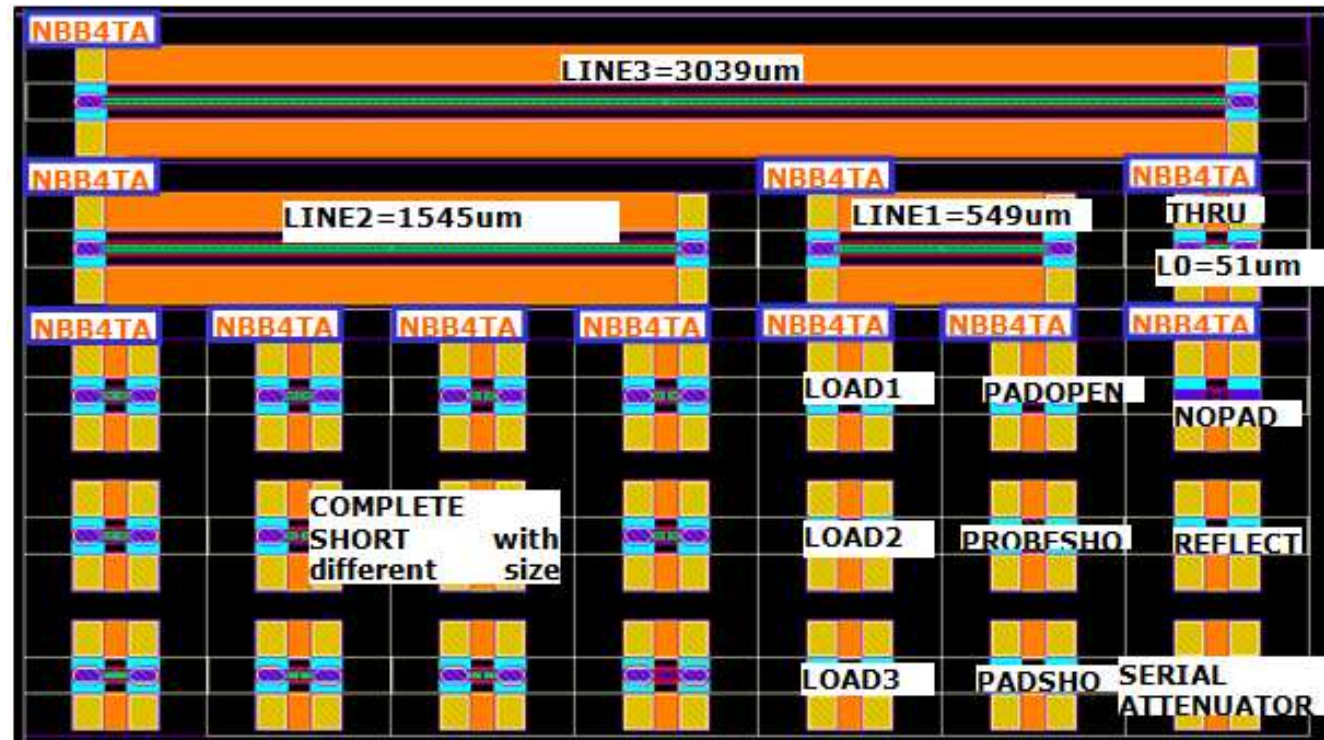
- Known standards (frequency dependence)
- Discussion
 - +: SOLT-Programming is straightforward
 - +: The advantage of the SOLT is that it can be very broadband
 - +: can be used for automatic probing (repeatable contacts)
 - -: but the standards have to be known very precisely for the given frequency range, so not useful for direct on-Si calibration and it.
- De-embedding structures (Si) are needed
- De-embedding procedure must be applied
- Change of EM environment : ISS → Si





On Si-Calibration (TRL)

- Specific Si-Testchip designed by ST-TUD *
 - We need:
 - Thru
 - Line 1
 - Load (2)
 - Reflect



*A. Rumiantsev, P. Sakalas, F. Pourchon, P. Chevalier, N. Derrier, M. Schroter, "Application of On-Wafer Calibration Techniques for Advanced High-Speed BiCMOS technology", IEEE-BCTM 2010 (Austin, Oct. 05-06, 2010)



Pros and Cons of On Si-Calibration

- **Pros**

- TRL programming is quite tricky
- The advantage of the TRL is that the conditions to get useable standards are easily fulfilled
 - 2 lines with different lengths but same characteristic impedance,
 - one identical reflect standard for both ports
 - a dc resistance of a load
- So it is suitable for on-Si calibration.

- **Cons**

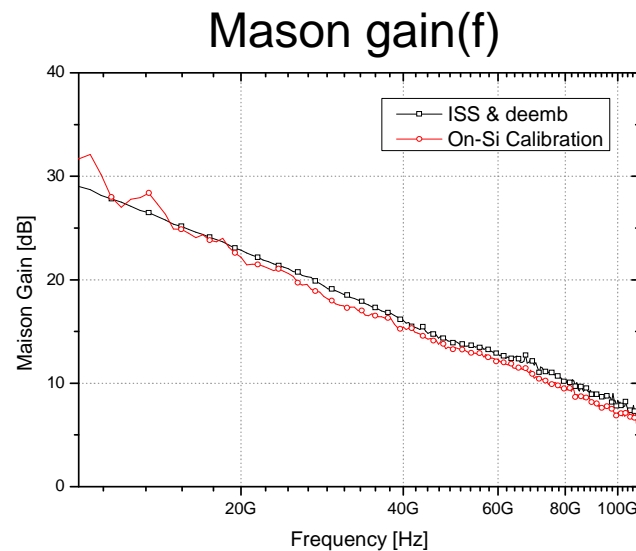
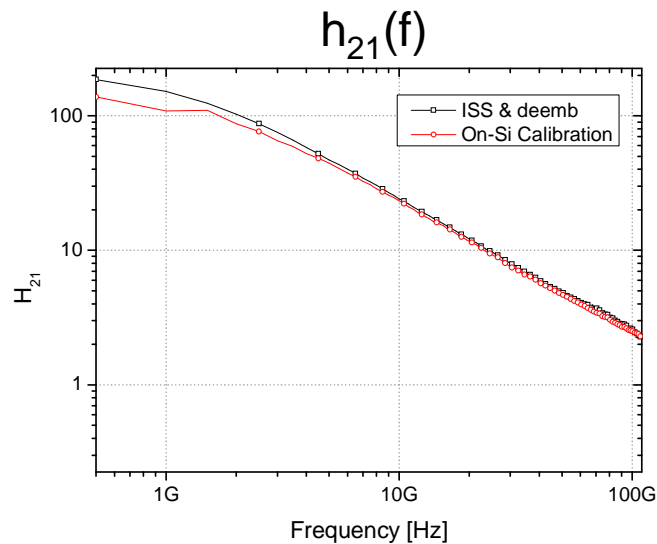
- The disadvantages of the TRL are: the line lengths define the useable frequency range (mostly limited, at least at low frequency – below 5GHz)
- Automatic probing cannot be applied.



SOLT (ISS) vs On Si-calibration (TRL)

- **Development of On-Si calibration procedure**

- Comparing different calibration methods (ISS, on-Si) gives similar results
- Furthermore the on-Si calibration brings the following advantages:
 - (i) It calibrates the system in one step, thus significantly reducing the calibration time.
 - (ii) Detailed equivalent circuits of backend parasitics are not required anymore.
 - (iii) Possible distributed behavior of backend parasitics has no impact on calibration accuracy.
- We expect that this method will obviate the regular ISS cal substrate.





Perspectives

- New test-structures for on-Si calibration “layouted”
 - Get rid of de-embedding
 - Measurement and analysis to be done when hardware available
- Test of on-Si calibration on S-parameters measurements beyond 110GHz



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