Dynamic Ageing Modeling for Reliability Simulation

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OUTLINE

- Context
- Introduction
- Initial Modeling
- Tansistor aging model
- VerilogA implementation in HiCuM model
- Methodology validation
- Reliability aware circuit design example
- Conclusion

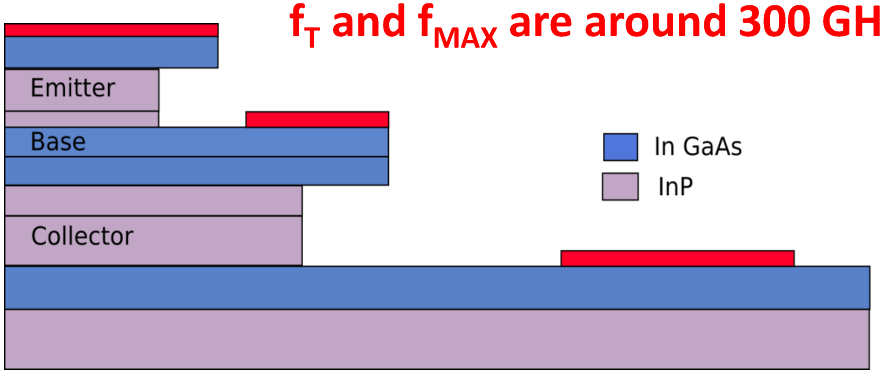
CONTEXT

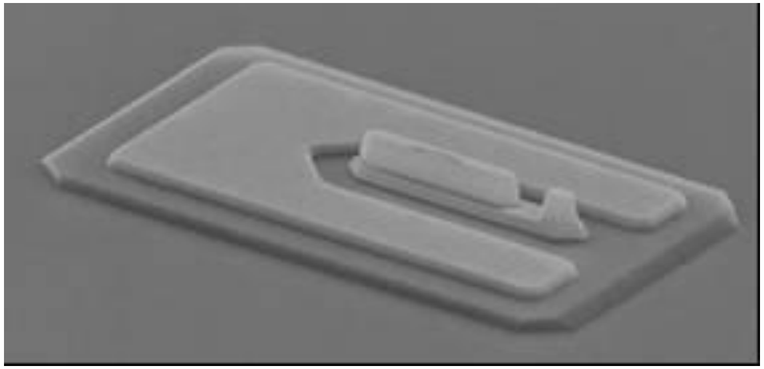
- III-V lab InP/InGaAs HBT technology
- Challenging applications:
  - High speed optical communications systems (working above 100 Gbit/s)
- Very high reliability requirements
  - (e.g., submarine communication systems)
- Accurate reliability modeling is desirable

Note: this methodology is not process specific.

Can be applied to SiGe HBT, BiCMOS or CMOS

f_T and f_{MAX} are around 300 GHz





INTRODUCTION

Standard method based on a static approach:

- Simulate circuit & estimate bias / temperature constraints for each device
- Calculate device degradations
- Simulate circuit again with new device parameters (eventually iterate)

ISSUES:

- Degradation mechanisms are dynamic

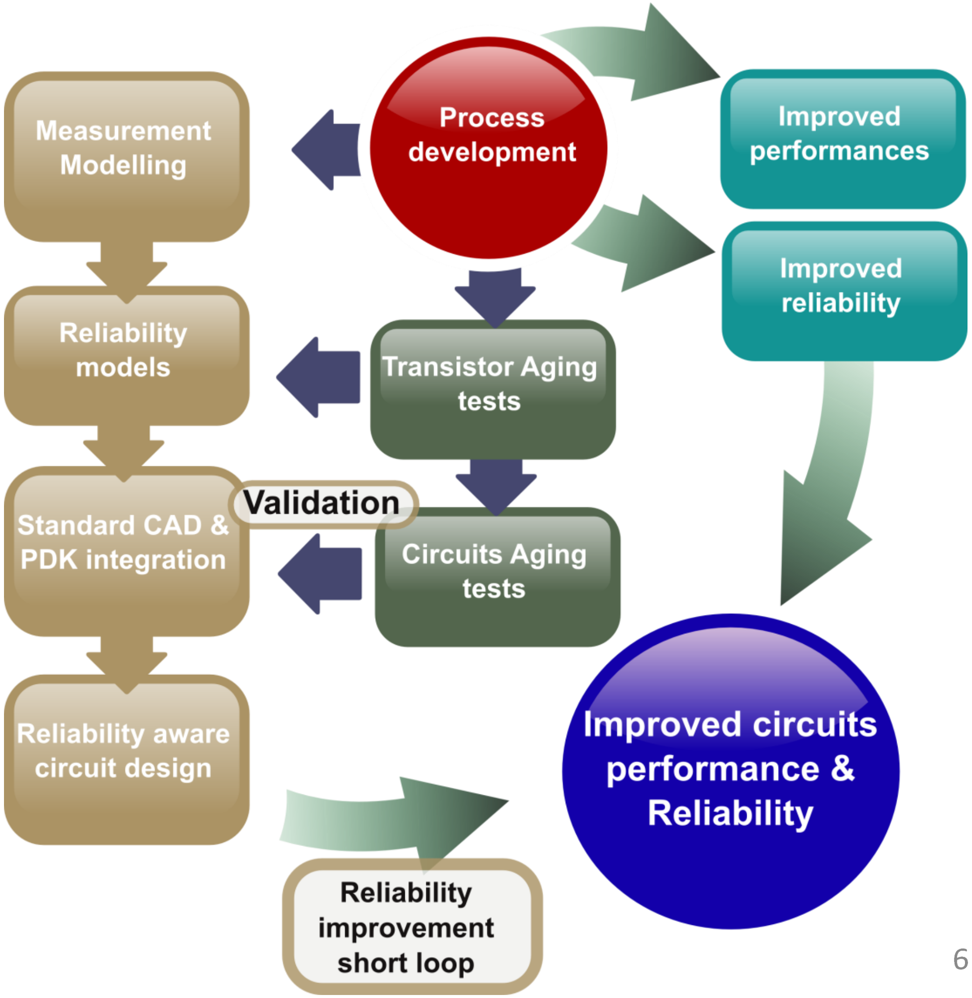
INTRODUCTION

Need for a “real-time” dynamic degradation model

- Directly integrated in CAD environments (i.e. in PDK for easy adoption)
- Use compact model with slowly varying parameters as a function of bias and temperature under real circuit operating conditions
- Can be realized easily in VerilogA language (straightforward implementation in commercial simulators)
- Small performance penalty (compiled code)

INTRODUCTION

- New methodology (reliability improvement short loop)



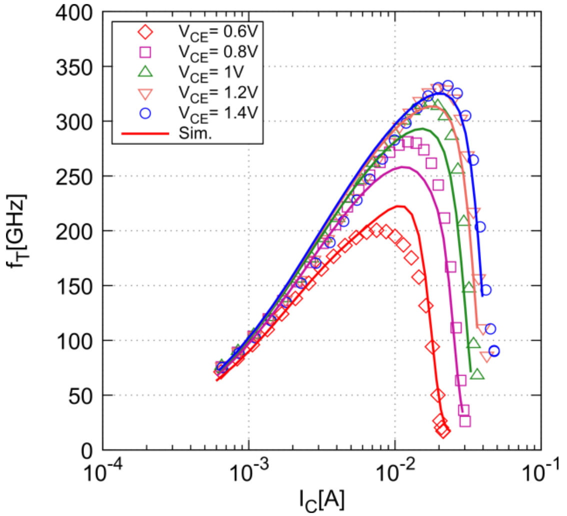
INITIAL MODELING

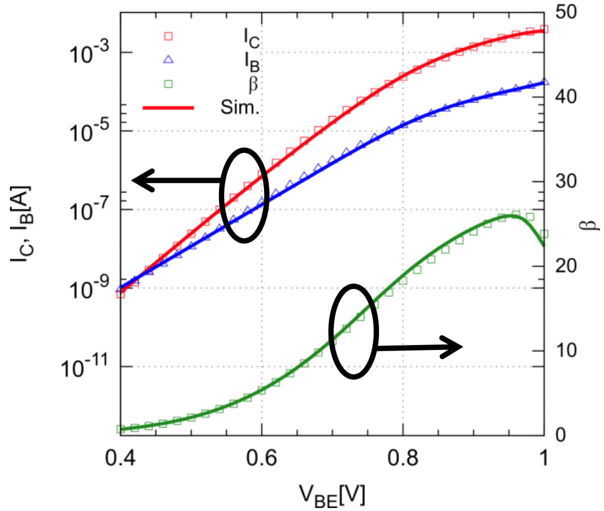
- Why choosing HiCuM L2 v2.30 compact model ?
- CMC labeled model (Available in most commercial simulators)
- VerilogA code available
- HiCuM accuracy + Specific improvements of version v2.30
  - Modeling of advanced HBTs

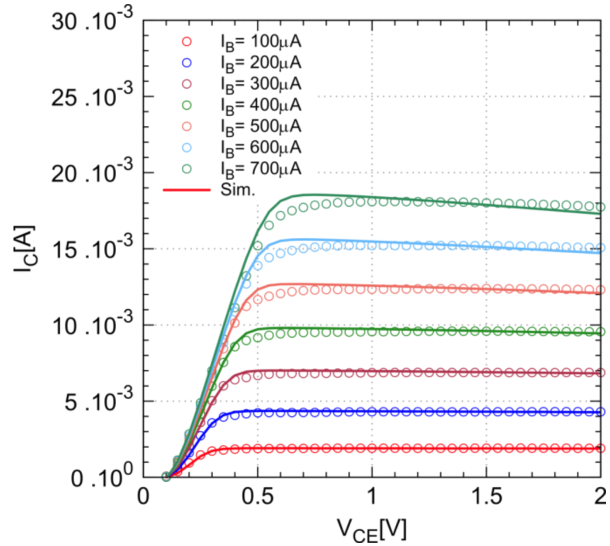
Parameter extraction for good initial model (@ transistor level and @circuit level) is already very challenging

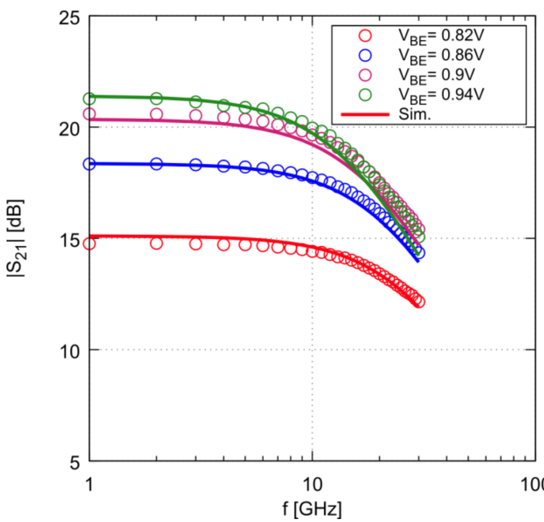
INITIAL MODELING

Results for T7 (W_E=0.5µm and L_E=7µm)







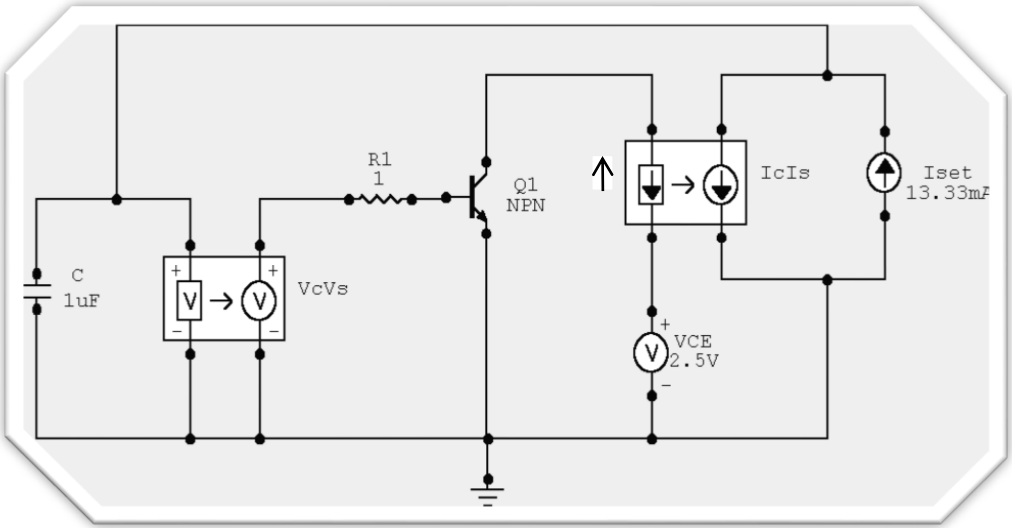


TRANSISTOR AGING MODEL

Accelerating aging set up in: to observe degradations

- Stress conditions: P1, P2, P3, P4 (and P2')
- JC = 400 kA/cm² for P1, P2, P3, P4 (and 610 kA/cm² for P'2)
- VCE = 1.5, 2, 2.5 and 2.7 V for P1, P2, P3 and P4
- Tj =80, 92, 106 and 112°C

Need feedback loop to maintain V_{CE} and J_C

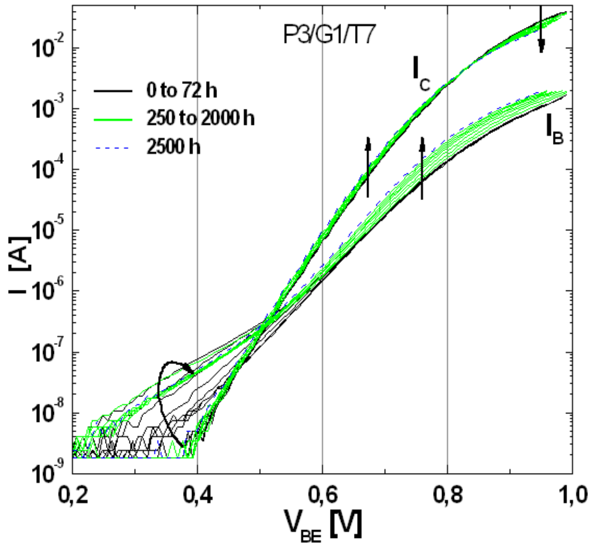


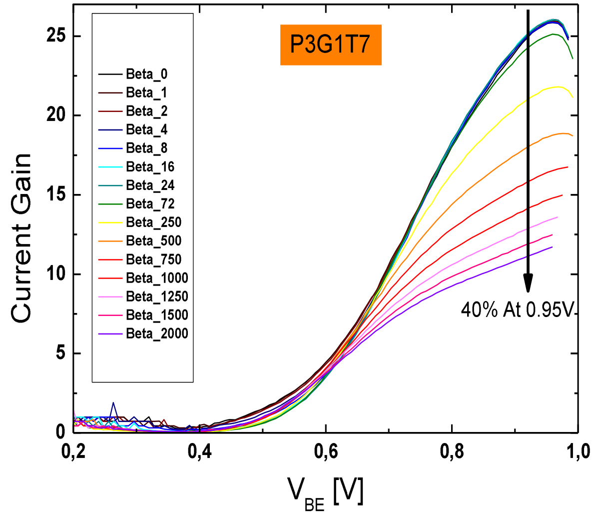
TRANSISTOR AGING MODEL

Observed Gummel characteristic

- Moderate IC increase
- Important IB increase

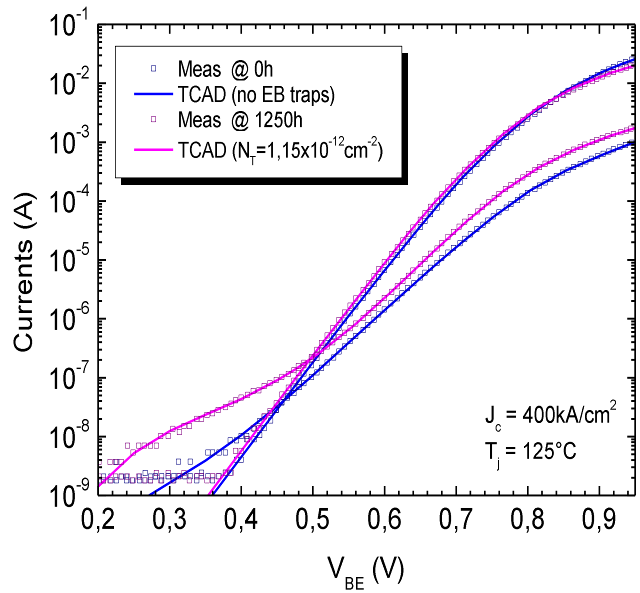
- Moderate IC decrease (high J_C)

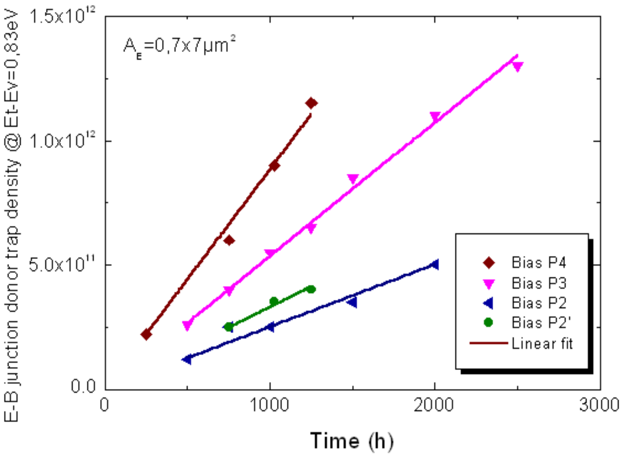




TRANSISTOR AGING MODEL

- 2D Calibrated TCAD Hydrodynamic simulations
- Donor traps at E-B junction surface are responsible for the current increase
- Trap concentration increase linearly with stress time





TRANSISTOR AGING MODEL

- Trap density is not a compact model parameter : need saturation currents

$$i_{jBEi} = I_{BEiS}\left[\exp\left(\frac{v_{B'E'}}{m_{BEi}V_T}\right)-1\right]+I_{REiS}\left[\exp\left(\frac{v_{B'E'}}{m_{REi}V_T}\right)-1\right]$$

$$i_{Tf} = \frac{I_S}{Q_{p,T}/Q_{p0}}\left[\exp\left(\frac{v_{B'E'}}{V_T}\right)-\exp\left(\frac{v_{B'C'}}{V_T}\right)\right]$$

- IS and IBEIS are extracted from post stress measurements
- IS and IBEIS follow the same linear evolution (as traps) with stress time
- IS and IBEIS can be advantageously used as variables of the aging model

TRANSISTOR AGING MODEL

Donor trap density can be modeled as a generation mechanism

$$\frac{dN_{trap}(t)}{dt} = G(T, J_C)$$

Same holds for IBEis and IS

$$\frac{dI_{BEiS}(t)}{dt} = A_{IBEIS}(T, J_C) \qquad \frac{dI_S(t)}{dt} = A_{IS}(T, J_C)$$

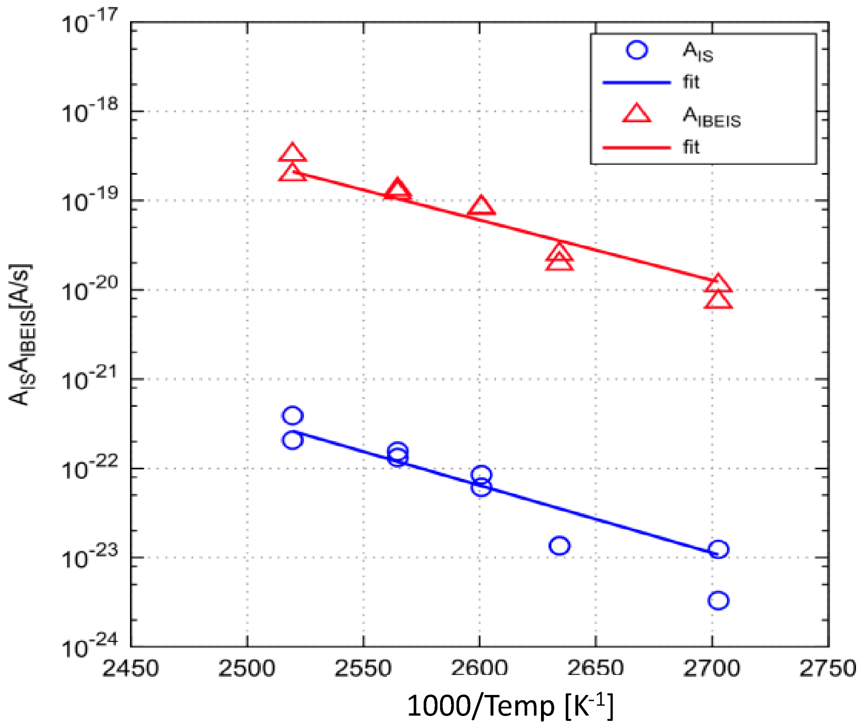
Constant increasing rates follow an Arrhenius law

$$A_{IBEIS}(T, J_C) = B_{IBEIS}\left[\exp\left(\frac{-E_{IBEIS}}{k_B T}\right)\right] J_C^{\alpha_1} \qquad A_{IS}(T, J_C) = B_{IS}\left[\exp\left(\frac{-E_{IS}}{k_B T}\right)\right] J_C^{\alpha 2}$$

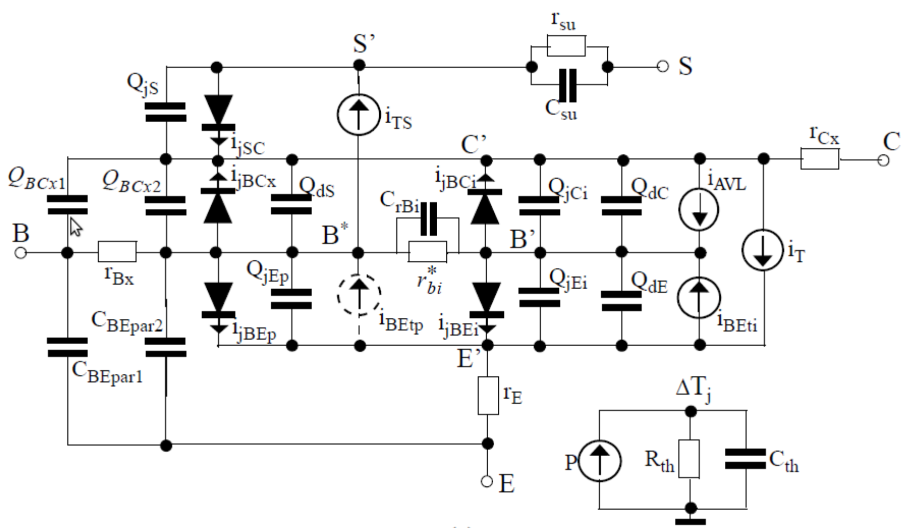
EIS, EIBEIS, BIBEIS, AIS are new model parameters

TRANSISTOR AGING MODEL

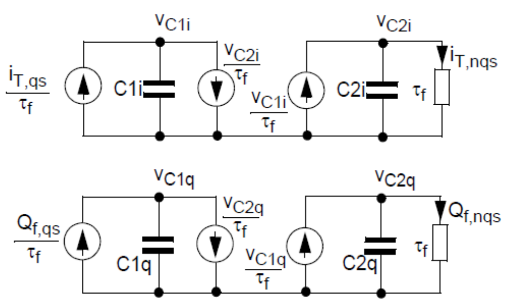
- Parameter extraction of IS and IBEIS (P2, P3, P4) (T5, T7, T10)
- extract constant generation rates (AIS and AIBEIS)
- AIS and AIBEIS follow an Arrhenius law
- EIBEIS = 1.34 eV
- EIS =1.5 eV



VERILOGA IMPLEMENTATION IN HiCuM MODEL

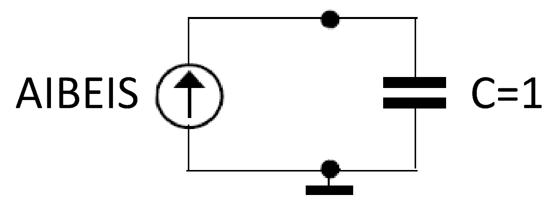


(a)



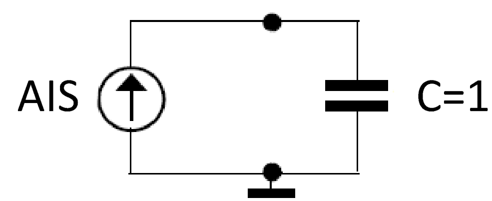
2 new nodes

Ibeis_out



$$\frac{dI_{BEiS}(t)}{dt} = A_{IBEIS}(T, J_C)$$

Is_out



$$\frac{dI_S(t)}{dt} = A_{IS}(T, J_C)$$

VERILOGA IMPLEMENTATION IN HiCuM MODEL

```
module hic2_full_XDK (c,b,e,s,tnode,  ibeis_out,    is_out);
...
branch                    (ibeis_out)   br_ibeisout
branch                    (is_out)      br_isout;
```

New nodes and branch

```
ibeis        = V(br_ibeisout)          +ibeis0;
is           = V(br_isout)             +is0;
```

Update model parameters: new nodes voltage represent degradation

```
aibeis       = bibeis*exp(-eibeis/((`P_K/`P_Q)*Tdev))         *pow( jc ),alpha1);
ais          = bis*exp(-eis/((`P_K/`P_Q)*Tdev))               *pow( jc ),alpha2);
```

Temp & J_C dependence

```
        I(br_ibeisout)          <+ -aibeis;
        I(br_ibeisout)          <+ ddt(V(br_ibeisout));

        I(br_isout)             <+ -ais;
        I(br_isout)             <+ ddt(V(br_isout));
```

Branch equations

VERILOGA IMPLEMENTATION IN HiCuM MODEL

```
module hic2_full_XDK (c,b,e,s,tnode,  ibeis_out,    is_out);
…
branch                    (ibeis_out)   br_ibeisout
branch                    (is_out)      br_isout;
```

```
ibeis        = V(br_ibeisout)          +ibeis0;
is           = V(br_isout)             +is0;
```

```
aibeis       = bibeis*exp(-eibeis/((`P_K/`P_Q)*Tdev))        *pow( jc ),alpha1);
ais          = bis*exp(-eis/((`P_K/`P_Q)*Tdev))              *pow( jc ),alpha2);
```

```
             I(br_ibeisout)          <+ -atsf * aibeis;
             I(br_ibeisout)          <+ ddt(V(br_ibeisout));

             I(br_isout)             <+ -atsf * ais;
             I(br_isout)             <+ ddt(V(br_isout));
```

Simulation of degradations is too slow: 10000 years of CPU time !!!

ATSF is the Accelerating Time Scale Factor: new parameter

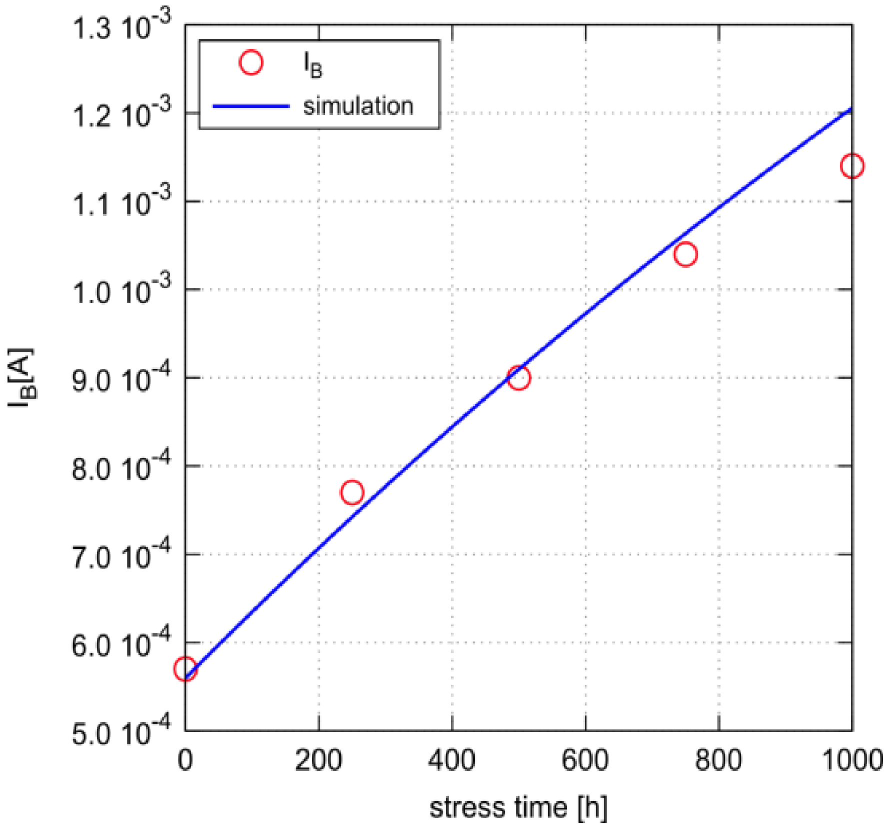
ATSF=3.6E13   100ns -> 1000 h
ATSF=3.15E15 100ns -> 10 years

METHODOLOGY VALIDATION

- Verification on base current (monitored during stress – 1000 h)
- Transistor T7
- Bias condition P4

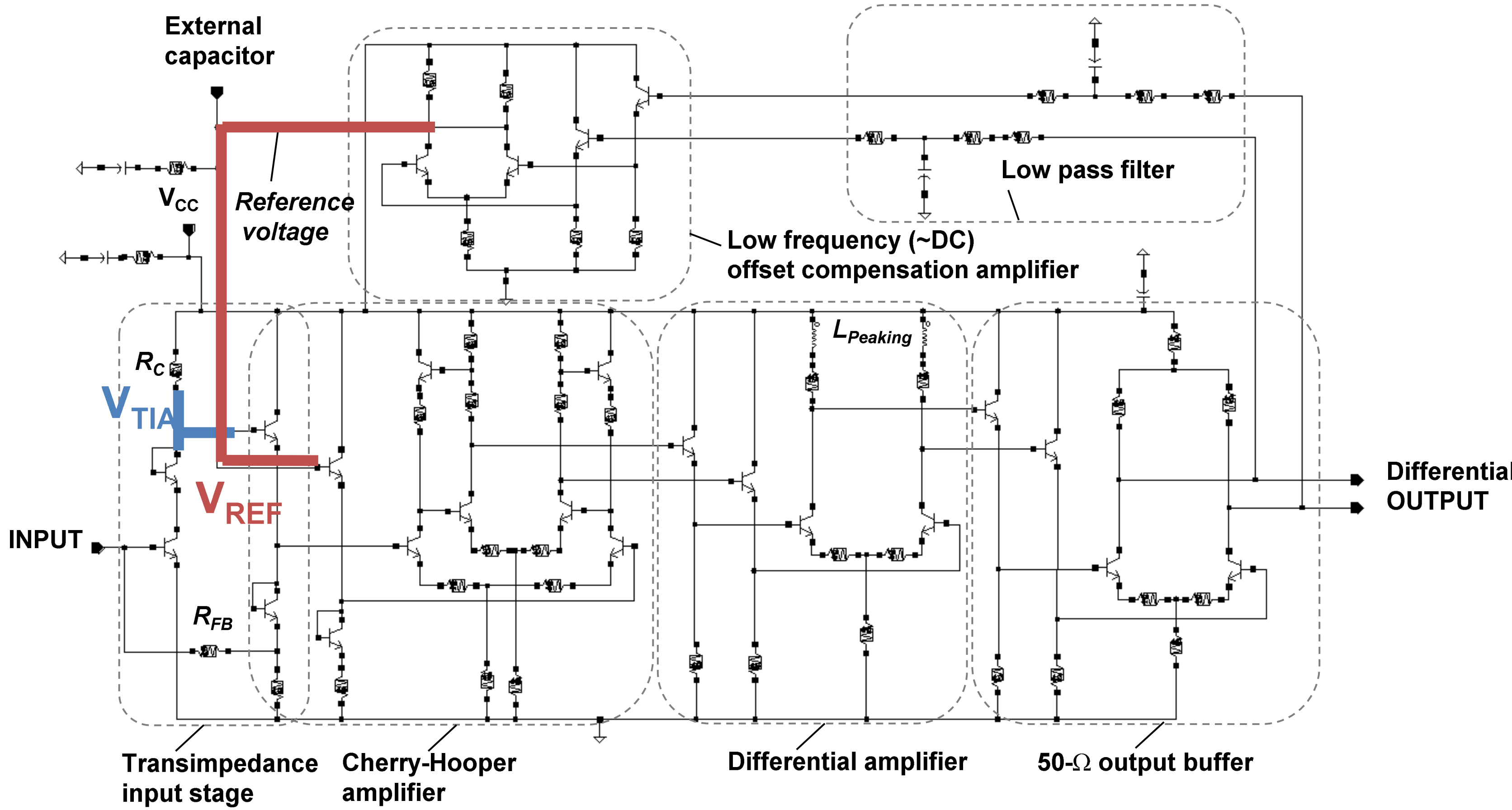
Model is accurate at

Transistor level



METHODOLOGY VALIDATION

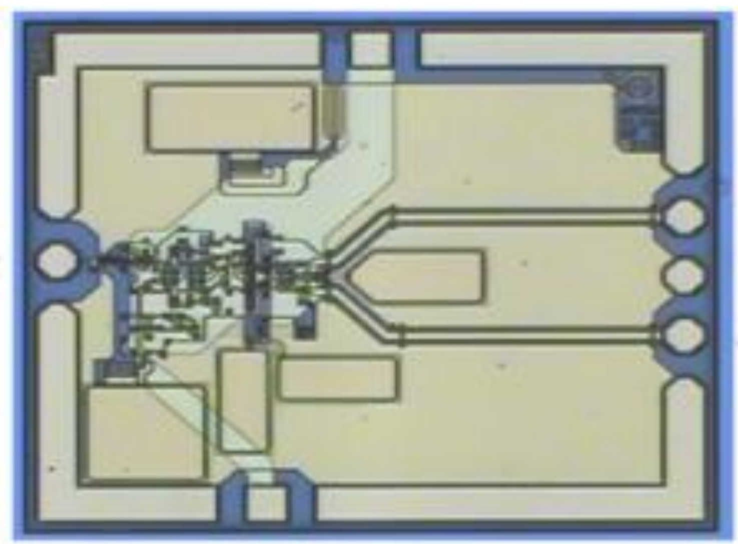
- Transimpedance Amplifier (TIA)



METHODOLOGY VALIDATION

2 versions of the TIA available

- TIA (high DC gain – low cutoff frequency)
- TIA-HF (lower DC gain – Higher bandwidth)
- 22 samples submitted to accelarated aging for 1008 hours
- chuck temperature70°C
- Tj up 125°C



METHODOLOGY VALIDATION

Transient simulation of the TLIA

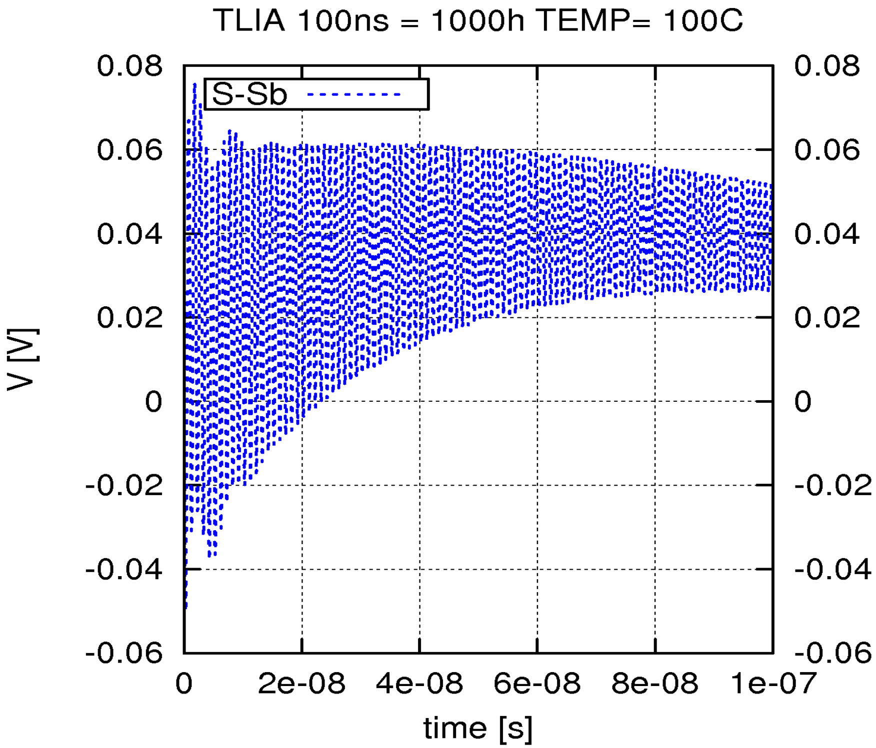
- ATSF=36e12 (100ns=10years)
- TEMP=100°C
- Differential output voltage (S-Sb)

Circuit degradation can be observed

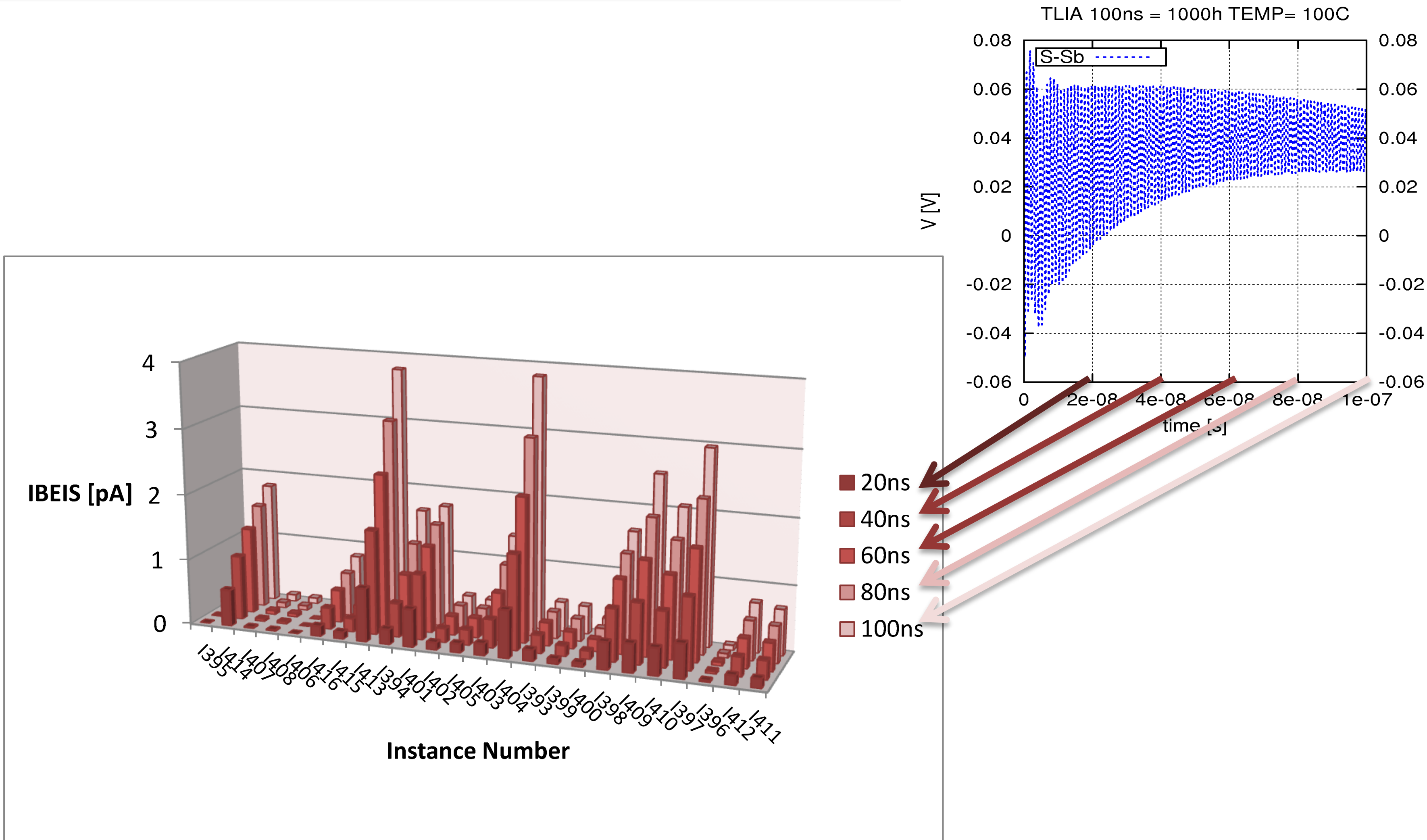
Dynamically

Altered parameters can be extracted at

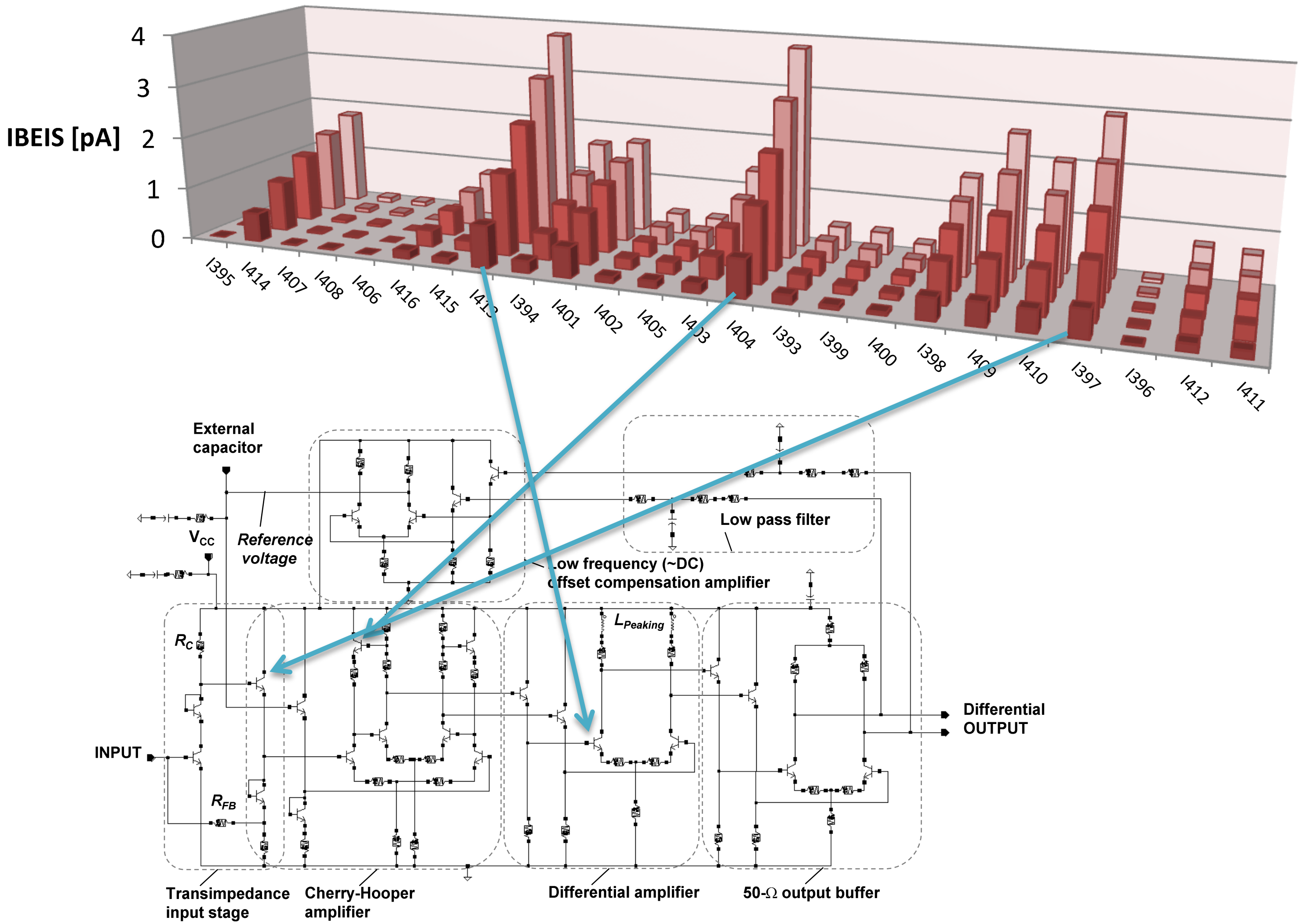
Any time step



METHODOLOGY VALIDATION

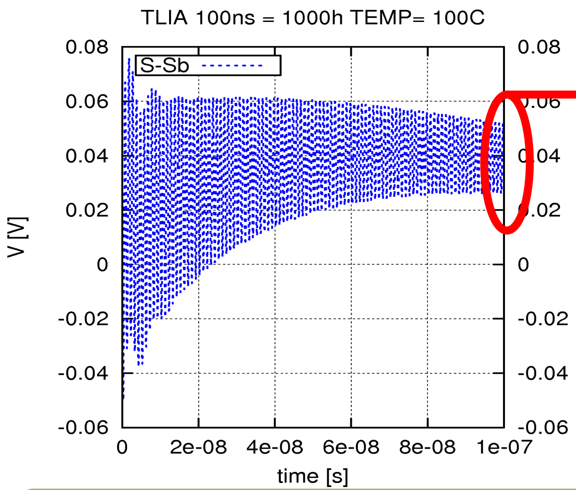


METHODOLOGY VALIDATION



METHODOLOGY VALIDATION

Transient simulation of the TLIA



Steady state @ selected time step:
run AC simulation with aged parameters
Using a script to generate "alter" statements
gathered in a include file

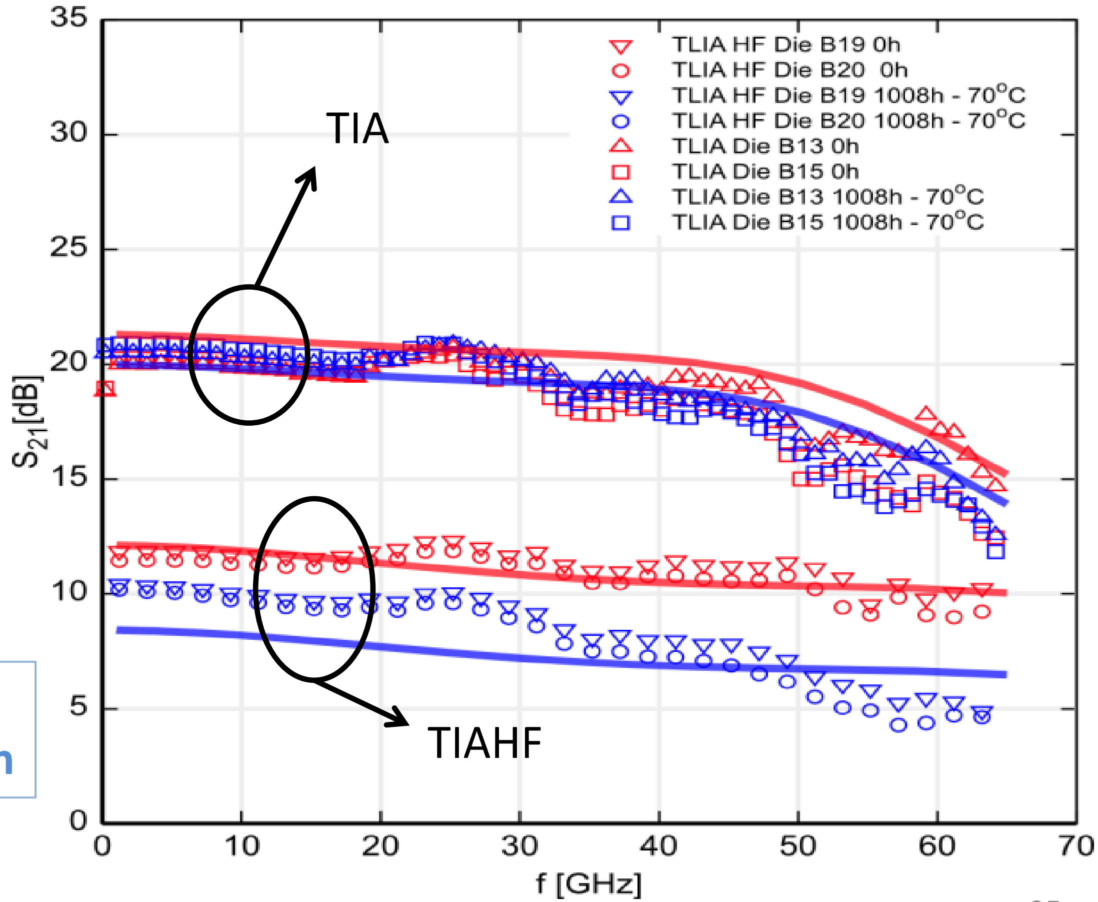
```
Alter:AGINGalter0 var="I182.I395.Q1.AGED_RE0" VarValue=1.051097526541248e+00
Alter:AGINGalter1 var="I182.I395.Q1.AGED_IS0" VarValue=2.296752299864880e-05
Alter:AGINGalter2 var="I182.I395.Q1.AGED_IBEIS0" VarValue=2.720339978065819e-02
Alter:AGINGalter4 var="I182.I414.Q1.AGED_IS0" VarValue=2.477855478244199e-03
Alter:AGINGalter5 var="I182.I414.Q1.AGED_IBEIS0" VarValue=1.822901099996015e+00
Alter:AGINGalter7 var="I182.I407.Q1.AGED_IS0" VarValue=1.003050582644627e-04
Alter:AGINGalter8 var="I182.I407.Q1.AGED_IBEIS0" VarValue=1.021350703026095e-01
Alter:AGINGalter10 var="I182.I408.Q1.AGED_IS0" VarValue=8.399430332061722e-05
..
```

METHODOLOGY VALIDATION

S parameters |S21| up to 65GHz

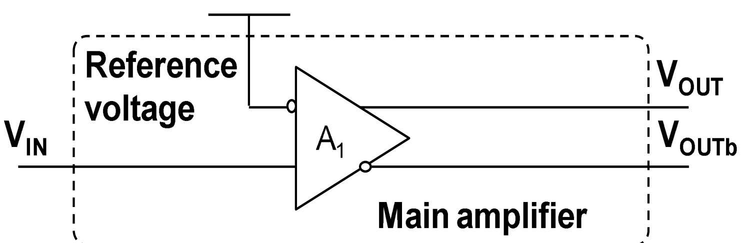
- Measurements versus simulations (Agilent ADS)
- Excellent initial model
- Slightly pessimistic aging
- But fairly accurate predictions

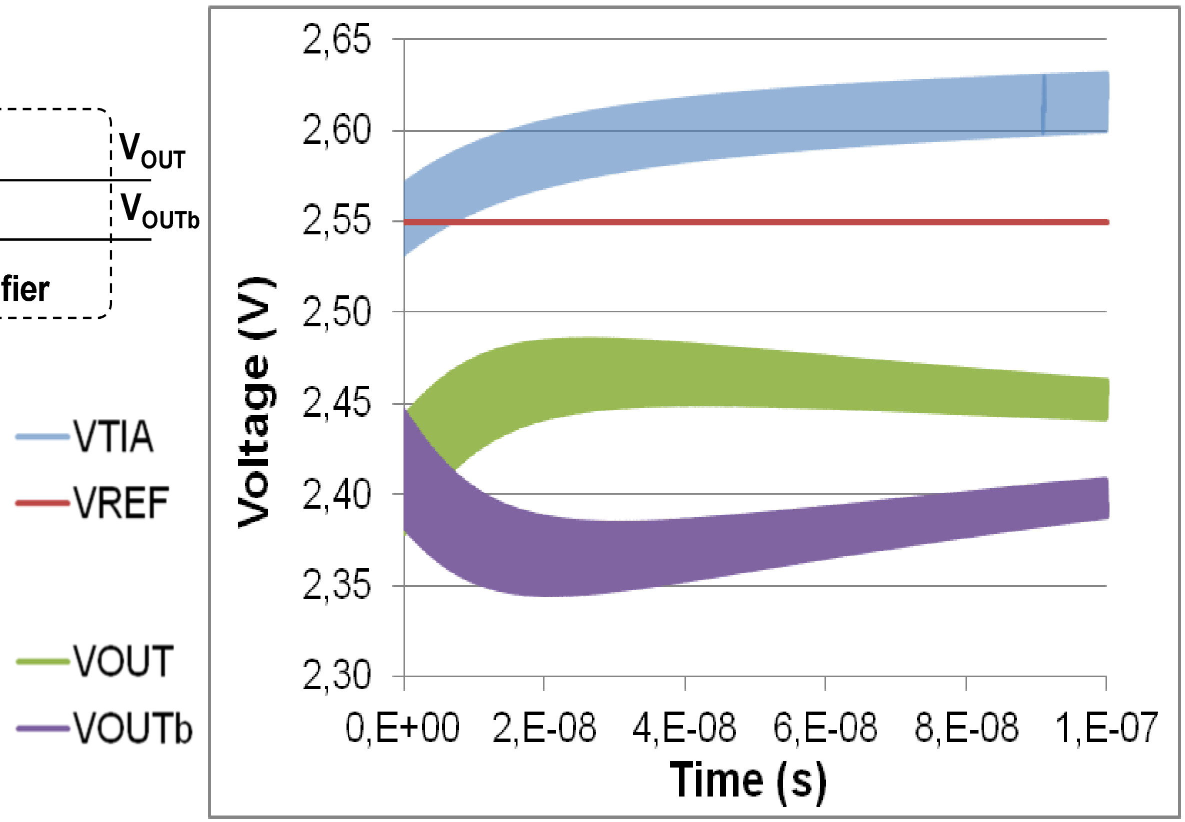
Perl scripting is used to automate aged circuit simulation



RELIABILITY AWARE DESIGN EXAMPLE

- TIA transiant simulations (Cadence spectre)
- No DC offset compensation loop

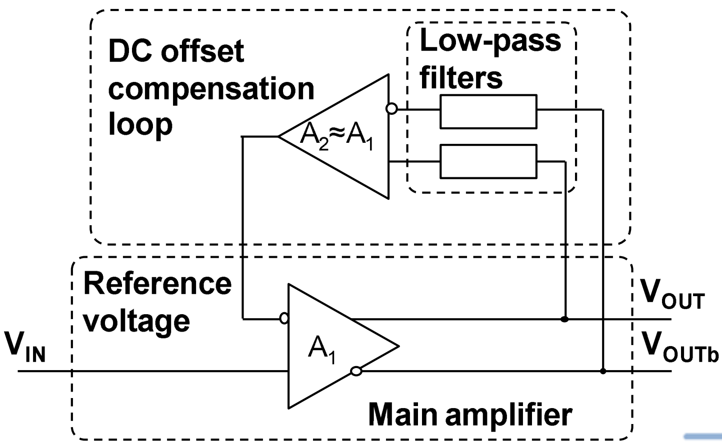


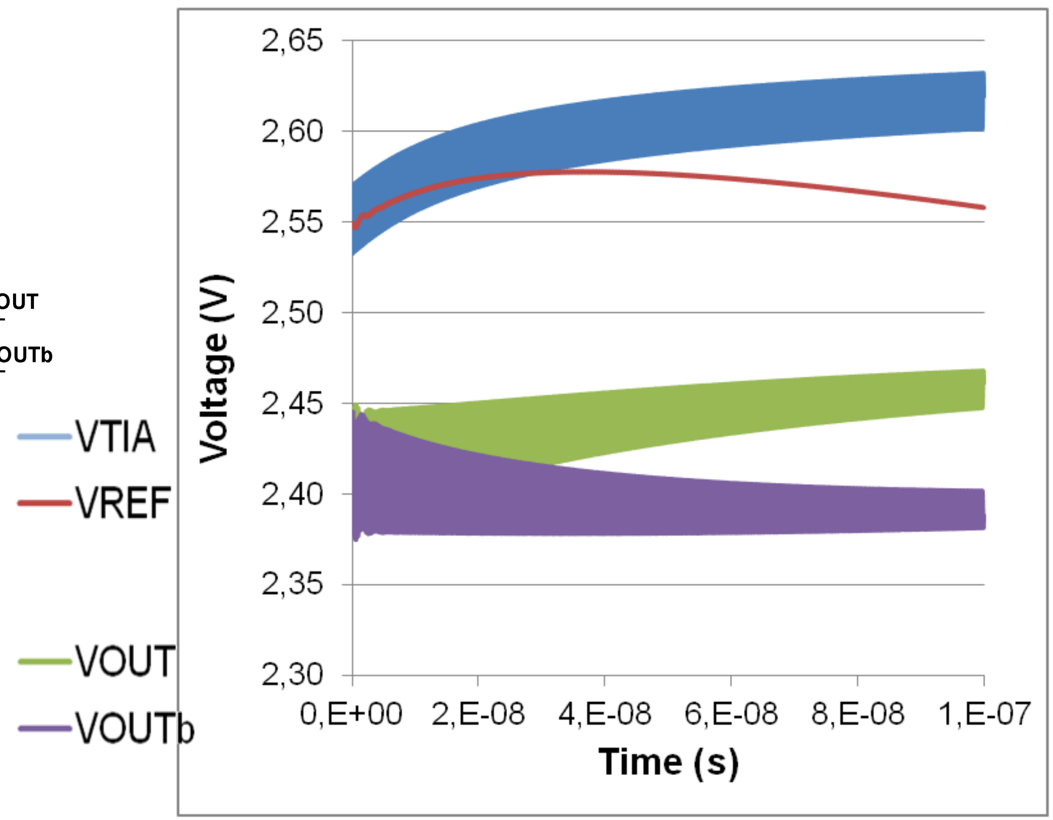


VREF is constant

RELIABILITY AWARE DESIGN EXAMPLE

- TIA transiant simulations (Cadence spectre)
- DC offset compensation loop with small gain

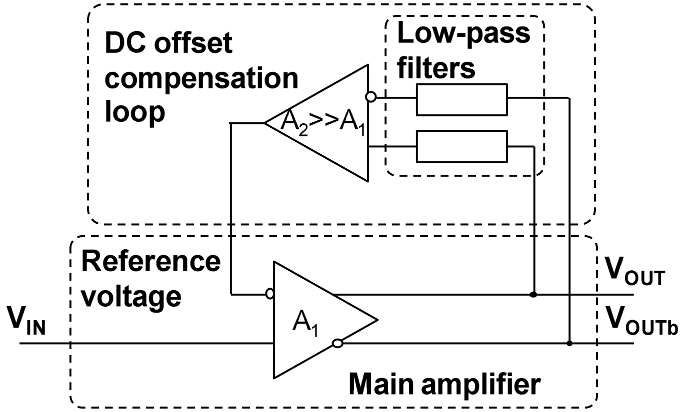


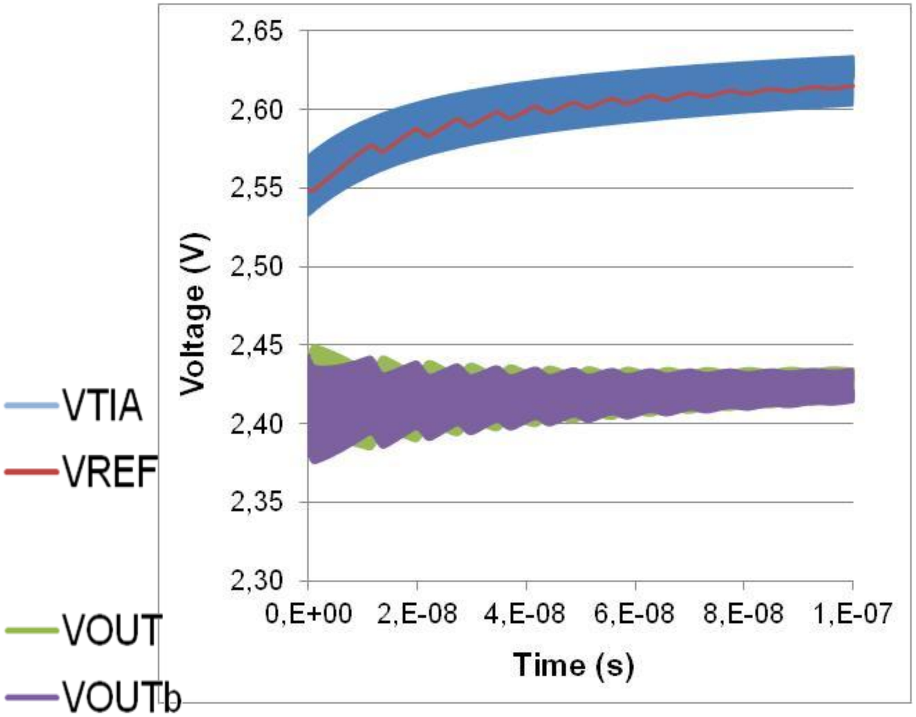


VREF can't follow VTIA over time

RELIABILITY AWARE DESIGN EXAMPLE

- TIA transiant simulations (Cadence spectre)
- DC offset compensation loop with high gain





VREF follows VTIA over time due to higher loop gain

Only the aging model allows understanding this phenomenon

CONCLUSION

- New method for device dynamic reliability simulation
- Straightfoward initial implementation in simulators (VerilogA)
- But good convergence properties needs careful rework
- Available in a standard PDK (easy to adopt)
- Simulates complex interactions between stress conditions (bias/temperature) and device degradations
- Methodology is physics based
- Validated at transistor level (InP/InGaAs HBT process)
- Validated at circuit level (24 transistors TIA – working above 100GHZ – complex offest compensation loops)
- Allows reliability aware circuit design
- Shortens reliability improvement feedback loops

AKNOWLEDGEMENT

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