Transistor's self-und mutual heating and its impact on circuit performance

M. Weiß, S. Fregonese, C. Maneux, T. Zimmer

26th BipAk, 15 November 2013, Frankfurt Oder, Germany
Outline

1. Motivation. Research overview
2. Device-level electrothermal investigations
3. Circuit-level electrothermal investigations
4. Conclusion. Future work.
Research Overview

Multi-transistor array

3D temperature distribution in a 3 finger multi-transistor array (Figure taken from “Electrothermal HBT modeling”, G. Wedel et al., HiCuM Workshop 2012)

Higher device temperature!

Thermal coupling effects!

ΔT (K)

ΔT

x
Outline

1. Motivation. Research overview

2. Device-level electrothermal investigations

3. Circuit-level electrothermal investigations

4. Conclusion. Future work.
Thermal Coupling Network

- $P \rightarrow$ power dissipations (Current)
- $R_{th} \rightarrow$ thermal resistances
- $\Delta T \rightarrow$ temperature increase (Voltage)
Thermal Coupling Network

- \( P_1, P_2 \rightarrow \) power dissipations
- \( R_{th\_11}, R_{th\_22} \rightarrow \) self-heating thermal resistances
- \( c_{12}, c_{21} \rightarrow \) mutual thermal coupling factors
- \( \Delta T_1, \Delta T_2 \rightarrow \) temperature increase in the transistors

Test Structure

Inter Device Coupling

Intra Device Coupling

Test structure

Micrograph
Temperature Measurement

Intra device coupling in multi-finger transistor

Inter device coupling in multi-transistor array

Distance D between deep trench

Wafer
T=300K

T4 is heating

$\Delta T$ in T1 @ 300K, T4 heating
$\Delta T$ in T2 @ 300K, T4 heating
$\Delta T$ in T3 @ 300K, T4 heating

$\Delta T[K]$ vs. $P_{\text{diss}}[\text{mW}]$ for different distances D:
- D=1.5µm
- D=3µm
- D=5µm
Coupling Factors

Intra device coupling in multi-finger transistor

Inter device coupling in multi-transistor array with distance $D=1.5\mu$m
3D Thermal Simulation

Intra device coupling in multi-finger transistor

\[ C_{XY} = \frac{dT_X}{dT_Y} \frac{dP_Y}{dP_X} = \frac{R_{th,XY}}{R_{th,YY}} \]

X – Sensing
Y – Heating

Model Verification

Output characteristics for 5 devices operating parallel

Intra device coupling in multi-finger transistor

Inter device coupling in multi-transistor array, D=1.5µm

Outline

1. Motivation. Research overview
2. Device-level electrothermal investigations
3. Circuit-level electrothermal investigations
4. Conclusion. Future work.
Ring Oscillator: Optimization

Specifications
• 53 CML Inverter
• Voltage Swing: 200mV

Variables
• Transistor Configuration
• Emitter Length $L_E$
• Current Source $I_0$
• Resistance $R_L$

Propagation Delay
$$t_p = \frac{1}{2 \cdot 53 \cdot f_{osc}}$$

Simplified CML Inverter

![CML Inverter Diagram]
Fabricated RO including 53 CML inverter stages and a temperature sensor

Wafer map of the gate delay, HBT 0.18x5µm², $I_{\text{gate}}=12.5\text{mA}$

Ring Oscillator: Circuit temperature

Measured and simulated circuit temperature vs. $I_{\text{gate}}$

$\tau_{\text{gate}}$ vs. $I_{\text{gate}}$: Measurements (symbols) and HICUM simulation (solid lines)

Ring Oscillator: Coupled Simulation

\[ \Delta T_{3} [K] \]

\[ \Delta T_{5} [K] \]

\[ t [\text{ns}] \]

\[ \tau_{\text{gate}} [\text{ps}] \]

\[ I_{\text{gate}} [\text{mA}] \]
Power amplifier

- A five-finger transistor and five transistor array are operated as a PA
- Each emitter has a drawn emitter area $A_E=5\times0.18\mu m^2$
- Matching with load-pull tuners
Power amplifier: Single transistor

Compact model verification: Comparison simulation vs. power measurements for 1 transistor

\[
\begin{align*}
P_{\text{out}}, \text{Gain}, \text{PAE} & \text{ vs. } P_{\text{in}} \text{ in matched condition} \\
\text{Load pull contours for constant power gain}
\end{align*}
\]
Power amplifier: Transistor array

- Characteristics of both devices are close at low power dissipation
- At higher bias ($V_{BE}=0.9\,\text{V}, V_{CE}=1.5\,\text{V}$) significant performance degradation of the multi-finger transistor due to thermal coupling
- Good agreement with circuit simulations in both cases
Outline

1. Motivation. Research overview
2. Device-level electrothermal investigations
3. Circuit-level electrothermal investigations
4. Conclusion. Future work.
Conclusion (1/2)

• Novel test structures to characterize thermal coupling of state of the art trench isolated SiGe HBT technology
• Thermal coupling factors were extracted from multi-finger transistor (INTRA) and multi-transistor array (INTER)
• Standard thermal network has been replaced by distributed networks in order to model accurately thermal impedance and thermal coupling between neighboring devices
• The models were implemented as netlist in Agilent ADS (easy to use for circuit designers)
Conclusion (2/2)

• Electrical performance of the multi-finger transistor is degraded due to the significant thermal coupling effect between the emitter stripes.

• Coupled simulation accurately predict thermal effects in multi-finger SiGe HBTs, often used for high speed applications due to lower input resistance and capacitance.

• Model has been already successfully applied for two circuits (PA and of a RO with 218 transistors).

• Device performance is often limited by thermal effects rather than the electronic limitations → circuit designers need accurate models to exploit full potential of a technology.
Future work

• Thermal stability can be improved, access to the thermal nodes of each finger allows to estimate ballasting resistors
• The thermal stability in multiple-finger transistors can be increased by adjustment of emitter to emitter distances to make the spatial temperature distribution across the device approximately uniform
• Thermal coupling capacitances should be considered in a next step
• Parameter extraction based on isothermal pulsed DC/RF measurements
Acknowledgement

• This work is part of the:

• DOTSEVEN project supported by the European Commission through the Seventh Framework Programme for Research and Technological Development.

• Acknowledgements to Catrene “RF2THz” project

• We want to thank ST microelectronics for helpful discussions and PDK support