Integrated IGBTs: Challenges in Characterization and Modelling

- AK-Bipolar Workshop 2015
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*igbt = insulated gate bipolar transistor
Wiki about igbt (->insulated-gate bipolar transistor):

The IGBT combines the simple gate-drive characteristics of the MOSFETs with the high-current and low-saturation-voltage capability of bipolar transistors. The IGBT combines an isolated gate FET for the control input, and a bipolar power transistor as a switch, in a single device. The IGBT is used in medium- to high-power applications like switched-mode power supplies, traction motor control and induction heating.

- customers demanded igbts in XFABs SOI technologies
Introduction

- igbt are often used as discrete devices
- integrated igbt are developed by XFAB for different SOI processes
- intended for low ohmic switching with high current capability
- -> customers need models to do their circuit design*

BUT:
- NO CMC model for IGBT released yet
- NO compact model available in ALL mainstream simulators
- Verilog-A implementation would have some drawbacks
- HiSIM_IGBT: available in ELDO (V1.2) and Spectre (V1.0), but NO HSPICE
- BUT still development status
- BAD convergence behavior in real circuits
- NO free code (C- or Verilog-A) available
- Our solution: SUBCIRCUIT model

*XFAB CTO’s statement: “... a device without a model makes no sense at all ..."
Example

(a) MOSFET part

(b) MOSFET part
Model Structure HiSIM_IGBT

- igbt has 3 terminals (Collector, Gate, Emitter)
- 4 terminals (Collector, Gate, Emitter, and Base) are considered in HiSIM_IGBT
- based on the MOSFET-model framework of HiSIM_HV
- drain contact of MOSFET is treated as the base terminal in HiSIM_IGBT
  The terminal is NOT a real external node, however an important model-
  internal node!
- the base potential can be observed through circuit simulations
- users have to treat the model as a four-terminal device and let the base
  terminal float by connecting a zero-ampere current source between the
  base terminal and the ground, or by not connecting any circuit element
  to the base terminal!

Warning:
Notice from spectre during topology check.
Only one connection to node `XCKT.b1'.

Bad convergence observed in transient simulation!
Model Structure HiSIM_IGBT

model like HiSIM_HV, BUT:
• Source/drain drift resistances \( r_d \), \( r_{dvd} \), etc...
• Gate resistance (RF)
• Bulk resistance network (RF)
• NQS effect (transient)
• Substrate leakage current
• Gate leakage currents
• Gate-induced drain leakage currents
• Noise

inactivated!
Basic Model Structure Subckt model

HiSIM_HV model

VBIC model
Extraction Strategy

1. Implement correct subckt (take care of Body node!)
2. Include geometrical parameters from layout (Base width!)
3. Extract CV of gate oxide (as for MOSFET)
4. Extract CV of junctions (as for BJT)
5. Start transient extraction (as first guess)
6. Transfer curve and output (pulsed IV) fitting at $T=TNOM$ of large device
7. Check DC output curve + transfer large device
8. Iterative 4) -> 6)
9. Include scaling (Width)
10. Temperature extraction
Additional parameters in the HiSIM_IGBT model

HiSIM_IGBT Model Parameters for the BJT Part:

- **BJTNINJ** - Electron injection into the depletion layer
- **BJTNINJMAX** - Parameter for $W_{dep}$
- **BJTWDEPMAX** - Parameter for $W_{dep}$
- **BJTMUEP** - Hole mobility in the quasi-neutral region
- **BJTMUEN** - Elec. mobility in the quasi-neutral region
- **BJTMUEQN** - Parameter for mobility
- **BJTTAUE** - Basic lifetime in the emitter
- **BJTTAUB** - Basic lifetime in the base
- **BJTTAUC** - Basic lifetime in the collector
- **BJTNREF** - Reference doping concentration
- **BJTGMINC** - Coefficient for minimum conductance
- **BJTGMIN** - Coefficient for minimum conductance
- **BJTLDEC** - Parameter for excess carrier distribution
- **BJTPMIN** - Minimum carrier density in the base
- **BJTRB** - Coefficient for base resistance
- **BJTRBVG11** - Gate-voltage dependence on $R_{Base}$
- **BJTRBVG12** - Gate-voltage dependence on $R_{Base}$
- **BJTRC** - Collector resistance
- **BJTRE** - Emitter resistance
- **BJTQDEP** - Coefficient for $Q_{dep}$
- **BJTQEX** - Coefficient for $Q_{excess}$
Parameters to set from layout

- TOX, TPOLY as MOSFET
- W,L,M, NRD, NRS, AD, AS, PD, PS as MOSFET
- LOVERLD, XLDDL - > compare with CV
- BJTWDEPMAX - > important: \(\sim\) base width (HiSIM_IGBT)
- ignore LDRIFT...has no meaning here!

BJTWDEPMAX is \(\sim\) base width
Measurements and Simulation: DC, pulsed IV

- pulsed IV is VERY important
- transient is VERY important
- Very high currents -> take care of parasitic series resistance (needles, wiring)

DC

Pulsed IV

- can be modelled by „HiSIM_IGBT V1.2“
  and also by „Spice-SUBCKT“ model (shown here)
Measurements and Simulation: CV, transient

-> can be modelled by „HiSIM_IGBT V1.2“
and also by „Spice-SUBCKT“ model
**Summary**

> we have tested “HiSIM_IGBT” and a “Spice-SUBCKT-IGBT” model
> extraction flow is established, but tricky!
> some customer already complained about HiSIM_IGBT (bad convergence)
> “Spice-SUBCKT-IGBT” has better convergence
> simulator status HiSIM_IGBT hspice (NO); spectre (only V1.0) and ELDO (V1.2) will not be changed in medium time scale
> “HiSIM_IGBT” V1.2 is needed
> No free source code available
> Much better accuracy with „Spice-SUBCKT-IGBT“ model achieved

> Spice SUBCKT model is better alternative!
Add: Verilog-A

> in Verilog-A there are 2 igbts models free available: 1) Lauritzen model (Washington State Uni.) or 2) Cambridge Uni. model,

> they work in principle, BUT:
- more intended for discrete devices
- big effort to extract and check for all simulators
- not all effects are included
- simulation speed reduced
- not well accepted at customer side
- not easy to get latest Code
- no good documentation ... etc ...
Version 1.1 Enhancements
• Including the temperature dependence of the base resistance model.
• Adding the effect of the collector-emitter leakage current and its temperature dependence.
• Adding some bug fixes for the self-heating model.

Version 1.2.0 Enhancements
• NQS effect is introduced to the excess charge ...
• Add BJTWBUFF for the buffer length.
• Add TOXEDGE for the gate-edge MOS capacitor.
• Add SHEMAX to limit the self-heating effect (SHE).
• Add GMINSCALE to reduce too large gmin current in some cases.
• Change default values of some model parameters.
• Add OP functions.
• Disable unnecessary memory allocations for b-c and bP-c elements.
• Correction of two floating-point-exception (FPE) errors (about Ninj and Wdep bc).
• Correction of the AC load function for the self-heating-effect (SHE) model.
• Correction of bP-g and bP-e entries in the AC load function.