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Aging modeling of an LDMOS device using the new built-in age model of HiSIM HV 2.4.

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Content

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- Introduction to HiSIM HV 2.4 aging model
- Aging simulation procedure
- Aging experiment with LDMOS devices
- Extraction of model parameters
- Modification of model code
- Summary

Aging regions in HiSIM HV 2.4 model

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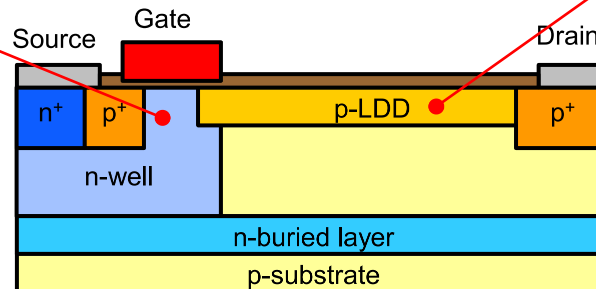
The HiSIM HV model is a compact simulation model for high voltage MOS transistors (HiSIM = Hiroshima-university STARC IGFET Model). The HiSIM HV 2.4 simulation model covers two regions where aging takes place in a Power MOSFET.

Channel region

- Hot electron induced (HCI)
  - Shallow Trap Level
  - Deep Trap Level
- Negative (positive) bias temperature instability N(P)BTI

Drift region

- Ndrift (Impurity concentration of drift region)



[1] HiSIM HV 2.4.0 User's Manual, © 2017, Hiroshima University & STARC, T. Iizuka, H. Kikuchihara, H. Miyamoto, M. Miyake, H. J. Mattausch, M. Miura-Mattausch

Channel region, HCI

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The HCI aging mechanism in HiSIM HV 2.4 is modeled as an increase of the trap density N_{tA}. N_{tA} is an essential part of the iteratively solved surface potential based formulation of HiSIM HV:

$$\nabla^2 \phi = -\frac{q}{\epsilon_{Si}} (p - n + N_{\mathrm{D}} - N_{\mathrm{A}} - \boxed{N_{\mathrm{tA}}})$$

Therefore, a change of N_{tA} will automatically affect the complete model behavior.

Two trap density distributions are considered, the shallow and the deep level, where the deep trap level is considered to be responsible for the aging.

Aging as a function of substrate current

Apply stress in: DC simulations:

$$I_{\mathrm{sub}}{}' = I_{\mathrm{sub}}$$

Requires good internal I_{sub} modeling !

Transient simulations:

$$I_{\mathrm{sub}}{}' = \frac{\sum^{\mathbf{DEGTIME0}} I_{\mathrm{sub}}}{\mathbf{DEGTIME0}}$$

Aging integration is done inside the model!

Time independent part of aging

Shallow trap level:

$$N_{0,2} = \mathbf{TRAPGC2} \cdot \mathbf{TRAPES2} \frac{\frac{kT}{\mathbf{TRAPES2}}}{\sin \frac{kT}{\mathbf{TRAPES2}}}$$

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Channel region, HCI (2)

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Time dependent part of aging

Deep trap density

$$g_{c1,\mathrm{deg}} = \mathbf{TRAPGC1} + \frac{\mathbf{TRAPGC1MAX}}{gc,time1} \exp\left[-\frac{1}{2}\left(\frac{gc,time - gc,time2}{gc,time1}\right)^2\right]$$

$$gc,time = \ln\left(I_{\mathrm{sub}}' \cdot \mathbf{DEGTIME}/W\right)$$

$$gc,time1 = \ln\left(I_{\mathrm{sub}}' \cdot \mathbf{TRAPGCTIME1}/W\right)$$

$$gc,time2 = \ln\left(I_{\mathrm{sub}}' \cdot \mathbf{TRAPGCTIME2}/W\right)$$

Shallow trap density

$$E_{s1,\mathrm{deg}} = \mathbf{TRAPES1} + \frac{\mathbf{TRAPES1MAX}}{gc,time1} \exp\left[-\frac{1}{2}\left(\frac{es1,time - es1,time2}{es1,time1}\right)^2\right]$$

$$es1,time1 = \ln\left(I_{\mathrm{sub}}' \cdot \mathbf{TRAPESTIME1}/W\right)$$

$$es1,time2 = \ln\left(I_{\mathrm{sub}}' \cdot \mathbf{TRAPESTIME2}/W\right)$$

$$N_{0,\mathrm{limit}} = \mathbf{TRAPGCLIM} \cdot \mathbf{TRAPESLIM} \frac{\frac{kT}{\mathbf{TRAPESLIM}}}{\sin\frac{kT}{\mathbf{TRAPESLIM}}}$$

Degradation time (DEGTIME)

Time at which
- observable aging starts (TRAPGCTIME1)
- aging enhancement ends (TRAPGCTIME2)

Limits for aging (TRAPGCLIM · TRAPESLIM)

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Channel region, N(P)BTI

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Hole trapping at Si/Oxide interface is modelled as a shift of the threshold voltage

$$\delta V_{\mathrm{th,trap}} = \mathbf{TRAPA} \cdot \exp\left(\mathbf{TRAPB} \cdot E_{\mathrm{ox}}\right) \cdot \left[1 - \exp\left(-\frac{t_{\mathrm{s}}}{\mathbf{TRAPBTI}}\right)\right]$$

$$E_{\mathrm{ox}} = \frac{V_{\mathrm{Gon}} - \delta V_{\mathrm{th,trap}} - \phi_{\mathrm{S}}}{T_{\mathrm{ox}}}$$

$$t_{\mathrm{s}} = T_{\mathrm{cycle}} \cdot \mathbf{DEGTIME}$$

Tcycle is calculated by integrating the stress time during circuit operation for a long DEGTIME0.

“The present implementation focuses on long-term aging, and no trap emission in included.” [1]

→ There may be no relaxation of NBTI effects. We have not tried this.

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Drift region

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At high Vds, the electric field in the drift region increases, which results in impact ionization.
Aging modeling of this effect is done through the carrier density change.

$$N_{\mathrm{drift}} = \mathbf{NOVER}\left\{1+\mathbf{RDRCAR}\left(\frac{V_{\mathrm{ddp}}}{L_{\mathrm{drft}}-\mathbf{RDRDL2}}\right)\left(1-\frac{1}{1+\frac{\mu_{\mathrm{drift0}}}{V_{\mathrm{max_drift}}}\cdot\frac{V_{\mathrm{ddp}}}{L_{\mathrm{drift}}}}\right)\right\} + \left(\mathbf{RDRQOVER}\frac{-Q'_{\mathrm{over}}}{q}\right) + \mathbf{NOVER}\cdot D_{\mathrm{vddp}}$$

Standard equation in HiSIM HV

Extension for aging

$$D_{\mathrm{vddp}} = D_{\mathrm{vddp,deg}}\cdot\exp\left(-\frac{V_{\mathrm{dseff}}-\phi_{\mathrm{SL}}+\phi_{\mathrm{S0}}}{\mathbf{TRAPDLX}}\right)$$

$$D_{\mathrm{vddp,deg}} = \mathbf{TRAPDVDDP} + \frac{\mathbf{TRAPD1MAX}}{time1}\exp\left[-\frac{1}{2}\left(\frac{time-time2}{time1}\right)^2\right]$$

$$time = \ln\left(I_{\mathrm{ds}}{}'\cdot\mathbf{DEGTIME}/W\right)$$

$$time1 = \ln\left(I_{\mathrm{ds}}{}'\cdot\mathbf{TRAPDTIME1}/W\right)$$

$$time2 = \ln\left(I_{\mathrm{ds}}{}'\cdot\mathbf{TRAPDTIME2}/W\right)$$

Simulations:

DC:

$$I_{\mathrm{ds}}{}' = I_{\mathrm{ds}}$$

Transient:

$$I_{\mathrm{ds}}{}' = \frac{\sum^{\mathbf{DEGTIME0}} I_{\mathrm{ds}}}{\mathbf{DEGTIME0}}$$

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Aging Simulation

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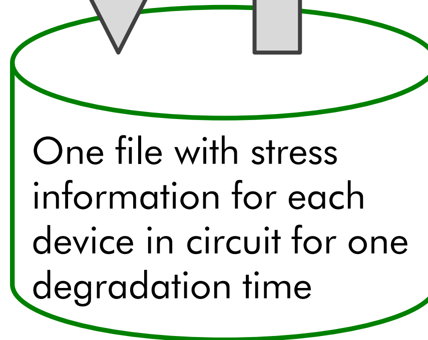
Doing reliability simulation with the built-in HiSIM HV 2.4 aging model requires 2 simulation runs:

Stress simulation

- Devices are stressed
- Possible analyses:
  - DC
  - transient



Post stress simulation

- Devices are aged
- Any kind of analysis is possible

Aging Simulation

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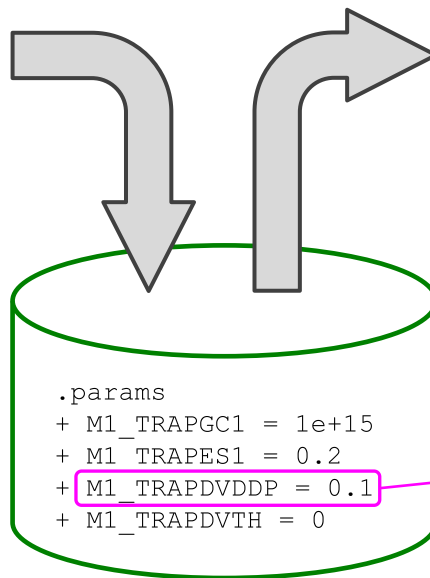
DC stress simulation

```
* Voltage sources with stress values
vd d 0 DC=10
vg g 0 DC=1

.model nmos hisim_hv_va TYPE=1
+ CODEG     = 1 * Stress
+ TRAPDVDDP = 0.05
+ TRAPDTIME1= 10

M1 d g 0 0 nmos l=0.5u w=20u
+DEGTIME=1e5
```



Post stress simulation

```
* Voltage sources circuit
vd d 0 DC=1
vg g 0 DC=1

.model nmos hisim_hv_va TYPE=1
+ CODEG     = 0 * Post stress
+ TRAPDVDDP = 0.05
+ TRAPDTIME1= 10

.include age_file

M1 d g 0 0 nmos l=0.5u w=20u
+ TRAPGC1 = M1_TRAPGC1
+ TRAPES1 = M1_TRAPES1
+ TRAPDVDDP = M1_TRAPDVDDP
+ TRAPDVTH = M1_TRAPDVTH
```

Intermediate file:

- Contains degradation time and 4 parameters for each transistor.
- Each parameter for a specific aging effect: HCI deep trap, HCI shallow trap, R_{drift}, NBTI
- Parameters describe the effective aging after "degtime"

- Model parameters and effective aging values share the same name.
- Model parameters are overloaded by effective aging values directly assigned to each device.

Aging Simulation

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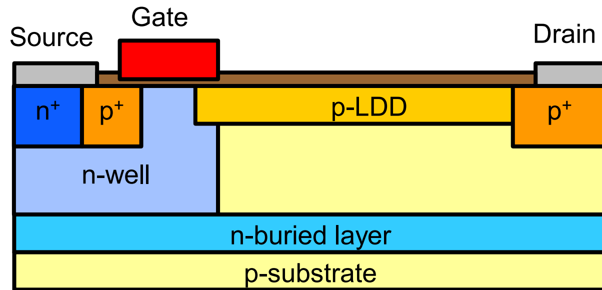
Intermediate file details:

- ASCII
- Is generated by the Verilog-A code of the model
- Currently in HSPICE format, needs to be adjusted for other simulators.
- Contains effective aging values plus all other model parameters and bias information

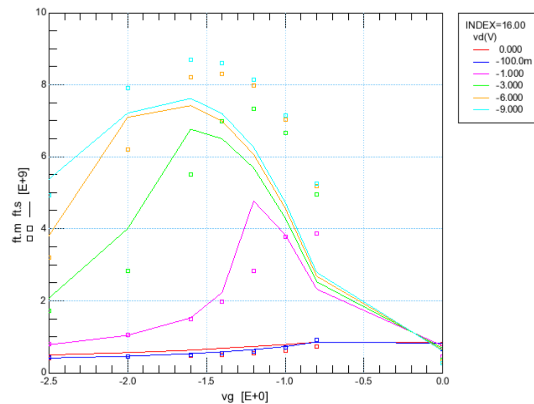
Post stress simulation:

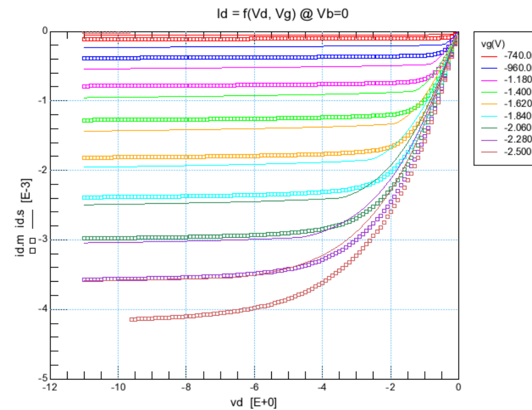
- Flag codeg =0 sets effective aging time to 0 and the effective aging values of the intermediate file replaces the model parameters in the aging equations.
- This procedure is not fully documented in the model manual and can only be seen by looking at the Verilog-A code.

Example: PLDMOS

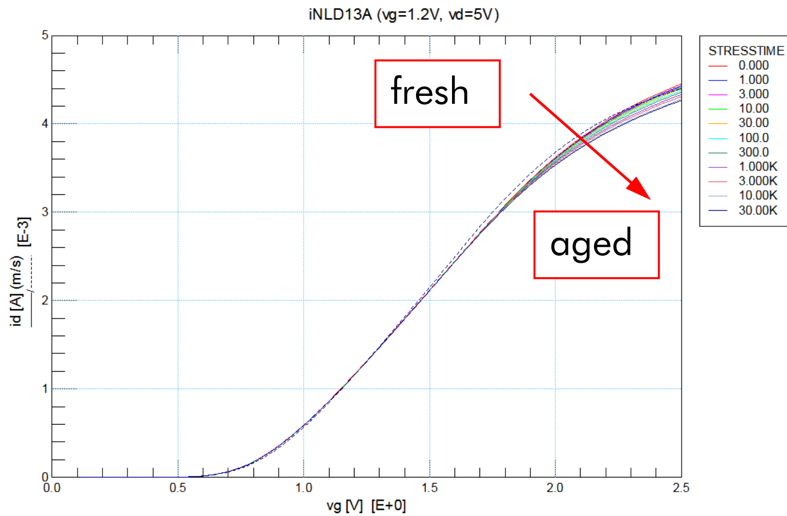


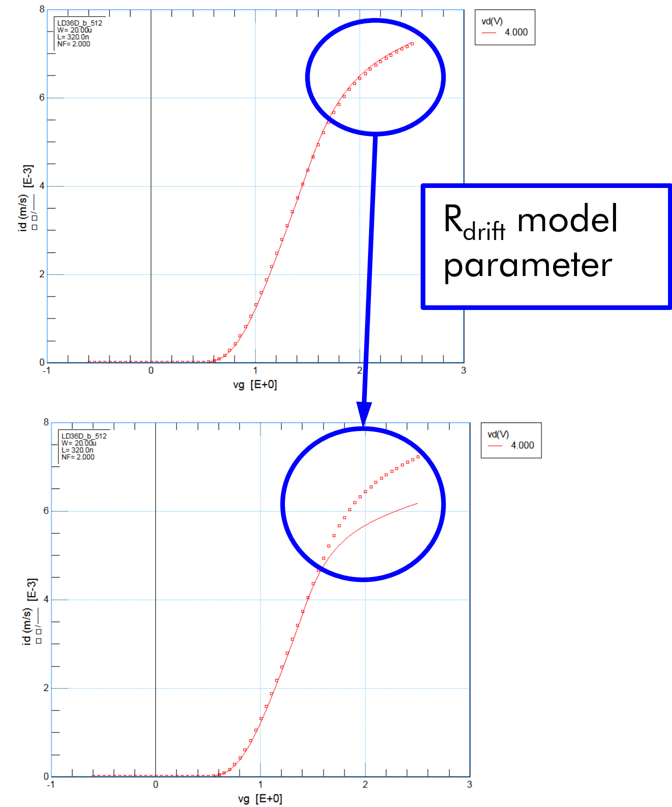
- The task is to implement an aging model to a set of LDMOS device types (PLDMOS, NLDMOS, iNLDMOS).
- All devices uses HiSIM HV models
- The first attempt was to use Cadence RelExpert but it turned out, that the HiSIM HV is obviously not supported.





Aging effects visible in the LDMOS





Aging effects:

- No Vth shift visible
- Simulation experiment insists that the aging of the drift region may be the main aging effect.

Aging effects visible in the LDMOS

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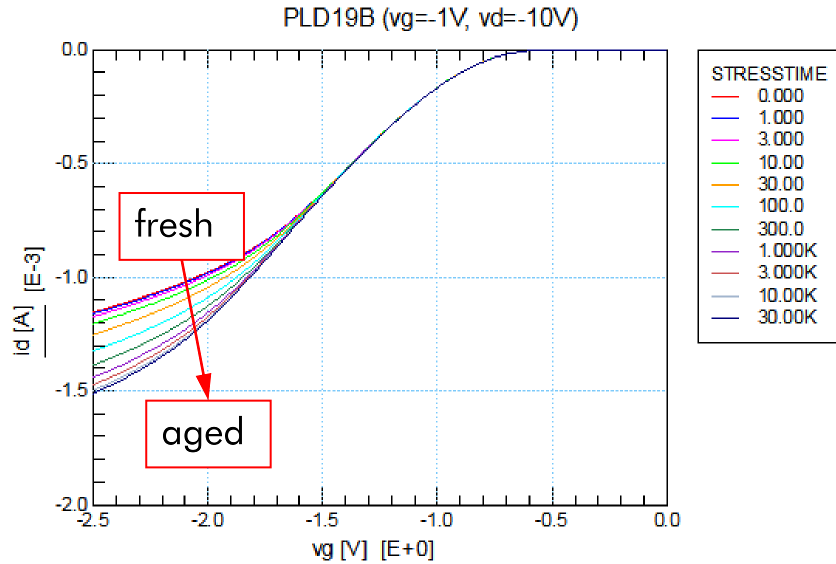
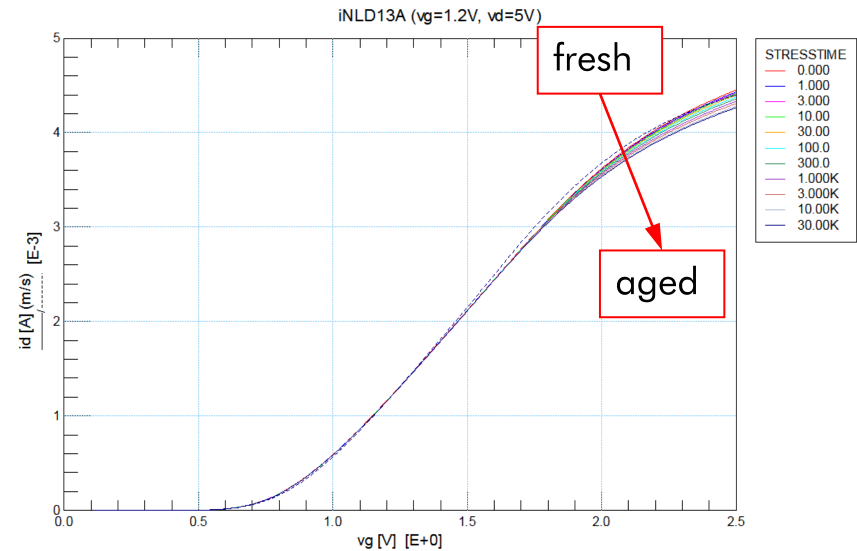


PLDMOS

- Negative degradation of current with longer stress time
- Current increases with longer stress time !

NLDMOS

- Degradation of current with longer stress time.



Aging modeling of PLDMOS with HiSIM HV 2.4

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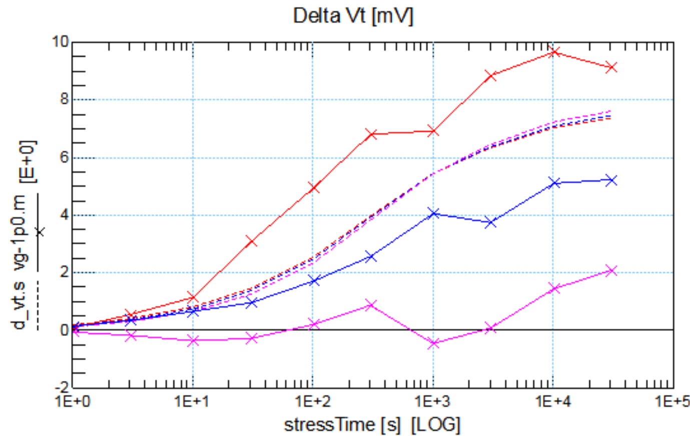
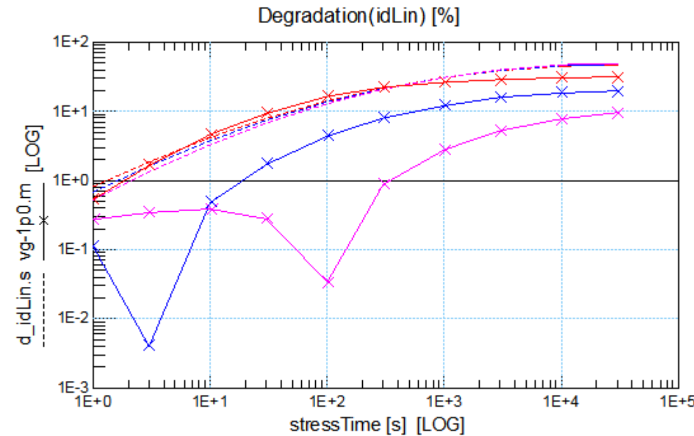
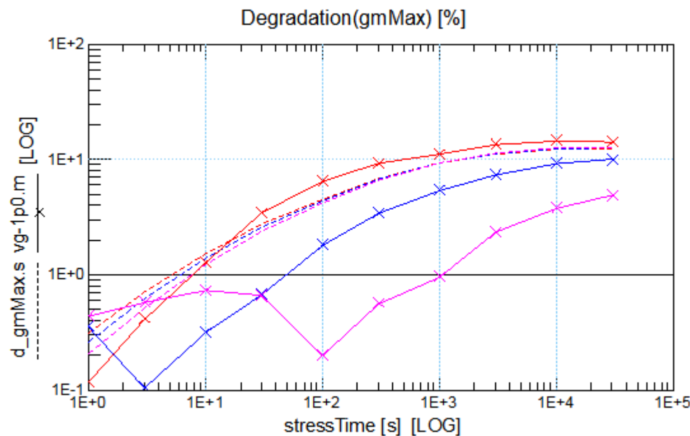
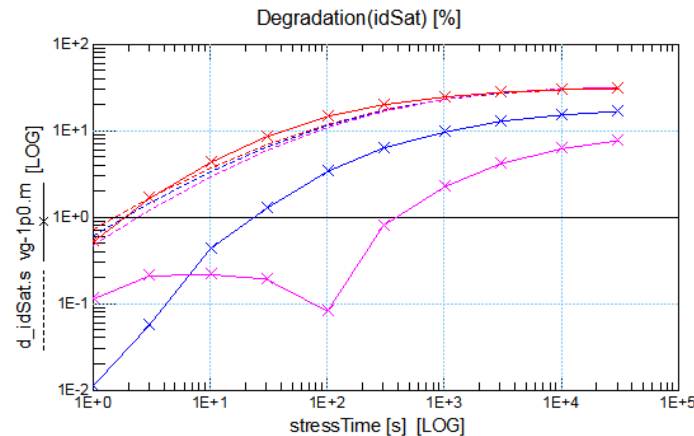




stressVd(V)
-10.00
-9.000
-8.000





Aging modeling

- Procedure was implemented in IC-CAP.
- PCM like values: $V_{t(gmmax)}$, I_{dlin}, I_{dsat}, g_{mmax}, have been extracted from aging measurements with constant stress
- HiSIM HV aging parameters are used to adjust aging behavior.

Aging modeling of PLDMOS with HiSIM HV 2.4

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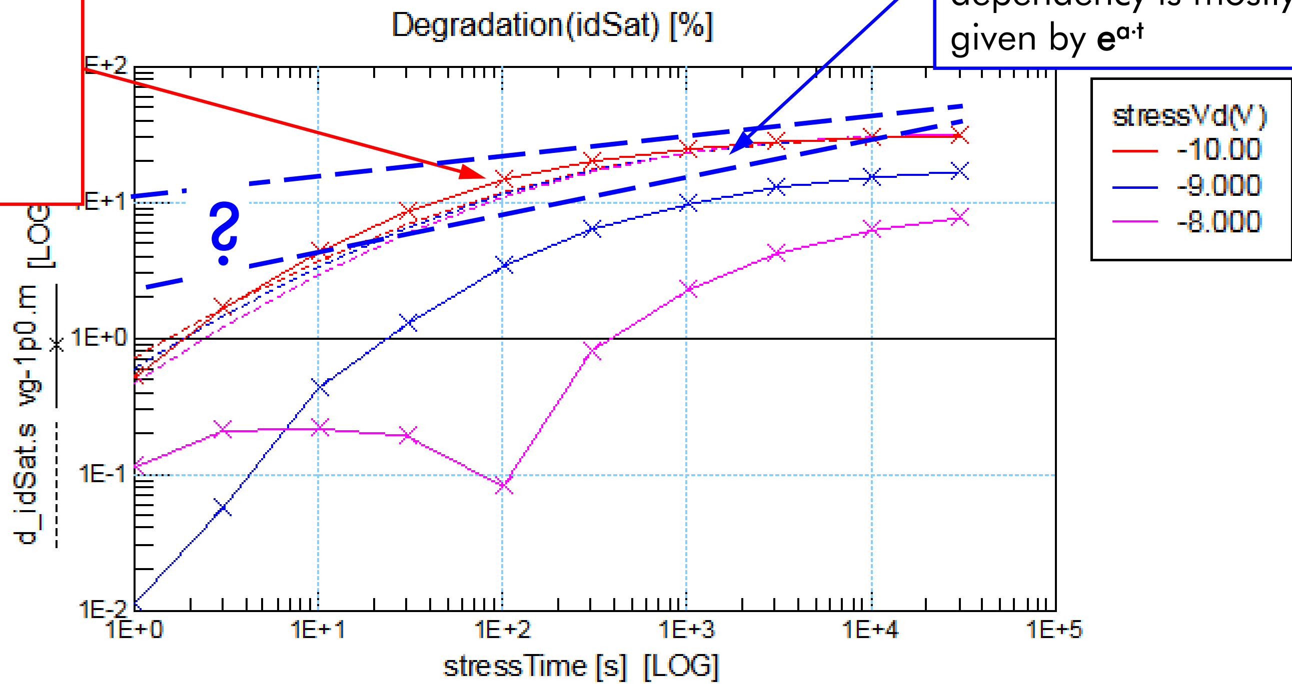
Time dependency through:

- TRAPDTIME1
- TRAPDTIME2

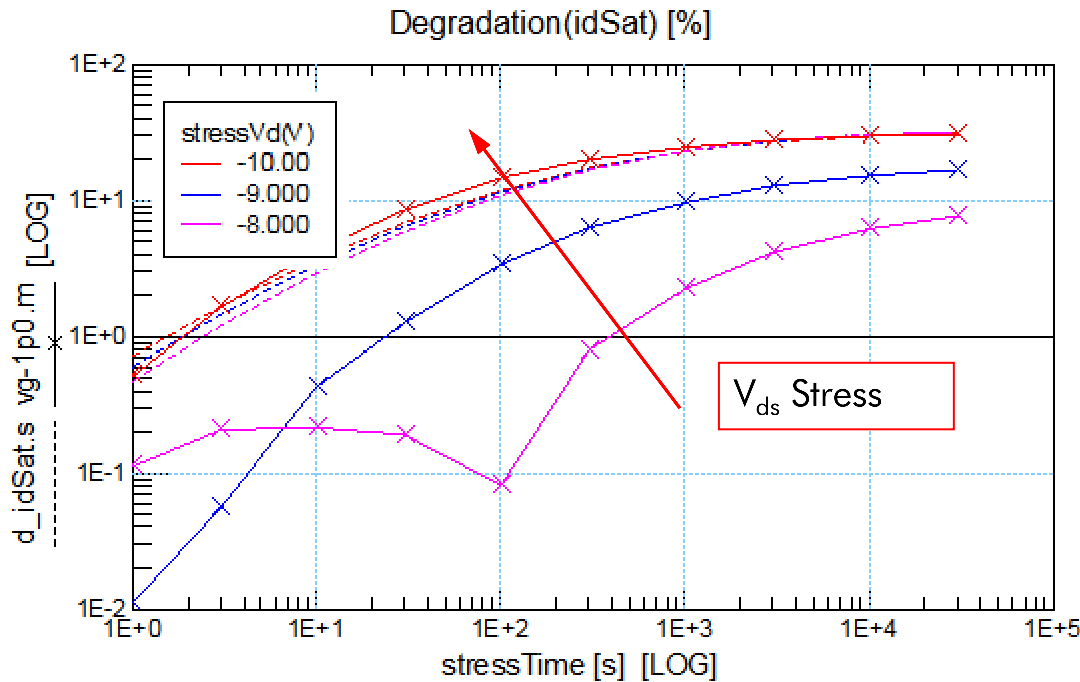
Starting time and saturation time



In conventional aging equations, time dependency is mostly given by $\mathbf{e}^{a \cdot t}$

Aging modeling of PLDMOS with HiSIM HV 2.4

AdMOS



V_{ds} stress dependency

$$D_{\mathrm{vddp}} = D_{\mathrm{vddp,deg}} \cdot \exp\left(\frac{V_{\mathrm{dseff}} - \phi_{\mathrm{SL}} + \phi_{\mathrm{S0}}}{\mathbf{TRAPDLX}}\right)$$

$$V_{\mathrm{dseff}} = V_{\mathrm{ds}} - I_{\mathrm{ds}} \cdot (R_{\mathrm{s}} + R_{\mathrm{drift}})$$

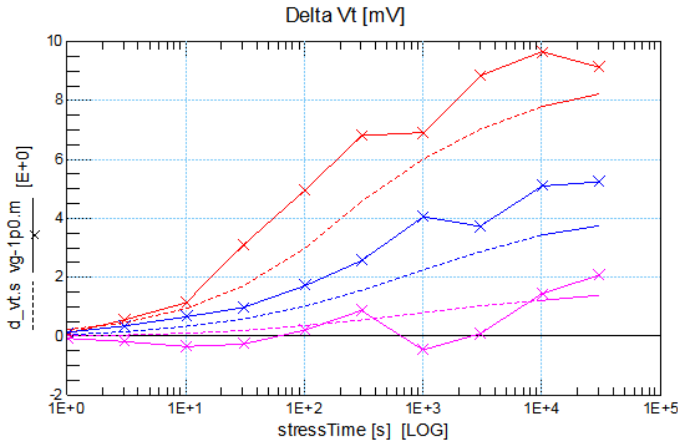
V_{dseff} determines the electrical field inside the intrinsic transistor. It is roughly constant in saturation.

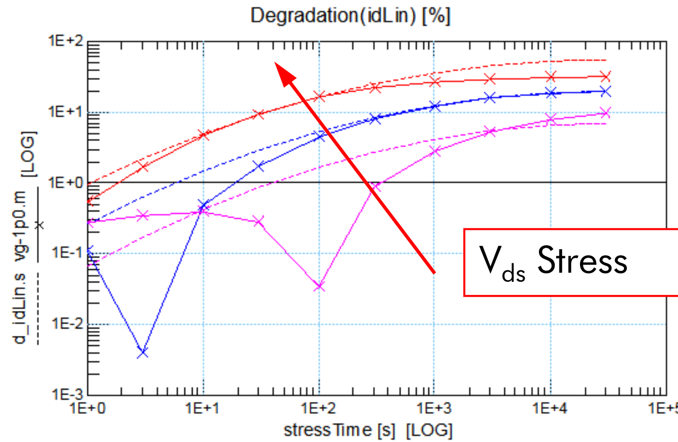
As the degradation happens in the drift region, the electrical field over the drift region is determined by:

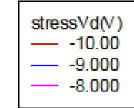
V_{ds} - V_{dseff}.

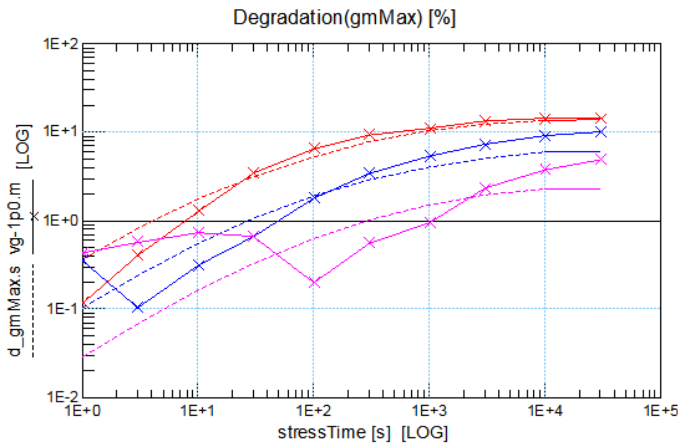
→ Therefore, V_{dseff} is replaced by V_{dse}.

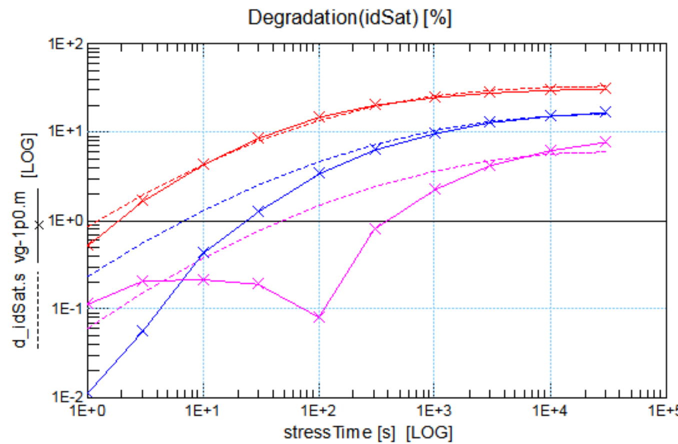
Aging modeling of PLDMOS with modified HiSIM HV 2.4











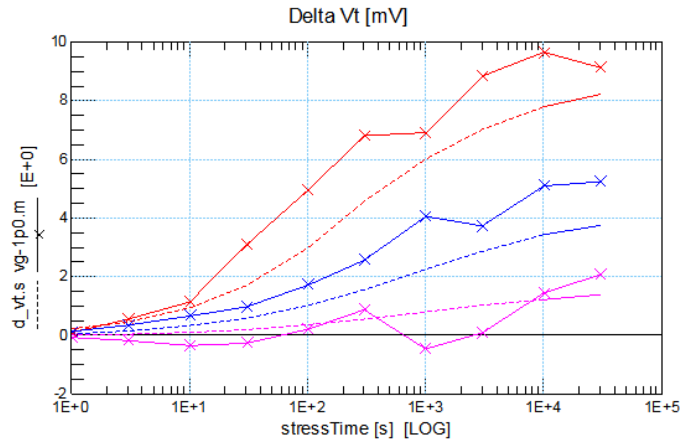
V_{ds} Stress dependency

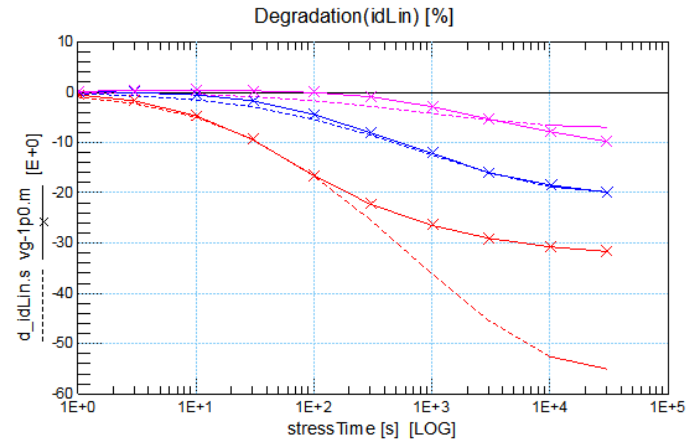
$$\left(\frac{V_{\mathrm{dse}} - \phi_{\mathrm{SL}} + \phi_{\mathrm{S0}}}{\mathrm{TRAPDLX}}\right)$$

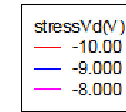
Realistic behavior of $V_{t(gmmax)}$, I_{dlin}, I_{dsat} and g_{mmax} could be achieved with drift resistance aging only:

- TRAPDTIME1
- TRAPDTIME2
- TRAPD1MAX
- TRAPDVDDP
- TRAPDLX

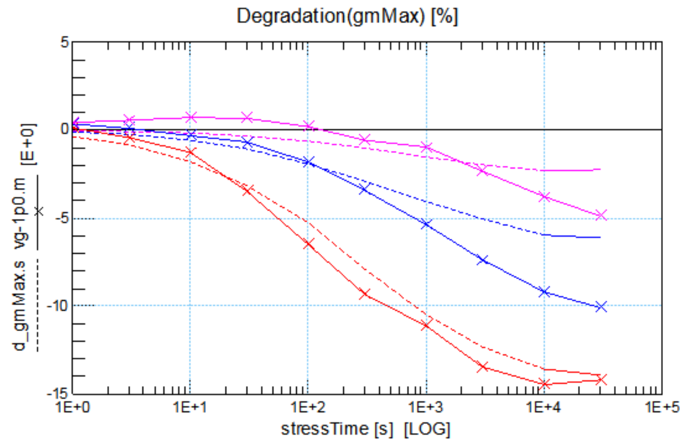
Aging modeling of PLDMOS with modified HiSIM HV 2.4

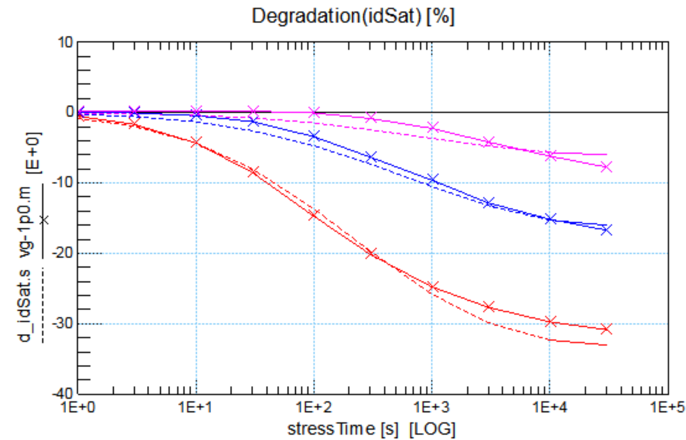






Linear scale





Summary

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HiSIM HV 2.4 model

- Introduction to aging equations from HiSIM HV 2.4 from University of Hiroshima
- Two-step aging simulation sequence without the need of having an external tool involved.
- This procedure can be implemented into a CAD environment.
- The aging information in a transient simulation is calculated and kept inside the model.

Application to real devices

- LDMOS transistors from IHP
- It seems that aging happened only in the drift region!
- Adjustment over time was very good but over V_{ds}-stress failed.
- A modification of the Verilog-A code of the HiSIM HV 2.4 model resulted in good agreement over V_{ds}-stress