POWER MOS MODELING FOR COMMUTATION CELL APPLICATIONS

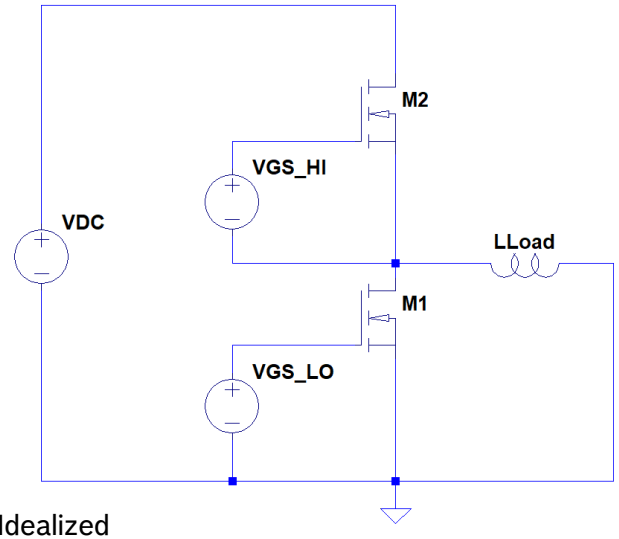
BOSCH

Power MOS Modeling
Challenge

- Simulation of power modules with (SiC) MOSFETs
- Range up to 1kV/ 100A per half bridge

- Accurate calculation of
  - static & dynamic losses
  - current/voltage transients
  - Oscillations

- Compatibility between different simulators
  - Pspice, Saber, Ltspice, Spectre



Idealized

Commutation Cell Circuit

Power MOS Modeling
Procedure

- Transistor model refers to bare die
- (Electrical) setup parasitic circuitry from Ansys Q3D
- Circuit models for gate control etc.
- Simulation currently with Pspice

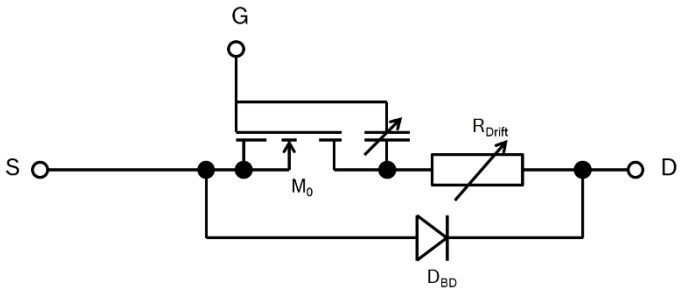
Power MOS Modeling
Models for Discrete Power MOS Transistors

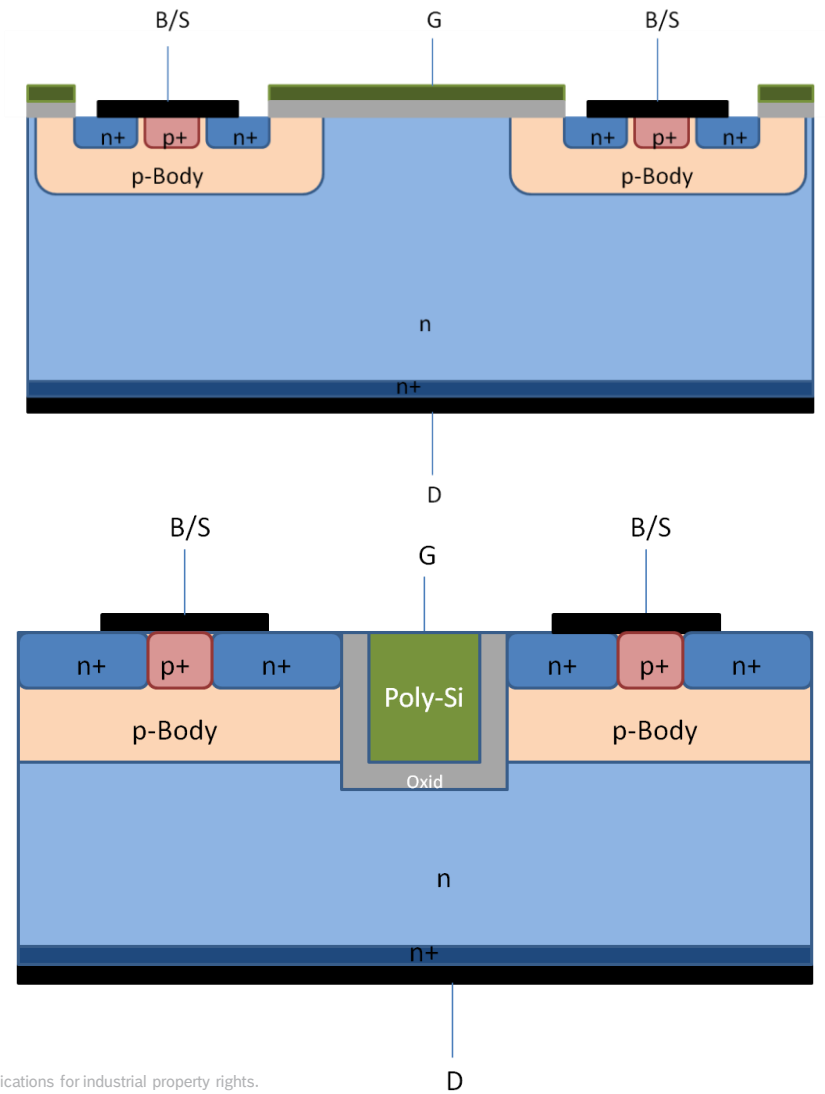
- Available from different vendors
- Mainly subcircuits in Pspice syntax
- Different levels of accuracy

- Tradeoff between model accuracy and convergence behaviour; main issues:
  - Modelling of Drain Current
  - RDSon vs Temp, RDSon vs ID
  - Body Diode Modelling
  - Capacitance Modelling
  - Self Heating

Power MOS Modeling
Modeling Regions

- Channel
- Drain Resistance
- Capacitances
- Body Diode





Power MOS Modeling
Channel Model

- Which complexity is needed ?
- Available vendor models for
  - Si: mainly MOS Level3 based
  - SiC : only behavioural approach ID=f(VGS,VDS,Temp)

- Behavioural modelling (i.e. algebraic functions in controlled sources etc.)
  - Convergence ?

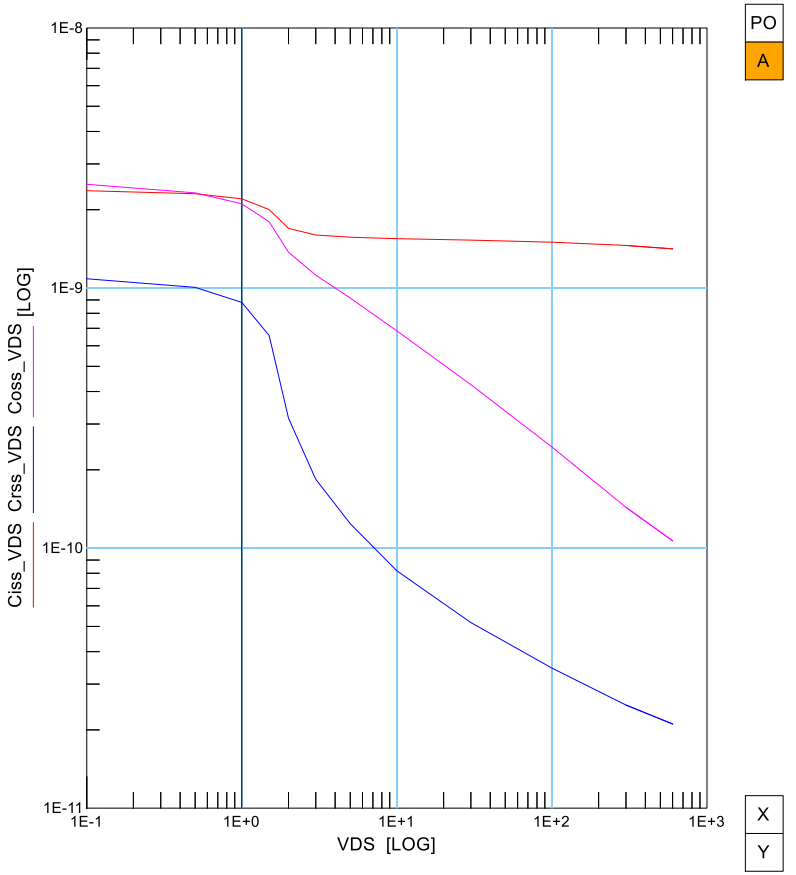
- Usage of standard models (Level3, BSIM)
  - Accuracy ?
  - How to de-activate unused effects (especially diodes) ?

Power MOS Modeling
Capacitances

- Strong VDS dependence of CGD
- Datasheets do not show CGD for VGD>0
- Vendors use behavioural or table models

- Vendor Models: CGS=const

- “Classical” PN junction approach for CDS ok also for SiC ?



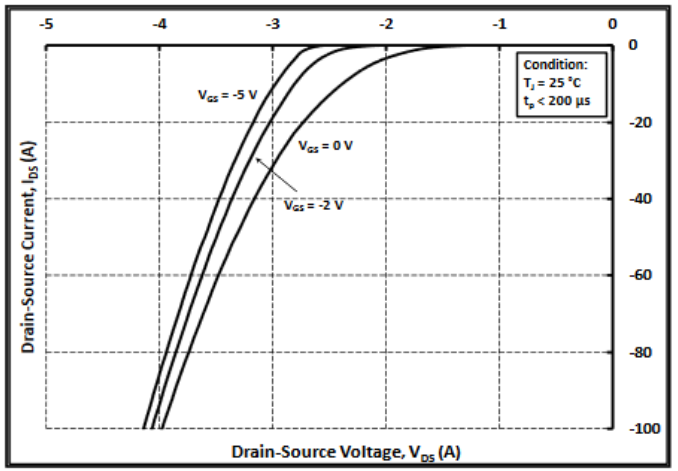
Ciss = CGS + CGD

Crss = CGD

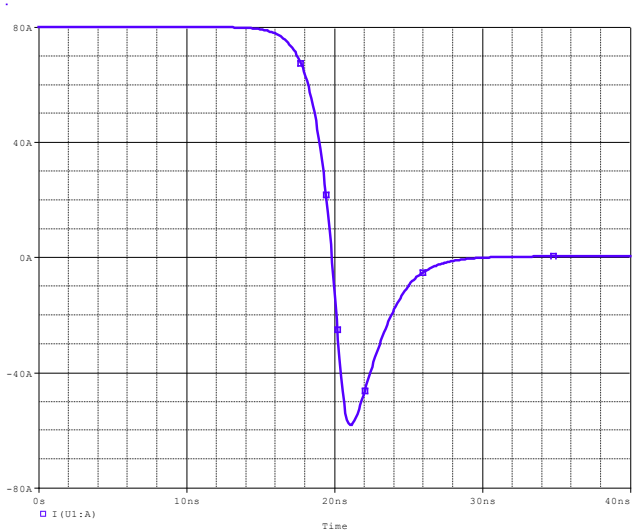
Coss = CDS + CGD

Power MOS Modeling
Body Diode

- Vendor SiC models: partly behavioural, partly standard SPICE diode model
- Too rough (if any) reverse recovery modelling (is a better one needed for SiC?)
- QRR/QOSS separation



SiC MOSFET behaviour in 3rd Quadrant (VDS<0)



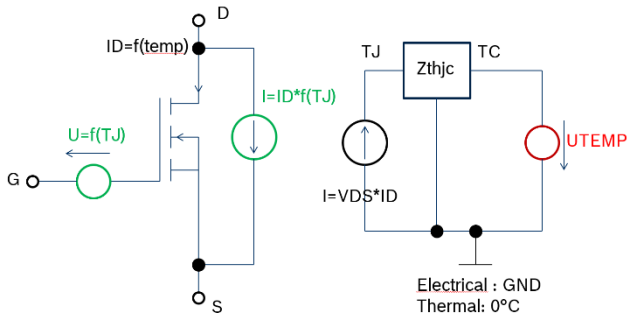
Diode current turn off behaviour

Power MOS Modeling
Self Heating

- "Classical" Spice Approach: Fixed device temperature (.TEMP, DTEMP…) ➔ no self heating modelled

- Self heating can be modelled by additional symbol pin, representing junction temperature as voltage
  - Connected to current source controlled by power dissipated in the device
  - Connected to thermal network to be extracted from the mechanical setup
- This voltage controls additional voltage/current sources in the model circuit (e.g. for modelling the threshold voltage shift with temperature
- Sacrifice:Convergence!

Principle of Self Heating Modeling



Power MOS Modeling
SiC MOSFET Model Proposal

- Level 3 for channel model
- Additional constant drain resistance
- Constant CGS
- Behavioural model for CGD needed
- Standard diode model for body diode (incl. CDS) + behavioural addition for reverse recovery needed
- “thermal” pin