

An Approach for Improving Circuit Convergence using HiSIM-HV as an Example

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Introduction

- › DC-Op simulation of a circuit netlist crashes with convergence error in SPECTRE

- › The circuit design has no exceptional elements, e.g.
 - The ground is well connected
 - No resistors with 1mOhm or even less

Observations and counter measures

Circuit inventory:

nodes 5487
bjt 127
bsim4 2038
capacitor 3412
diode 1409
hisim_hv 246
iprobe 930
isource 37
pcccs 759
resistor 1535
vbic 323
vsource 132

Global user options:

inlinesubcktcurrent = subckt
vabstol = 1e-06
iabstol = 1e-12
temp = 150
gmin = 1e-12
rforce = 1
digits = 6
dc_pivot_check = yes
pivrel = 0.001
highvoltage = yes
dochecklimit = yes
checklimitdest = file
save = selected
pwr = none
currents = selected
subcktprobelvl = 4
useprobes = yes
saveahdlvars = all
reltol = 0.001
tnom = 27

Simulation Errors in Detail

Simulation with **spectre +diagnose_fpe** netlist.scs

› **Convergence error with 100 floating point exceptions (FPE's)**

– BSIM4 during reading in:

FPE when initializing device: I302.core.ilim.P6 of bsim4, at file 'netlist_DP07_new_test_final.scs' line: 1482.

– HiSIM-HV during iterations:

FPE: I302.gain_sel.I138.M0.sx11mp11a.sx11mp11a_p.corner_mos of hisim_hv, at file './test_labrador/models/sx_xt11_hpmosa.scs' line: 930.

d : 0 = 246.6846 mV

g : I302.gain_sel.net0228 = -57.96606 mV

s : I302.gain_sel.net0187 = 305.4129 mV

b : I302.gain_sel.net0187 = 93.4658 V

I302.gain_sel.I138.M0.sx11mp11a.sx11mp11a_p.corner_mos:int_d = 2.856708 V

I302.gain_sel.I138.M0.sx11mp11a.sx11mp11a_p.corner_mos:int_s = 80.26226 V

FPE in BSIM4

First FPE's occur at reading parameters

FPE when initializing device: I302.core.ilim.P6 of bsim4, at file 'netlist_DP07_new_test_final.scs' line: 1482.

This message is due to a typo in the model card of sxmp0a

› lintnoi has to be corrected to $2.4e-08$ (instead of $2.4e+08$)

**Number of FPE's reduces from 100 to 42,
but simulation still does not converge.**

Debugging Strategy

1. Create a one-transistor netlist with the device and the specified operating point of the FPE message and reproduce the error.
2. Replace the model with the VerilogA reference model (v2.33 and v2.50) and inspect the error message

Warning gives information about problematic device and its operating point

FPE: I302.gain_sel.I138.M0.sx11mp11a.sx11mp11a_p.corner_mos of hisim_hv, at file './test_labrador/models/sx_xt11_hpmosa.scs' line: 930.

d : 0 = 246.6846 mV

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I302.gain_sel.I138.M0.sx11mp11a.sx11mp11a_p.corner_mos:int_d = 2.856708 V

I302.gain_sel.I138.M0.sx11mp11a.sx11mp11a_p.corner_mos:int_s = 80.26226 V

One transistor netlist with spectre model

```
// Netlist netlist_DP07_new_test.scs
// Instance I302.gain_sel.gain_sel_bias.M76.sx11mp11a.sx11mp11a_p.corner_mos
// Primitive hisim_hv, Master pch2
simulator lang=spectre
global 0
Vd (d 0) vsource type=dc dc=-1
Vg (g 0) vsource type=dc dc=-2
Vs (s 0) vsource type=dc dc=3
Vb (b 0) vsource type=dc dc=20
Mtest ( d g s b ) pch2
+ w          = 1.598200e-06   l          = 1.380000e-06   nf          = 2.000000e+00
+ nrs        = 2.276923e-01   nrd          = 4.368932e-02
+ m          = 1.000000e+00   trise        = 0.000000e+00
dcOp dc writefinal="spectre.dc"
model pch2 hisim_hv
+ type       = p
+ level      = 73
+ version    = 2.330000e+00
+ ...
```

One transistor netlist with VerilogA model

...

ahdl_include

"/home/pieper/simulation/HiSim/HiSIM_HV_2.5.0_Release_20190426/HiSIM_HV_2.5.0_VA-Code/hisimhv_va/hisimhv_n4.va"

simulator lang=spectre

global 0

Vd (d 0) vsource type=dc dc=-1

Vg (g 0) vsource type=dc dc=-2

Vs (s 0) vsource type=dc dc=3

Vb (b 0) vsource type=dc dc=20

Mtest (d g s b) pch2

+ W = 1.598200e-06 **L** = 1.380000e-06 **NF** = 2.000000e+00

+ NRS = 2.276923e-01 **NRD** = 4.368932e-02

+ m = 1.000000e+00 **DTEMP** = 0.000000e+00

dcOp dc writefinal="spectre.dc"

model pch2 **hisimhv_n4_va**

+ TYPE = -1

+ //LEVEL = 73

+ //VERSION = 2.330000e+00

+ ...

Simulation Result test case 1

- › One-transistor netlist with VerilogA models reveals:

WARNING (ASL-6246):

"/home/pieper/simulation/HiSim/HiSIM_HV_2.5.0_Release_20190426/HiSIM_HV_2.5.0_VA-Code/hisimhv_va/hisimhv_n4.va" **4572**: Mtest: A domain error occurred while calculating pow(x,y) for real numbers because a negative value -2176186.584267 has been specified for x and the value -0.650000 specified for y is not an exact integer. Therefore, the function has returned the value 0.0.

- › In the verilogA code I find at **line 4572**:

```
T5 = `Fn_Pow( Eeff , MUEPH0 - 1.0e0 ) ;
```

1. Conclusion

- › MUEEFB must be ≤ 0 , because otherwise E_{eff} becomes negative. Since MUEPH0 is not an integer μ_{PH} can not be calculated.

$$E_{\text{eff}} = E_{\text{eff0}} \cdot (1 + \text{MUEEFB} \cdot V_{\text{bs}})$$

$$\mu_{\text{PH}}(\text{phonon}) = \frac{M_{\text{uephonon}}}{E_{\text{eff}}^{\text{MUEPH0}}}$$

$$\mu_{\text{SR}}(\text{surface roughness}) = \frac{\text{MUESR1}}{E_{\text{eff}}^{M_{\text{uesurface}}}}$$

If MUEEFB > 0 set it to 0 !

Number of FPE's reduces from 42 to 32 and simulation converges.

Simulation Result test case 2

- › One-transistor netlist with VerilogA models reveals:

WARNING (ASL-6240):

"/home/pieper/simulation/HiSim/HiSIM_HV_2.5.0_Release_20190426/HiSIM_HV_2.5.0_VA-Code/hisimhv_va/hisimhv_n5.va" 4757: Mtest: A negative value -0.000086 has been specified in the square root function 'sqrt()'. Therefore, the function has returned the value 0.0.

- › In the verilogA code I find at **line 4757**:

```
T0 = sqrt (Psab * Psab + 4.0 * `sti2_dlt * Psbsti) ;
```

2. Conclusion

- › The error occurs at high temperature only. It is not possible to inhibit it in the equation, but using the equation can be avoided by setting the parameter COISTI to 0 (instead of 1). STI leakage current model is switched off.

If COISTI = 1 set it to 0 !

Number of FPE's reduces from 32 to 18.

Now it becomes harder ...

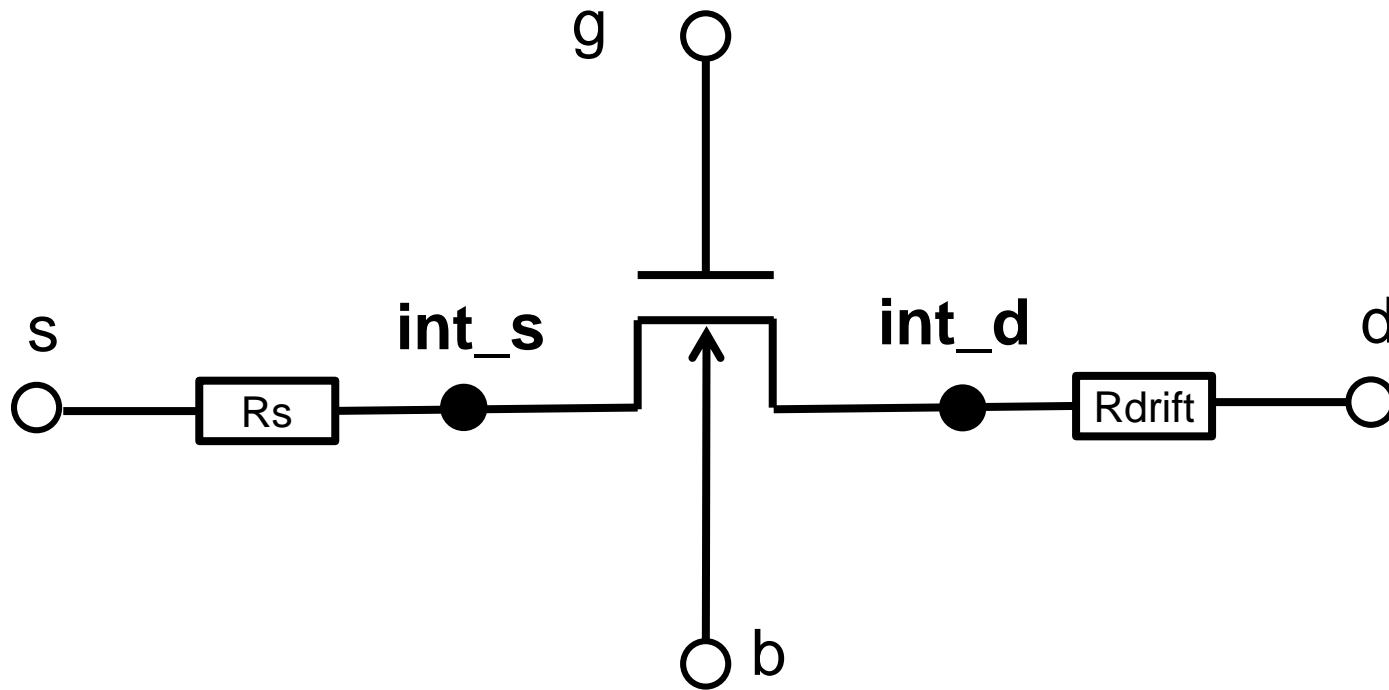
- › The remaining FPE's show a special behavior:

FPE: I302.gain_sel.gain_sel_bias.M97 of hisim_hv, at file 'netlist_DP07_new_test_final.scs' line: 3187.

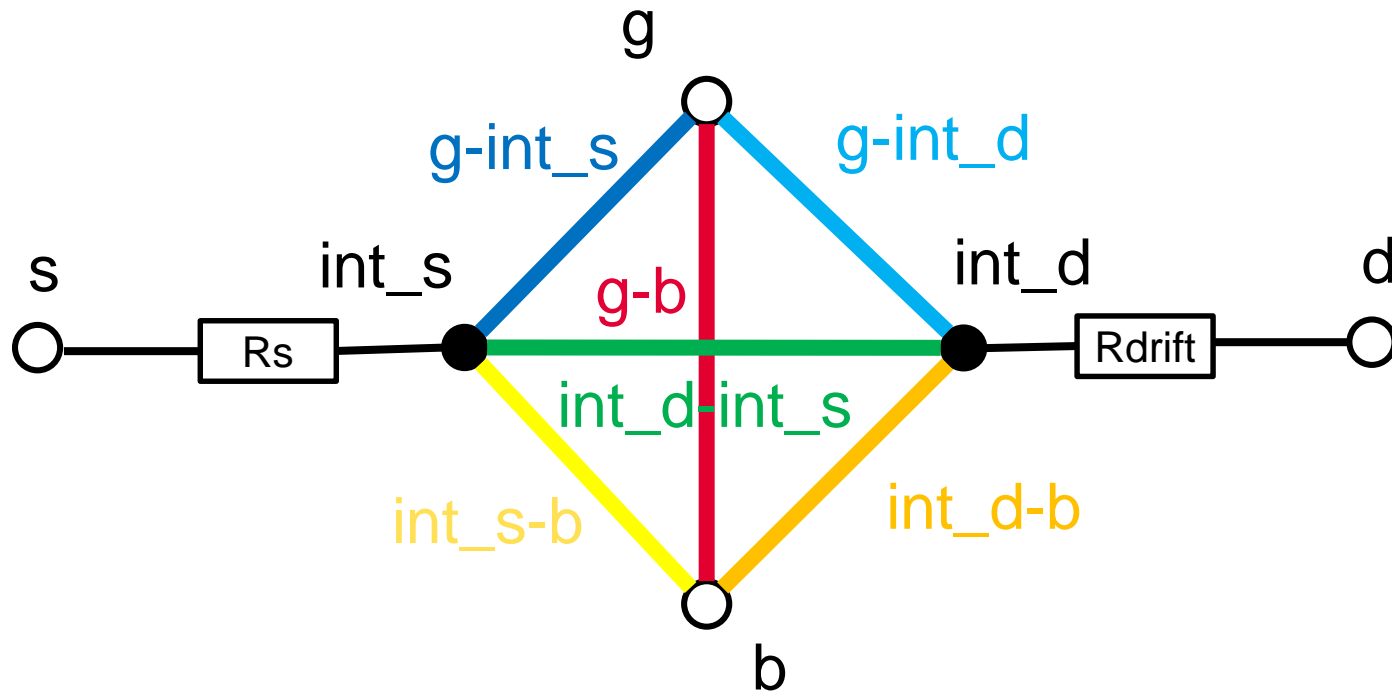
d : I302.gain_sel.gain_sel_bias.net0298 = -164.169 mV
g : I302.gain_sel.gain_sel_bias.net051 = 8.519913 V
s : I302.gain_sel.gain_sel_bias.net0264 = 8.222461 V
b : I302.gain_sel.net086 = 8.422461 V
sub : I302.gain_sel.net086 = 8.422461 V
I302.gain_sel.gain_sel_bias.M97:int_d = -54.40905 kV
I302.gain_sel.gain_sel_bias.M97:int_s = -1.005263 kV

Internal nodes (int_s and int_d) are running away while external nodes stay moderate.

HiSIM-HV model, external and internal nodes

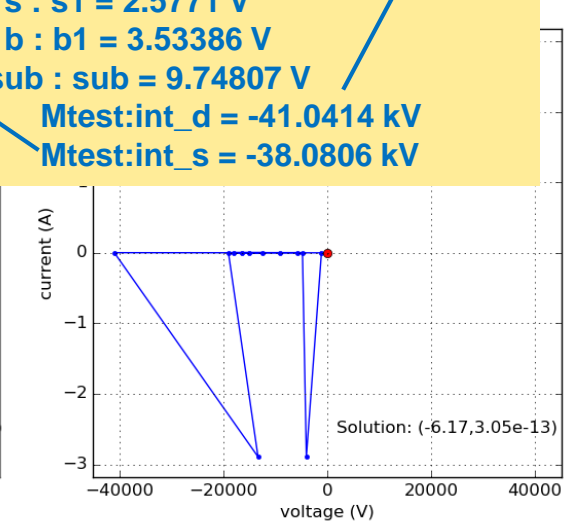
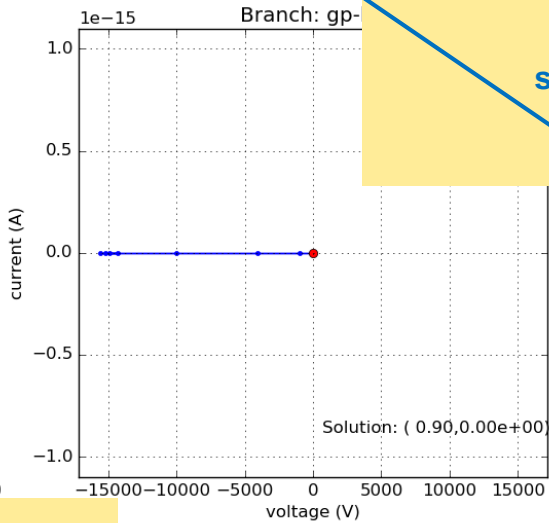
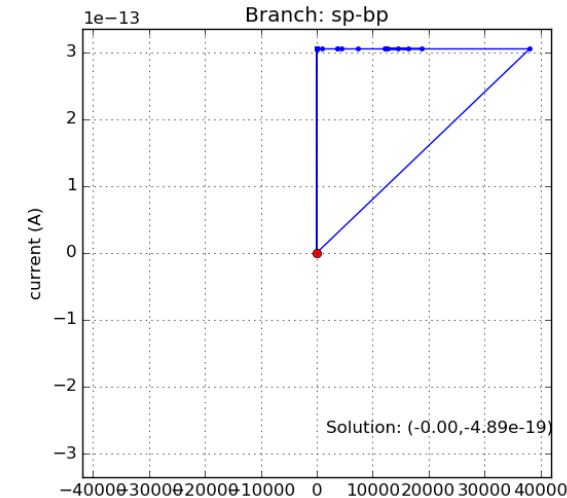
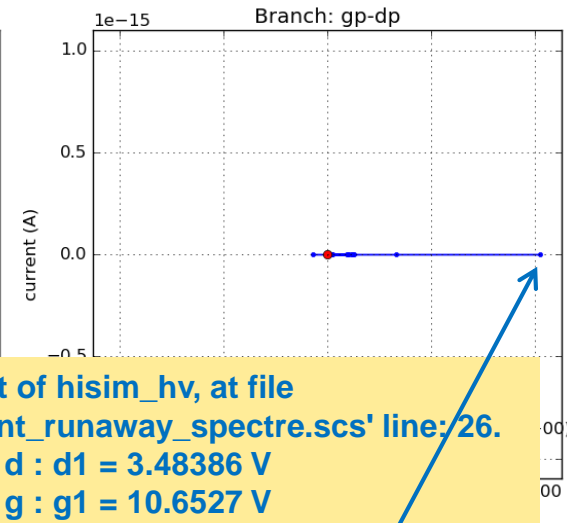
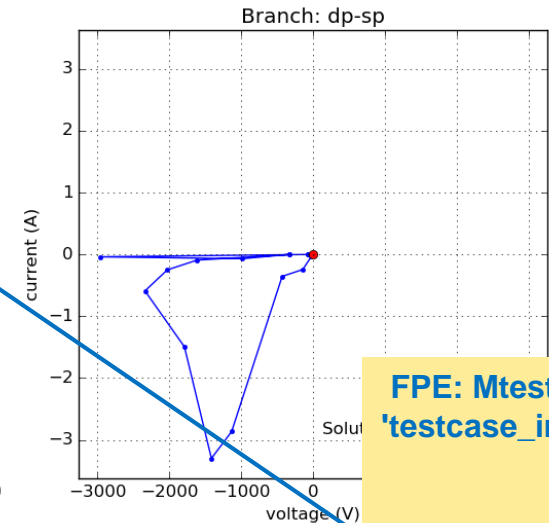
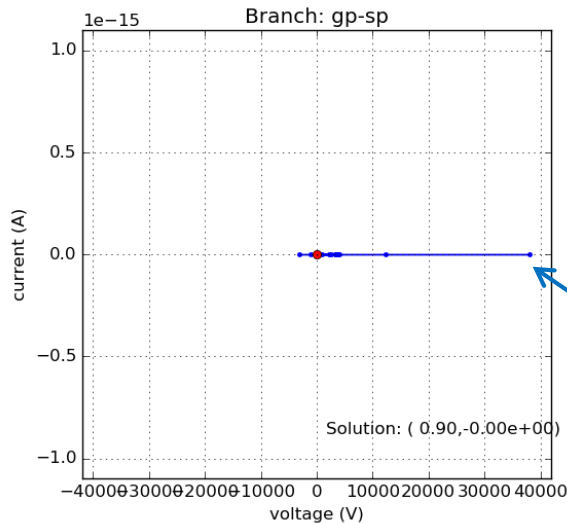


HiSIM-HV model internal branches



Branch Analysis: What are the branches doing on the way to the solution?

Branch Analysis HiSIM-HV Spectre model Version 2.33
 Simulator spectre Version 18.1.isr8 Total Number of Iterations: 85

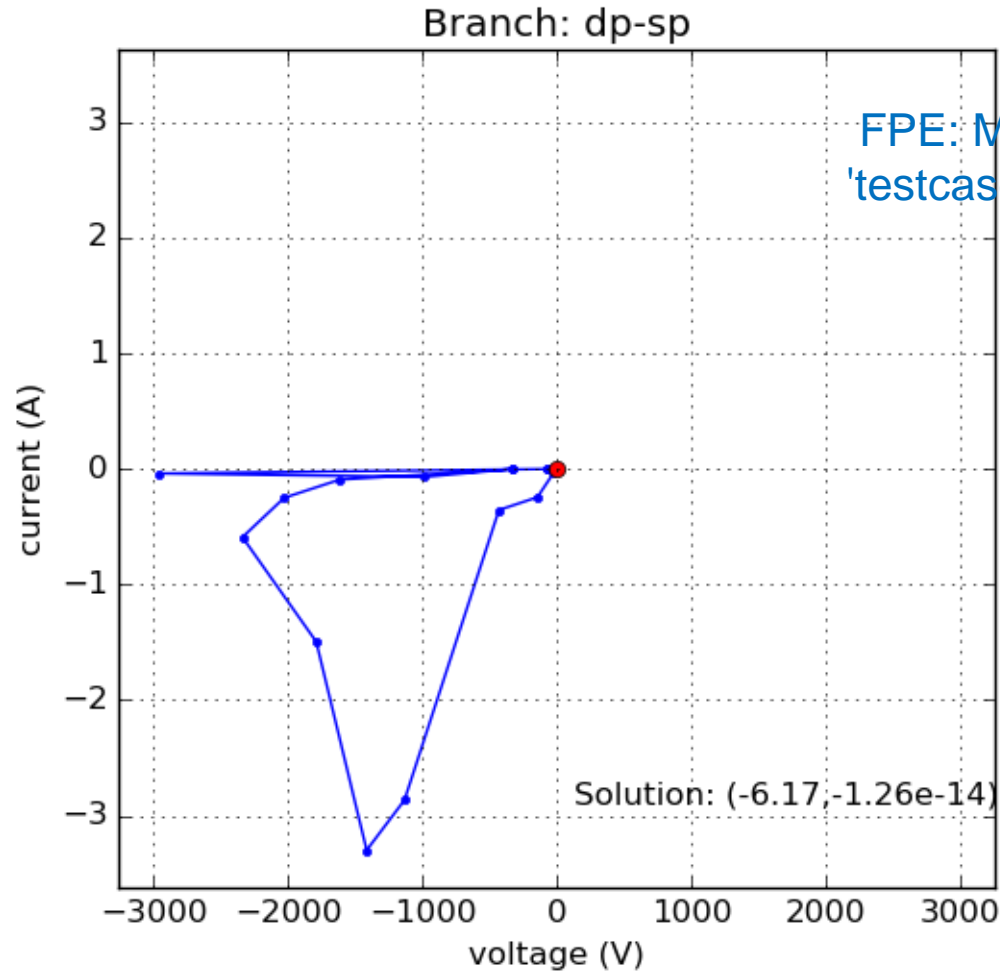


FPE: Mtest of hisim_hv, at file 'testcase_int_runaway_spectre.scs' line:26.
 d : d1 = 3.48386 V
 g : g1 = 10.6527 V
 s : s1 = 2.5771 V
 b : b1 = 3.53386 V
 sub : sub = 9.74807 V
 Mtest:int_d = -41.0414 kV
 Mtest:int_s = -38.0806 kV

Different names of internal nodes
 VerilogA: sp, dp Spectre: int_s, int_d

Branch Analysis

Branch Analysis HiSIM-HV Spectre model Version 2.33
 Simulator spectre Version 18.1.isr8 Total Number of iterations: 85



FPE: Mtest of hisim_hv, at file
 'testcase_int_runaway_spectre.scs' line: 26.

d : d1 = 3.48386 V

g : g1 = 10.6527 V

s : s1 = 2.5771 V

b : b1 = 3.53386 V

sub : sub = 9.74807 V

Mtest:int_d = -41.0414 kV

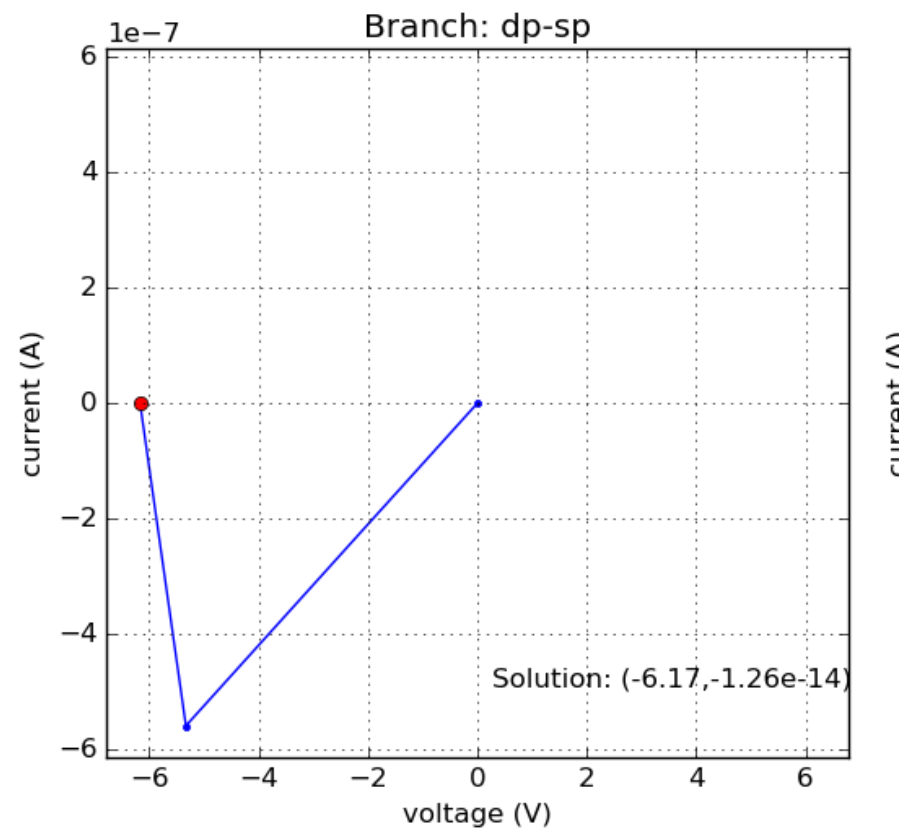
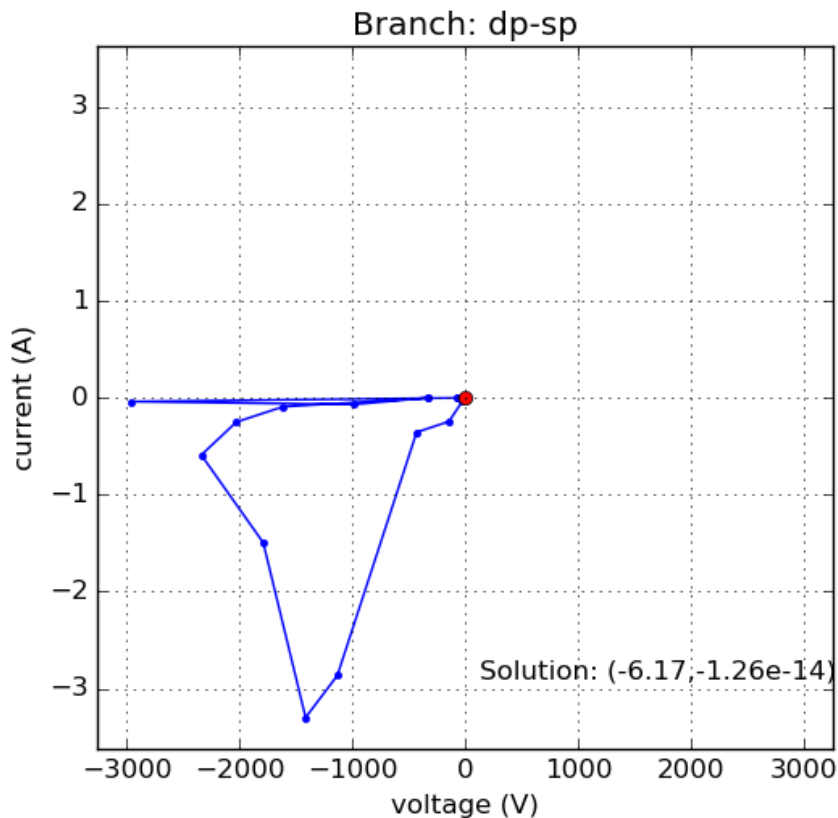
Mtest:int_s = -38.0806 kV

Branch Analysis: comparison v2.33 Spectre model with VerilogA model



Branch Analysis HiSIM-HV Spectre model Version 2.33
Simulator spectre Version 18.1.isr8 Total Number of Iterations: 85

Branch Analysis HiSIM-HV VerilogA model Version 2.33
Simulator spectre Version 18.1.isr8 Total Number of Iterations: 4

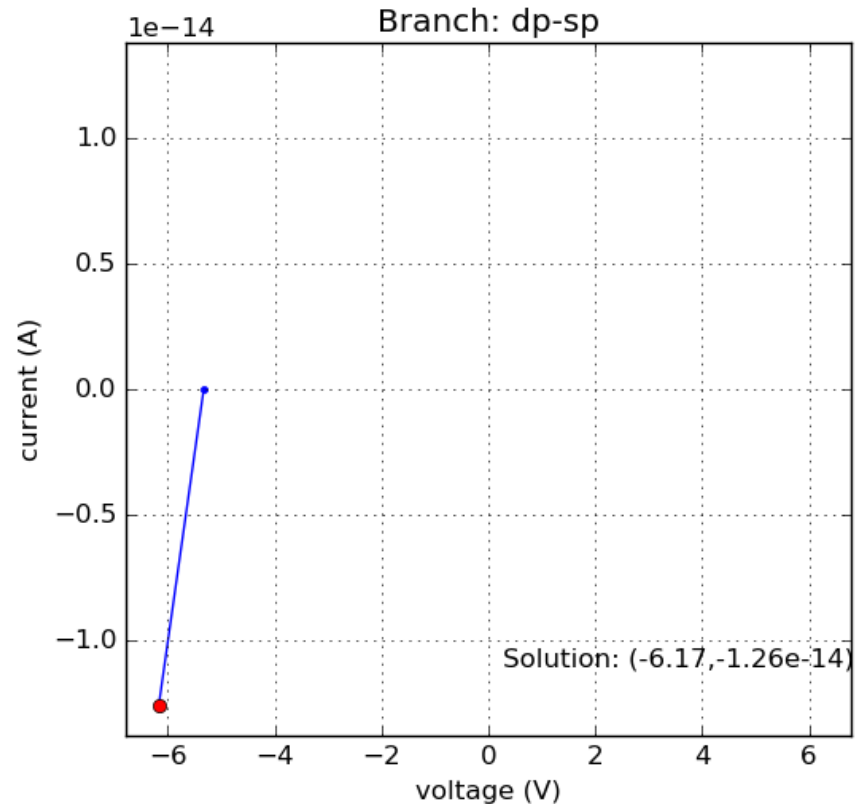
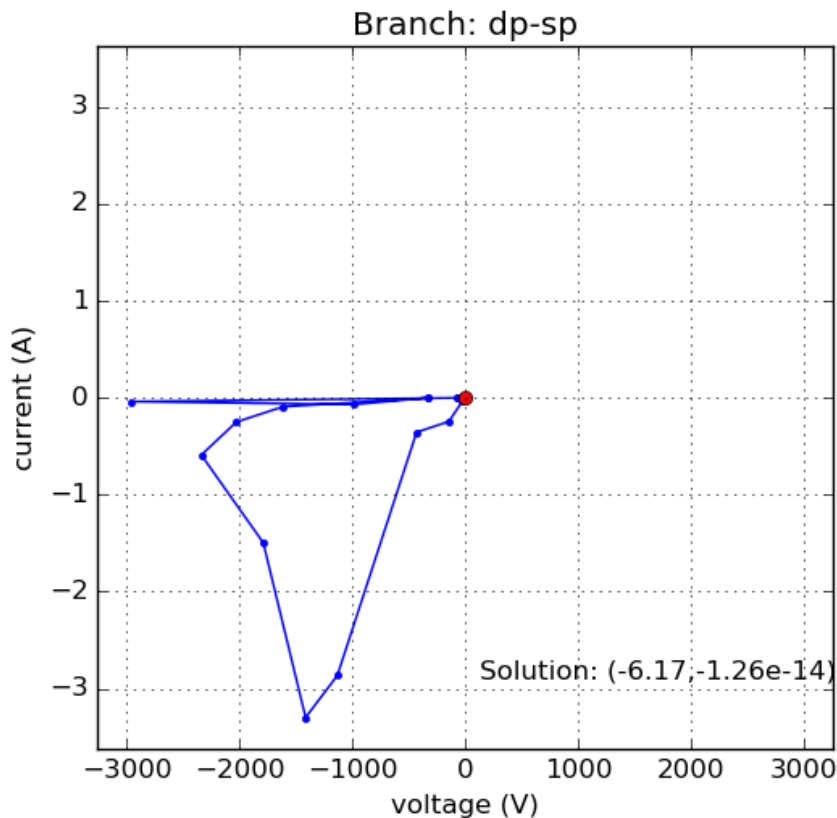


Branch Analysis: comparison v2.33 Spectre model with v2.40



Branch Analysis HiSIM-HV Spectre model Version 2.33
Simulator spectre Version 18.1.isr8 Total Number of Iterations: 85

Branch Analysis HiSIM-HV Spectre model Version 2.4
Simulator spectre Version 18.1.isr8 Total Number of Iterations: 4



> **Let's try HiSIM-HV version 2.40!**

HiSIM-HV v2.40

Some of our parameter sets had problems simulation the all-0V test case

- › It was found that some smoothing parameters have to be set in a way that $\Delta \geq 1$ in the following equation.

CODDLT=1 (default) :

$$\Delta = \frac{\text{DDLTMAX} \cdot T1}{\text{DDLTMAX} + T1} + \text{DDLTICT}$$

$$T1 = \text{DDLTSPL} \cdot L_{\text{gate}} \cdot 10^6$$

$$V_{\text{ds,eff}} = \frac{V_{\text{ds}}}{\left[1 + \left(\frac{V_{\text{ds}}}{V_{\text{ds,sat}}} \right)^\Delta \right]^{\frac{1}{\Delta}}}$$

E.g. with **DDLTSPL=0** and **DDLTICT \geq 1**

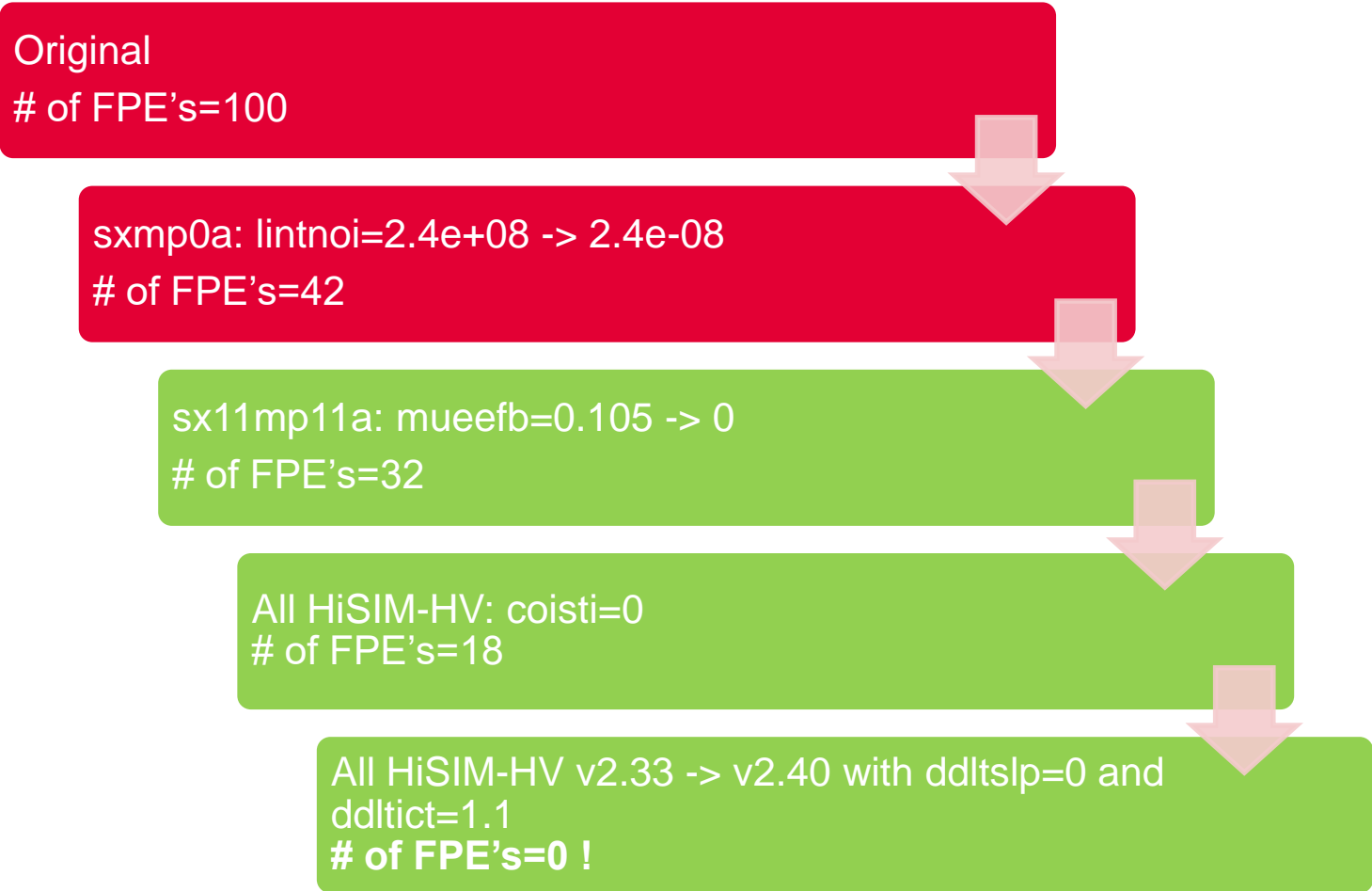
3. Conclusion

**Replacing all HiSIM-HV v2.33 with v2.40 and setting
DDLTSPLP=0 and DDLTICT=1.1**

**Number of FPE's reduces from 18
to 0!**

Conclusion

> Simulation with spectre +diagnose_fpe netlist.scs



Conclusion

- › **Bug 1:** Error occurred while calculating $\text{pow}(x,y)$ for real numbers

VerilogA test cases were sent to Hiroshima University, confirmed and fixed in version 2.50

- › **Bug 2:** A negative value in the square root function 'sqrt()'.

VerilogA test cases were sent to Hiroshima University, confirmed and fixed in version 2.50

- › **Bug 3:** Run-away of internal nodes in HiSIM-HV v2.33

Spectre&VerilogA test cases were sent to Cadence, confirmed.

- › **Bug 4:** All-0V cannot be simulated with HiSIM-HV v2.40

Spectre&VerilogA test cases were sent to Cadence, confirmed. Fix in next SPECTRE version.

Tool developed for circuit analysis... To be continued ...

tk _ □ ×

Netlist:

```

// Cell name: B_104_I_DIST_A
// View name: schematic
subckt B_104_I_DIST_A ena_1v5 icsa1_10u icsa2_10u icsa3_10u \
  iref1_6uh_l2v5 iref2_6uh_l2v5 iref3_6uh_l2v5 iref4_6uh_l2v5 \
  iref7_1uh_l2v5 iref8_1uh_l1v5 iref9_1uh_l1v5 iref10_2uh_l1v5 \
  iref11_2u_l2v5 iref13_2uh_l2v5 iref80_2u5 iscr_10u isnkcsa1_2u5 \
  isnkcsa2_2u5 isnkcsa3_2u5 v_ncasc_vss v_nlb_vss v_pcasc_vdd \
  v_plb_vdd vdd_gnd_1v5 inh_hSup inh_lSup
P141 (icsa2_10u net090 net058 inh_hSup) pana w=8u l=400n nf=1 \
  XdefDrain=contact XdefSource=contact mfact=8
P110 (iref8_1uh_l1v5 net038 net037 vdd_gnd_1v5) pana w=8u l=400n nf=1 \
  XdefDrain=contact XdefSource=contact mfact=8
P144 (net089 net089 inh_hSup inh_hSup) pana w=8u l=2u nf=1 \
  XdefDrain=contact XdefSource=contact mfact=2
P148 (isnkcsa1_2u5 net023 net091 inh_hSup) pana w=8u l=400n nf=1 \
  XdefDrain=contact XdefSource=contact mfact=2
P149 (net091 net027 inh_hSup inh_hSup) pana w=8u l=2u nf=1 \
  XdefDrain=contact XdefSource=contact mfact=2
P2A (net039 net029 vdd_gnd_1v5 vdd_gnd_1v5) pana w=8u l=10u nf=1 \
  XdefDrain=contact XdefSource=contact mfact=2

```

Start
Choose an analysis
dcOp ▾
Simulate
Clear Results Window
Close

Open Model files for
hisim_hv
Filter
Apply

Model Parameter	coisti	of Model	hisim_hv	Filter	any ▾	0.001	Find	Set to	0	Apply	
Inst Parameter	r	of Model	resistor	Filter	R1	any ▾	0.001	Find	Set to	0	Apply

OP Parameter	rseff	of Model	hisim_hv	Filter	M0	any ▾	0.001	Find
--------------	-------	----------	----------	--------	----	-------	-------	------

Write 1-device test case of
I302.refb_buff.M3
primitive
hisim_hv
Apply

Find Internal Nets
Find Vpulse/Vpwl
Find Ipulse/Ipwl
Check hisim_hv

Results:

```

Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M17.sx11mp11a.sx11mp11a_p.corner_mos
Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M13.sx11mp11a.sx11mp11a_p.sx11hpmosa
Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M13.sx11mp11a.sx11mp11a_p.corner_mos
Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M3.sx11mp11a.sx11mp11a_p.sx11hpmosa
Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M3.sx11mp11a.sx11mp11a_p.corner_mos
Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M14.sx11mp11a.sx11mp11a_p.sx11hpmosa
Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M14.sx11mp11a.sx11mp11a_p.corner_mos
Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M0.sx11mp11a.sx11mp11a_p.sx11hpmosa
Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M0.sx11mp11a.sx11mp11a_p.corner_mos
Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M21.sx11mp11a.sx11mp11a_p.sx11hpmosa
Found: hisim_hv v2.33 coisti = 0 in Instance: I302.core.M21.sx11mp11a.sx11mp11a_p.corner_mos

```


Questions to the Audience

- › Do you have similar experiences, of how convergence behavior can be improved by setting model parameters to certain values?
- › Which model versions should be used/avoided?

Thank you for your Attention!



Part of your life. Part of tomorrow.