FOSS TCAD/EDA Tools for Compact Modeling
Technology - Devices - Applications

Wladek Grabinski
MOS-AK Association (EU)
wladek@mos-ak.org
Over two decades of MOS-AK in brief

17 subsequent MOS-AK modeling workshops
3 consecutive TRACK4: Compact Modeling at ESSDERC/ESSCIRC Conferences
27 international MOS-AK modeling workshops in Europe, USA, India, China (planning Latin America)
16 special compact modeling sessions at MIXDES Conference
50+ active sponsors and technical program promoters
300+ MOS-AK technical CM papers and posters (available on line www.mos-ak.org)
4 modeling MOS-AK modeling books http://www.mos-ak.org/books/
Special Compact Modeling Issues

Compact/SPICE Modeling Books

TPC TRACK: Compact Modeling and Process/Device Simulation

wladek@mos-ak.org
MOS-AK 2020 Events

- 12th MOS-AK (IEDM / Q4 CMC timeframe)
  Santa Clara (US), Dec. 11, 2019
- MOS-AK at LAEDC
  San Jose (Costa Rica), February 25, 2020
- Spring MOS-AK Workshop with SBMOS and IEEE EDS MQ
  THM Giessen (D), March 17-18, 2020
- FOSS TCAD/EDA at 5NANO2020
  Kottayam (IN), April 22, 2020
- MIXDES CM Session with IEEE EDS MQ
  Wroclaw (PL), June 25-27, 2020
- WCM at the Nanotech
  Washington DC (USA), June 30, 2020
- 5th Sino MOS-AK Workshop
  Xi’an (CN), July 8-10, 2020
- 18th MOS-AK at ESSDERC/ESSCIRC
  Grenoble (F), Sept. 14-17, 2020
- 3rd MOS-AK/India Conference
  Hyderabad (IN), Feb. 2021
FOSS TCAD/EDA Tools for Compact Modeling
Technology - Devices - Applications

Outline

• Moore’s Law
• Open Source CAD for Compact Modeling
  <www.mos-ak.org/books/CAD_CM_Book.php>
  – 2/3D Numerical TCAD Device Simulations
  – Schematic entry and circuit simulation
  – Device Level Parameter Extraction
  – Standardized Data Exchange Format For Device Modeling
• 2019 MOS-AK Compact/SPICE Modeling Events
Moore’s Law

Moore’s Law is the fundamental driver of the semiconductor industry, what’s even more important is what it delivers to the end user.
Moore’s Law (cont.)

The first working monolithic devices (IC) presented by Fairchild Semiconductor on May 26, 1960

The Raspberry Pi a tiny and brilliantly inexpensive proto-computer ($25 as of 2014)
Moore’s Law (cont.)

The Raspberry Pi Zero is half the size of a Model A+, with twice the utility. A tiny Raspberry Pi that’s affordable enough for any project! ($5 or even free as early 2016)
<www.raspberrypi.org/products/pi-zero>

The first working monolithic devices (IC) presented by Fairchild Semiconductor on May 26, 1960
Choose Wisely Your $999

<table>
<thead>
<tr>
<th>1 * Apple's New Monitor Stand</th>
<th>199 * Raspberry Pi Zero</th>
</tr>
</thead>
</table>
Five Powerful Lab Instruments
One Open Source Board

On-board is a complete arsenal of electronic engineering instruments: only $29

A. Power Supply (4.5 to 15V, 1.5W max)
B. Digital Output
C. Function Generator (2 channel, 1MSPS)
D. Oscilloscope/Multimeter (2 channel, 750kSPS)
E. Logic Analyzer (2 channel, 3MSPS)

[REF] https://espotek.com/labrador
EspeTek Labrador

4007 CMOS inverter chip measurement

[REF] https://espotek.com/labrador
Qucs: Quite Universal Circuit Simulator

FOSS Modeling/Simulation Flow

- **Process/Technology**
  - TCAD
  - Other EM Simulators

- **Compact Modeling Model Libraries**
  - Spice/Verilog-A Simulators
  - Verilog-A Standardization
    - ADMS
    - MAPP
  - Measurements
  - Parameterization
  - Other

- **Analog/RF IC Simulation**
  - Ngspice
  - Qucs
  - Xyce
  - GnuCap
  - Other
Compact/SPICE Modeling

- A model of semiconductor device charges, currents and voltages
- Built from physically-motivated equations
- Intended for use in an analog circuit simulator

Process TCAD Simulation

• DevSim TCAD

• Cogenda TCAD

2D MOSFET simulation

3D SRAM Cell
# Stanford TCAD Software

<table>
<thead>
<tr>
<th>Device Modeling</th>
<th>Process Modeling</th>
<th>Framework/Utilities</th>
</tr>
</thead>
<tbody>
<tr>
<td>PROPHET</td>
<td>SUPREM3</td>
<td>ET3D</td>
</tr>
<tr>
<td>Monet</td>
<td>SUPREM IV</td>
<td>FOREST</td>
</tr>
<tr>
<td>PISCES</td>
<td>SUPREM IV GS</td>
<td>HDFVset</td>
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<tr>
<td>PISCES 2ET</td>
<td>SUPREM ALAMOD</td>
<td>VIP3D</td>
</tr>
<tr>
<td>PISCES 2H-B</td>
<td>SPEEDIE</td>
<td>Mixed Mode</td>
</tr>
<tr>
<td>SEDAN III</td>
<td></td>
<td></td>
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<tr>
<td>STRIDE</td>
<td></td>
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</tr>
</tbody>
</table>

# TU Wien TCAD Software

## Open Source Software

<table>
<thead>
<tr>
<th>ViennaCL</th>
<th>ViennaMesh</th>
</tr>
</thead>
<tbody>
<tr>
<td>ViennaData</td>
<td>ViennaProfiler</td>
</tr>
<tr>
<td>ViennaFEM</td>
<td>ViennaSHE</td>
</tr>
<tr>
<td>ViennaGrid</td>
<td>ViennaSiSpin</td>
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<tr>
<td>ViennaIPD</td>
<td>ViennaTS</td>
</tr>
<tr>
<td>ViennaMag</td>
<td>ViennaWD</td>
</tr>
<tr>
<td>ViennaMath</td>
<td>ViennaX</td>
</tr>
</tbody>
</table>

## No Longer Supported

- deLink 1.0
- Promis
- SIESTA
- ViennaMOS
- VMC
- VSP
- Minimos-NT

[REF] http://www.iue.tuwien.ac.at/software/
GTS Minimos-NT: Mixed Mode

Mixed mode TCAD simulation can be done using industry-standard Spice compact models, including BSIM; the easy-to-use schematic editor allows to quickly edit circuits and sub-circuits.
FOSS Computational Electromagnetic (EM) Modeling Tools

The software in this list is either free or available at a nominal charge and can be downloaded over the internet. Some of the codes require the user to register with the distributor's web site. If you are familiar with other free EM modeling software that should be added to this list, please send the name of the software, a hypertext link, and a brief description to CVEL-L@clemson.edu.

ASAP - Antenna Scatterers Analysis Program
AtaiTec Free 2D Field Solver
ATLC - Arbitrary Transmission Line Calculator
ATLC2 - Arbitrary Transmission Line Calculator 2
emAnalyse
EMAP
EMCoS Antenna VLab SV
EM Explorer
emGine Environment
ERMES
FastCap and FastHenry
FEKO LITE
FEMM - Finite Element Method Magnetics
gprMax
MagNet (Infolytica)

MMANA-GAL (basic version)
MEEP
MMTL
Multiple Multipole (MMP) Algorithms
NEC2
newFasant (student version)
openEMS
pdnMesh
Puma-EM
Qsci
Radia
SATE Static Field Analysis Toolkit (Educational)
Students' QuickField
Sonnet Lite
Trace Analyzer
openEMS: FOSS Electromagnetic Field Solver

Horn antenna
Conical horn antenna
Helix antenna
Helix antenna array
Large helix antenna array
Biquad antenna
CRLH antenna
MRI birdcage model
MRI ring antennas

[REF] http://openems.de
SUGAR: FOSS Tool for MEMS

Two-degree-of-freedom optical scanner prototype
Mode 1 = 739Hz, mode 2 = 745Hz.

[REF] www-bsac.eecs.berkeley.edu/cadtools/sugar/
SPICE Development Timeline

SPICE (Simulation Program with Integrated Circuit Emphasis)
• Developed at University of California, Berkeley in 1973
• Nodal analysis, few circuit elements, fixed timestep transient analysis, written in Fortran

SPICE 2
• UCB Released in 1975
• Major improvements: modified nodal analysis, variable timestep transient using trapezoidal and BDL integration

SPICE 3
• UCB Released in 1989, rewritten in C
• Added X Window system plotting

<table>
<thead>
<tr>
<th>Simulator</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPICE</td>
<td>1973</td>
</tr>
<tr>
<td>SPICE2</td>
<td>1975</td>
</tr>
<tr>
<td>HSPICE</td>
<td>1981</td>
</tr>
<tr>
<td>PSPICE</td>
<td>1984</td>
</tr>
<tr>
<td>ELDO</td>
<td>1984</td>
</tr>
<tr>
<td>MDS</td>
<td>1988</td>
</tr>
<tr>
<td>SPECTRE</td>
<td>1989</td>
</tr>
<tr>
<td>SPICE3 (GPL)</td>
<td>1989</td>
</tr>
<tr>
<td>LIBRE</td>
<td>1991</td>
</tr>
<tr>
<td>ADS</td>
<td>1994</td>
</tr>
<tr>
<td>SPECTRE RF</td>
<td>1996</td>
</tr>
<tr>
<td>ELDO RF</td>
<td>1998</td>
</tr>
<tr>
<td>SPICEOPUS</td>
<td>1999</td>
</tr>
<tr>
<td>QUCS (GPL)</td>
<td>2003</td>
</tr>
<tr>
<td>HSPICE RF</td>
<td>2004</td>
</tr>
<tr>
<td>NGSPICE</td>
<td>2008</td>
</tr>
<tr>
<td>QUCSSTUDIO</td>
<td>2012</td>
</tr>
<tr>
<td>Xyce (GPL)</td>
<td>2013</td>
</tr>
</tbody>
</table>

Lung/Airway SPICE Model
Qucs Implementation

[REF] Francesc N. Masana “Lung/Airway Dynamic Model Using ABM Elements and PSPICE”
Proceedings of the 22nd International Conference MIXDES, June 25-27, 2015, Torun, Poland
**Design of Bio/Med Electronic Systems**

- **Thermics**
- **Optics**
- **Mechanics**
- **Fluidics**
- **Electronic Circuit**

- **SPICE**
- **VHDL-AMS**
- **Verilog-AMS**

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**Modelica** [http://modelica.org](http://modelica.org)
**VHDL-AMS** [http://www.eda.org/vhdl-ams/](http://www.eda.org/vhdl-ams/)
**Verilog-AMS** [http://www.accellera.org](http://www.accellera.org)

**SBML**
**SBML XML** [http://sbml.org/](http://sbml.org/)
**FAME** [http://f-a-m-e.fame-vu.cloudlet.sara.nl/](http://f-a-m-e.fame-vu.cloudlet.sara.nl/)
**Cell Designer** [http://celldesigner.org/](http://celldesigner.org/)

- VHDL-AMS is a derivative of the hardware description language VHDL (IEEE standard 1076-1993). It includes analog and mixed-signal extensions (AMS) in order to define the behavior of analog and mixed-signal systems.
- The Systems Biology Markup Language (**SBML**) is a representation format, based on XML, for communicating and storing computational models of biological processes.

[REF] A. Rezgui et al, "Integration of SBML models for the description of biological system in a lab-on-chip" MIXDES 2015
ngspice & KiCAD

Xyce & ADMS

- Verilog-A interface, via ADMS model compiler
  - VBIC, Mextram, EKV, HiCUM, etc.
- Verilog-A: industry standard format for new models
- ADMS translates Verilog-A to compilable C/C++ code;
- API automatically handles data structures, matrices, tedious details.

[REF] https://xyce.sandia.gov/
Gnucap: GNU Circuit Analysis Package

• Gnucap is a modern post-spice circuit simulator with several advantages over Spice derivatives.

• Additional Gnucap GIT repositories:
  – ADMS model compiler
  – Device models
  – Gnucap-modelgen Verilog model compiler

[REF] www.gnucap.org
Berkeley MAPP is a MATLAB-based platform for prototyping numerical models and simulation algorithms. MAPP also runs in Octave.

[REF] https://nanohub.org/groups/needs/mapp
MAPP eases the process of developing new device models and simulation algorithms, especially for those who do not have an extensive background in compact modelling or experience coding algorithms in simulators.

[REF] https://nanohub.org/groups/needs/mapp
ADMS - Overview

Simulator-Specific ADMS-XML Interfaces

Verilog-A Model Code

Testing prior implementation

c-code for: ADS, Eldo, Mica, hspice, Spectre, Titan, zspice, ngspice, QUCS, GnuCap, Xyce

Foss EKV2.6 Verilog-A Compact MOSFET Model

Wladek Grabinski1, Marcelo Pavanello2, Michelly de Souza2, Daniel Tomaszewski3, Jola Malesinska3, Grzegorz Gólszko3, Matthias Bucher4, Nikolaos Makris4, Aristeidis Nikolaou4, Ahmed Abo-Elhadid5, Marek Mierzynski6, Laurent Lemaitre7, Mike Brinson8, Christophe Lallement9, Jean-Michel Sallese10, Sadayuki Yoshitomi11, Paul Malisse12, Henri Oguey13, Stefan Cserveny13, Christian Enz10, François Krummenacher10 and Eric Vittoz10

1 MOS-AK Association (EU), 2 Centro Universitario FEI, Sao Bernardo do Campo (BR),
3 Institute of Electron Technology, Warsaw (PL), 4 Technical University of Crete, Chania (GR),
5 Mentor Graphics (USA), 6 Keysight Technologies (USA), 7 Lemaitre EDA Consulting,
8 London Metropolitan University (UK), 9 Icube, Strasbourg University (F), 10 EPFL Lausanne (CH),
11 Toshiba (J), 12 Europractice/IMEC (B), 13 CSEM S.A., Neuchatel (CH)

Accepted for ESSDERC/ESSCIRC 2019 in Krakow

Extraction of the threshold voltage, flatband voltage and gate capacitance in n-MOSFETs based on C-V

Input power spectral density $S_{VG}(f)$ for nMOSFETs

CMOS inverter characteristics

Acknowledgments: The authors would like to acknowledge Europractice for providing free access to UMC 180nm CMOS silicon and all corresponding libraries and PDKs for the EKV2.6 test chip design and manufacturing. M. A. Pavanello and M. de Souza thank the financial support of Brazilian funding agency CNPq.
Benefits Using Verilog-AMS

- For the model developers
  - Develop once and run everywhere
  - Focus on model equation, not on implementation

- For the software vendors
  - Simplified implementation of the standard models
  - Proprietary Verilog-A models are also supported

- For the silicon fabs
  - Standardized model parameter set

- For the end-users (designers)
  - Standardized libraries and design kits
MS Excel VBA Parameter Extraction

- Local parameter extraction using MS Excel VBA optimization

Integrated Tools for Modeling and Parameter Extraction

MPFIT - Robust non-linear least squares curve fitting

The IDL routines provide a robust and relatively fast way to perform least-squares curve and surface fitting. The algorithms are translated from MINPACK-1, which is a rugged minimization routine found on Netlib, and distributed with permission. This algorithm is more desirable than CURVEFIT because it is generally more stable and less likely to crash than the brute-force approach taken by CURVEFIT, which is based upon Numerical Recipes.

TRADICA
TRAnnsistor DImensioning and CAalculation program

- Provide criteria for transistor sizing
  - calculation of device dimensions
  - calculation of device configuration

- Fast means for generating consistent sets of compact model parameters based on design rules and process information

- Compact modeling/extractions for various types of devices and different compact model types
  - MOS (EKV)
  - Bipolar (SGPM, HICUM)
  - Passives (diode, res, mincap, …)

- Hierarchy modeling with different complexities w.r.t. physical effects

[REF]  K.E.Moebus, M.Schröter, H.Wittkopf, Y.Zimmermann, M.Claus; TRAnnsistor DImensioning and CAalculation program
DMT: Device Modeling Toolkit

Open License Parameter Extraction Toolkit For SiGe HBTs
HiCUM Group at TU Dresden

- **Python + Git**
  - Reasonable code quality with focus on readability
  - Automated code documentation
- "Glue" open-source software components
- Framework for extending functionality
- Interface to include circuit/SPICE and TCAD DEVICE simulators
- Modular and Reusable widgets for new GUIs
- Not restricted to a single model!

PROFILE: Inverse Modeling Tool

The PROFILE [1] is a tool for inverse modeling of the semiconductor devices using 2D data and advanced optimization driver. All the files and its documentation is available at the official homepage of PROFILE:

http://profile.ewi.tudelft.nl/
http://sourceforge.net/projects/profile2d

PROFILE: Inverse Modeling Tool

: main.pro : main optimization loop
type v_m i_m i_s $
var real VTO UO KP $
: read measured IV data
get IdVg.dat v_m i_m $
: set LEVEL3 parameters
VTO = 1.0
UO  = 425
KP  = 2E-4
: Constrain specifications
constrain VTO 0.1 2
constrain UO 100 500
constrain KP 0.1E-4 1E-3
setlm deltapr 0.01
: call external non-linear model
setext call ~/bin/profile ngspice.pro > ngspice.log
setlm talk 2
setlm itermax 15
: levmar fits a non-linear model to measurement data.
levmar pro i_m v_m i_s VTO KP | UO $

Transfer MOSFET IV characteristic after VTO, U0, KP extraction
(o :measured, - :simulated)

Standardized Data Exchange
For Device Modeling Tools

The **MDM** file format (developed and open by **Agilent**) provides the following advantages:

- **ASCII based file**
- **Table-based, row-column format with column header lines that make reading easy**—includes a list of the innermost independent variables.
- **All data tables have identical shape. A header at the top of the file provides an outline of all the data in the file. After the header has been parsed, the location of any data group can be computed quickly, permitting rapid location of arbitrary data groups scattered throughout the file.**

  Comment lines are denoted by the exclamation character(!). The file extension for the data files is .mdm (**measured data management**).
FOSS Modeling/Simulation Flow

Process/Technology TCAD
- Cogenda TCAD
- DevSim TCAD
- other EM Simulators

Compact Modeling Model Libraries
- Spice/Verilog-A Simulators
- Verilog-A Standardization
  - ADMS
  - MAPP
- measurements
- parameterization
- other

Analog/RF IC Simulation
- Ngspice
- Qucs
- Xyce
- GnuCap
- other
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SUMMARY (Open Topics)

• Process TCAD Simulation
  – Interoperability:
    Data Exchange Formats

• Compact/SPICE Modeling
  – Verilog-A Standardization
  – Simulated/Measured Data Exchange

• Analog/RF Circuit Simulation
  – Interoperability:
    Netlist/Schematic Exchange Formats
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