Finding root causes of convergence failures in circuit simulation

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Agenda

1. **Introduction**
2. What is a simulation convergence issue?
3. How to find convergence issues
4. Conclusions

Introduction: Convergence Issues

Convergence Problems in Designs are of the kind

- DC-Op Simulation not working
- Transient simulation stopping before end
- Often accompanied by spikes or oscillations in signals

What can we do against it?

- Avoiding certain equations in models by setting switching/mode parameters
- Avoiding certain model parameter values / combinations
- Changing model by sending requests to Compact Model Coalition (CMC)

Introduction:Compact Modeling Coalition: https://si2.org/cmc/

The Compact Model Coalition (CMC) is a working collaborative group focused on the standardization of SPICE (Simulation Program with Integration Circuit Emphasis) device models.

When a new or enhanced chip is designed, it must be simulated prior to manufacturing. This can be thought of as proof of concept and is vitally important to validate the concept before it enters the capital intensive phase of manufacturing. The simulations are based on standard models (expressed in the form of equations) governed by CMC.

Once the standard models are proven and accepted by CMC, they are incorporated into design tools widely used by the semiconductor industry. The equations at work in the standard models setting process are developed, refined and maintained by leading universities the CMC directs and funds to standardize and improve the models.

The members of our coalition are modeling experts. All join the CMC for an important and highly valuable reason: they want to be a voice, an influencer, for themselves and their companies in the standard-model- setting process.

Members

- >20 semiconductor companies
- model developing universities/institutes
- all big EDA vendors

Introduction: Compact Models of Compact Model Coalition (CMC)

Name	Description	CMC standard	Reference code
VBIC	Bipolar	no	Not available
BJT	Bipolar	no	Not available
HiCUM	Bipolar	yes	VerilogA
BSIM3V3	CMOS	yes	C code
BSIM4	CMOS	yes	C code
BSIMBulk (+HV option)	CMOS/LDMOS	yes	VerilogA
HiSIM-HV	LDMOS	yes	VerilogA
Diode_CMC	Rev rec diode	yes	VerilogA

... and many others

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Transient Convergence: Error Criteria

Convergence in a transient simulation is achieved if three conditions are fulfilled:

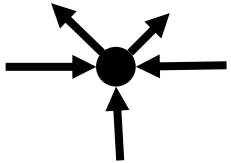
› Voltage: for each node n, between successive iterations k and k+1

$$|V(n,k+1) - V(n,k)| < vabstol + reltol\, V_{ref}(n)$$ Voltage Condition

› Current: for certain branches b, between successive iterations k and k+1

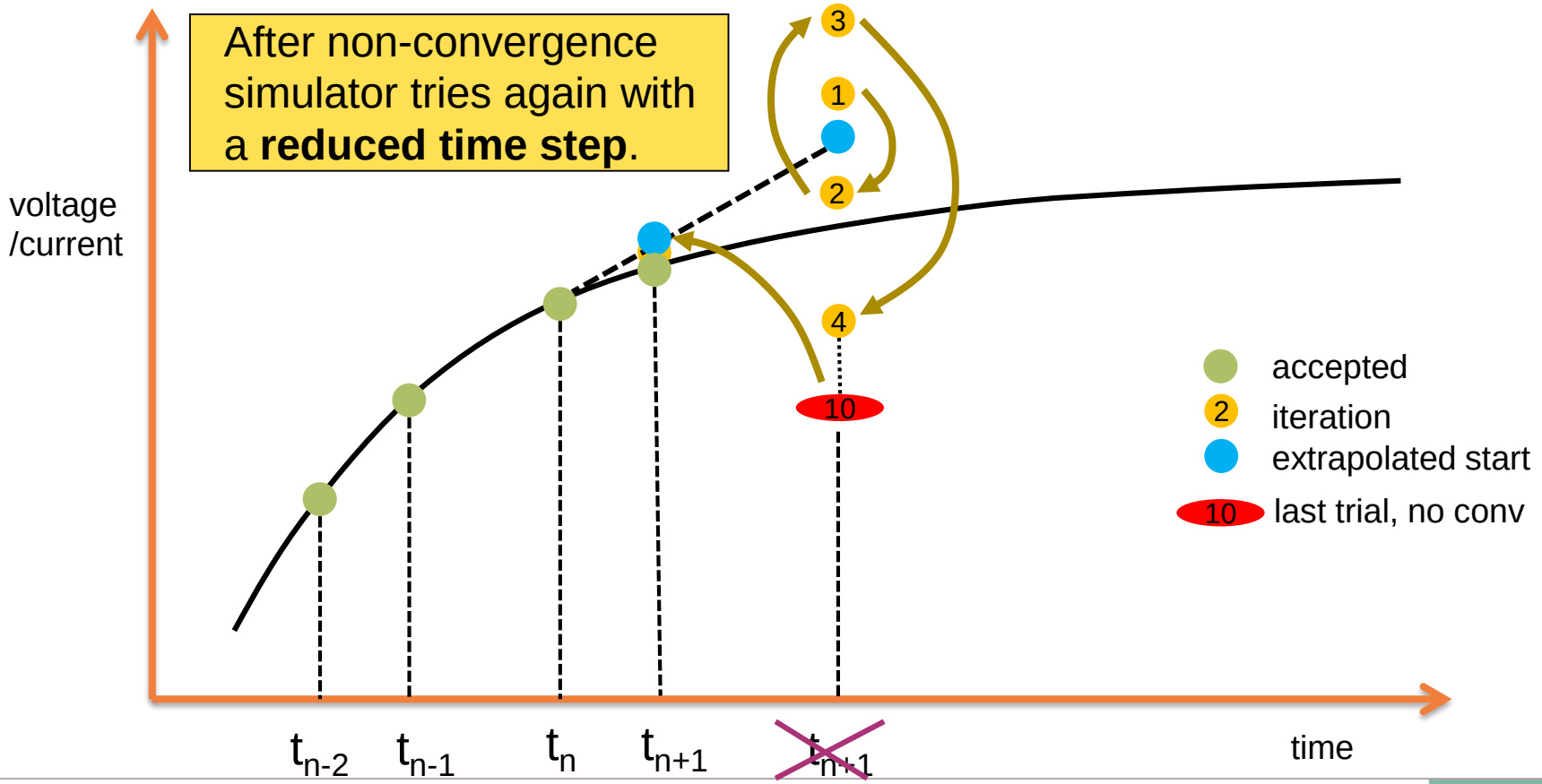
$$|I(b,k+1) - I(b,k)| < iabstol + reltol\, I_{ref}(b)$$ Branch Current Condition

› Kirchhoffs Current Law (KCL):
For each node n, the sum of all branch currents into n is close to zero

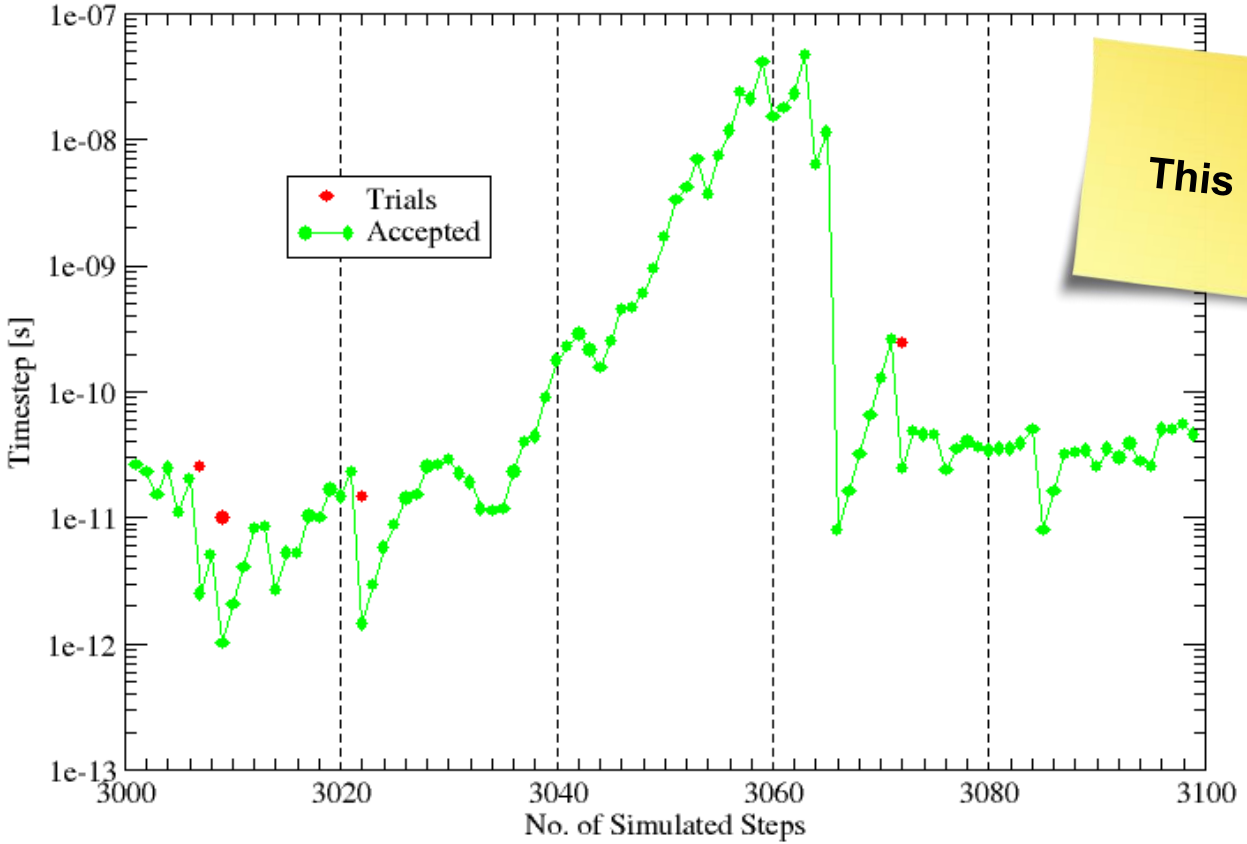


$$Residue = \sum_{branches\ into\ n} I(b) < iabstol + reltol\, I_{ref,KCL}(n)$$ Residue Condition

Non convergence incidence

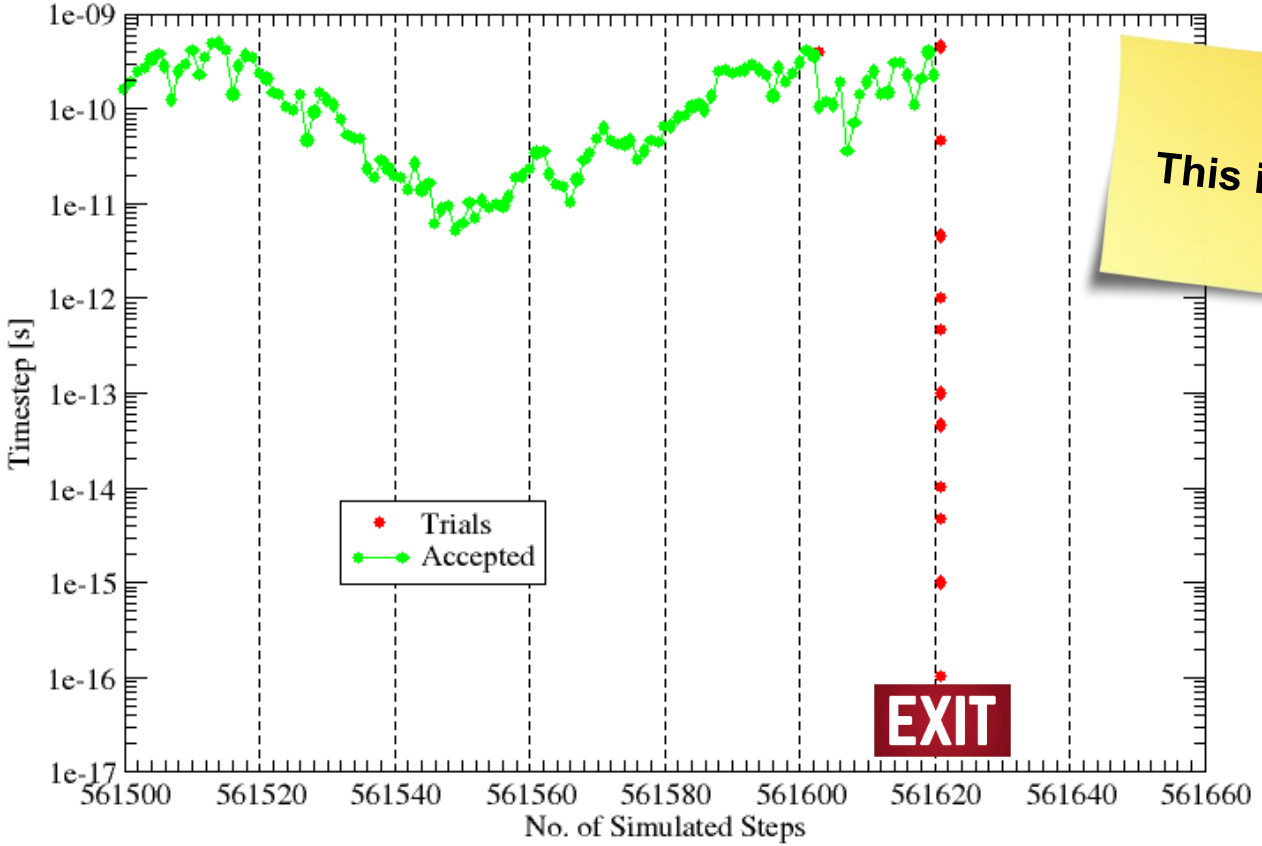


Convergence: normal simulation



This is ok.

Convergence: failing simulation



This is fatal!

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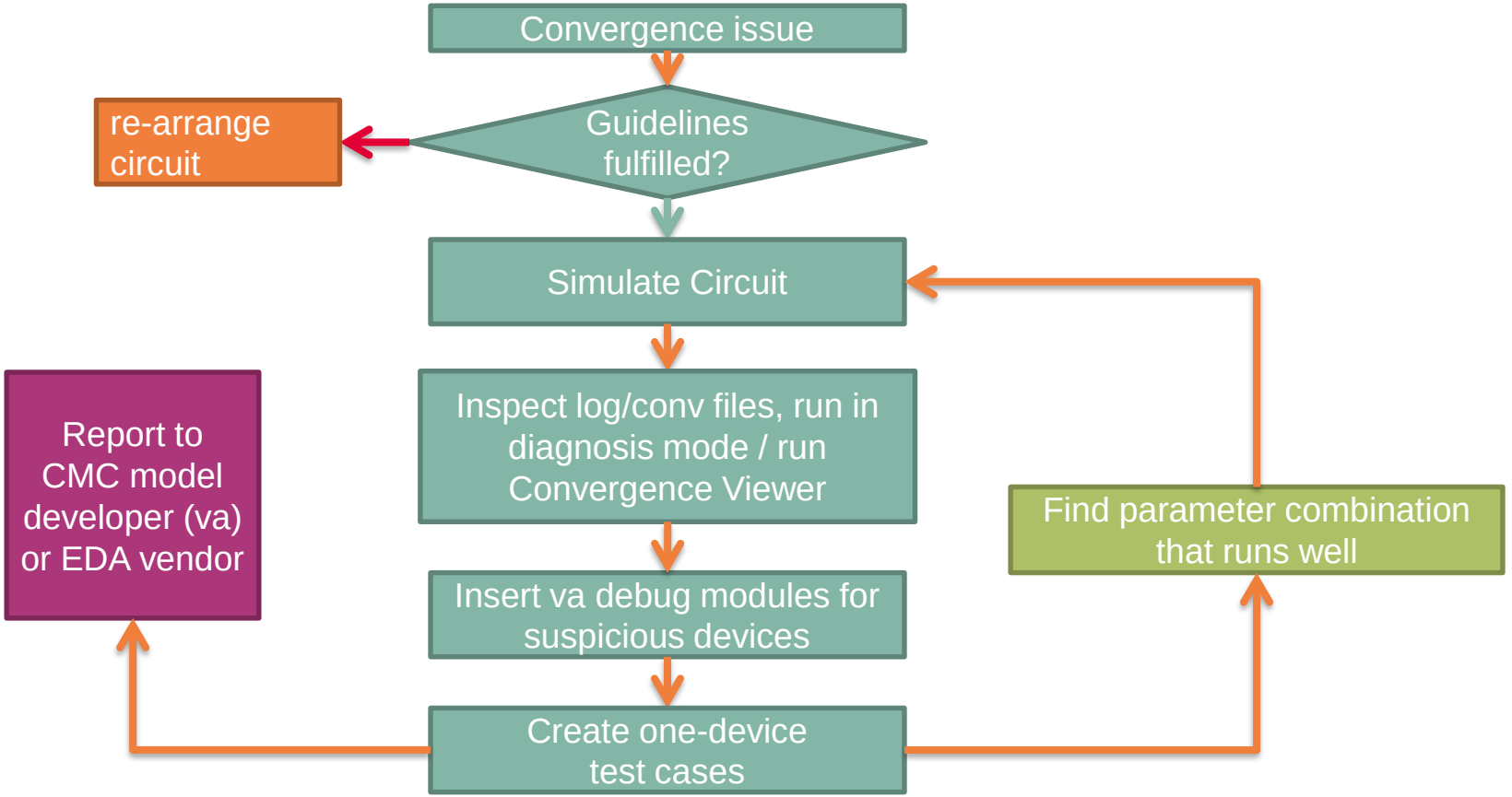
Process Flow for convergence issues



The „spy“ modules written in verilogA for debugging

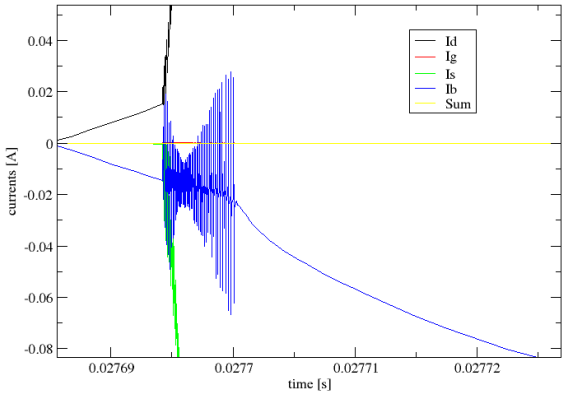
```
module monitor_overv_4(a, b, c, d);
inout a, b, c, d;
electrical a, b, c, d;

integer niter, l_flag;
real xtime, deltat, ia, ib, ic, id, csum;
real vlimit=1000;
analog begin
    @(initial_step("tran")) begin
        niter=0; xtime=0.0;
    end
    niter=niter+1;
    deltat=$abstime-xtime;
    xtime=$abstime;
...
        if (l_flag > 0) begin
            $debug("data_overv_4_overflow     %M %d %e %e %e %e %e %e", niter, xtime, deltat, V(a), V(b), V(c), V(d));
        end
        $strobe("data_overv_4_sol        %M %d %e %e %e %e %e %e", niter, xtime, deltat, V(a), V(b), V(c), V(d));
    end
end
endmodule
```

Detection of

- timing, time steps for each iteration
- over-currents, over-voltages for each iteration step
- oscillations
- current sum for a device > epsilon

Output Example: Oscillations



Output and IC/nodeset summary:
save 26 (current)
save 18 (voltage)

.....9.....8.....

====> Possible Convergence Issue at stepid= 4414, t= 2.769424e-02 s!!!! Sum of currents = 4.343089e-05 A
====> at V(d) = -1.380687e+00, V(g) = -1.052857e+00, V(s) = -1.453365e-04, V(b) = -2.612077e-03

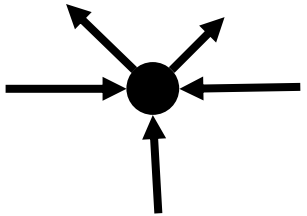
====> Possible Convergence Issue at stepid= 4519, t= 2.769468e-02 s!!!! Sum of currents = 6.106508e-05 A
====> at V(d) = -1.312721e+00, V(g) = -1.004916e+00, V(s) = -1.821515e-03, V(b) = -4.384443e-03

.....9.....8.....7.....6.....5.....4.....3....

====> Possible Convergence Issue at stepid= 14192, t= 7.280580e-02 s!!!! Sum of currents = 1.980038e-05 A
====> at V(d) = -1.389452e+00, V(g) = -1.065566e+00, V(s) = -1.209514e-04, V(b) = -2.410340e-03

.....9.....8.....7.....6.....5.....4.....3.....2.....1.....0
Number of accepted tran steps = 18385

Idea: Watch the residues that do no fulfill the residue condition

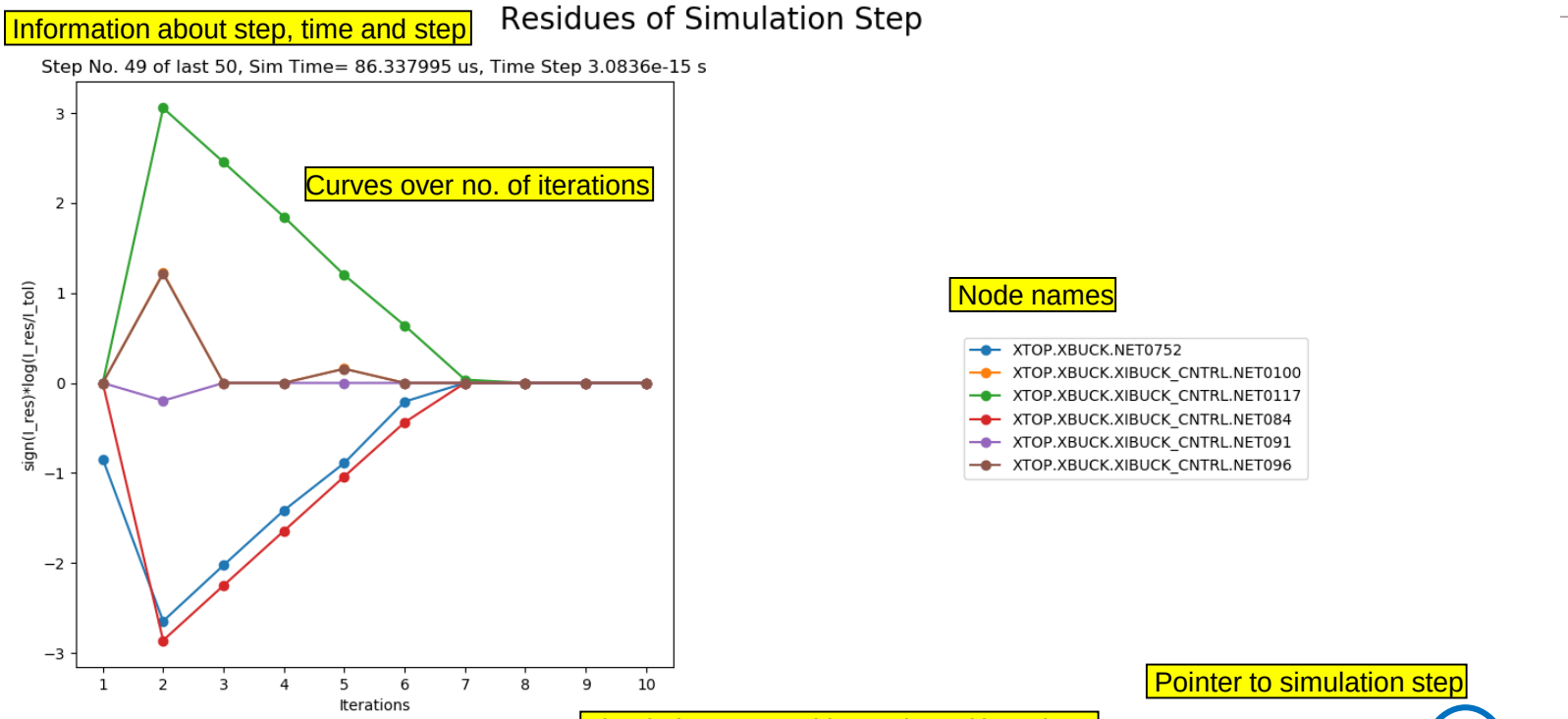


$$I_{Residue} = \sum_{branches\ into\ n} I(b) < iabstol + reltol\ I_{ref,KCL}(n) = \mathrm{I_{Tol}}$$

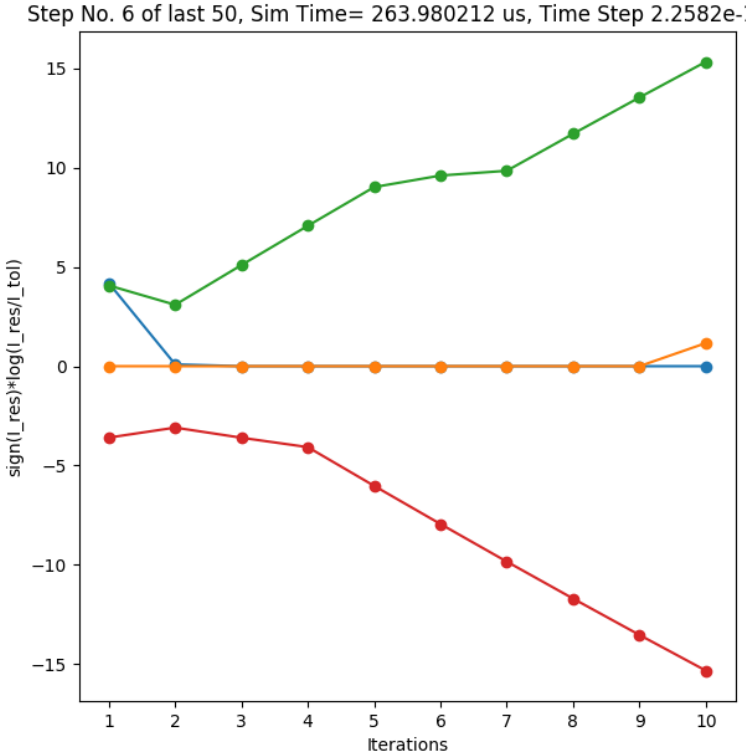
- For reaching convergence it is necessary that the residues of all nodes are beyond a small tolerance.
- Finding the nodes where this criteria is not fullfilled can lead us to the root cause of convergence failures

Convergence Analyzer Tool: Residues

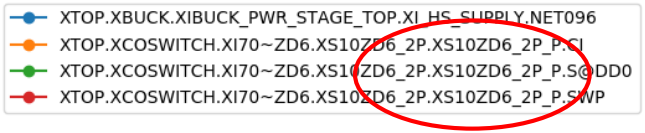
Information about step, time and step



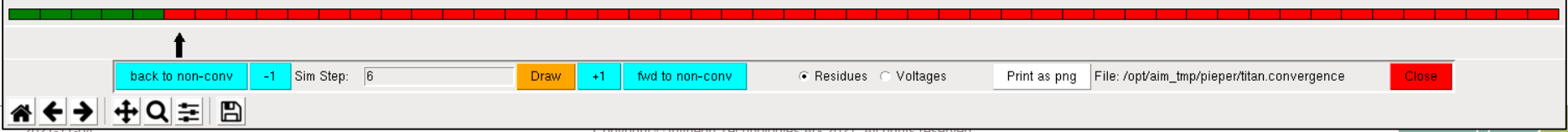
Residues of Simulation Step



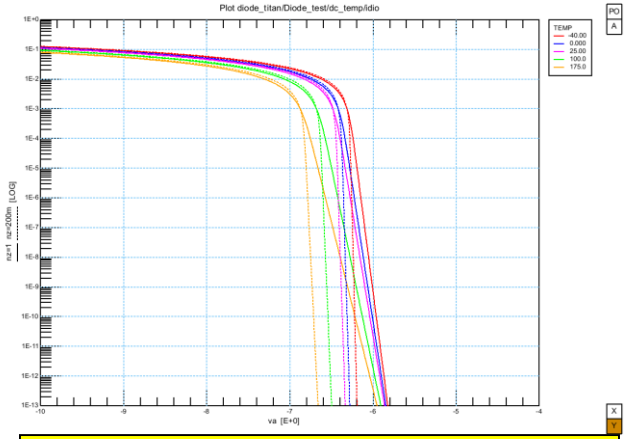
Example 1



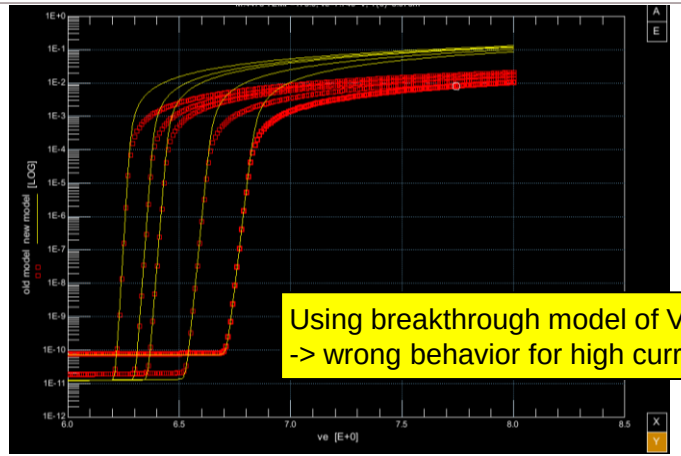
Here: Analysis points to zener diode model s10zd6



Example1: Possible solutions changes in zener diode model

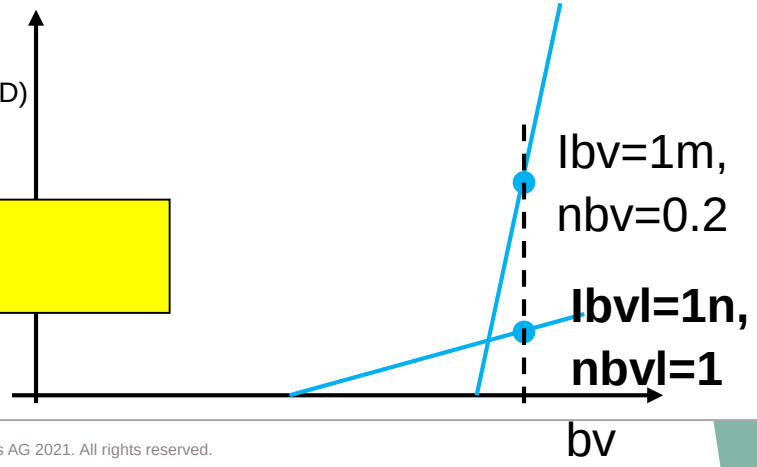


Changing parameter nz (nbv) from 0.2 to 1
-> wrong slope in breakthrough characteristic



Using breakthrough model of VBIC
-> wrong behavior for high currents

Final solution: use parameters nbvl and ibvl for smooting the corner



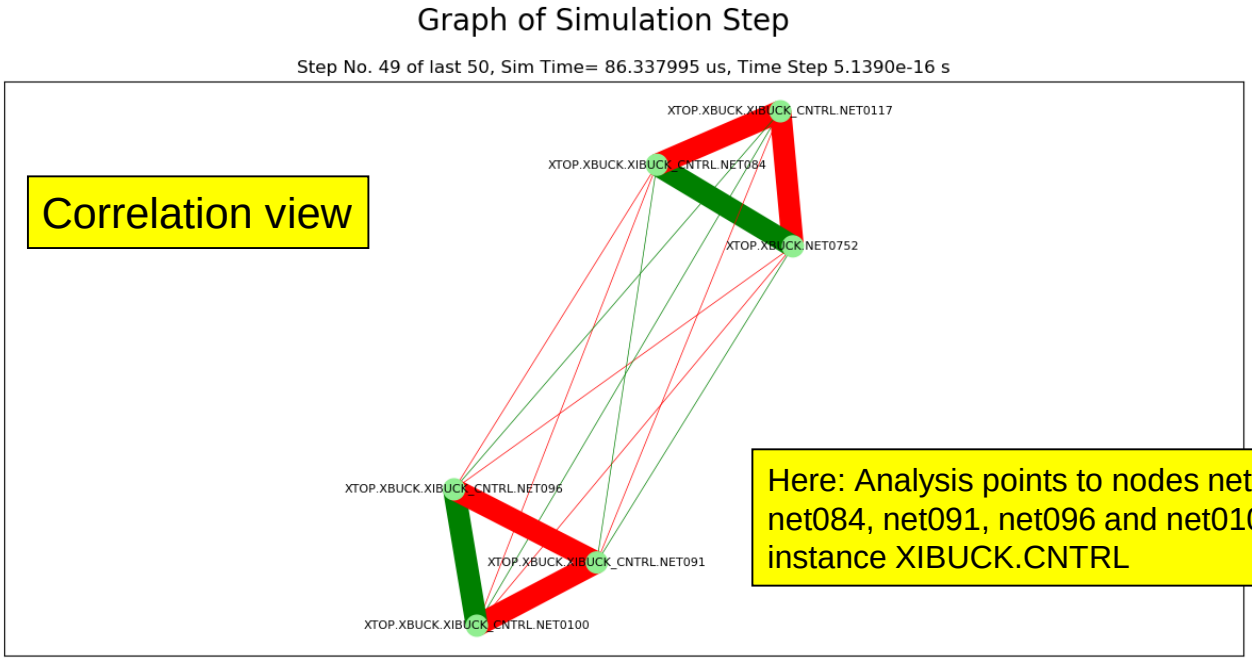
Correlation of residues

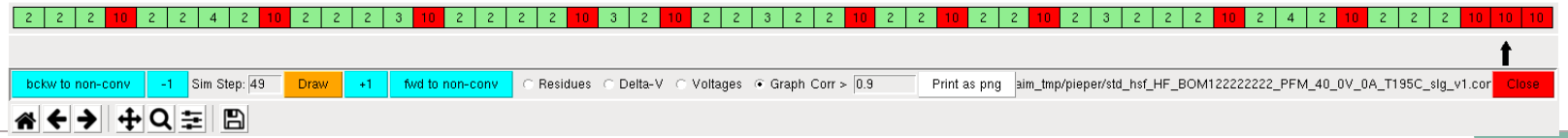
If a model changes behavior so rapidly that residue conditions of nodes A and B cannot be fullfilled, the residues on A and B should be strongly (anti-) correlated or anti-correlated.

Crazy model / equations

A negative correlations of residues between nodes might give us a hint that there is something wrong in the model between these two nodes.

Convergence Analyzer Tool: Correlations





The „Killer-NOR Gate“ Problem (BSIM4)

Problem of MOSFET models with quasi static approach

› when transistor is turned on with a fast voltage ramp at the gate a negative current is flowing in the very first moment (where I_D is neglectable).

$$I_D(t) = I_D - C_{gd}\frac{dv_{GS}}{dt}$$

› The longer the channel the bigger the error, since C_{gd} is higher

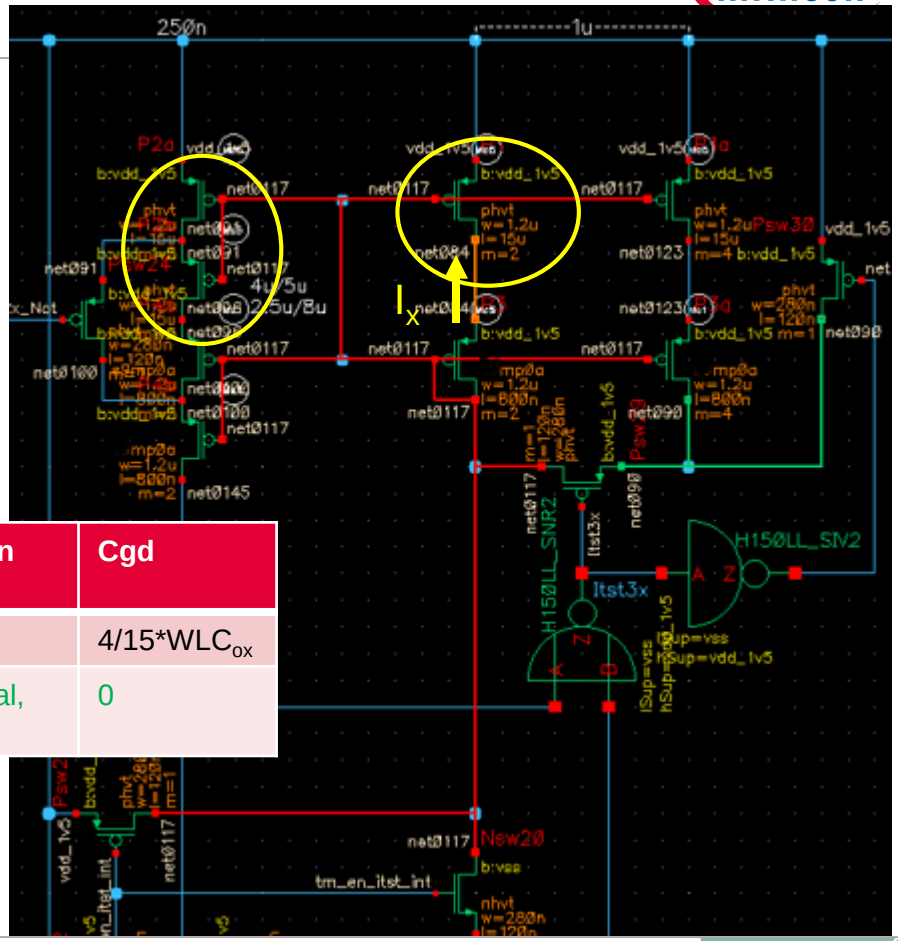
xpart	Charge partition d/s	Cgd
0	40/60	4/15*WLC_{ox}
1	0/100 (unphysical, but working)	0

Solution

› Set parameter „xpart“ to 1

or

› Use NQS model (trnqsmod=1)



See William Liu: MOSFET Models for SPICE Simulation page 284 ff.

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Conclusions

- Finding root causes of simulation convergence failures is still a challenge
- Inspection of what the simulator does during iterations is necessary
- Remaining residues give valuable hints on critical nets / devices
- Negative correlations between remaining residues give even more insight

Part of your life. Part of tomorrow.