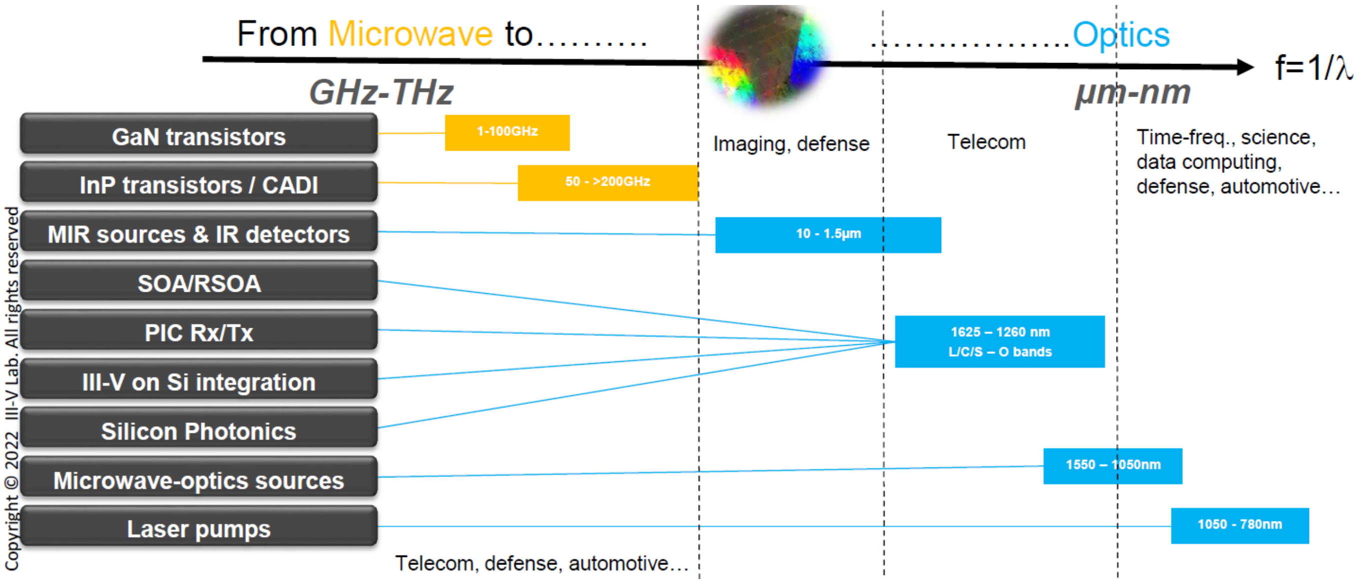
III-V Lab presentation
AKB 2023

Bertrand ARDOUIN - Romain HERSENT

Nov 9-10 2023

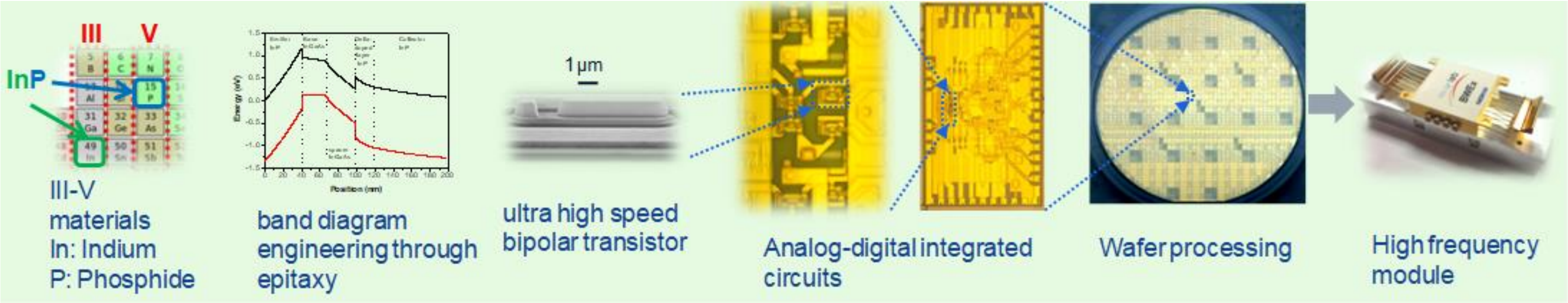
III-V lab : an industrial research lab dedicated to III-V material

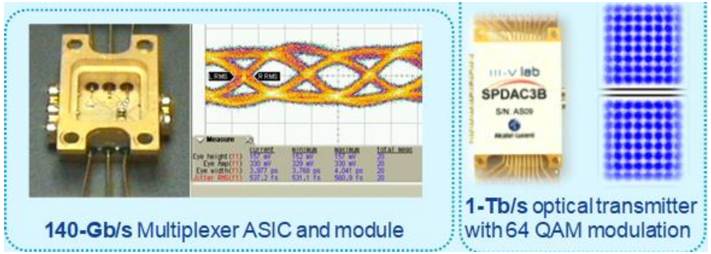
- III-V lab topics : microlectronics and optics
- Key activities: from epitaxy to device fabrication, integrated circuits design and packaging

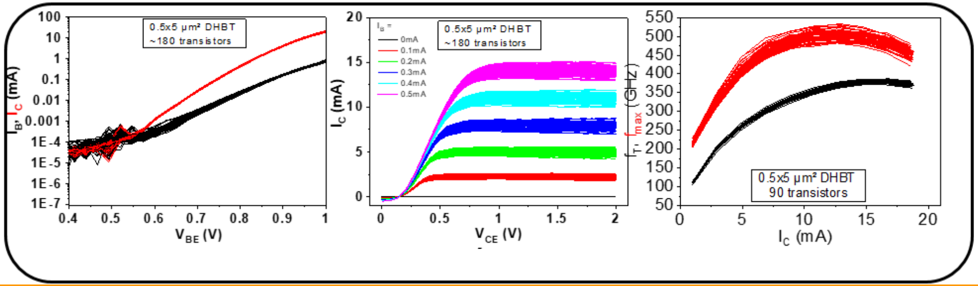


Focus on the High Speed Analogue digital interfaces group (CADI)

- In house InP DHBT technology, modeling, circuit design and packaging







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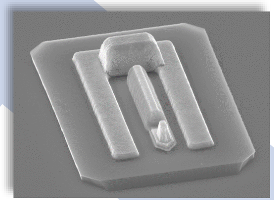
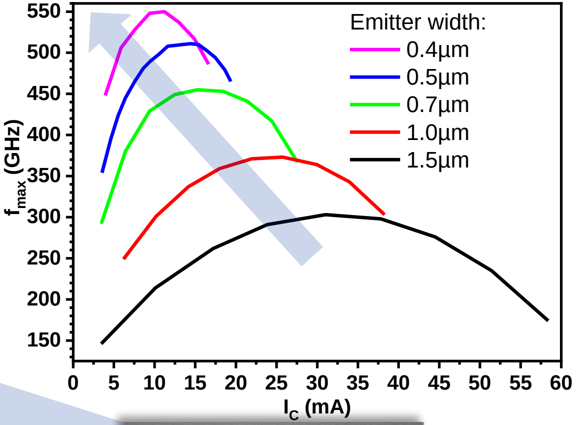
III-V Lab technology over the years



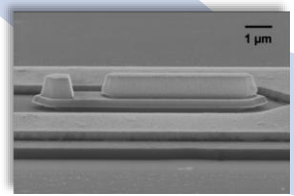
2021
0.4-µm HBT

2020
0.5-µm HBT circuit

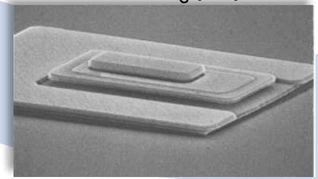


Technological improvements drivers:

- Transistor geometry
- Epitaxial structure
- e-beam/stepper lithography
- Material etching
- Under-etching control
- Quality of ohmic contacts

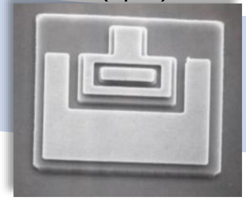


2010
0.7-µm HBT



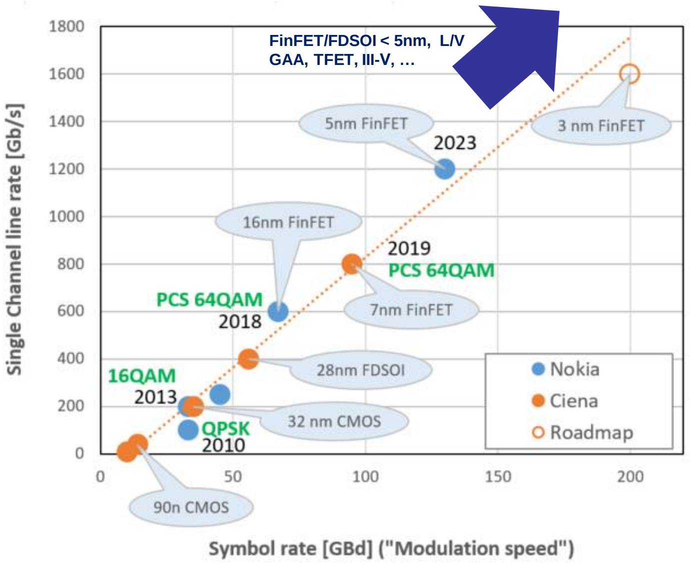
2003
Self-aligned
contacts (2µm)

1994
First InP HBTs
(4µm)



1980
GaAs HBT
(150µm)

Application context of our technology



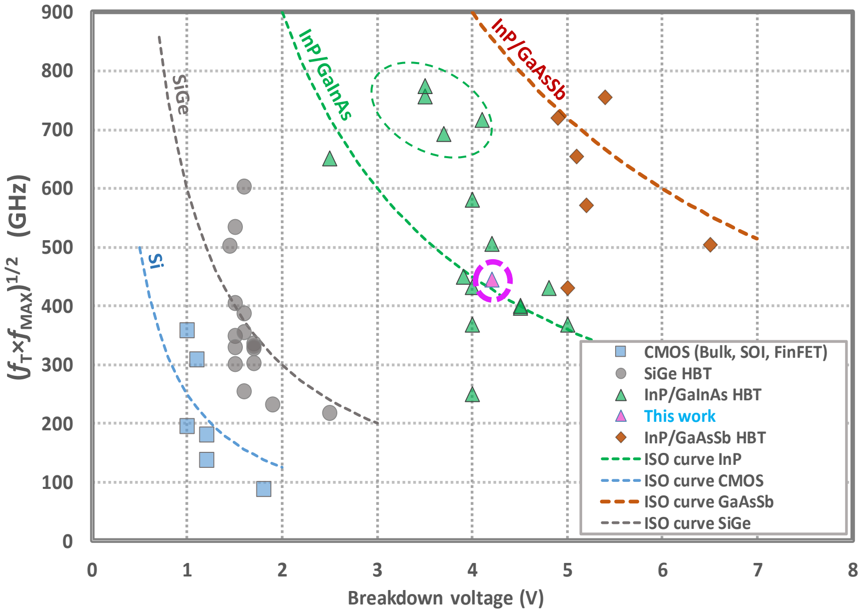
Optical interfaces Competition
(optical fiber communications)

Nokia PSE-VI: **Current GEN ASICs at 130 GBd generating up to 1.2 Tb/s**

PSE-6 super-coherent optics opens a new frontier in network scale, performance and sustainability

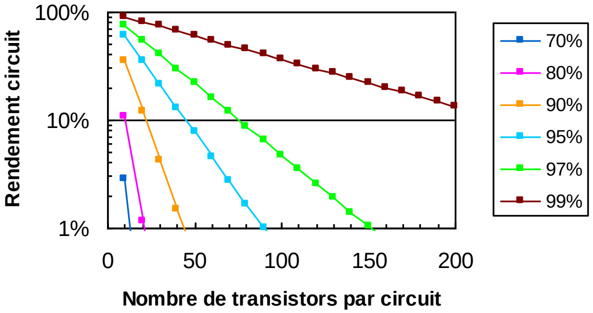
Towards 200 GBd PCS-QAM coherent transmissions

Our baseline technology Benchmark



III-V lab InP DHBT baseline technology aims small to medium scale IC fabrication

(ie, > 99% transistor yield)



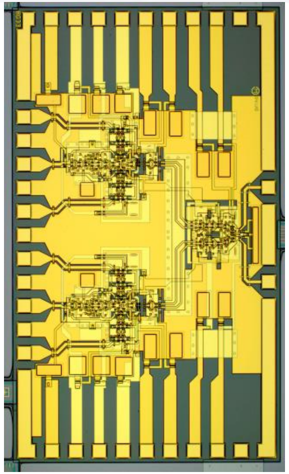
R. Hersent et al., "InP DHBT Linear Modulator Driver With a 3-Vppd PAM-4 Output Swing at 90 GBaud: From Enhanced Transistor Modeling to Integrated Circuit Design," in IEEE Transactions on Microwave Theory and Techniques, doi: 10.1109/TMTT.2023.3305150.

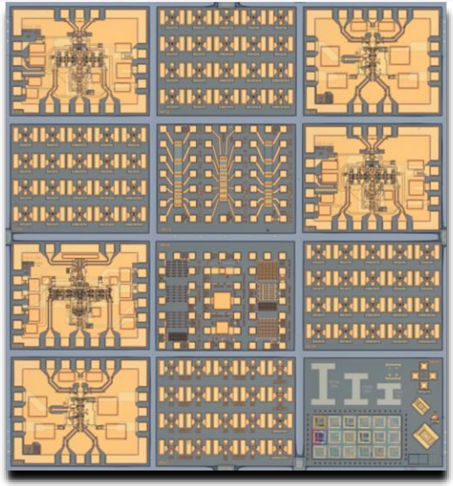
Note: although some circuits can work beyond that limit, BVCEO still constitute a limitation to be considered

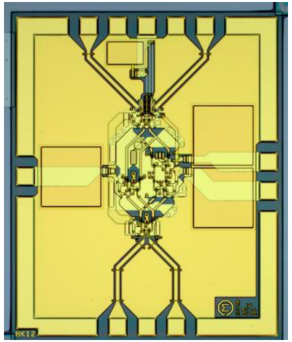
Technology usage

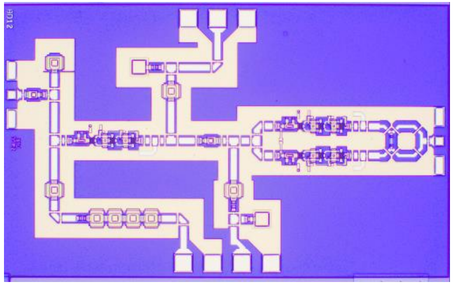
- The process itself is used to fabricate very high performance circuits on a regular basis (MPW)
- It's also used as a validation vehicle for technology developments

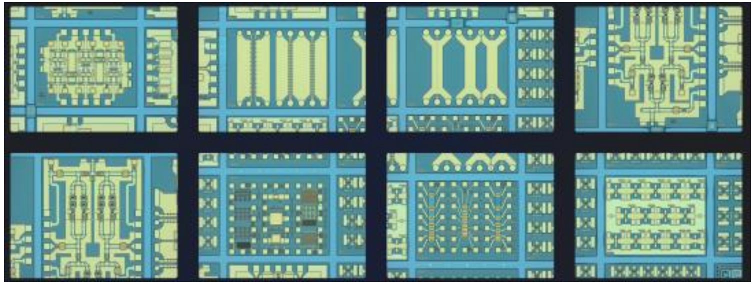
Our main target is to maintain yield across technology variants → this is a constraint for performance improvement











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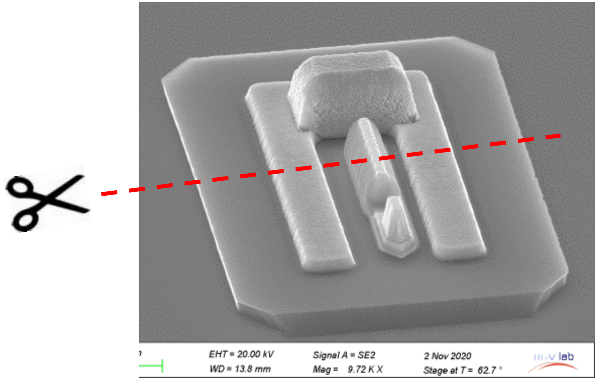
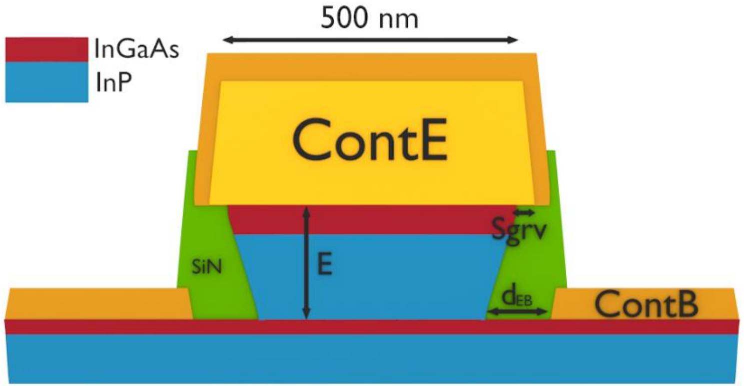
Current process « Work Horse »
0.5µm InP DHBT / TiPdAu emitter



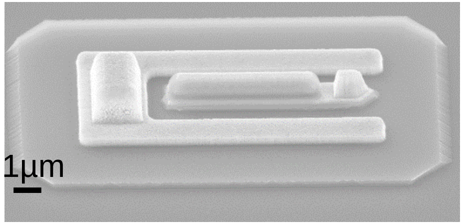
Baseline HBT

- 0.5µm
- Lift-off TiPdAu
- dEB > 60nm

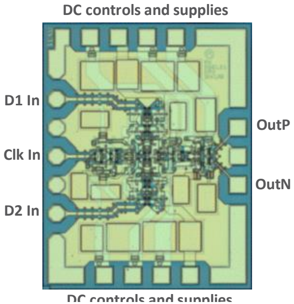


Baseline technology description

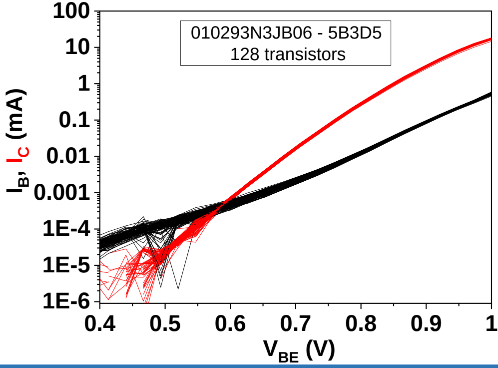
- Fabrication yield > 98 %
- Performances:
  - β > 30
  - BV_{CE0} > 4.5 V
  - f_T = 370 GHz, f_{max} **> 500 GHz**
  - J_C ~ 6 mA/µm

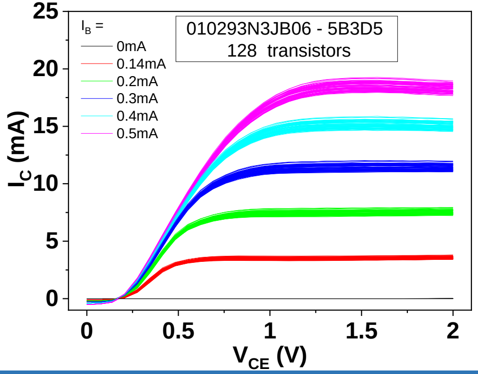


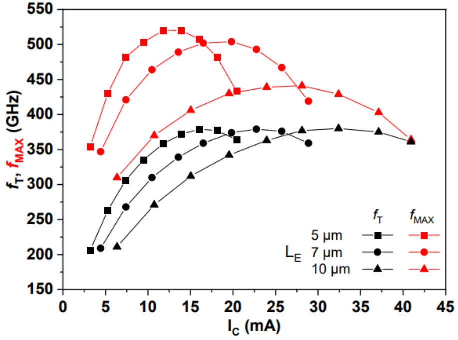
Beyond-160-GSa/s 0.5-µm InP DHBT AMUX-driver



R. Hersent et al.,"160-GSa/s-and-beyond 108-GHz-bandwidth over-2-Vppd output-swing 0.5-µm InP DHBT 2:1 AMUX-driver for next generation optical communications", 2022 MTT-S IMS Symposium Proceedings, June 2022





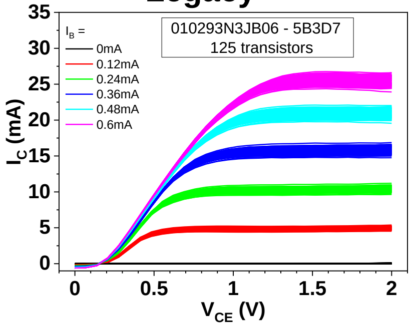


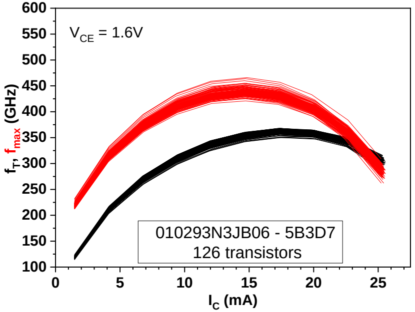
3 emitter lenghts are available :
5-, 7- and 10-µm

0.5-µm InP DHBT with f_T ~ 370 GHz and f_{MAX} > 500 GHz

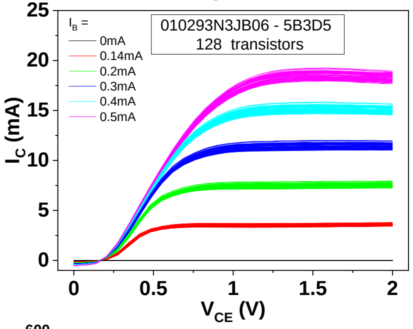
Different HBT generations on the same wafer

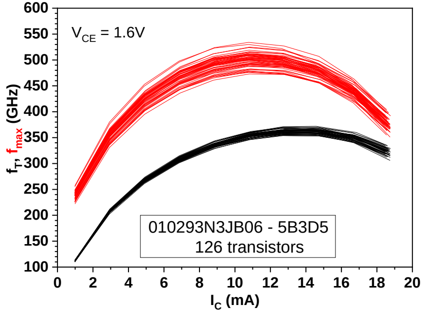
$W_E = 0.7\ \mu m$ Legacy



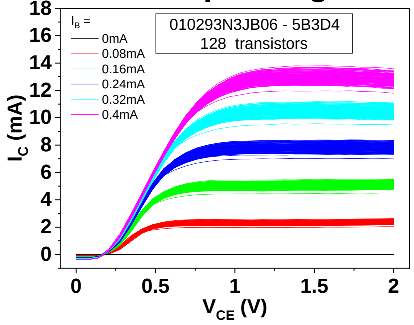


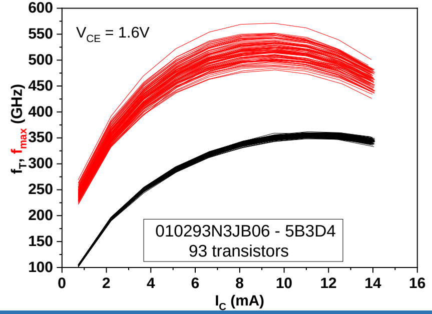
$W_E = 0.5\ \mu m$ current generation





$W_E = 0.4\ \mu m$ Under-development generation

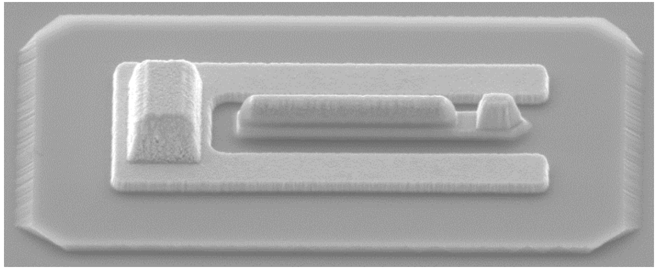




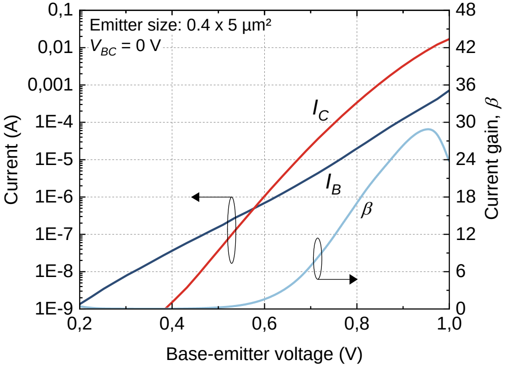
Homogeneous performances and high fabrication yield for 3 different emitter sizes

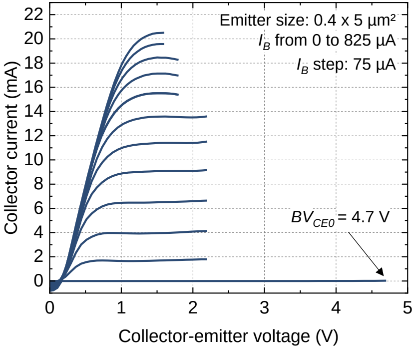
0.4-µm InP DHBT next generation

- Fabrication yield > 98 %
- Performances:
  - β =29
  - BV_{CE0} > 4.5 V
  - f_T = 380 GHz, $\boldsymbol{f_{max}}$ **> 600 GHz**
  - J_C ~ 6 mA/µm

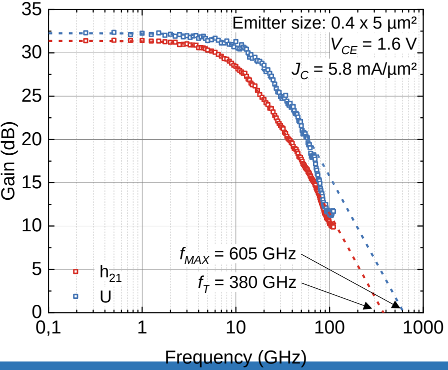


W_E=0.4µm, L_E=5µm
W_B=0.2µm





N. Davy , V. Nodjiadjim, M. Riet, C. Mismer, M. Deng, C. Mukherjee, J. Renaudier, C. Maneux, "0.4-µm InP/InGaAs DHBT with a 380-GHz f_T, > 600-GHz f_{MAX} and BV_{CEO} > 4.5 V", 2021 IEEE BiCMOS and Compound Semiconductor Integrated Circuits and Technology Symposium (BCICTS)



Improved frequency performances demonstrated: f_T=380 GHz and f_{max} > 600 GHz

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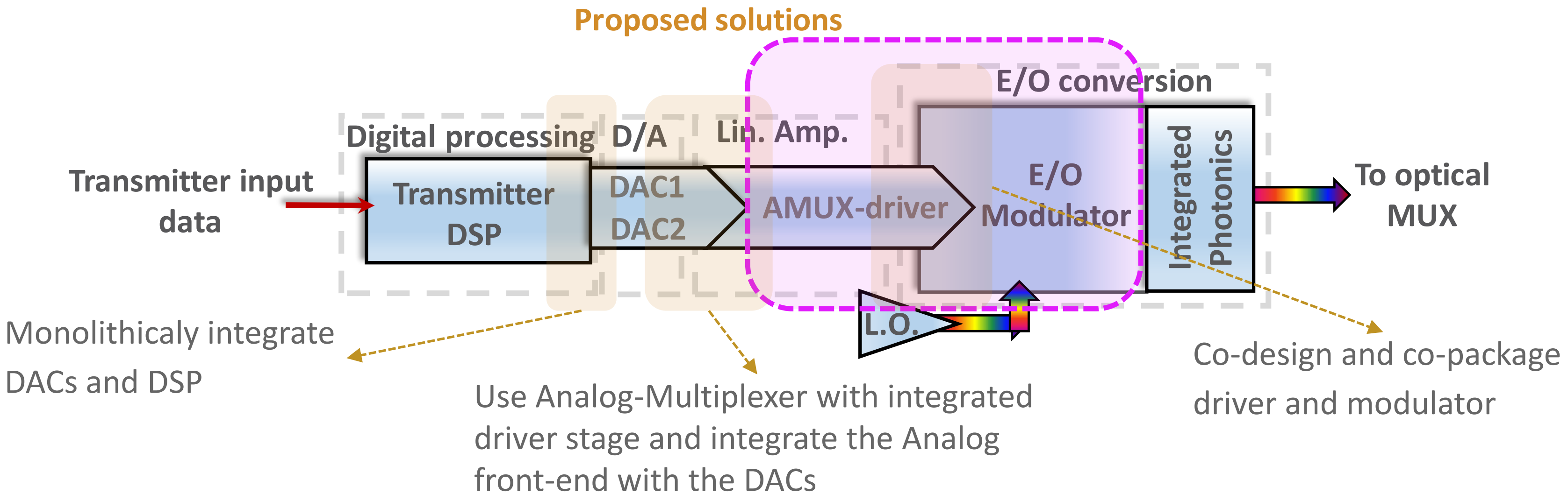
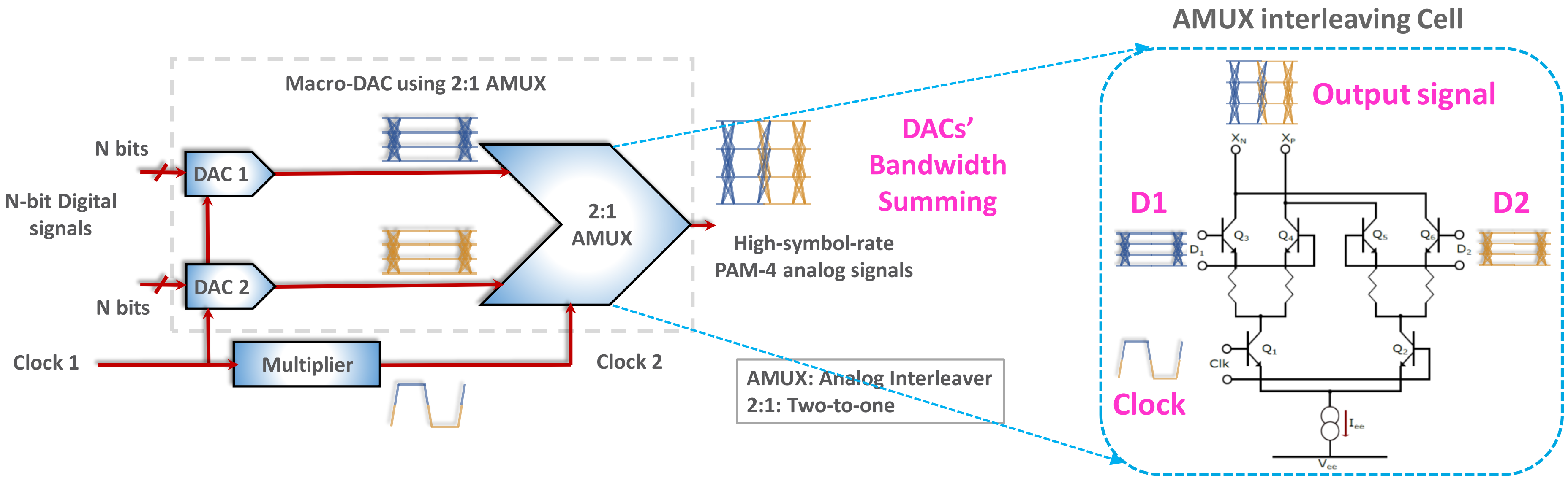
Optical transmission

- Reduce sources of bandwidth degradations and use innovative approaches



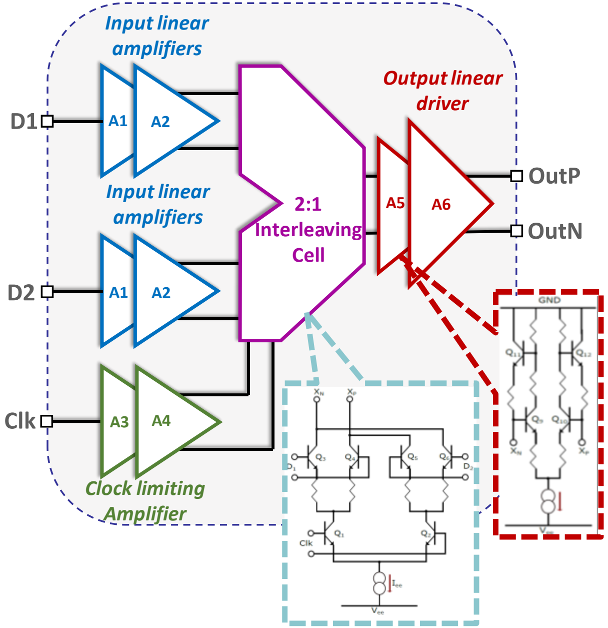
Analog multiplexer (AMUX) principle of operation

DACs’ Bandwidth Summing using a High-Sampling-Rate AMUX



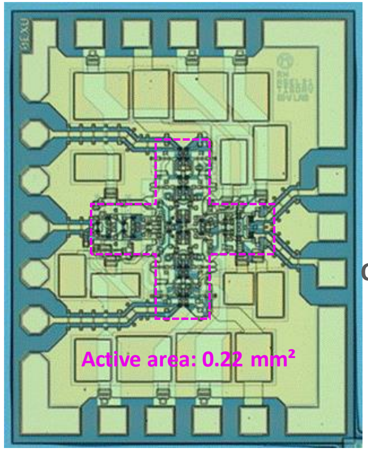
AMUX-driver details and performance

Block Schematic



Die: 1.2 x 1.5 mm²

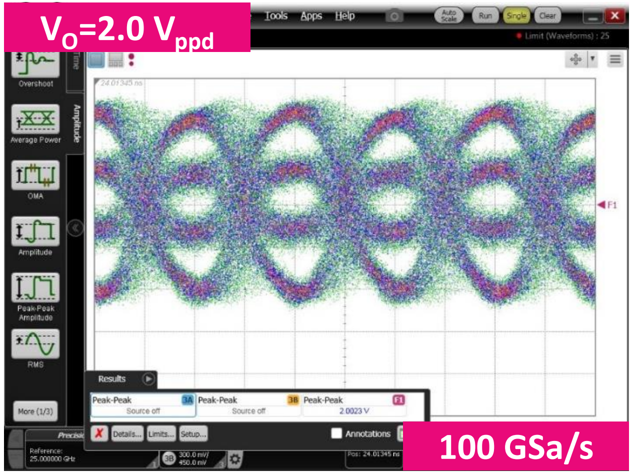
DC controls and supplies



DC controls and supplies

IC fabrication at III-V Lab
by M. Riet and C. Mismer

100-GBaud PAM-4 output (electrical) eye diagram

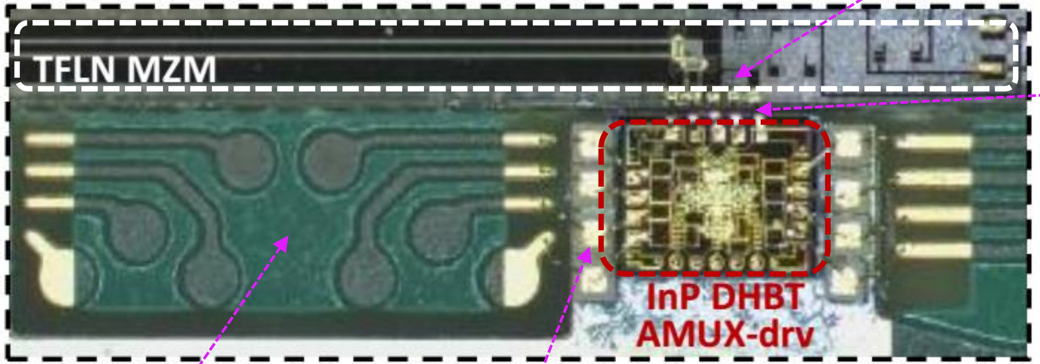


Total power consumption @ 2-Vppd: 1.2W

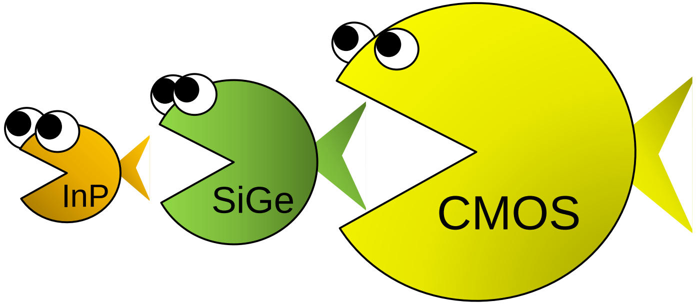
R. Hersent et al, "100 GBaud DSP-free PAM-4 optical signal generation using an InP-DHBT AMUX-driver and a Thin-Film Lithium Niobate Modulator Assembly", BCICTS 2023

High-performance InP-DHBT AMUX-driver IC with large output swing

- AMUX-driver assembly with TFLN MZM optical modulator at III-V Lab
- Assembly picture



What about the future of InP technology ?



Common (accepted) vision:

- What can be done in CMOS will be done in CMOS
- What can't be done in CMOS will be done in SiGe
- What can't be done in SiGe will be done in III-V

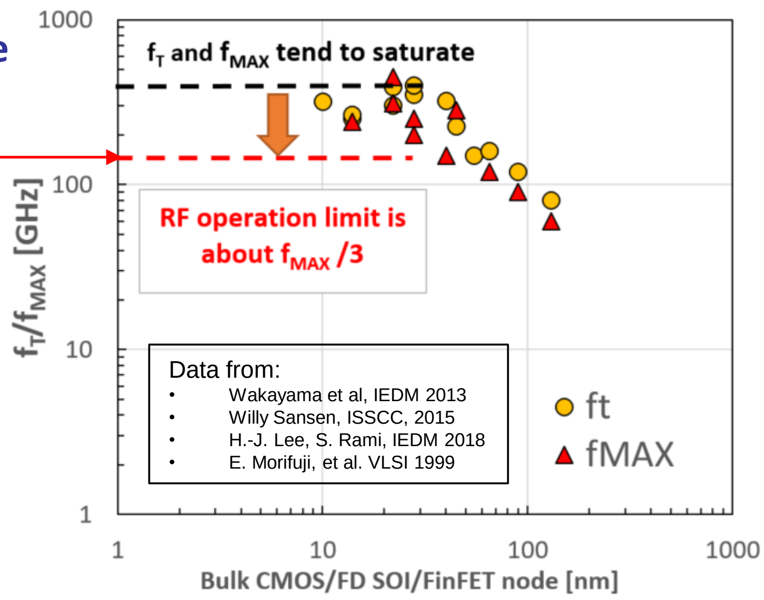
The driving force for CMOS is digital baseband (huge market = huge investments)

What can be done in CMOS, will be done in CMOS

What about the future of InP technology ?

CMOS f_t and f_{MAX} reached saturation around 28 nm node

approximately equal to the start of D band



Where CMOS is not fast enough, SiGe BiCMOS comes into play

The limit is partly determined by market size and amount of digital content

What's left for III-V and InP?

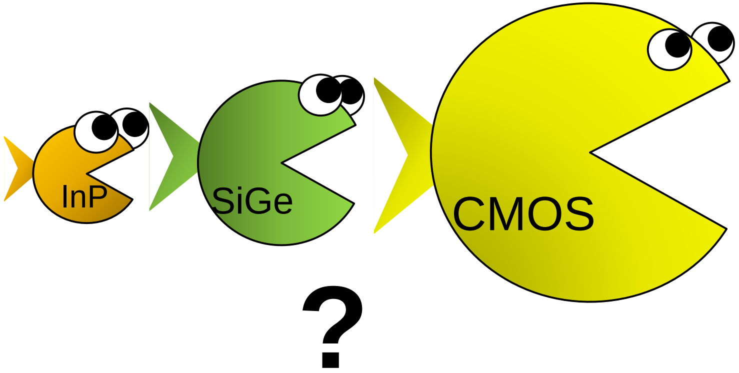
CMOS f_t and f_{MAX} reached saturation @ 28 nm node

What about the future of InP technology ?

So what ? Shouldn't it be the opposite ?

Despite superior performance: InP stays a niche market technology

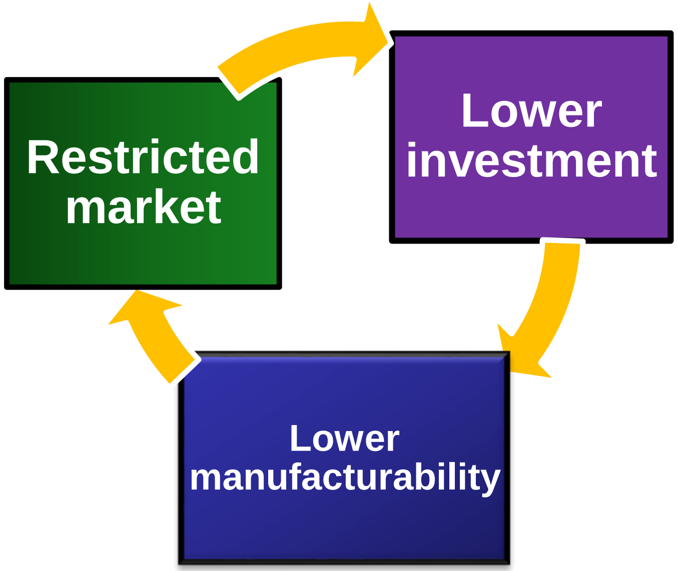
- **InP is more expensive**
  - Small diameter wafers
  - More expensive & rare material
  - Brittle material
  - No economy of scale
- **Lower integration level, lower yield**
- **Not easily compatible with digital CMOS (baseband)**
- **Reliability**
  - no foreseen penalty wrt silicon, but limited literature and work published
- **Modeling /PDK ?**
  - When a silicon designers has a modeling issue, he asks for a fix
  - When a III-V designer has a modeling problem, he thinks “is it really useful to fix it, process variations are larger in anyway”
- **Lower maturity**
- **backend not compatible with mainstream Silicon packaging**



→ **Lower manufacturability**

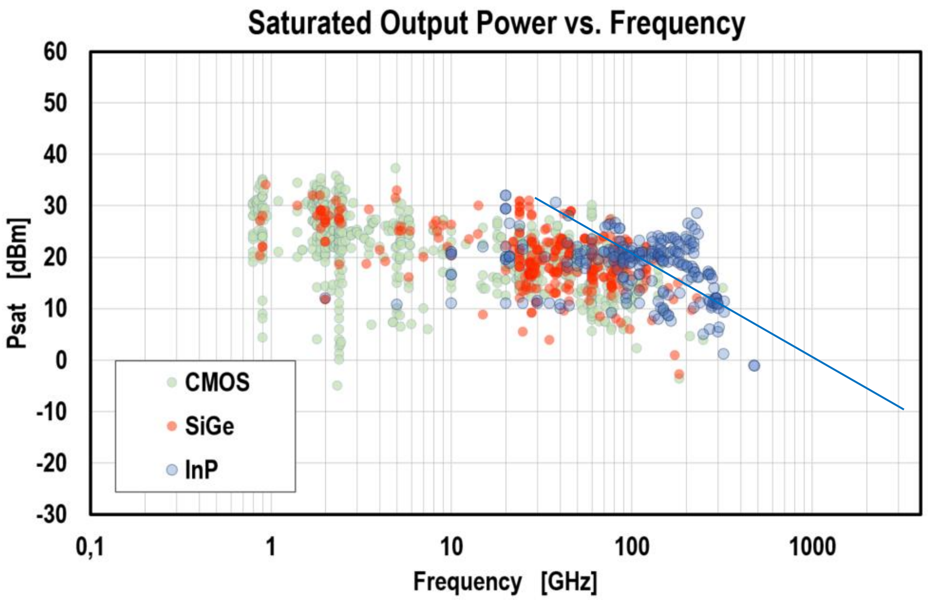
Lower manufacturability induces negative feedback cycle

It could be a status quo forever!



What about the future of InP technology ?

- InP has a higher Johnson limit
- InP yields higher PSAT above 100 GHz



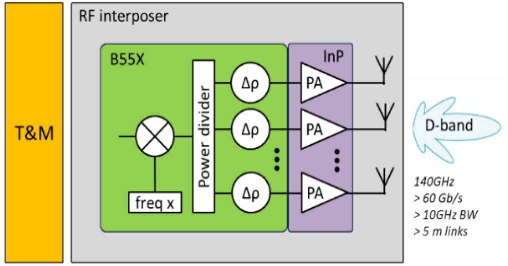
source: Georgia tech PA survey

InP has the best intrinsic potential for frequencies above 100 GHz

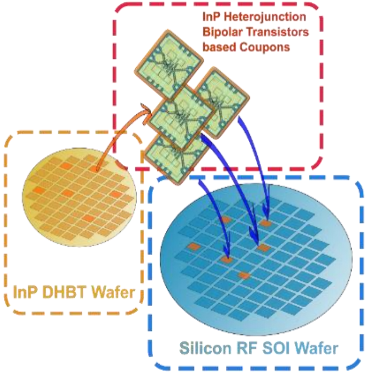
This could be the future of InP technology …

… these strategies may help to break the negative feedback circle

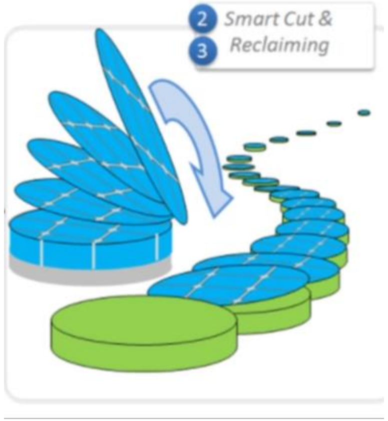
Co-packaging (SHIFT project)



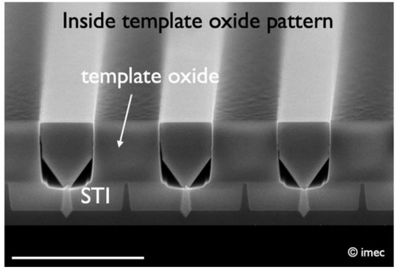
XFAB / IMEC µtransfer printing approach



SOITEC SMARTCUT™ approach



IMEC nano ridges approach



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Conclusion

Our vision:

- Continuous performance improvement while maintaining yield
- Improve reliability and provide accurate models & modern PDK
- Improve InP manufacturability & decrease cost to widen technology adoption (InPoSI, µTP)
- Strengthen the InP ecosystem
  - Provide InP technology access to external partners for R&D and pre-production
  - Provide a path to higher volume via external foundry / technology licensing