Remarks on RF and Breakdown Modeling of Integrated Diodes

AKB 2023, Corbeil-Essonnes, France

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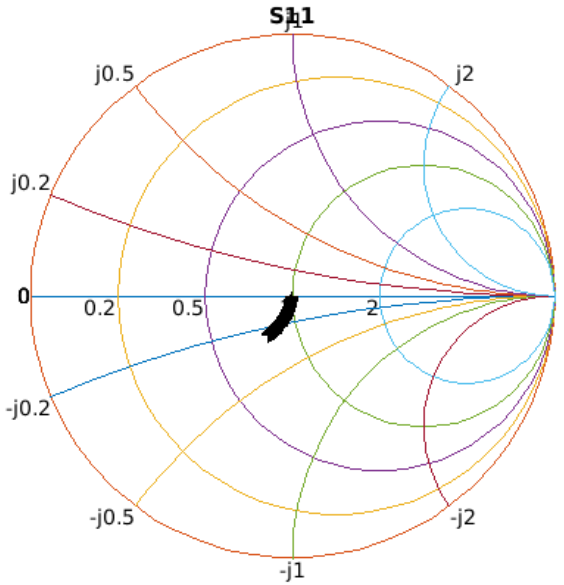
Agenda

1. Level-1 RF Extractions with 1 Internal Node.
2. Level-1 RF Extractions with 2 Internal Nodes.
3. Diode_CMC Shortcoming in RF Modeling.
4. Soft Breakdown Modeling Options.
5. Conclusions

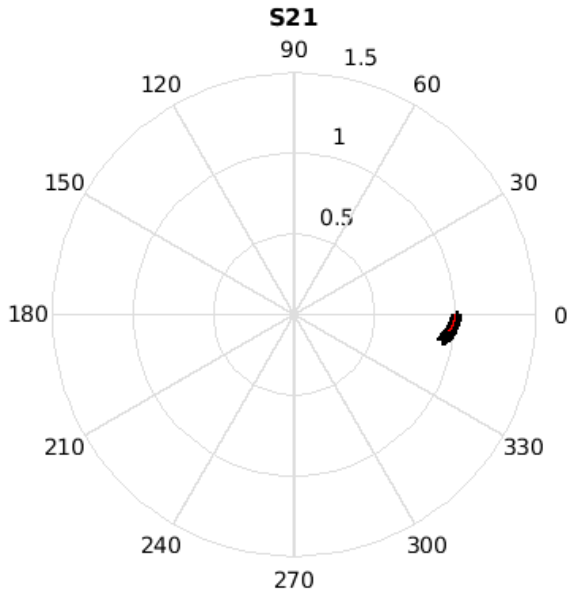
Diode RF Extractions: S-Parameter Setup

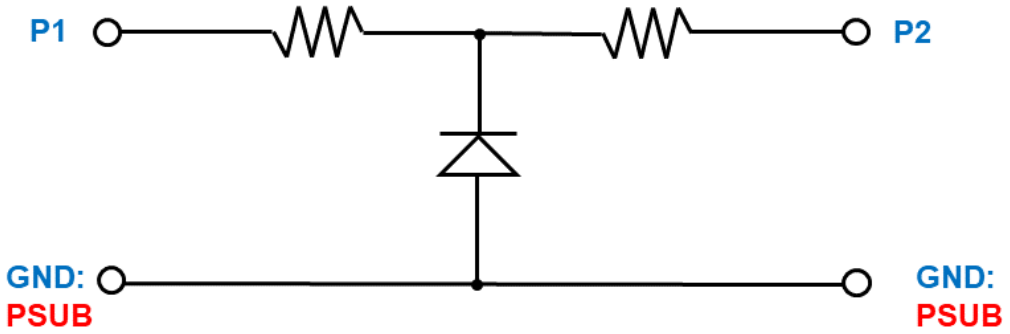
Diode RF Modeling

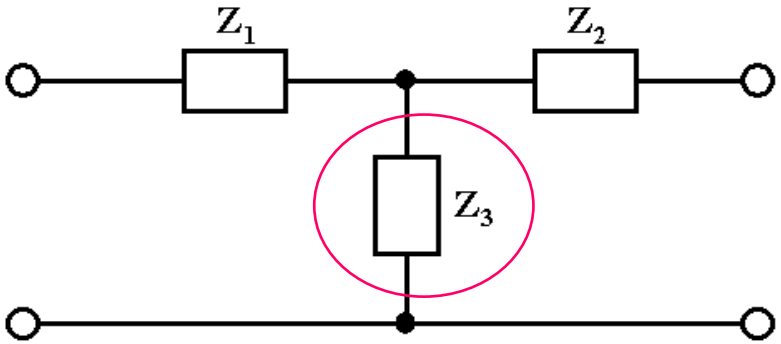
S_{11}



S_{21}

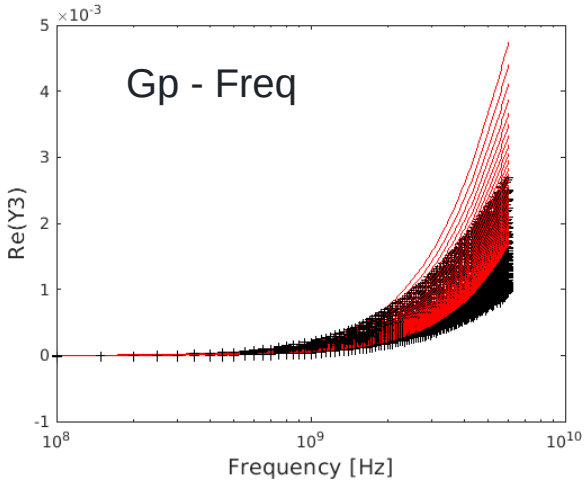




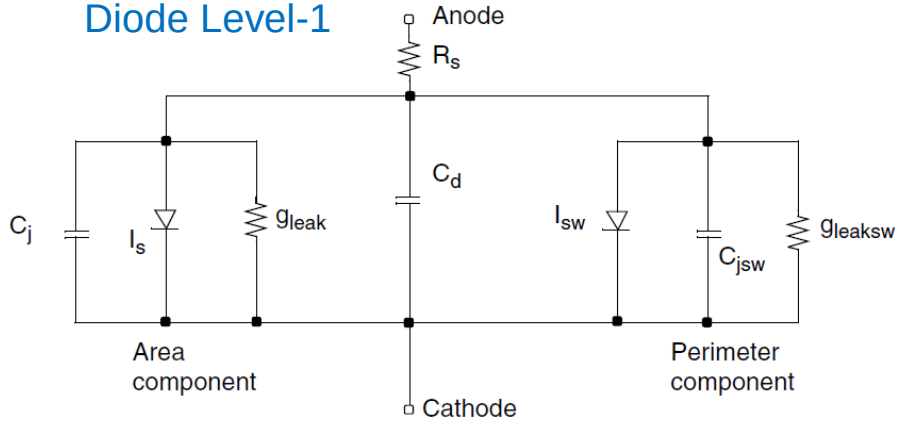


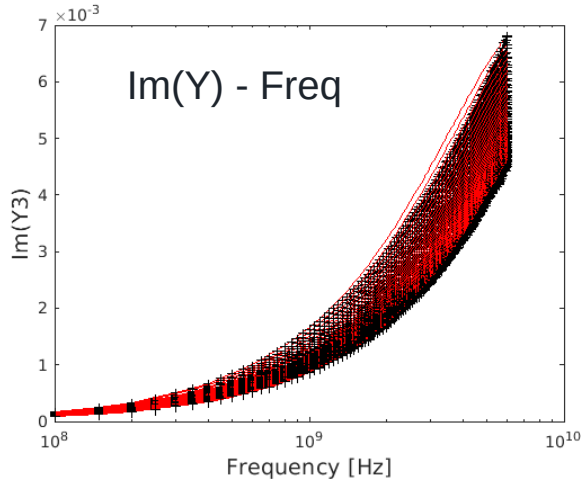
Diode RF Extractions: Cp-Gp from Admittance

Diode RF Modeling



Diode Level-1

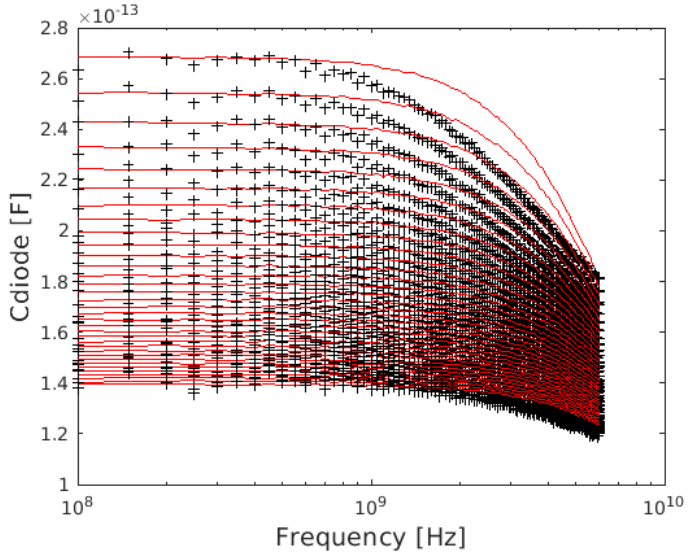




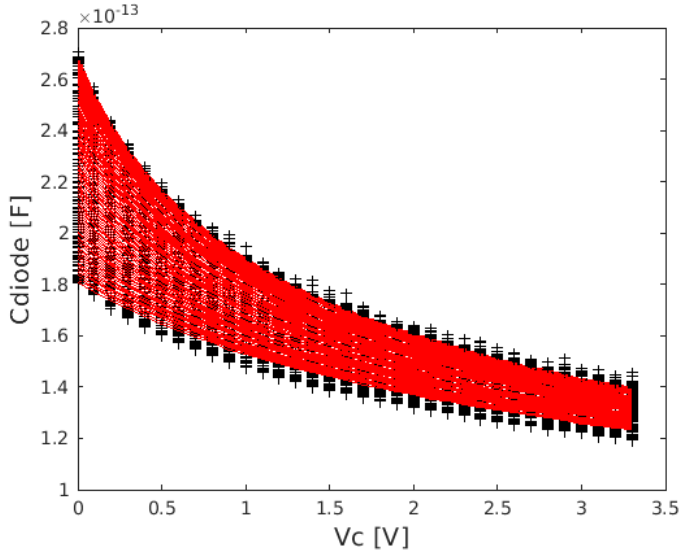
Adjusting Rs seems to be a good solution...

$$C_D = \frac{Im(Y)}{\omega}$$

C_D - Freq

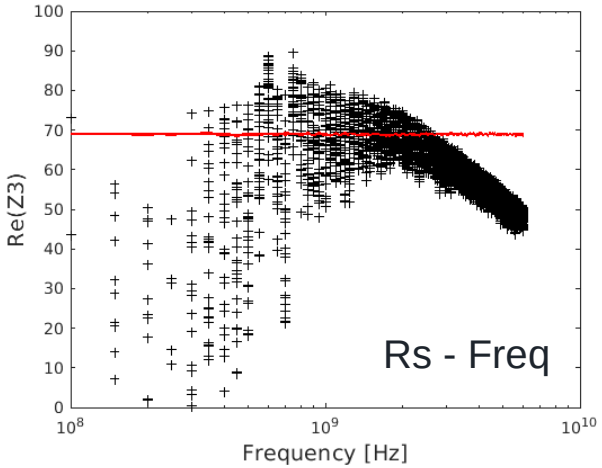


C_D - Vc

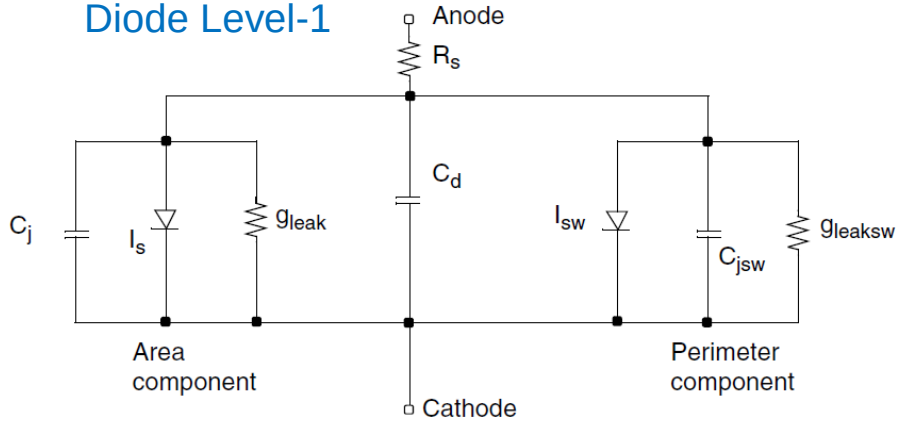


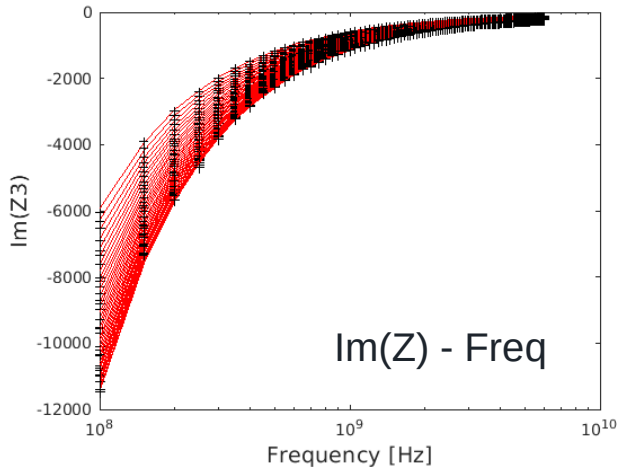
Diode RF Extractions: Cs-Rs from Impedance

Diode RF Modeling



Diode Level-1

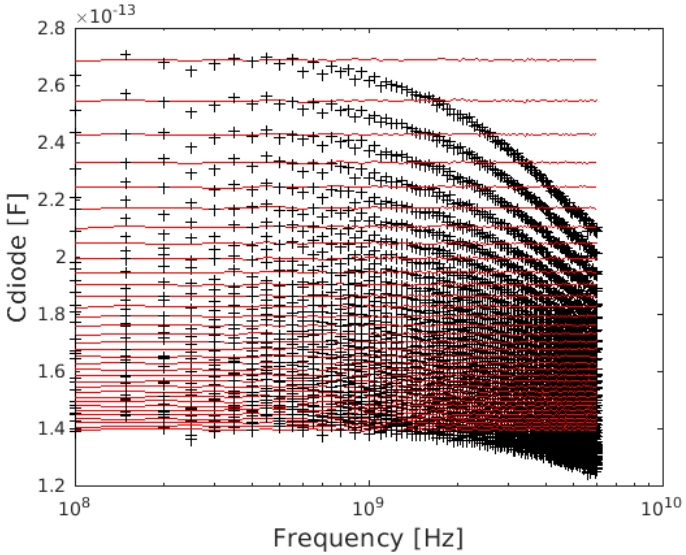




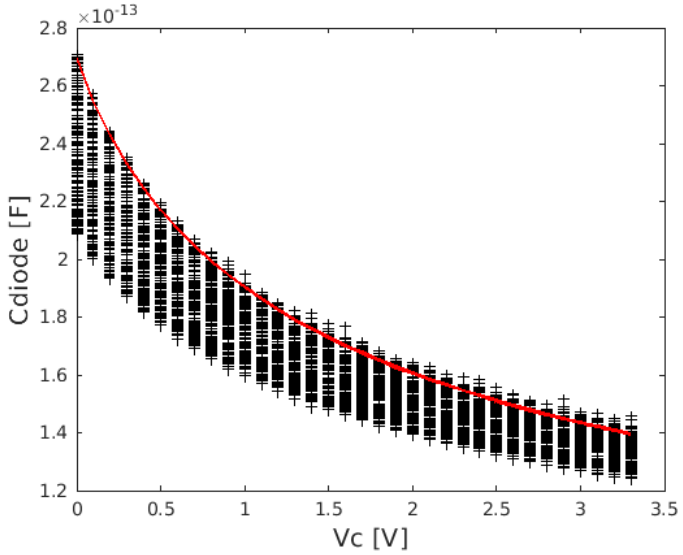
Not sufficient to reproduce the frequency dependence.

$$C_D = -\frac{1}{\omega \cdot Im(Z)}$$

C_D - Freq

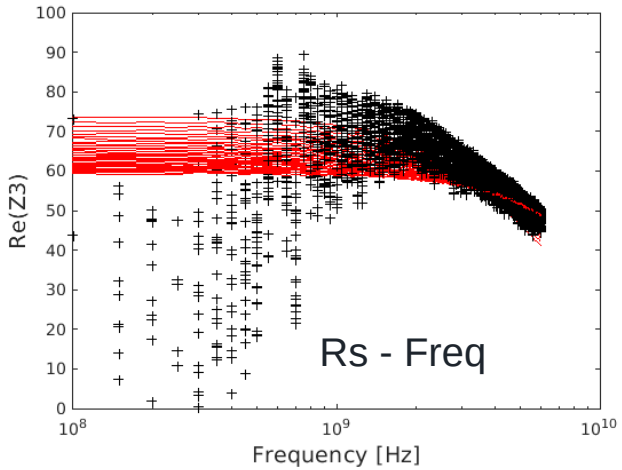


C_D - Vc

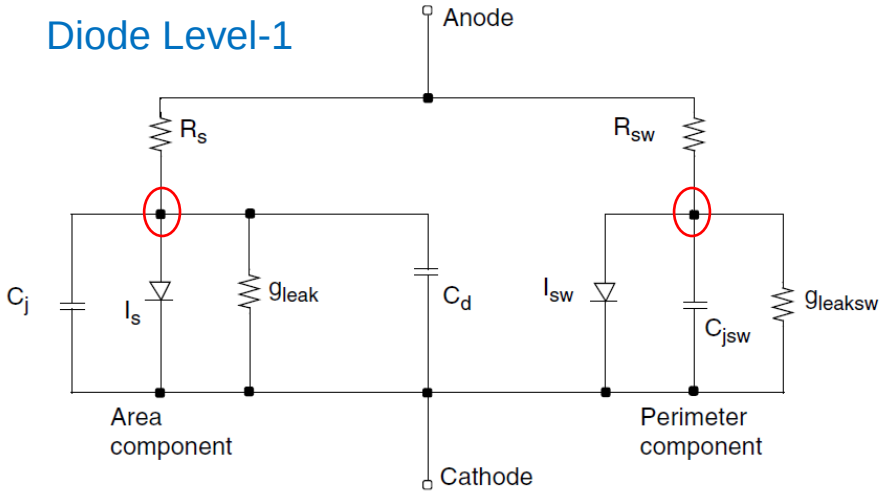


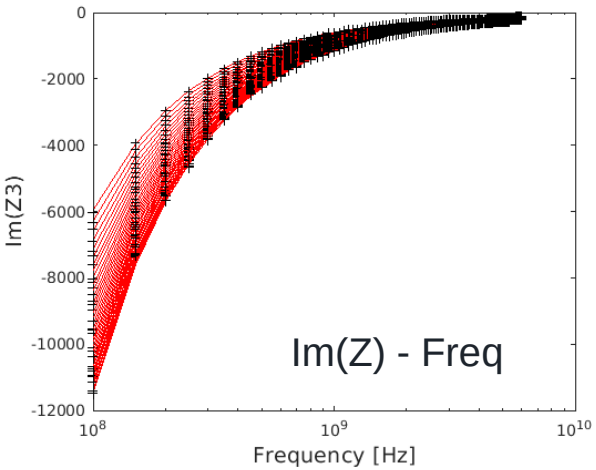
Diode RF Extractions: Cs-Rs from Impedance with 2 Internal Nodes

Diode RF Modeling

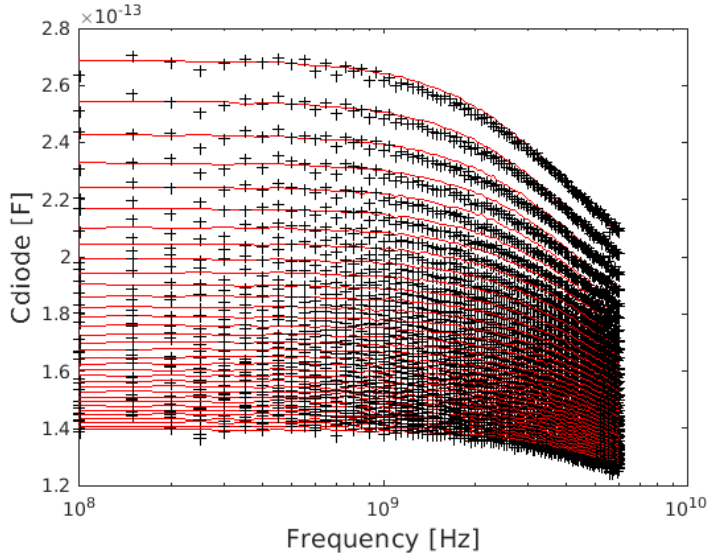


Diode Level-1

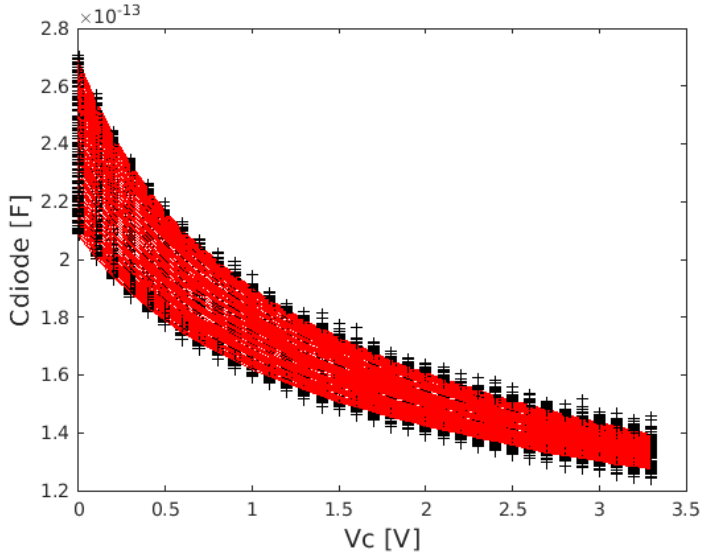




2 internal nodes are needed to produce this behavior!



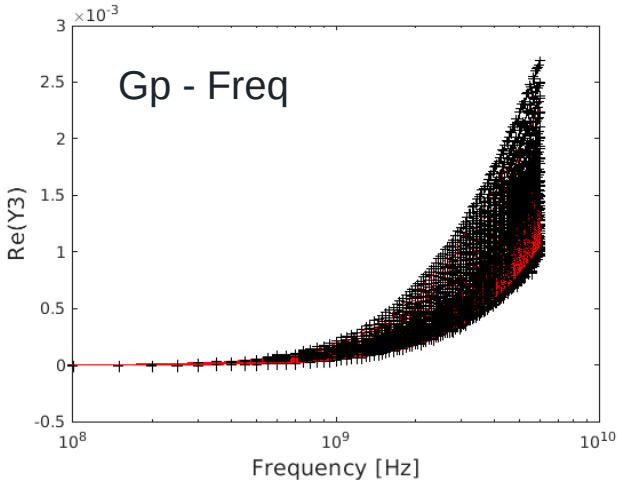
C_D - Freq



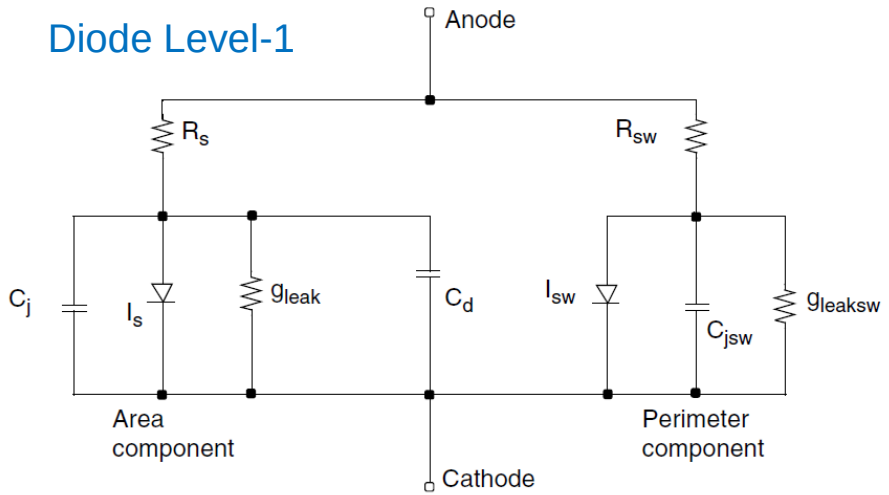
C_D - Vc

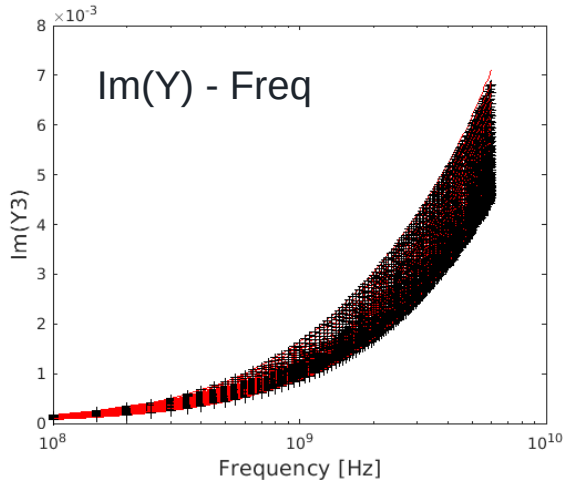
Diode RF Extractions: Cp-Gp from Admittance with 2 Internal Nodes

Diode RF Modeling



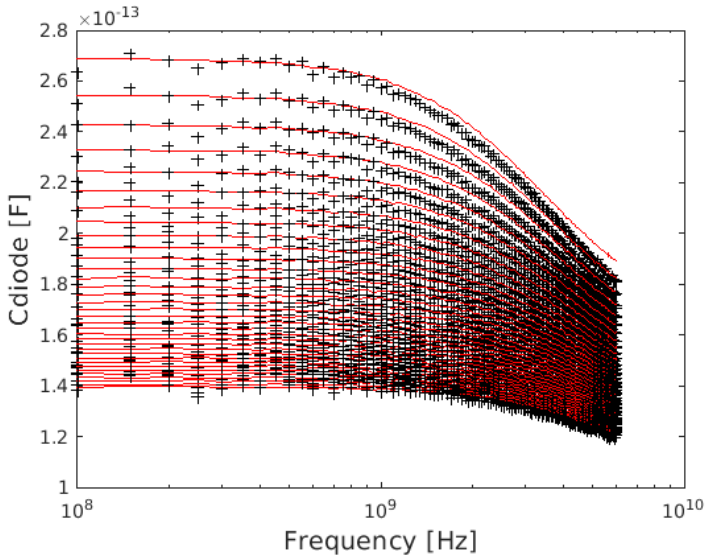
Diode Level-1



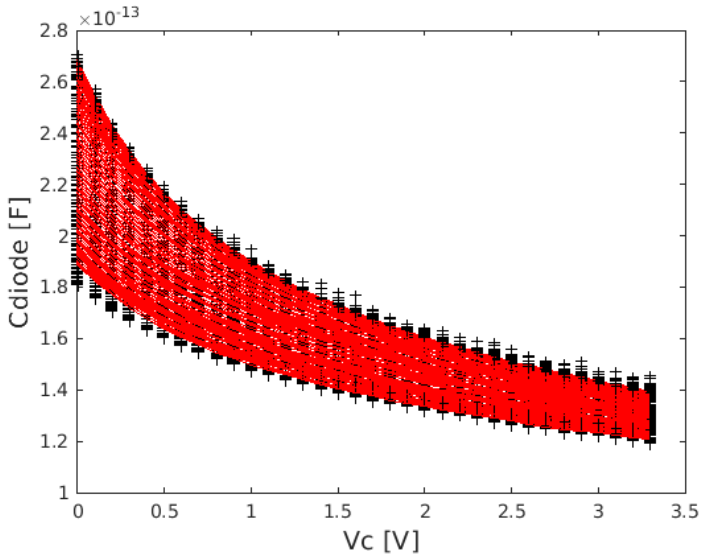


Can be produced by simple Rs – Cs equivalent circuit too.

$$G_p = \frac{\omega^2 C_s^2 R_s}{1 + (\omega C_s R_s)^2}$$



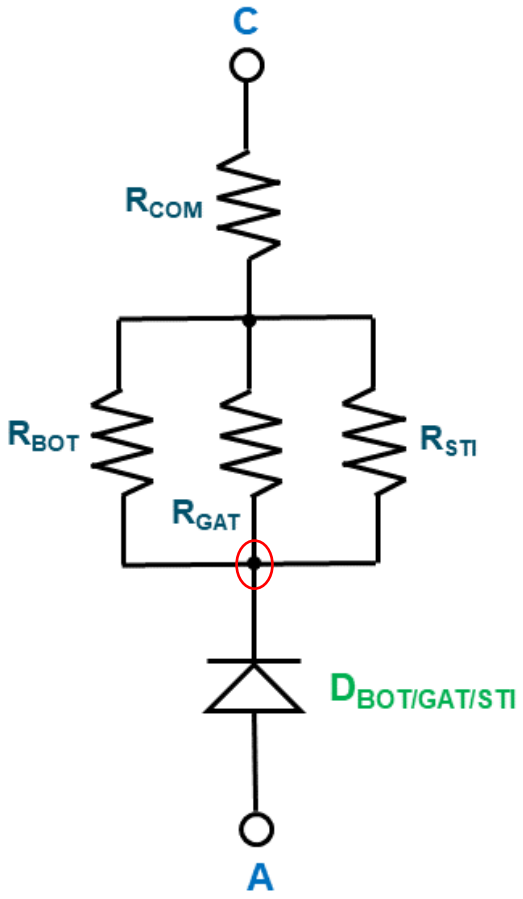
C_D - Freq



C_D - Vc

Diode_CMC Shortcoming

Diode RF Modeling

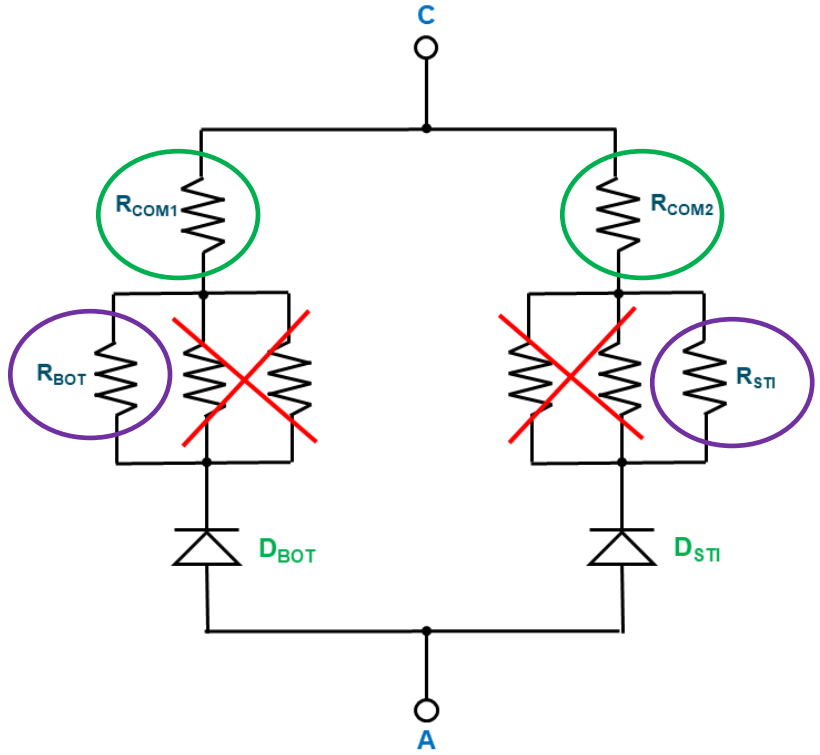


Resistance: one component with 4 possible scaling rules:
Area (RSBOT), Gate-edge (RSGAT), Perimeter (RSSTI) and fixed (RCOM)

$$RS_{nom} = \frac{1}{\frac{AB}{RSBOT} + \frac{LG}{RSGAT} + \frac{LS}{RSSTI}} + RCOM$$

Capacitance: fully compatible with Level-1

- Single branch implementation with one internal node.
- Not suggestiv of RF modeling.
- Subcircuit of 2 Diode_CMC diodes needed.

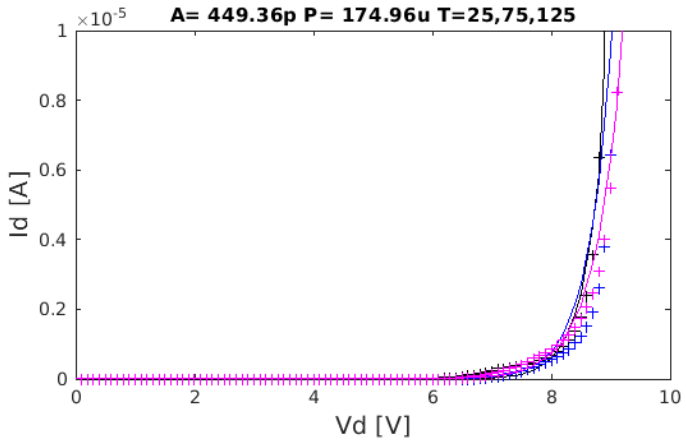


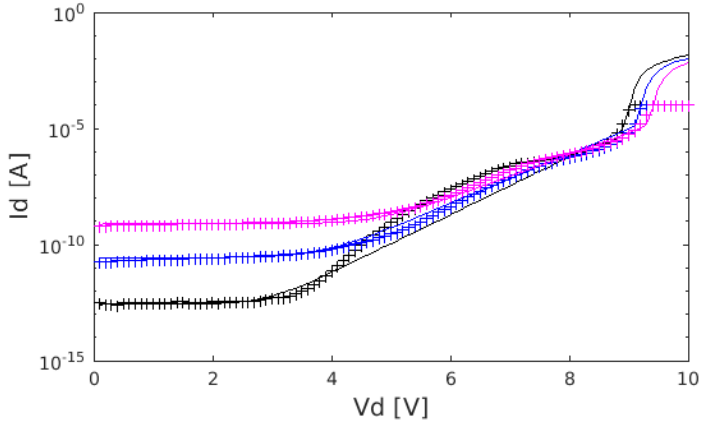
Unused components are to be eliminated:

1. Setting R_{COM1} & R_{COM2} (unscaled), R_{sbot}=R_{ssti}=R_{sgat}= 0
2. Setting R_{SBOT1} & AB_1 and R_{SSTI2} & LS_2 , R_{COM1}=R_{COM2}=0, R_{SBOT2}=R_{SSTI1}=R_{SGAT} = 1e9

Diode Soft Breakdown I

Diode Breakdown Modeling





T= 25, 75, 125 °C

Level1:

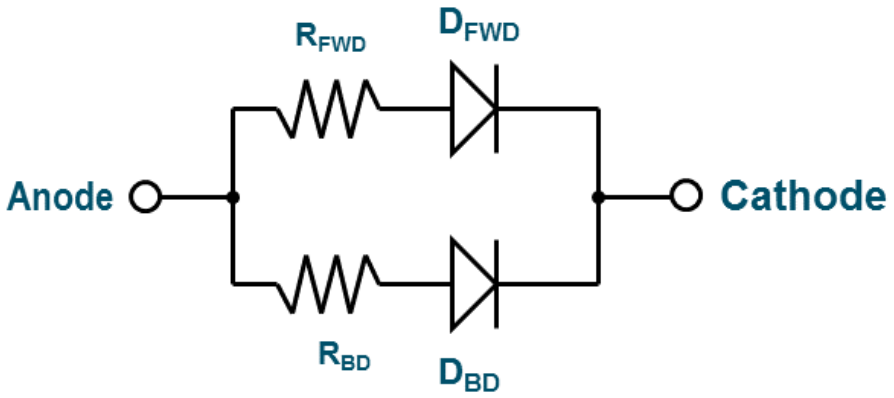
- Trap-assisted tunneling current used for modeling the soft breakdown region:
  - JTUN, JTUNSW (tunneling saturation currents)
  - NTUN (emission coeff., set to a large value e.g. ntun>10)
- Hard breakdown: BV, NZ=1
- Area/Perimeter components (JS, JSW, CJ0, CJSW etc) as usual.

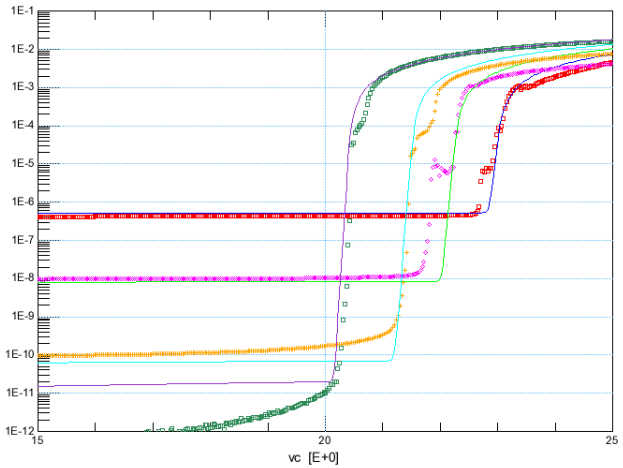
Diode Soft Breakdown II

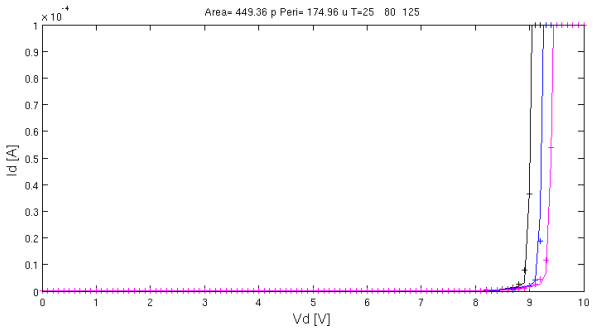
Diode Breakdown Modeling

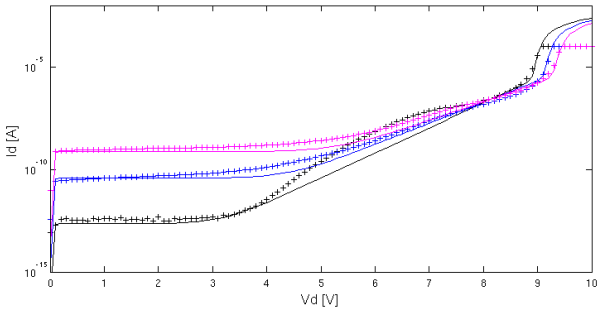
Diode Subcircuit:

- Composed of two Level1 diodes in parallel with series resistance.
- D_{FWD} : Forward and reverse DC including soft breakdown.
- D_{FWD} : Soft breakdown modeling using IBV, BV and NZ (slope).
- D_{BD} : Hard breakdown only, JS=JSW=CJ0=CJSW=0.
- D_{BD} : Resistance after BD can be adjusted with R_{BD} (fwd bias is not affected).









T=25, 80, 125 C

Conclusions

Diode RF & Breakdown Modeling

- Level-1: Cs-Rs extractions from impedance indicates best whether both internal nodes need to be activated.

- Diode_CMC: Should be extended to 2 internal nodes to make it more suitable for RF modeling.

- Two different approaches have been discussed with Level-1 for modeling complex BD behavior:
  - Utilizing the trap-assisted tunneling current.
  - Sharing the BD effect between two diodes. No advanced effects are needed. Resistance after BD.

Thank you