HICUM

- A Geometry Scalable Physics-Based Compact Bipolar Transistor model

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List of often used symbols and abbreviations

\( A_{E0}, L_{E0} \)  
emitter window area and perimeter

\( A_E, L_E \)  
effective (electrical) emitter area and perimeter

\( b_{E0}, l_{E0} \)  
emitter window width and length

\( b_E, l_E \)  
effective (electrical) emitter width and length (for definition see [24, 40])

\( \gamma_C \)  
ratio of periphery to area specific collector current; equal to emitter width increase due to periphery injection, e.g. \( b_E = b_{E0} + 2\gamma_C \)

\( I_T, i_T \)  
DC and time dependent transfer current of the vertical npn transistor structure

\( I_{CK} \)  
critical current (indicating onset of high-current effects)

\( \mu_n, \mu_p \)  
electron (hole) mobility

\( N_{Ci} \)  
(average) collector doping under emitter

\( N_{Cx} \)  
collector doping under external base

\( Q_p \)  
hole charge

\( \tau_f \)  
forward transit time

\( w_B, w_{B0} \)  
neutral/metallurgical base width

\( w_{Ci} \)  
(effective) collector width under emitter

\( w_{Cx} \)  
(effective) collector width under external base

\( w_i \)  
width of collector injection zone (for charge storage calculation in collector region)

GICCR  
Generalized Integral Charge-Control Relation [36]

TRADICA  
TRAnsistor DImensioning and CAIculation program [44]
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1 Introduction

1.1 Preliminary remarks

The purpose of the following remarks is to provide (i) a motivation behind the compact modeling approach pursued with HICUM, (ii) an overview on its targeted application area, and (iii) a list of requirements for a compact model from different point of views.

Bipolar technology has recently seen a tremendous growth, fuelled mostly by applications that require high speed and driving power on one hand and low noise and distortion on the other hand. Presently, major applications of bipolar technology are:

- Wireless communications in the 0.9 to 5.6 GHz range for, e.g. GSM, Bluetooth, DECT, in the 4-12 GHz range for, e.g. satellite TV, WLAN, and in the 20 to 60GHz range for short range communications, with the first application dominating.
- Fiber-optic communications in the 10 to 60 Gb/s range for, e.g. fast internet access and data transfer (LAN, WAN) as well as TV/HDTV (FTTC, FTTH); production and related design has started for systems up to 10Gb/s, seeing a significant push also for higher integration, such as cross-point switches in BiCMOS processes with emphasis on low-power high-speed bipolar circuits.
- “Linear analog” circuits for, e.g. disc drives, consumer electronics in general, power and automotive electronics. Many of these components require reliable and well-established processes with higher breakdown voltages rather than advanced high-speed bipolar processes.
- Fast data acquisition and conversion (ADCs) for, e.g., instrumentation and measurement equipment.
- Advanced automotive components at very high frequencies in the range of 24 to 100 GHz for, e.g. collision warning and avoidance. The respective circuits so far have been realized mostly with III-V processes, such as HBTs.

The above sequence is assumed to be roughly in the order of present importance from a business point of view; exact breakdowns are difficult to find, and the ranking can change quickly in areas of rapid growth. The first two applications are perceived to comprise the largest number of designs. As a consequence, compact bipolar transistor modeling should focus on these areas which, fortunately, include most of the critical issues of the other applications.

Compact modeling is also strongly connected to development and deployment of process technologies. A physics-based compact model together with the related parameter extraction and generation methodology can contribute significantly to improve the alignment of process development with product design requirements by enabling quick evaluations of the impact of process changes.
on device and circuit performance. Compact modeling basically provides a link between processing and design.

In general, bipolar processes span over quite a variation in device structure as well as device type. It is recommended to split compact bipolar models into at least two categories:

- vertical devices including high-speed npn and pnp transistors
- lateral devices, mostly pnp transistors.

HICUM is targeted towards the first category. It might be necessary though to divide the first category again into “low-power” ($BV_{CEO} < 10V$) and “high-power” ($BV_{CEO} > 10V$) transistors if the difference in device design and the electrical application range turns out to be too large for a single model. So far, HICUM has been verified to be accurate for transistors with $BV_{CEO}$ values up to about 15V, but there is no reason why the model should not work for higher voltages.

From the above, the following requirements for a compact model can be derived from an industrial point of view:

- high accuracy over a wide electrical (and temperature) range;
- laterally scalable parameter calculation, including variable contact configurations, in order to allow circuit optimization;
- numerical stability and fast execution time, although this is somewhat dependent on the application.
- physics-based formulation, allowing predictive and statistical modeling;
- reliable and well-defined extraction procedure should be available together with test structures; also, the use of standard equipment and set-ups are only important for, e.g., fast throughput.
- modular formulation of the model equations, minimizing interrelations between different electrical regions and facilitating simple implementation into circuit simulators.

Since the limitations of the standard SPICE Gummel-Poon model (SGPM), especially for designing high-speed circuits, have been well-known for many years (cf. examples in [42]), the advanced model HICUM has been developed to address the above mentioned requirements.
1.2 Model features overview

HICUM is a semi-physical compact bipolar transistor model. Semi-physical means that for arbitrary transistor configurations, defined by emitter size as well as number and location of base, emitter and collector fingers (or contacts, respectively), a complete set of model parameters can be calculated from a single set of technology specific electrical and technological data (cf. [44]). For this, the value of each element in the equivalent circuit is related to a function describing the dependence on so-called specific electrical data (such as sheet resistances and capacitances per unit area or length), technological data (such as width and doping of the collector region underneath the emitter), physical data (like mobilities), transistor dimensions (such as design rules), operating point, and temperature. The availability of such a semi-physical compact model is an important precondition for circuit optimization with respect to, e.g., maximum speed and low power consumption as well as for including process variations in the design.

The name HICUM was derived from *High-CUrent Model*, indicating that HICUM initially was developed with special emphasis on modelling the operating region at high current densities which is very important for certain high-speed applications. The first version was described in detail in [31,47,26,32,33] and was verified for digital applications based on a conventional technology. Later, formulas for the calculation of the base resistance were developed [27,34,35] which include three-dimensional effects occurring in short transistors with an emitter length approaching the emitter width. The latter sizes are important for low-power designs. The introduction of self-aligning poly-silicon technologies as well as the extension of the model to high-frequency analog operation led to improvements [29,14] w.r.t. the first version, which were also verified for very fast large-signal digital-type applications [39].

HICUM is based on an extended and Generalized Integral Charge-Control Relation (GICCR) [30,25,32,36]. However, in contrast to the (original) Gummel-Poon model (GPM) [1] as well as the SPICE-GPM (SGPM) [2] and its variants, in HICUM the (G)ICCR concept is applied consistently without inadequate simplifications and additional fitting parameters (such as the Early voltages). Since reliable design and optimization of high-speed circuits requires accurate modeling mainly of the dynamic transistor behavior, quantities like depletion capacitances and the transit time of mobile carriers as well as the associated charges, which determine the dynamic behaviour, are considered as basic quantities of the model. An accurate approximation of these basic quantities as a function of bias yields, thus, not only an accurate description of the small-signal and dynamic large-
signal behaviour but also via the (G)ICCR [36] - of the d.c. behaviour. This coupling between static and dynamic description leads, moreover, to a reduction of "artificial" model parameters like Early voltages and knee currents. Furthermore, the above mentioned basic quantities can be easily and accurately determined by standard small-signal measurement methods.

The modularity and physics-based approach of HICUM allows the construction of a model hierarchy without additional effort in parameter extraction. Based on HICUM Level2 (HICUM/L2) and its corresponding set of specific electrical parameters, the simplified version HICUM Level0 (HICUM/L0) with the same equivalent circuit as the SGPM as well as an electrically and thermally distributed model, HICUM Level4 [60], can be generated. In contrast to the SGPM though, HICUM/L0 eliminates many problems while maintaining similar overall simplicity. The HICUM/Level0 model is presently being implemented in commercial simulators.

The important physical and electrical effects taken into account by HICUM/L2, which is described in Chapter 2.1, are briefly summarized below:

- high-current effects (incl. quasi-saturation)
- distributed high-frequency model for the external base-collector region
- emitter periphery injection and associated charge storage
- emitter current crowding (through a bias dependent internal base resistance)
- two- and three-dimensional collector current spreading
- parasitic (bias independent) capacitances between base-emitter and base-collector terminal
- vertical non-quasi-static (NQS) effects for transfer current and minority charge
- temperature dependence and self-heating
- weak avalanche breakdown at the base-collector junction
- tunneling in the base-emitter junction
- parasitic substrate transistor
- bandgap differences (occurring in HBTs)
- lateral (geometry) scalability

Modelling of these effects is reflected not only in the model equations but also in the topology of the equivalent circuit. Although the above listed effects are taken into account, the standard HICUM/L2 equivalent circuit still corresponds to a one-transistor model (see Fig. 2.1.1/1), which has turned out as sufficiently accurate for the vast majority of circuit applications. HICUM/L2 contains elements for describing the internal transistor (index $i$), the emitter periphery (index $p$) and the external transistor regions (index $x$). The internal transistor is defined by the region under the emitter which is assigned an effective emitter width [24,40] and area, respectively, in order to retain a one-
transistor model with an as simple as possible equivalent circuit topology as well as a sound physical background. In contrast to MOS transistor models, the geometry dependent calculations have been implemented in a separate program (TRADICA, cf. [44]) for various reasons (e.g. [63]).

Due to its semi-physical nature HICUM/L2 possesses geometry scaling capabilities up to high current densities [40]. In order to make use of these scaling capabilities specific parameters have to be determined from measurements, for which instructions have been developed (e.g., [23,26,28,15,16]). Parameter extraction as well as generation of model parameters for different transistor configurations will be addressed in Chapter 4. Notes on operating point information that need to be available in (commercial) circuit simulators are provided in Chapter 5.

As the experimental results in chapter 6 show, the accuracy and applicability of HICUM has been demonstrated for a variety of different technologies, ranging from a low-speed and relatively high-voltage process to present SiGe production processes, as well as for many different operating modes.

This documentation includes the contents of change notes up to the version specified on the title page. The differences of new model releases will be documented first separately in order to simplify code updates, and will then be incorporated into this documentation.
Acknowledgments

Many individuals have contributed to the development of HICUM through various activities such as valuable feedback and model testing. It is impossible to list everybody who in some way participated in the model related development, but I feel that it is appropriate and important to name at least the most important contributors.

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2 Model equations

In the following text all equations that are actually used in the implemented model code are marked by a frame. The physical background of the equations is briefly discussed and references for more detailed explanations are provided. The model equations are discussed on the basis of a vertical npn transistor. A vertical pnp transistor requires for most processes the addition of a parasitic n-well transistor (e.g. in a subcircuit).

The presently available version of HICUM (named HICUM/Level2) includes many physical effects that are relevant for today’s silicon-based processes (incl. SiGe technologies). As a consequence, its equivalent circuit is fairly complicated and not well-suited for rough analytical calculations often performed by circuit designers in the preliminary design phase. Therefore, a strongly simplified version of the model, called HICUM/Level0, is being offered. The combination of these different levels of complexity during circuit design is expected to also save computational effort and time.
2.1 HICUM/Level2

2.1.1 Equivalent circuit

Compared to the SGPM the equivalent circuit (EC) of HICUM/Level2 contains two additional circuit nodes, namely B* and S' in Fig. 2.1.1/1. The node B*, which separates the operating point dependent internal base resistance from the operating point independent external component, is required to take into account emitter periphery effects, which can play a significant role in modern transistors. This node is also employed for an improved modelling of the distributed nature of the external base-collector (BC) region by splitting the external BC capacitance $C_{BCx}$ over $r_{Bx}$ in the form of a $\pi$-type equivalent circuit for the corresponding $RC$ transmission line(s). As a further advantage of introducing the node B*, high-frequency small-signal emitter current crowding can be correctly taken into account by the capacitance $C_{rBi}$. An emitter-base isolation capacitance $C_{BEpar}$, that becomes significant for advanced technologies with thin spacer or link regions, as well as a BC oxide capacitance $C_{BCpar}$, which is included in the $C_{BCx}$ element, are taken into account.

In contrast to other models, the influence of the internal collector series resistance is (partially) taken into account by the model equations for the transfer current $i_T$ and the minority charge which is represented by the elements $C_{dE}$ and $C_{dC}$ in Fig. 2.1.1/1. As a consequence, the collector terminal $C'$ of the internal transistor is (physically) located at the end of the epitaxial (or n-well) collector region. This approach not only avoids additional complicated and computationally expensive model equations for an "internal collector resistance" but also saves one node. The chosen approach has been demonstrated to be accurate for a wide range of existing bipolar technologies (cf. chapter 6).

The reliable design of high-speed circuits often requires the consideration of the coupling between the buried layer and the substrate terminal S. Since the substrate material consists of both a resistive and capacitive component, as a first (rough) approach a substrate network with a resistance $r_{Su}$ and a capacitance $C_{Su}$ is introduced, leading to the “internal” substrate node S*.

A possibly existing substrate transistor has been taken into account by using a simple transport model. Like in the SGPM, this can also be realized by a subcircuit (cf. Section 2.1.12) and setting $r_{Su}$ and $C_{jS}$ to zero in the HICUM equivalent circuit. In advanced bipolar processes, the emitter terminal of the substrate transistor (B*) moves towards the (npn) base contact (B) which makes the external realization of such a parasitic transistor by a subcircuit even easier. The substrate transistor
- if it is not avoided by proper layout measures - only might turn on for operation at very low CE
voltages (”very” hard saturation).

The physical meaning and modelling of all EC elements in Fig. 2.1.1/1 is discussed below in
more detail.

The description in the following text is given for an npn transistor, which is the most widely used
type of bipolar transistors. For vertical pnp transistors, the model can be applied by interchanging
the signs of terminal voltages and currents. Lateral pnp transistors can be described by a composi-
tion of HICUM/L2 models but usually a subcircuit consisting of three simple transport models (e.g.
HICUM/L0) is considered to be more appropriate.

---

Fig. 2.1.1/1: (a) Large-signal HICUM/Level2 equivalent circuit. The external BC capacitance
consists of a depletion and a bias independent (e.g., oxide) capacitance with the ratio
\( C_{BCx}' / C_{BCx}'' \) being adjusted with respect to proper modelling of the h.f. behavior.
(b) Thermal network used for self-heating calculation.
2.1.2 Quasi-static transfer current

The transfer current of a vertical homo- and hetero-junction bipolar transistor can be described by a generalized form of the ICCR that can also be extended to 2D and 3D transistor structures with narrow emitter stripes or very small contact windows. The various steps to arrive at the final equation for the transfer current \( i_T \) are outlined below, demonstrating the modular structure of the model equations. For a detailed derivation of the GICCR the reader is referred to the Appendix.

A. Basic formulation

The result of the one-dimensional (1D) GICCR is

\[
i_T = \frac{c_{10}}{Q_{p,T}} \left[ \exp \left( \frac{V_{BE}'}{V_T} \right) - \exp \left( \frac{V_{BC}'}{V_T} \right) \right]
\]

with the constant

\[
c_{10} = (qA_E^2)V_T \mu_{nB} \frac{h_{iB}}{\bar{v}_{iB}}^2 .
\]

As discussed in the Appendix, \( V_{BE}' \) and \( V_{BC}' \) are the (time dependent) terminal voltages of the 1D transistor if the integration leading to the modified hole charge, \( Q_{p,T} \), is performed throughout the total 1D transistor, i.e. between its emitter and collector contact. The term \( \mu_{nB} \frac{h_{iB}}{\bar{v}_{iB}}^2 \) is an average value for the base region.

\( Q_{p,T} \) consists of a weighted sum of charges,

\[
Q_{p,T} = Q_{p0} + h_{jEi}Q_{jEi} + h_{jCi}Q_{jCi} + Q_{f,T} + Q_{r,T} ,
\]

The charge formulations designated with the index “\( T \)” result when the transfer current is derived from the transport equation and hetero-junctions as well as current spreading are included. The hole charge at thermal equilibrium, \( Q_{p0} \), is a model parameter. \( Q_{jEi} \) and \( Q_{jCi} \) are the depletion charges stored within the BE and BC junction. \( Q_{f,T} \) and \( Q_{r,T} \) are (weighted) forward and reverse minority charges stored in the total (1D) transistor [36]. The various components in the minority charges and the weighting factors will be discussed in more detail later.
The correspondence to the conventional model formulation can be maintained by realizing that the usual collector saturation current is simply given by

\[ I_S = \frac{c_{10}}{Q_{p0}}, \]  

so that (2.1.2-1) can also be written in normalized form:

\[ i_T = \frac{I_S}{Q_{p,T}/Q_{p0}} \left[ \exp\left(\frac{V_{BE}^\prime}{V_T}\right) - \exp\left(\frac{V_{BC}^\prime}{V_T}\right) \right]. \]  

Mathematically, \( i_T \) in (2.1.2-1) can be split into a "forward" component,

\[ i_{Tf} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{V_{BE}^\prime}{V_T}\right), \]  

and a "reverse" (better to say inverse) component,

\[ i_{Tr} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{V_{BC}^\prime}{V_T}\right), \]  

which will be referred to in the discussion below. Physically, \( i_{Tf} \) represents the electron current flowing from emitter to collector at forward operation at \( \exp(V_{CE}^\prime/V_T) >> 1 \). Analogously, \( i_{Tr} \) represents the electron current flowing from collector to emitter at inverse operation with \( \exp(-V_{CE}^\prime/V_T) >> 1 \). This separation of \( i_T \) simplifies both the implementation of the solution of the non-linear transfer current formulation as well as the modelling of the minority charge components.

B. Extension to the 2D (3D) case and influence of internal base resistance

The 1D transistor structure can be transformed into a 2D or 3D structure by multiplying all area specific 1D model parameters with the emitter area of the transistor. This defines the internal transistor, i.e. the structure under the emitter window. As a result, the lateral voltage drop caused by the base current has to be taken into account for calculating \( v_{BE}^\prime \) and \( v_{BC}^\prime \) in (2.1.2-1). This requires an appropriate definition and model for the internal base resistance by which then \( v_{BE}^\prime \) and \( v_{BC}^\prime \)
are becoming "averaged" terminal voltages to ensure a correct description of the electrical (terminal) characteristics of the internal transistor.

C. Emitter periphery injection

The carrier injection at the emitter periphery junction and the corresponding transfer current component through the external base can be taken into account by defining an effective electrical emitter width $b_E$ and length $l_E$ [24, 26, 40], which are usually larger than the emitter window dimensions. This results in an effective size for the internal transistor in the 2D and 3D case with the effective emitter area $A_E$. By multiplication of all area specific 1D model parameters with $A_E$ (rather than $A_{E0}$) it was shown in [40], that (2.1.2-1) can then be directly applied without any loss of accuracy at low current densities. At high current densities, however, this approach can become less accurate, and another extension is usually required which will be discussed later. $v_{B'E'}$ and $v_{B'C'}$ are now the terminal voltages of the effective internal transistor (cf. Fig. 2.1.1/1), and the components $Q_{jEi}$ and $Q_{jCi}$ in the charge $Q_{p,T}$ are now defined for the effective internal transistor.

Besides the lateral scalability of the model, the major advantages of this approach are that (i) a single equation can be used throughout the total operating region and (ii) a single transfer current source element can be used in the EC (Fig. 2.1.1/1) to describe even transistors with strong 2D and 3D effects.

D. Heterojunction bipolar transistors (HBTs)

The generalized ICCR [36] results in the following expression for the weighted minority charge

$$Q_{f,T} = Q_{f0} + h_{fE} \Delta Q_{Ef} + h_{fB} \Delta Q_{Bf} + h_{fC} \Delta Q_{Cf}$$

(2.1.2-8)

with $Q_{f0}$ as low-current charge component, and $\Delta Q_{Ef}$, $\Delta Q_{Bf}$, $\Delta Q_{Cf}$ as the actual minority charges in the neutral emitter, base, collector. $\Delta Q_{Cf}$ can include bias dependent lateral current spreading (see later). The weighing factors $h_{fE}$ and $h_{fC}$ as well as $h_{fEi}$ and $h_{fCi}$ in (2.1.2-3) are given by the differences and grading of the bandgap between the various transistor regions in a HBT. Note, that $Q_{f,T}$ is generally not equal to the stored minority charge $Q_f$ used during dynamic operation. The charge components of $Q_{f,T}$ are discussed in ch. 2.1.3.
Assuming a linear bandgap change in the base with the grading coefficient \(a_G\), the model parameter \(h_{jci}\) can be expressed analytically as \([49]\)

\[
h_{jCi} \approx \exp\left(\frac{a_G w_{B0}}{V_T}\right)
\]

(2.1.2-9)

with \(w_{B0}\) as the neutral base width in equilibrium. The corresponding factor for the BE charge, \(h_{jEi}\), is close to 1 for Si-based processes, but is usually larger than 1 for (SiGe) HBTs.

The weighting factors \([36]\)

\[
h_{jE} = \frac{\mu_{nB} n_{iB}^2}{\mu_{nE} n_{iE}^2} \quad \text{and} \quad h_{jC} = \frac{\mu_{nB} n_{iB}^2}{\mu_{nC} n_{iC}^2}
\]

(2.1.2-10)

are model parameters that take into account the different values for effective intrinsic carrier concentration \(n_i\) and mobility \(\mu_n\) of the neutral transistor regions. The factors \(h_{jCi}\), \(h_{jE}\), and \(h_{jC}\) are considered to be model parameters in order to make the model applicable also in cases where the doping concentrations and other physical values are unknown.

For SiGe heterojunction transistors, \(h_{jC}\) can be significantly larger than 1 while \(h_{jCi}\) is less than 1, explaining the larger Early voltages measured in those transistors. In contrast, for most homojunction transistors these parameters assume values close to 1 although they are becoming more relevant, too, in advanced homojunction transistors due to high-doping effects.

For HBTs, such as those fabricated in III-V semiconductors, that contain a significant energy difference in the conduction band, transport effects such as thermionic emission and tunneling may have to be accounted for. There are various ways of doing this which differ in complexity and, therefore, convergence rate and simulation time. For the present model, the most simple approach has been adopted by introducing a non-ideality coefficient \(m_{Cf}\) in the forward component of the transfer current:

\[
i_{TF} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{V_{BE}}{m_{Cf} V_T}\right).
\]

(2.1.2-11)
This approach is believed to offer sufficient flexibility for practical purposes, while keeping down additional computational burden.

E. High current densities

Earlier investigations of a variety of doping profiles have shown that (2.1.2-1) becomes less accurate at high collector current densities due to current spreading in the (epitaxial) collector [32,26]. This 2D/3D effect can also be taken into account as a physics-based expression by using the GIC-CR and by applying the same methodology as described in [40].

The previously described version of HICUM [32] contains a simplified modelling of this effect by replacing the constant $c_{10}$ with the empirical function $c_1 = c_{10}(1 + i_T/I_{Ch})$ in which $I_{Ch}$ is a model parameter that is (roughly) proportional to the emitter area. In the presently implemented version, the simplified description is still maintained, but a numerically more stable expression is being used:

$$c_1 = c_{10}(1 + \frac{i_T}{I_{Ch}})$$

(2.1.2-12)

with the 1D forward transfer current:

$$i_{Tf1} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{V_{BE'}}{m_{Cf}V_T'}\right) = I_s \frac{Q_{p0}}{Q_{p,T}} \exp\left(\frac{V_{BE'}}{m_{Cf}V_T'}\right)$$

(2.1.2-13)

For $Q_{r,T}$ the actual charge $Q_r$ is being used.

F. Final transfer current model formulation

The "forward" component defined in (2.1.2-6) is repeated here with the modifications in (2.1.2-11) and (2.1.2-12):

$$i_{Tf} = \frac{c_1}{Q_{p,T}} \exp\left(\frac{V_{BE'}}{m_{Cf}V_T'}\right)$$

(2.1.2-14)

The "reverse" (better to say inverse) component remains identical to (2.1.2-7); in the latter, the influence of collector current spreading at forward operation is not included, i.e. $c_f = c_{10}$. (2.1.2-14) can be re-arranged to give an explicit expression for the forward transfer current,
The total transfer current is then
\[ i_T = i_{Tf} - i_{Tr}. \]  

(2.1.2-16)

At high reverse bias across either junction, the respective space-charge region can extend throughout the whole base region (base punch-through or reach-through effect). As a result, \( Q_{p,T} \) would become zero or even less than zero which would cause numerical problems. This situation is most likely to occur at low current densities, where the (always positive) minority charge is negligible. Therefore, in HICUM the hole charge at low current densities,

\[ Q_{p,T,low} = 0.05Q_{p0}, \]

is limited to a positive value \( Q_{B,rt} = 0.05Q_{p0} \), using a smoothing function, and is replaced by

\[ Q_{p,T,low} = Q_{B,rt}\left(1 + \frac{x + \sqrt{x^2 + a}}{2}\right) \]

\[ \text{with } x = \frac{Q_{p,T,j}}{Q_{B,rt}} - 1 \]

(2.1.2-18)

and \( a=1.921812 \) which reproduces the values of the former exponential smoothing function. Compared to version 2.1, only the exponential smoothing function in \( Q_{p,T,low} \) has now been replaced by a hyperbolic smoothing function. Also, the previous conditional statement, which turned on the evaluation of the smoothing function for \( Q_{p,T,j} < 0.6Q_{p0} \) has been removed to avoid slight inconsistencies in the calculated values and, especially, the associated derivatives. For the usual operating range with \( Q_{p,T,j}/Q_{p0} > 1 \), the difference \( Q_{p,T,low}-Q_{p,j} \) is much smaller than \( 10^{-6}Q_{p0} \), so the smoothing and the associated computational effort could be skipped in the code.

Also note that the effect of base reach-through is extremely unlikely, so that any additional (numerical) effort to take into account the physical mechanisms occurring under these circumstances does not seem to be justified for a compact model.

In general, the GICCR is a non-linear implicit equation for either \( i_T \) or \( Q_{p,T} \), respectively. Since \( Q_{p,T} \) is the common variable in both current components \( i_{Tf} \) and \( i_{Tr} \), the GICCR is solved in HICUM.
for $Q_{p,T}$ by employing Newton-Raphson iteration*. However, as long as $Q_{f,T}$ and $Q_r$ are linearly varying functions of the respective current, i.e. the transit times are current independent, the GIC-CR reduces to a quadratic equation, with an explicit solution for $Q_{p,T}$ (assuming $c_1 = c_{10}$ at low current densities)

$$Q_{p,T} = \frac{Q_{p,T,low}^2}{2} + \sqrt{\left(\frac{Q_{p,T,low}^2}{2}\right)^2 + \tau_0 c_{10} \exp\left(\frac{V_{BE}}{m_{cf} V_T}\right) + \tau_r c_{10} \exp\left(\frac{V_{B'C}}{V_T}\right)}$$  \hspace{1cm} (2.1.2-19)

with $Q_{p,low}$ from (2.1.2-18). Inserting the above solution into $i_{Tf}$ and $i_{Tr}$ and adding the minority charge terms provide quite a useful initial guess for the Newton iteration at higher current densities:

$$Q_{p,T,initial} = Q_{p,T,low} + \tau_0 i_{Tf} + \tau_r i_{Tr} .$$  \hspace{1cm} (2.1.2-20)

For the practical implementation of the GICCR the reader is referred to the model code.

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*In the SGPM, the solution is obtained by significant simplifications of the minority charge terms, leading to an (explicit) quadratic equation. Such an approach is physically consistent and accurate only at low current densities.
2.1.3 Minority charge, transit times, and diffusion capacitances

The minority charge is divided into a "forward" and a "reverse" (or inverse) component. The forward component, $Q_f$, is considered to be dependent on the forward transfer current, $i_{Tf}$, while the reverse component, $Q_r$, is considered to be dependent on the reverse transfer current, $i_{Tr}$. The large-signal charge components can be determined by integrating the respective small-signal transit times, defined as

$$\tau = \frac{dQ}{dl}$$  \hspace{1cm} (2.1.3-1)

rather than $\tau = Q/I$.

2.1.3.1 Minority charge component controlled by the forward transfer current

The operating point dependent minority charge stored in a forward biased (vertical) transistor can be determined from the transit time $\tau_f$ by simple integration (cf. Fig. 2.1.3/1),

$$Q_f = \int_{I_f^0}^{i_{Tf}} \tau_f di$$  \hspace{1cm} (2.1.3-2)

Fig. 2.1.3/1: Illustration of the forward minority charge and transit time as a function of current and definition of the bias regions.
τ_f can be extracted from the measured transit frequency vs. d.c. collector current \( I_C (=I_T) \) at forward operation for different voltages \( v_{CE} \) or \( v_{BC} \) as a parameter (cf. [23] and chapter 4). The current and voltage dependent transit time is modelled in HICUM by two components,

\[
\tau_f(v_{CE}, i_T) = \tau_{0f}(v_{BC}) + \Delta \tau_f(v_{CE}, i_T),
\]

(2.1.3-3)

where \( \tau_{0f} \) is the low-current transit time, and \( \Delta \tau_f \) represents the increase of the transit time at high collector current densities. Fig. 2.1.3/2 shows the typically observed behavior of \( \tau_f \) and its various components, for which physics-based equations will be given later in this chapter. It is important to note, that the sum of all physically (from carrier densities) calculated storage times, \( \tau_{mΣ} \), equals the transit time \( \tau_f \), that is extracted from small-signal results using the measurement method.

Fig. 2.1.3/2: Charge storage and transit time components vs. collector current density. The components \( \tau_{Bf}, \tau_{pC}, \tau_{pE}, \tau_{BE}, \tau_{BC} \), and \( \tau_{mΣ} \) were calculated from 1D device simulation, while \( \tau_B \) was extracted from small-signal simulations and \( f_T \) using the measurement method.
The minority charge model in HICUM uses an “effective” collector voltage

\[ v_{\text{ceff}} = V_T \left[ 1 + \frac{u + \sqrt{u^2 + a_{\text{ceff}}}}{2} \right] \]

with the argument \( u = \frac{v_c - V_T}{V_T} \) (2.1.3-4)

with

\[ v_c = v_{CE} - V_{CE's} \approx V_{DCi} - v_{HC} . \] (2.1.3-5)

The value of the constant \( a_{\text{ceff}} = 1.921812 \) has been adjusted to yield the same results as the exponential smoothing formulation (used in the previous version) and, thus, is not a model parameter. The internal CE saturation voltage \( V_{CE's} \approx V_{DE'i} V_{DCi} \) is a model parameter. The smoothing function for \( v_{\text{ceff}} \) has been implemented in order to provide a smooth behavior of the critical current (see later) and the forward minority charge for very small and negative values of \( v_c \). As Fig. 2.1.3/3 shows, \( v_{\text{ceff}} \) is equal to \( v_c \) for values larger than about \( 2V_{CE's} \) and approaches the thermal voltage \( V_T \) as the limit for negative values.

The transit time and minority charge model used in HICUM and its derivation are discussed in detail in [43]. In this text, the most important equations and their physical meaning are summarized.
A. Low-current densities

The low-current component $\tau_{f0}$ depends on the collector-base (or collector-emitter voltage) only,

$$\tau_{f0}(v_{BC}) = \tau_0 + \Delta \tau_{0h}(c - 1) + \tau_{Bvl} \left( \frac{1}{c} - 1 \right)$$

(2.1.3-6)

with the normalized internal BC depletion capacitance $1/c = C_{jCi,t}/(V_{BC})/C_{jCi0}$. Note, that $C_{jCi,t}$ is evaluated for the same model parameters as the internal BC depletion capacitance $C_{jCi}$, but with infinite punch-through voltage in order to roughly take into account the impact of the bias dependent space-charge region moving into the base and buried layer beyond the punch-through voltage.

The first time constant in (2.1.3-6), $\tau_0$, represents the sum of voltage independent components of various transistor regions at $V_{BC} = 0$; this condition already defines how to extract its value. The second term represents the net voltage dependent change caused by the Early-effect and the transit time through the BC space charge region: for $\Delta \tau_{0h} < 0$ the Early effect dominates while for $\Delta \tau_{0h} > 0$ the transit time increase caused by the widening of the BC space charge region at large voltages dominates. The third term takes into account the finite carrier velocity in the BC space charge region resulting in a carrier jam at low $V_{C'E'}$ voltages.

Fig. 2.1.3/4 shows two examples for the voltage dependence of the low-current transit time and its two voltage dependent components. The axis values have been normalized to the model parameters $\tau_0$ and $V_{DCe}$, respectively. The upper figure (a) contains a behavior that is (more) typical for a relatively slow high-voltage transistor, which is characterized by a relatively wide and low-doped collector region under the emitter. In this case, $\tau_{f0}$ increases with increasing $V_{C'E'} (=V_{BE'}-V_{BC'})$ due to the widening of the BC space charge region. Towards very low $V_{C'E'}$ the drift velocity within the BC space charge region decreases, and the respective (third) term in (2.1.3-6) dominates the voltage dependence, which leads again to an increase of $\tau_{f0}$ and to a minimum around $V_{BC} = 0$.

The lower figure (b) shows the typical behaviour for a high-speed transistor with, e.g., a selectively implanted collector and a thin base. With increasing reverse bias, the BC space charge region does extend noticeably also into the base, resulting in a (slightly) negative value of $\Delta \tau_{0h}$ and a decrease of the respective component. Therefore, $\tau_{f0}$ decreases with increasing $V_{C'E'}$.

The respective low-current forward minority charge is simply given by
Fig. 2.1.3/4: Normalized low-current transit time and its components as a function of normalized (internal) BC voltage: (a) for a “high-voltage” transistor \((\tau_0=10\text{ps}, \Delta\tau_{0h}=2.5\text{ps}, \tau_{Bfvl}=3\text{ps})\), (b) for a “high-speed” transistor \((\tau_0=2.5\text{ps}, \Delta\tau_{0h}=-0.4\text{ps}, \tau_{Bfvl}=0.1\text{ps})\).
B. Medium and high current densities

At medium current densities, the electric field at the BC junction starts to decrease, and the BC junction region becomes quasi-neutral at high current densities. This is often called Kirk-effect [13]. In HICUM, the onset of high-current effects is characterized by the critical current [33]

\[
I_{CK} = \frac{v_{ceff}}{r_{Ci0}} \frac{1}{\left[1 + \left(\frac{v_{ceff}}{V_{lim}}\right)^2\right]^{\frac{1}{2}}} \left[1 + \frac{x + \sqrt{x^2 + a_{ickpt}}}{2}\right]^{-1}\]

(2.1.3-8)

with \(x = (v_{ceff} V_{lim})/V_{PT}\) in the smoothing function that connects the cases of low and high electric fields in the collector, and with the constant \(a_{ickpt} = 10^{-3}\). The other (model) parameters are the internal collector resistance at low electric fields,

\[
r_{Ci0} = \frac{w_C}{q\mu nC_0N_{Ci} A E f_{cs}} ,
\]

(2.1.3-9)

the voltage defining the boundary between low and high electric fields in the collector,

\[
V_{lim} = \frac{v_{sn}}{\mu nC_0} w_C ,
\]

(2.1.3-10)

and the (collector) punch-through voltage

\[
V_{PT} = \frac{q N_{Ci}}{2\varepsilon} w_C^2 .
\]

(2.1.3-11)

As the above relations show, \(I_{CK}\) depends on the electron saturation drift velocity, \(v_{sn}\), and the electron low-field mobility, \(\mu nC_0\), as well as on width \(w_C\) and (average) doping \(N_{Ci}\) of the internal collector. The current spreading factor \(f_{cs}\), which is discussed in chapter 2.1.17, facilitates lateral scaling [40] and is calculated by TRADICA (or any other parameter generation program). Despite their physical relationship, \(r_{Ci0}, V_{lim}\) and \(V_{PT}\) are considered to be model parameters in order to offer a more flexible parameter extraction and broader application of the model. However, their physics-based relationship is very useful for temperature and statistical modelling.
Fig. 2.1.3/5: Normalized critical current $I_{CK}$ vs. normalized internal CE voltage and related single components: $I_{CKl} = \left(\frac{v_{ceff}}{r_{Ci0}}\right) \sqrt{1 + \frac{(v_{ceff} - V_{lim})^2}{V_{PT}^2}}$ from low-voltage theory; $I_{CKh} = I_{lim} \left[1 + \frac{(v_{ceff} - V_{lim})}{V_{PT}}\right]$ from high-voltage theory with $I_{lim} = \frac{V_{lim}}{r_{Ci0}}$.

The consequence of the changing electric field in the BC junction at medium current densities is, first of all, an increase in the neutral base width and, therefore, in the base component of the transit time; secondly, also the transit time through the BC space charge region may increase, depending on how large the electric field is. Thirdly, the corresponding decrease of the small-signal current gain leads to an increase of the emitter component. Since the current independent part of this component has already been taken into account in $\tau_{f0}$ only the change (increase) has to be modelled,

$$\Delta \tau_{Ef} = \tau_{Ef0} \frac{g_{tE}}{I_{CK}}$$  \hspace{1cm} (2.1.3-12)
which depends on the low-frequency common-emitter small-signal current gain $\beta_0$ and the hole transit time $\tau_{pE0}$ in which $w_E$, $\mu_{pE}$, and $v_{Ke}$ are the width, hole mobility, and the effective hole contact recombination velocity of the neutral emitter, respectively. The corresponding charge stored in the neutral emitter is:

$$\Delta Q_{Ef} = \Delta \tau_{Ef} \frac{i_{Tf}}{1 + g_{\tau E}}.$$  \hspace{1cm} (2.1.3-14)

In the neutral collector, minority (hole) charge storage starts only at high current densities [32, 33]. Therefore, the charge difference to its negligible low-current contribution is equal to the total hole charge $Q_{pC}$ in the collector:

$$\Delta Q_{Cf} = Q_{Cf} = Q_{pC} = \tau_{pCs}i_{Tf} w^2$$ \hspace{1cm} (2.1.3-15)

with the saturation storage time of the neutral collector,

$$\tau_{pCs} = \frac{w_C^2}{4 \mu_{nC0} V_T}.$$ \hspace{1cm} (2.1.3-16)

The normalized injection width,

$$\frac{w}{w_C} = \frac{i + \sqrt{i^2 + a_{hc}}}{1 + \sqrt{1 + a_{hc}}}$$ \hspace{1cm} (2.1.3-17)

is bias dependent via the variable

$$i = 1 - \frac{I_{CK}}{i_{Tf}}$$ \hspace{1cm} (2.1.3-18)
while $a_{hc}$ is considered to be a model parameter. By using a smoothing function for $w$ rather than
the original expression $i$ in (2.1.3-17), the collector charge is made continuously differentiable over
the whole bias region. The corresponding collector storage time is given by

$$\Delta \tau_{Cf} = \tau_{Cf} = \tau_{pC} = \frac{dQ_{pC}}{dI_{Tf}} = \tau_{pCs} w^2 \left[ 1 + \frac{2}{ \frac{l_{Tf}}{I_{CK}} \sqrt{l^2 + a_{hc}} } \right]$$

(2.1.3-19)

Device simulations for many different processes have shown that the shape of the current de-
pendence of the neutral base component $\tau_{Bf}$ is very similar to that of the collector portion $\tau_{pC}$ due
to the coupling of these regions by the carrier density at the BC junction. As a consequence, the
bias dependent increase of the base charge at high-current densities is similarly expressed as

$$\Delta Q_{Bf} = \tau_{Bfvs} l_{Tf} w^2$$

(2.1.3-20)

with the saturation storage time reached at high current densities,

$$\tau_{Bfvs} = \frac{w_{Bm} w_C}{2 G_{\xi} \mu_n C_0 V_T}.$$  

(2.1.3-21)

$w_{Bm}$ is the metallurgical base width, and $G_{\xi}$ ($\geq 1$) is a factor that depends on the drift field in the
neutral base [43]. The corresponding additonal base transit time reads

$$\Delta \tau_{Bf} = \frac{d\Delta Q_{Bf}}{dI_{Tf}} = \tau_{Bfvs} w^2 \left[ 1 + \frac{2}{ \frac{l_{Tf}}{I_{CK}} \sqrt{l^2 + a_{hc}} } \right].$$

(2.1.3-22)

In HICUM, the total storage time constant,

$$\tau_{hcs} = \tau_{pCs} + \tau_{Bfvs} = \frac{w_C^2}{4 \mu_n C_0 V_T} + \frac{w_{Bm} w_C}{2 G_{\xi} \mu_n C_0 V_T},$$

(2.1.3-23)
is used as a model parameter to make the model application more flexible and easy to use. As discussed in chapter 2.1.17, the accurate and physics-based description of collector current spreading and associated lateral scaling at high current densities require a partitioning between base and collector component. For this, the partitioning constant

\[ f_{thc} = \frac{\tau_{pCs}}{\tau_{hcs}} = \frac{w_C}{w_C + 2w_{BM}} \]  

(2.1.3-24)

is introduced as model parameter. A value of \( f_{thc} \) between 0 and 1 allows a gradual partitioning, with the 1D expressions given above (i.e. no collector current spreading) being employed for \( f_{thc} = 0 \), while a dominating influence of the collector term (including current spreading) can be taken into account by \( f_{thc} \to 1 \).

Fig. 2.1.3/6 shows a sketch of the current dependence of the additional transit time \( \Delta \tau_f \) and its various components, calculated with the equations given above and using model parameters that are typical for a high-speed process.

In case of negligible collector current spreading (corresponding to 1D current flow), the collector and base component can be lumped together \( (f_{thc} = 0) \), leading to the expression for the additionally stored minority charge in the base and collector region at high current densities,

\[ \Delta Q_{fh} = \Delta Q_{Bf} + Q_{Cf} = \tau_{hcs} i_T w^2 \]  

(2.1.3-25)

The corresponding increase of the transit time at high-current densities is then given by

\[ \Delta \tau_{fh} = \Delta \tau_{Bf} + \tau_{Cf} = \tau_{hcs} w^2 \left[ 1 + \frac{2}{i_T} i_T \left( \frac{I_{CK}^N}{I_{CK}^N + a_{hc}} \right) \right] \]  

(2.1.3-26)

The 1D current flow is detected by the model if the model parameters LATB and LATL (cf. chapter 2.1.17) are zero.
Fig. 2.1.3/6: Sketch of normalized transit time $\Delta \tau_f$ vs. normalized forward collector current $I_{Tf}$ including the various components: collector component $\tau_{pC}$, additional base component $\Delta \tau_{Bf}$, and additional emitter contribution $\Delta \tau_{Ef}$.

The total minority charge in the various operating regions, that is used for transient or high-frequency analysis, is then calculated according to (2.1.3-1) and it consists of the following contributions:

$$Q_f = Q_{f0} + \Delta Q_{Ef} + \Delta Q_{fh} \quad (2.1.3-27)$$

while the total forward transit time (or storage time) is given by

$$\tau_f = \tau_{f0} + \Delta \tau_{Ef} + \Delta \tau_{fh} \quad . \quad (2.1.3-28)$$

If the lateral scaling capability is used, $\Delta Q_{fh}$ and $\Delta \tau_{fh}$ are composed of their separately calculated base and collector contribution (cf. chapter 2.1.17). The above equations contain physical and process parameters that facilitate the predictions of the electrical characteristics as a function of process variations.
2.1.3.2 Minority charge component controlled by the inverse transfer current

For forward transistor operation in high-speed applications, the portion of the minority charge which is exclusively controlled by the base-collector voltage is often negligible or only a small fraction of the total minority charge. Therefore, including this charge in $Q_f$ causes only negligible error in transient operation of transistors in high-speed circuits. For small-signal high-frequency operation in the high-current region, which is a very unusual case, the base-collector voltage controlled charge may be taken into account by including its diffusion capacitance in the total internal base collector capacitance [14].

Alternatively, the BC diffusion charge can be modelled by the simple relation

$$Q_r = \tau_r i_{Tr}$$  \hspace{1cm} (2.1.3-29)

with the inverse transit time $\tau_r$ as a model parameter.
2.1.4 Depletion charges and capacitances

Modelling of depletion charges \(Q_j\) and capacitances \(C_j\) as a function of the voltage \(v\) across the respective junction is partially based on classical theory that gives within a certain operating range

\[
Q_j = \int_0^v C_j dv' = \frac{C_{j0} V_D}{1 - z} \left[ 1 - \left( 1 - \frac{v}{V_D} \right)^{(1 - z)} \right]
\]  

(2.1.4-1)

and

\[
C_j = \frac{C_{j0}}{(1 - \frac{v}{V_D})^z}.
\]

(2.1.4-2)

The zero bias capacitance \(C_{j0}\), the diffusion (or built-in) voltage \(V_D\) as well as the exponent coefficient \(z\) are the model parameters. Due to the pole at forward bias, i.e. at \(v=V_D\), however, the above formula is not yet suited for a compact model from both a numerical and physics-based point of view. The respective modification will be described for the BE depletion capacitance.

At high reverse voltages the epitaxial collector can become fully depleted up to the buried layer. This punch- (or reach-)through effect is also not included in the classical equation above (and in the SGPM). The corresponding extension will be discussed for the BC depletion capacitance.

2.1.4.1 Base-emitter junction

Fig. 2.1.4/1 shows the voltage dependence of a BE depletion capacitance at forward bias. The symbols were obtained from 1D device simulation, with depletion and minority charge defined as in [38]. The depletion capacitance follows quite well the classical equation up to a certain voltage, which is close to the turn-on voltage of a transistor used for switching applications. In contrast to the classical equation, the capacitance then reaches a maximum within the “practical” operation range of a transistor. Towards very high forward bias, the capacitance even decreases to zero, since the total depletion charge has to be limited from a physical point of view.

The modified equation employed in HICUM is described below for the example of the internal BE depletion capacitance with the (classical) model parameters \(C_{jEi0}, V_{DEi}, z_{Ei}\), and the additional
model parameter $a_{ji}$. The latter is defined in Fig. 2.1.4/1 as the ratio of the maximum value to the zero-bias value and can directly be extracted from $f_T$ measurements at low current densities (e.g. [2, 15]). As a consequence, $C_{ji}$ is kept at its maximum value in HICUM to maintain consistency between measurement and model. Keeping $C_{ji}$ constant is also justified, because at high forward bias, i.e. beyond the maximum, the diffusion capacitance becomes orders of magnitude larger than $C_{ji}$. The reverse bias region of the BE depletion capacitance and charge is described by the classical equations.

For modeling the peripheral BE depletion capacitance, the corresponding model parameters $C_{ji0}$, $V_{DE}$, $z_{ji}$, $a_{ji}$ as well as the voltage and $v_{B*E'}$ have to be inserted.

Fig. 2.1.4/1: Typical dependence of BE depletion capacitance on junction voltage at forward bias: comparison between 1D device simulation, HICUM, classical theory. In addition, characteristic variables used in the model equations have been inserted.

The forward bias depletion capacitance model consists of a classical portion and a component for medium and large forward bias (cf. Fig. 2.1.4/1). The capacitance is calculated from the derivative of the charge yielding:
with the auxiliary voltage \( v_j \) as a hyperbolic smoothing expression,

\[
v_j = V_f - V_T \frac{x + \sqrt{x^2 + a_{fj}}}{2} < V_f
\]  

(2.1.4-4)

and the derivative of \( v_j \),

\[
\frac{dv_j}{dv_{B'E'}} = \frac{x + \sqrt{x^2 + a_{fj}}}{2\sqrt{x^2 + a_{fj}}}
\]  

(2.1.4-5)

using the argument,

\[
x = \frac{V_f - v_{B'E'}}{V_T}.
\]  

(2.1.4-6)

\( V_f \) is the voltage at large forward bias, at which the capacitance of the classical expression intercepts the maximum constant value (cf. Fig. 2.1.4/1):

\[
V_f = V_{DEi}[1 - a_{jEi}^{-1/(z_{Ei})}] .
\]  

(2.1.4-7)

The corresponding charge equation reads

\[
Q_{jEi} = \frac{C_{jEi0} V_{DEi}}{1 - z_{Ei}} \left[ 1 - \left( 1 - \frac{v_j}{V_{DEi}} \right)^{(1/z_{Ei})} \right] + a_{jEi} C_{jEi0}(v_{B'E'} - v_j),
\]  

(2.1.4-8)

and \( Q_{jEi} \) is calculated similarly.

In (2.1.4-4), the value of \( a_{fj} \) can be adjusted to yield results equivalent to the former formulation. If at \( x = 0 \), which corresponds to \( v_{B'E'} = V_f \), the exponential and hyperbolic function values for \( v_j \) are forced to be the same, and here one obtains:
which is not a model parameter, but a fixed constant within the code.

### 2.1.4.2 Internal base-collector junction

The BC junction is usually operated at reverse bias. If the internal voltage $-v_{B'C'}$ exceeds the effective punch-through voltage (see later), the epitaxial collector region becomes fully depleted. For an ideal step-like transition from the epitaxial collector to the buried-layer the corresponding capacitance would remain constant (like a plate capacitance). However, in reality the doping concentration increases with only a finite slope towards the maximum buried layer concentration. As a consequence, $C_{jCi}$ still decreases even beyond punch-through, but with a weaker voltage dependence.

![Typical dependence of BC depletion capacitance on junction voltage at reverse bias: comparison between 1D device simulation (symbols), HICUM (solid line), classical theory (dashed line). In addition, characteristic variables used in the model equations have been inserted.](image)

\[
a_{fj} = 4 \ln^2(2) = 1.921812
\]  

(2.1.4-9)
Before the capacitance equation is explained in detail, it is helpful to define a number of variables that are needed in the equations. The effective punch-through voltage is given by

\[ V_{jPCi} = V_{PTCi} - V_{DCi} = \frac{qN_{Ci}}{2e}w_{Ci}^{2} - V_{DCi}, \]  

(2.1.4-10)

which is shown in Fig. 2.1.4/2. For flexibility and accuracy reasons as well as in order to simplify and decouple parameter extraction, \( V_{PTCi} \) is considered as a separate model parameter rather than using \( V_{PT} \) from the \( I_{CK} \) formulation. For predictive modeling \( V_{PTCi}=V_{PT} \) is certainly a good initial guess.

The voltage defining the boundary between the classical expression and the maximum (constant) value at large forward bias was already defined for the BE junction capacitance (cf. Fig. 2.1.4/1); in terms of the respective BC model parameters it reads here as:

\[ V_{fCi} = V_{DCi}[1 - d_{jCi}^{-\frac{1}{2}}(z_{Ci})]. \]  

(2.1.4-11)

The voltage, at which the transition from medium to large reverse bias (slowly) starts, is defined as

\[ V_{r} = 0.1V_{jPCi} + 4V_{T}. \]  

(2.1.4-12)

In the following, “large reverse” bias is defined as \( v_{BCi} \leq V_{jPCi} \), “medium” bias is defined as \( V_{jPCi} < v_{BCi} < V_{fCi} \), and “large forward” bias is defined as \( v_{BCi} \geq V_{fCi} \).

The depletion capacitance consists of three components,

\[ C_{jCi} = C_{jCi,cl} + C_{jCi,PT} + C_{jCi,fb}, \]  

(2.1.4-13)

which are discussed below in more detail.

\( C_{jCi,cl} \) represents the contribution at medium bias,

\[ C_{jCi,cl} = \frac{C_{jCi0}}{(1 - v_{j,m}/V_{DCi})^{z_{Ci}}} \cdot \frac{e_{j,r}^{e_{j,m}}}{1 + e_{j,r}^{e_{j,m}}}. \]  

(2.1.4-14)

which contains the classical equation as the first term. The last two product terms result from smoothing functions for the respective BC junction voltage, that enable a continuously differenti-
able transition to the two adjacent bias regions. Like for the BE depletion capacitance, the numerical overflow at large forward bias is avoided by replacing $v_{B'C'}$ with the auxiliary (smoothed) voltage, $v_{j,m}$, defined in (2.1.4.18). To get the other two components, we need to define:

$$v_{j,r} = V_{fC_i} - V_T \ln[1 + e_{j,r}] \quad \text{with} \quad e_{j,r} = \exp\left(\frac{V_{fC_i} - v_{B'C'}}{V_T}\right) \quad (2.1.4-15)$$

which contains the actual junction voltage. Analogously to $C_{jiE}$, the forward bias value (for $e(v_{j,r}) = 0$) is limited to a maximum,

$$C_{jC_i,fb} = a_{jC_i} C_{jC_i0} \frac{1}{1 + e_{j,r}} \quad (2.1.4-16)$$

with $a_{jC_i}$ as constant. The last term is again a continuously differentiable function that enables a smooth transition between large forward and medium bias. Since $C_{jC_i}$ is of little practical relevance and is influenced at high forward bias, $a_{jC_i}$ is set to 2.4 in the code, rather than being a model parameter in order to keep the number of parameters as low as possible.

Finally, $C_{jC_i,PT}$ represents the large reverse bias region around and beyond punch-through,

$$C_{jC_i,PT} = \frac{C_{jC_i0,r}}{(1 - v_{j,r} / V_{DCi}) z_{C_i,r}} \frac{1}{1 + e_{j,m}} \quad (2.1.4-17)$$

Here, the first term contains the classical voltage dependence, but now with different parameters $C_{jC_i0,r}$ and $z_{C_i,r}$ which model the weak bias dependence under punch-through conditions, and will be discussed later. In this case, the auxiliary voltage is given by the smoothing function

$$v_{j,m} = -V_{jPC_i} + V_r \ln[1 + e_{j,m}] \quad \text{with} \quad e_{j,m} = \exp\left(\frac{V_{jPC_i} + v_{j,r}}{V_r}\right) \quad (2.1.4-18)$$

which now depends on the auxiliary voltage $v_{j,r}$ in order to enable a smooth capacitance and charge behavior over all bias regions. Note, that $v_{j,r}$ equals $v_{B'C'}$ at large reverse bias.

The corresponding depletion charge is then obtained by integration of $C_{jC_i}$,
with the component at medium bias,

\[
Q_{jCi,m} = \frac{C_{jCl0} V_{DCi}}{1 - z_{Cl}} \left[ 1 - \left( \frac{v_{j,m}}{V_{DCi}} \right)^{1 - z_{Cl}} \right], \tag{2.1.4-20}
\]

the component at large reverse bias,

\[
Q_{jCi,r} = \frac{C_{jCl0,r} V_{DCi}}{1 - z_{Cl}} \left[ 1 - \left( \frac{v_{j,r}}{V_{DCi}} \right)^{1 - z_{Cl}} \right], \tag{2.1.4-21}
\]

and a “correction” component,

\[
Q_{jCi,c} = \frac{C_{jCl0,c} V_{DCi}}{1 - z_{Cl}} \left[ 1 - \left( \frac{v_{j,m}}{V_{DCi}} \right)^{1 - z_{Cl}} \right], \tag{2.1.4-22}
\]

that results from the integration process. The parameters \(C_{jCl0,r}\) and \(z_{Cl}\) in the last two components are required to model the weaker voltage dependence under punch-through conditions, compared to the voltage dependence at medium bias. \(C_{jCl0,r}\) can be calculated from the punch-through voltage as

\[
C_{jCl0,r} = C_{jCl0} \cdot \left( \frac{V_{DCi}}{V_{PTCl}} \right)^{z_{Cl}} \tag{2.1.4-23}
\]

while \(z_{Cl}\) is internally set to \(z_{Cl}/4\). The latter turned out to be a good compromise for the investigated cases. As consequence, both \(C_{jCl0,r}\) and \(z_{Cl}\) are only internal parameters and do not have to be extracted and externally specified. If required, however, it would be sufficient to make \(z_{Cl}\) a user model parameter.

At high current densities \(C_{jCl}\) becomes also current dependent as discussed, e.g., in [32]. The respective (smooth) expressions for both capacitance and charge require complicated expressions which can increase simulation time significantly. As discussed in [14] for small-signal applications,
a pure voltage dependent model for $C_{jCl}$ proved to be sufficient, since transistors in (small-signal) analog circuits are not operated at high current densities. For large-signal transient applications, however, the influence of a current dependent $C_{jCl}$ is negligible, especially at higher current densities. Therefore, the current dependence of $C_{jCl}$ is neglected in the present HICUM version.

### 2.1.4.3 External base-collector junction

The total BC capacitance consists of a bias dependent external depletion capacitance, $C_{jCx}$, and a bias independent parasitic capacitance $C_{BCpar}$ (see also Section 2.1.7). The depletion portion in turn contains a SIC related bottom component, a background doping related bottom component and a perimeter component, that all usually have different voltage dependence and, hence, model parameters. For a compact model, the depletion components are merged into a single element by fitting a single set of model parameters to the overall voltage dependence (e.g. using TRADICA). The resulting capacitance (and charge), $C_{BCx} = C_{jCx}(v) + C_{BCpar}$, is then partitioned across the external base resistance $r_{Bx}$ (cf. Fig. 2.1.1/1) according to a first-order high-frequency approximation of the RC transmission line behaviour of the external base. This merging procedure, which is also required for simpler equivalent circuit structures, reduces the number of model parameters to be specified for the circuit simulator. A possible alternative is to determine the partitioning from measurements of, e.g., high-frequency S-parameters; however, it was found that such a partitioning factor (strongly) depends on the measurement method and conditions used and, therefore, can assume non-physical values.

The partitioning of the total capacitance $C_{BCx}$ across $r_{Bx}$ requires an additional model parameter,

$$f_{BCpar} = \frac{C_{BCx2}}{C_{BCx}}$$

and defines the ratio of the portion at the perimeter base node (“behind” $r_{Bx}$) to the total capacitance. The factor $f_{BCpar}$ depends on geometry and technology specific parameters (and can be calculated by, e.g., TRADICA). According to (2.1.4-24) the capacitances are split as follows in the present HICUM implementation (cf. Fig. 2.1.1/1):
\[ C_{BCx} = C_{BCx1} + C_{BCx2} = (1 - f_{BCpar}) C_{BCx} + f_{BC} C_{BCx} \]  

(2.1.4-25)

Depending on the values for \( f_{BCpar} \), \( C_{BCpar} \) and \( C_{jCx} \) as well as according to the nature of the capacitance components, different cases have to be distinguished. For instance, if \( f_{BCpar} > C_{BCpar}/C_{BCx} \) then part of \( C_{BCpar} \) has to be connected to node B* (i.e. behind \( r_{Bx} \)). Since \( C_{BCpar} \) is closest to the base contact, usually the major portion or even its total value has to be connected to the base terminal B. The various cases are taken into account based on the zero-bias depletion capacitance rather than the voltage dependent value in order to reduce arithmetic operation count. The implementation is as shown in Fig. 2.1.4/3.

\[
\begin{align*}
C_{BCx01} &= (1 - f_{BCpar}) C_{BCx0} \\
\text{if}(C_{BCx01} \geq C_{BCpar}) & \text{ then} \\
C_{BCpar} &= C_{BCpar} \\
C_{BCpar2} &= 0 \\
C_{jCx01} &= C_{BCx01} \cdot C_{BCpar} \\
C_{jCx02} &= C_{jCx0} \cdot C_{jCx01} \\
\text{else} & \\
C_{BCpar} &= C_{BCx01} \\
C_{BCpar2} &= C_{BCpar} \cdot C_{BCpar1} \\
C_{jCx01} &= 0 \\
C_{jCx02} &= C_{jCx0} \\
\end{align*}
\]

endif

Fig. 2.1.4/3: Implementation of B-C capacitance partitioning

Since the depletion charge of the external BC junction does not depend on the transfer current, the purely voltage dependent expressions given for \( C_{jCi} \) and \( Q_{jCi} \) can be employed for \( C_{jCx} \) and \( Q_{jCx} \) by simply inserting the model parameters \( C_{jCx0} \), \( V_{DCx} \), \( z_{Cx} \), and \( V_{PTCx} \). The punch-through voltage (and capacitance) of the external collector region is usually different from that of the internal region due to their different epi widths and - in case of a selectively implanted collector - the different doping concentrations in the internal and external region.
2.1.4.4 Collector-substrate junction

The CS depletion charge and capacitance are modelled by the same type of formula as employed for the bottom part of the external BC charge and capacitance. The corresponding model parameters are $C_{jS0}$, $V_{jS}$, $z_S$, and $V_{PTS}$. Taking into account the punch-through effect may be necessary for technologies containing a semi-insulating substrate (layer). For most technologies, however, there is no punch-through effect at the CS junction, and $V_{PTS}$ can be set to "infinity".

Since the CS junction is modelled by a single element, $C_{jS}$ contains - from a physical point of view - both the bottom and peripheral portion of that junction; i.e., the model parameters result from merging the corresponding voltage dependent portions [44] (see also Fig. 2.1.17/4).

For certain applications and processes, an additional substrate coupling network in series to $C_{jS}$ as well as a substrate transistor may be necessary. These extensions are discussed later.
2.1.5 Static base current components

The base current flowing into the emitter can be separated into a bottom and peripheral component. The bottom portion models the current injected across the \((effective)\) emitter area, and the peripheral component models the current injected across the peripheral BE junction. Each of these components contains the current contributions caused by volume (SRH and Auger) recombination, by surface recombination, by tunneling, and by an \((effective)\) interface recombination velocity at the emitter "contact". The physical modelling of all these effects, including e.g. the modulation of the neutral emitter width in advanced and heterojunction bipolar transistors, would require a complicated and computationally time expensive description as well as a significantly increased effort in parameter determination. From a practical application point of view, however, a simpler approach for most of the above mentioned components does exist that is sufficiently accurate.

The following equations describe the d.c. and quasi-static component of the base current, which are applicable also at high frequencies. Note, that at high switching speeds or frequencies, the dynamic (capacitive) component of the base current becomes much larger than the d.c./quasi-static component, so that its correct modeling is of higher importance for those applications.

The quasi-static internal base current, which represents injection across the bottom emitter area, is modelled in HICUM as

\[
 i_{jBEi} = I_{BEiS} \left[ \exp\left( \frac{V_{BE}}{m_{BEi} V_T} \right) - 1 \right] + I_{REiS} \left[ \exp\left( \frac{V_{BE}}{m_{REi} V_T} \right) - 1 \right]
\]  \hspace{1cm} (2.1.5-1)

The saturation currents \(I_{BEiS}\) and \(I_{REiS}\) as well as the non-ideality coefficients \(m_{BEi}\) and \(m_{REi}\) are model parameters. The first component in the above formula represents the current injected into the neutral emitter; a corresponding \(m_{BEi}>1\) represents effects such as Auger recombination and the (very small) modulation of the width of the neutral emitter region. The second component represents the loss in the space charge region due to volume and surface recombination; the value of \(m_{REi}\) is usually in the range of 1.5 to 2 so that this component only plays a role at low injection. It is used to model the decrease of the current gain at low current densities.

Analogously, the quasi-static base current injected across the emitter periphery is given by
The saturation currents $I_{BE_pS}$ and $I_{RE_pS}$ as well as the non-ideality factors $m_{BE_p}$ and $m_{RE_p}$ are model parameters.

Since the recombination at low forward bias is more pronounced at the emitter periphery compared to the bottom, its contribution ($I_{RE_iS}$ ...) to the internal base current component may often be omitted in order to simplify the model and the parameter determination.

In hard-saturation or for inverse operation the current contributions across the base-collector junction become significant. The component of the internal BC junction is

$$i_{jBC} = I_{BE_pS} \left[ \exp \left( \frac{V_{BE}'}{m_{BE_p}V_T} \right) - 1 \right] + I_{RE_pS} \left[ \exp \left( \frac{V_{RE}'}{m_{RE_p}V_T} \right) - 1 \right].$$  \hspace{1cm} (2.1.5-2)

In many practical cases, both components can be combined into one, $i_{jBC}$, between B* and C', without loss of accuracy (in, e.g., the output characteristics). This simplifies parameter extraction and reduces the number of model parameters.

In various SiGe-HBT processes, an additional base current is observable that mostly results from the additional minority charge storage in the base at the barrier caused by the Ge drop within the BC junction [7]. The typical behavior is shown in Fig. 2.1.5/1 for the base current of a SiGe-DHBT. Triggered by the collapse of the electric field in the collector at high current densities, which can be described by the critical current $I_{CK}$, the conduction band barrier for electrons starts to form at about $V_{BE} = 0.8V$ for the transistor under consideration. The resulting accumulation of electrons on the base side of the BC junction is compensated by an accumulation of holes, which leads to an excess recombination rate. As a consequence, the corresponding current can be approximated to a first order by
with $\Delta Q_{Bf}$ as the additional minority charge in the base, which increases rapidly above $I_{CK}$; the corresponding recombination constant $\tau_{Bhrec}$ is a new model parameter. The current has been taken into account by adding a (controlled) current source in parallel to $i_{jBEi}$.

Fig. 2.1.5/1: Base current vs. base-emitter voltage for a SiGe-DHBT. Comparison between device simulation (circles), model without additional recombination component (dashed line) and model with additional recombination component (crosses).
2.1.6 Internal base resistance

In HICUM, the internal and external base resistance are separately treated. The value of the internal base resistance $r_{Bi}$ depends strongly on operating point, temperature, and mode of transistor operation (d.c., transient, h.f. small-signal). Especially the last mentioned dependence is a very complicated issue for high-speed large-signal switching processes.

The d.c. internal base resistance is modelled by

$$ r_{Bi} = r_i \psi(\eta) $$

and is in HICUM/Level2 defined by the effective emitter dimensions $b_E$ and $l_E$. Both the resistance $r_i$ and the emitter current crowding function are bias and geometry dependent, and will be given below.

Conductivity modulation is described by the expression [26, 28]

$$ r_i = r_{Bi0} \frac{Q_0}{Q_0 + \Delta Q_p} $$

with $r_{Bi0}$ as zero-bias internal base resistance, and the bias dependent portion $\Delta Q_p$ of the stored hole charge,

$$ \Delta Q_p = Q_{jei} + Q_j + Q_r. $$

$Q_r$ is generally very small, hence may be neglected. $Q_0$ is a model parameter that is physically related and often is close to the zero-bias hole charge $Q_{p0}$ [26, 28]. Therefore, $Q_0$ is calculated from $Q_{p0}$ as

$$ Q_0 = (1 + f_{DQr0})Q_{p0} $$

with the factor $f_{DQr0}$ as model parameter. Fig. 2.1.6/1 shows the typical bias dependence of the (normalized) internal base sheet resistance due to conductivity modulation; the ratio $r_{SBi}/r_{SBi0}$ is proportional to $r_i/r_{Bi0}$.
The zero-bias resistance $r_{Bi0}$ is a model parameter which can be calculated (e.g., by TRADICA) as a function of emitter geometry and zero-bias internal base sheet resistance $r_{SBi0}$. For a transistor with $n_E$ emitter contacts (or stripes) and arbitrary aspect ratio $l_E/b_E \geq 1$:

$$r_{Bi0} = r_{SBi0} \frac{b_E}{l_E n_E} g_i$$ \hspace{1cm} (2.1.6-5)

with the geometry function [34, 35] for $n_E+1$ base contacts

$$g_i = \frac{1}{12} - \left( \frac{1}{12} - \frac{1}{28.6} \right) \frac{b_E}{l_E}.$$ \hspace{1cm} (2.1.6-6)

The effect of emitter current crowding is described for all aspect ratios $l_E/b_E \geq 1$ by the function [34, 35, 27]
The factor $f_{geo}$ is a model parameter which takes into account the geometry dependence of emitter current crowding (cf. Chapter 2.1.17).

For transistors with narrow emitter contacts (or stripes) the influence of the charge storage at the emitter periphery on the dynamic transistor behaviour can significantly increase. In order to obtain acceptable computation times and to keep the extraction effort reasonable, the HICUM/LEVEL2 equivalent circuit does not contain a complete peripheral transistor element. Therefore, the peripheral charge has to be taken into account by modifying existing elements. The internal base impedance seen between the terminals B*-E' is decreased by the (effective) peripheral charge $Q_{fp}$ to

$$r_{Bi}^* = r_{Bi} \frac{\Delta Q_i}{\Delta Q_p} = r_{Bi} \frac{\Delta Q_i}{\Delta Q_i + Q_{fp}}.$$  \hfill (2.1.6-9)

$\Delta Q_i$ is the change of the hole charge in the internal transistor during a switching process. For model implementation, however, $\Delta Q_i$ is approximated by the change of only the major charge contributions w.r.t. equilibrium,

$$\Delta Q_i = Q_{jei} + Q_{ji}$$  \hfill (2.1.6-10)

with $Q_{ji}$ as the internal minority charge. The latter as well as the peripheral minority charge $Q_{fp}$ can be calculated from the total minority charge $Q_f$, that is analytically described in the model, using the model parameter $f_{Qf}$,

$$Q_{ji} = f_{Qf} Q_f$$  \hfill (2.1.6-11)

and

$$Q_{fp} = (1 - f_{Qf}) Q_f$$  \hfill (2.1.6-11)
The parameter $f_{Q_i}$ depends on geometry and can be determined from the transit time of transistors with, e.g., different emitter widths. Note, the denominator of (2.1.6-9) contains $Q_f$ directly so that $Q_{fp}$ is not required to be explicitly known or calculated. Previous versions contained also the internal BC depletion charge in (2.1.6-9), which had to be dropped though to avoid potential division by zero for large BC reverse voltages and unfavorable combinations of model parameters. Thus, the implemented equation reads

$$r_{Bi}^* = \frac{Q_{jEi} + f_{Q_i}Q_f}{Q_{jEi} + Q_f}.$$  \hspace{1cm} (2.1.6-12)

For the (high-frequency) small-signal case a similar expression can be derived [14],

$$r_{Bi}^* = r_{Bi} \frac{C_i}{C_i + C_{dEp}}$$  \hspace{1cm} (2.1.6-13)

with $C_{dEp} = C_{dE}(1-f_{Q_i})$ as the peripheral diffusion capacitance and

$$C_i = C_{jEi} + C_{dEi}$$  \hspace{1cm} (2.1.6-14)

as the total capacitance connected to the internal base node $B'$. The use of $r_{Bi}^*$ from (2.1.6-9) gives for slow transients or low frequencies a (small) difference compared to the actual d.c. value of $r_{Bi}$. However, that deviation is usually insignificant because the influence of the peripheral charge or capacitance is large only for narrow emitter stripes where the d.c. internal base resistance is comparatively small. Note again, that for calculating the denominator of (2.1.6-13) $C_{dEp}$ does not need to be known explicitly, but only $C_{dE}$. Thus, the implemented equation reads

$$r_{Bi}^* = r_{Bi} \frac{C_{jEi} + f_{Q_i}C_{dE}}{C_{jEi} + C_{dE}}.$$  \hspace{1cm} (2.1.6-15)
2.1.7 External (parasitic) bias independent capacitances

In addition to junction and diffusion capacitances, that are both operating point dependent, there may exist constant parasitic capacitances between base and emitter as well as base and collector. The parasitic base-emitter capacitance $C_{BEpar}$ is caused by the spacer region and overlap of emitter poly over base poly. The parasitic base collector capacitance $C_{BCpar}$ is caused by the overlap of base poly and contact region over the buried layer (or the epi collector). The significance of these capacitances depends on the technology considered. In order to make HICUM applicable for an as large as possible variety of technologies, two parasitic capacitances are included in the equivalent circuit of Fig. 2.1.1/1.

$C_{BEpar}$ takes into account the overlap of emitter and base connection, e.g., $n^+$ poly-silicon separated from $p^+$ poly-silicon by the thin spacer oxide in double self-aligned transistors (cf. Fig. 2.1.7/1).

Physically, the BE isolation capacitance $C_{Eox}$, which is caused by the base-emitter spacer region, and the external base resistance have a distributed character, as shown in Fig. 2.1.7/2(a). Moreover, in advanced processes, the isolation capacitance increases due to a smaller spacer thickness, while the base-emitter perimeter junction capacitance $C_{jEp}$, represented by its charge element charge $Q_{jEp}$ in Fig. 2.1.7/2(b), is decreasing due to shallower emitter junction depths. The exact representation of these elements in a compact model for an accurate high-frequency description depends on the contributions of the various base resistance and capacitance portions and the geometry of the BE spacer isolation region. In addition to the BE spacer related capacitance $C_{Eox}$, the parasitic capacit-
ittance $C_{BE,metal}$ (and its associated charge $Q_{BE,metal}$) from the metal contact studs on top of the base and emitter poly-silicon increases with shrinking design rules. This capacitance, which belongs to the layout (p-cell) and thus to the transistor model, is connected directly between the base and emitter terminals.

For a compact model, a lumped representation of both the external base resistance and the parasitic capacitances is required. For this, a p-equivalent circuit is the best first-order compromise (cf. Fig. 2.1.7/2(b)) that allows an improved high-frequency modeling. Therefore, the distributed isolation capacitance is partitioned between the perimeter and external base node to make the model more flexible for a larger variety of processes. For instance, if the resistance contribution of the spacer region to the total external base resistance dominates, most of $C_{Eox}$ needs to be assigned to the internal base node ($C_{Eox,2}$). The partitioning of $C_{Eox}$ in form of a $\pi$-equivalent circuit also allows to include the metal capacitance without any additional effort.

The partitioning option requires as model parameters the specification of either the partial capacitance components at each node or the total parasitic BE capacitance,

$$C_{BEpar} = C_{Eox} + C_{BE,metal}$$

and a partitioning factor. The latter option is more convenient from a user’s point of view and, hence, employed in HICUM. The respective model parameter

$$f_{BEpar} = \frac{C_{BEpar,2}}{C_{BEpar}} = \frac{C_{Eox,2} + C_{BE,metal}}{C_{Eox} + C_{BE,metal}}$$

is defined as the ratio of the “inner” to the total (measured) parasitic capacitance. Thus, the value $f_{BEpar} = 0$ indicates that the whole parasitic capacitance is connected between the transistor terminals.
In many modern bipolar technologies the base contact is located on a field oxide and causes an additional isolation capacitance $C_{BCpar}$ between base and collector terminal (cf. Fig. 2.1.7/3). This capacitance is included in the equivalent circuit within $C_{BCx}$ since its partitioning across $r_{Bx}$ depends on the technology. The parameter $f_{BCpar}$ determines the actual partitioning of $C_{BCpar}$, too, as was shown earlier in Fig. 2.1.4/3.

Both the parasitic capacitances are strongly geometry dependent and either have to be measured using proper test structures or can be calculated by TRADICA.
Fig. 2.1.7/3: Physical origin of BC isolation (overlap) capacitance $C_{Cox}$, which is part of $C_{BCpar}$. 
2.1.8 External series resistances

The resistive regions of the external transistor and the emitter contact are represented in the equivalent circuit of Fig. 2.1.1/1 by bias independent series resistances. The reason for including a substrate resistance in the equivalent circuit will be discussed in Section 2.1.11.

A. External base resistance

Fig. 2.1.8/1 contains a cross section through the external base region of a double-poly self-aligned bipolar transistor. The external base resistance $r_{Bx}$ consists of the following components:

- base contact resistance, $r_{KB}$;
- resistance of the poly-silicon on the field oxide, $r_{po}$;
- resistance of the poly-silicon on the mono-silicon, $r_{pm}$;
- (link) resistance under the spacer, $r_{sp}$.

![Fig. 2.1.8/1: The various components of the external base resistance.](image)

The value of each of these components depends on the dimensions of the region and the corresponding sheet resistance or specific resistivity [34, 35]. The external base resistance is then given by:

$$r_{Bx} = r_{KB} + r_{po} + r_{pm} + r_{sp} \quad (2.1.8-1)$$

Many advanced processes use a silicide with a sheet resistance of typically 2...8 $\Omega$/sq. As a consequence, $r_{po}$ and a portion of $r_{pm}$ are significantly reduced and become small compared to the contact and, especially, the link resistance.

For short emitters and transistors with a one-sided base contact only, 3D effects become important that are taken into account by TRADICA’s resistance calculations according to [34, 35].
B. External collector resistance

Fig. 2.1.8/2 contains a cross section through the buried layer and collector region of a bipolar transistor. The external collector resistance $r_{Cx}$ consists of the following components:

- collector contact resistance, $r_{KC}$;
- resistance of the sinker region, $r_{\text{sink}}$, connecting contact and buried layer;
- resistance of the buried layer, $r_{bl}$.

The value of each of these components depends on the dimensions of the region and the corresponding sheet resistance or specific resistivity [44]. The external collector resistance is then given by:

$$r_{Cx} = r_{KC} + r_{\text{sink}} + r_{bl}$$

The external collector resistance does not contain any resistance component from the epitaxial layer under the emitter. If $r_{KC}$ is determined by the poly-mono-silicon interface resistance, it would be about the same as the emitter contact resistance.

The distributed collector current flow in multi-emitter transistors as well as a different number and location of collector stripes (or contacts) is taken into account in TRADICA by using special formulas. Also, for short emitter (and collector) stripes, current spreading in the buried layer is included in the resistance calculations.

Fig. 2.1.8/2: The various components of the external collector resistance.
C. Emitter resistance

The emitter resistance $r_E$ consists of the following (major) components:

- metallization resistance, $r_{Em}$;
- poly-silicon resistance, $r_{Ep}$;
- resistance of the interface between poly-silicon and mono-silicon, $r_{Ei}$;
- resistance of the mono-silicon bulk region, $r_{Eb}$.

![Diagram of emitter resistance components](image_url)

**Fig. 2.1.8/3: The various components of the emitter resistance.**

For many processes, measurements have been showing a direct proportionality of $r_E$ with the reciprocal emitter window area. As a consequence, it is assumed that the emitter resistance for technologies with poly-silicon emitter is mainly determined by the resistance $r_i$ at the interface between poly- and mono-silicon, and that contributions from the other regions are of minor importance. However, this has to be verified for each particular process.
Fig. 2.1.8/4: Measured emitter resistance vs. reciprocal emitter window area and comparison to the scaling equation $r_E = \frac{\hat{r}_E}{A_E} + r_0$ with $\hat{r}_E$ as area specific emitter resistance in $[\Omega \mu m^2]$ and $r_0$ as residual (parasitic) probe resistance.
2.1.9 Non-quasi-static effects

Non-quasi-static (NQS) effects are occurring at high-frequencies or fast switching processes. Note, that the designation "high" or "fast" is relative and depends on the technology employed. NQS effects exist in both vertical and lateral spatial direction.

a) Vertical direction

It is well-known from “classical” transistor theory that at high frequencies the minority charge $Q_f$ and the transfer current $i_T$ are reacting delayed w.r.t. the voltages across both pn-junction (e.g. [52]). This effect is taken into account in HICUM by introducing additional delay times for both $Q_f$ and $I_T$. These additional delay times are modelled as a function of bias by relating them to the transit time [14]:

$$\tau_2 = \alpha_{Qf}\tau_f \quad \text{and} \quad \tau_m = \alpha_{iT}\tau_f.$$

(2.1.9-1)

The factors $\alpha_{Qf}$ and $\alpha_{iT}$ are model parameters. The assumption of a stiff coupling between the additional delay times and the transit time has to be regarded as a first order approximation, especially at high current densities where a certain current dependence of $\alpha_{Qf}$ and $\alpha_{iT}$ has been observed [39]. However, it is questionable whether a more complicated modelling of $\tau_2$ and $\tau_m$ is justified from an application point of view [14]. Note, that the SGPM only allows $\tau_m$ to be specified for one (fixed) operating point. Fig. 2.1.9/1 shows the NQS factors as a function of collector current density for a 15GHz process.

The additional time delay, which results in an excess phase in the frequency domain, is implemented in HICUM using a second order Bessel polynomial [51] for both time and frequency domain analysis in order to maintain consistency of the respective results. The ideal delay proposed in [52] would cause implementation problems in a circuit simulator for time domain analysis. The use of a Bessel polynomial avoids those problems and leads to the same results in the frequency range of practical interest.
Fig. 2.1.9/1: NQS factors as a function of collector current density calculated from 1D device simulation; $V_{CE} = 1.5\text{V}$.

b) Lateral direction

Dynamic emitter current crowding causes at high frequencies (or fast transients) a reduction of the impedance seen into the internal base node compared to d.c. or low-frequency conditions.

For the small-signal case, the distributed character of the internal base region can be modelled by shunting an adequate capacitance $C_{rBi}$ in parallel to the d.c. resistance $r_{Bi}$. An analytical treatment of the small-signal input impedance of a stripe emitter transistor with $l_E/b_E>>1$ results for not too high frequencies in

$$
CrBi \cdot CrBi \cdot Ci = CrBi \cdot Ci \quad \text{(2.1.9-2)}
$$

with $C_i$ as the total capacitance connected to the internal base node B',

$$
C_i = C_{jEi} + C_{jci} + C_{dE} + C_{dc} \quad \text{(2.1.9-3)}
$$
From theory \( f_{CrBi} = 0.2 \) for a long rectangular emitter stripe [22]. In general though, \( f_{CrBi} \) depends on the emitter geometry; for instance, it increases (slightly) for smaller emitter aspect ratios. Therefore and to provide maximum flexibility, \( f_{CrBi} \) is considered as a model parameter.

The derivation of (2.1.9-2) is based on the assumption of negligible emitter current crowding. Therefore, if this assumption is violated, (2.1.9-2) must not be used. Note, that for fast large-signal transient applications, where lateral NQS effects are most pronounced, generally strong transient current emitter crowding occurs. Furthermore, the theory leading to (2.1.9-2) is entirely based on a small-signal consideration and does not provide any clue regarding the charge stored on the capacitor. In fact, due to the bias dependence of \( C_{rBi} \) according to (2.1.9-3), there is no simple charge representation in time domain that would produce just the parallel capacitor across \( r_{Bi} \) without any additional derivatives (i.e. transcapacitances).

As a consequence, it is strongly recommended not to use \( C_{rBi} \) for any type of transient analysis and to consider \( C_{rBi} \) only as a means for improving the model for small-signal circuit design. If for time-domain simulation, the associated charge needs to be implemented, it is given by

\[
Q_{rBi} = C_{rBi} V_{B-}^* B
\]

and not by \( Q_{rBi} = f_{CrBi} (Q_{Je} + Q_{jC} + Q_j + Q_r) \), which yields a completely different current.
2.1.10 Breakdown

2.1.10.1 Collector-Base Breakdown

HICUM contains a breakdown model for the base-collector junction that is valid for a weak avalanche effect and a planar breakdown occurring in the internal transistor, i.e. below the emitter. The latter is a reasonable assumption because published measurements for (self-aligned) poly-silicon emitter transistors show such a planar breakdown rather than a breakdown at the periphery of the external BC-junction. The model, which is described also in [41], is intended to indicate the onset of breakdown. In how far, however, it is suited for a simulation and design of circuits somewhat within the breakdown regime depends partially also on the numerical robustness of the particular circuit simulator. Also, the present model does not include breakdown at high current densities, where the maximum electric field occurs at the buried layer rather than at the BC junction. The related instabilities (such as snap-back) would cause convergence problems for most circuit simulators.

The model equation for the element $I_{AVL}$ in Fig. 2.1.1/1 is based on the well-known relationship

$$i_{AVL} = I_T f \int_0^{w_{BC}} a_n \exp(-b_n / |E|) \, dx$$  \hspace{1cm} (2.1.10-1)

The ionization rate $a_n$ and the field $b_n$ are coefficients describing the Avalanche process, $E$ is the electric field within the junction region, $x$ is the ordinate in vertical direction, and $w_{BC}$ is the width of the BC depletion region. From this, the avalanche generation current can be approximated by

$$i_{AVL} = i_T f_{AVL} (V_{DCi} - V_{BC}) \exp(-\frac{q_{AVL}}{C_{ji}(V_{DCi} - V_{BC})})$$  \hspace{1cm} (2.1.10-2)

with the model parameters

$$f_{AVL} = 2a_n / b_n$$  \hspace{1cm} (2.1.10-3)

$$q_{AVL} = b_n a_0 E / 2$$  \hspace{1cm} (2.1.10-4)

which depend on emitter area, physical data and temperature (via $a_n$ and $b_n$).
The possible numerical instability in (2.1.10-2) at \(v_{BC}=V_{DCi}\) can be avoided by replacing the term \((V_{DCi}-v_{BC})\) by \(V_{DCi}^{1/z_{Ci}}\), in which \(1/c = C_{jCi0}(v_{BC})/C_{jCi0}\) is the normalized depletion capacitance with an infinite \(V_{PTCi}\) value as also used in \(\tau_{f0}\). This leads to the expression

\[
i_{AVL} = I_T f_{AVL} V_{DCi}^{1/z_{Ci}} \exp\left(-\frac{q_{AVL}}{C_{jCi}V_{DCi}^{1/z_{Ci}}}\right),
\]

(2.1.10-5)

that is continuously differentiable at forward bias \(v_{BC}\). The terms \(f_{AVL} V_{DCi}\) and \(q_{AVL}/V_{DCi}\) are not merged into single parameters due to their different temperature dependence. From a computational point of view, \(i_{AVL}\) can simply be set to zero for \(v_{BC} \geq 0\). At large reverse bias \(v_{BC} < -q_{AVL}/C_{jCi0}\), \(i_{AVL}\) is linearized to avoid convergence problems.

Fig. 2.1.10/1 shows the ratio \(i_{AVL}/I_T\), which is proportional to the multiplication factor, as function of the normalized BC voltage for different values of the exponent coefficient \(q_{AVL}/(C_{jCi0}V_{DCi})\).

Fig. 2.1.10/1: Avalanche current \(i_{AVL}\), normalized to \(I_T\) (=\(I_{TF}\)), as a function of the normalized BC voltage for various values of the exponent coefficient \(q_{AVL}/(C_{jCi0}V_{DCi})\) (see labels). Model parameters used: \(C_{jCi0}=0.56fF/\mu m^2\), \(V_{DCi}=0.79V\), \(z_{Ci}=0.307\).
2.1.10.2 Emitter-base breakdown

In advanced bipolar transistors the EB breakdown voltage is usually around 1...3V due to the high doping concentrations. As a result, the breakdown effect in advanced (high-speed) transistors corresponds to a tunnelling mechanism.

The model equation employed in HICUM (cf. [41]) is based on the expression for the tunnelling current density [48]

\[ J_{BEi} = \sqrt{\frac{2m^*/E_G}{q^3}} \exp \left[ -\frac{8\pi \sqrt{2m^*/E_G} E_{BEj}}{3qhE_{BEj}} \right] \cdot \]

(2.1.10-6)

Here \( E_G \) is the bandgap energy, \( m^* \) is the effective electron mass, \( h \) is the Planck constant, and \( V \) is the voltage across the respective BE junction; i.e. \( V=V_{BE} \) for the bottom junction or \( V=V_{B*E} \) for the perimeter junction. \( E_{BEj} \) is the electric field at the junction which - according to the theory of abrupt junctions - can be expressed as

\[ E_{BEj} = 2 \frac{V_{DE} - V}{w_{BE}} \]

(2.1.10-7)

with \( V_{DE} \) as the built-in voltage of the respective junction. \( w_{BE} \) is the space charge region width of that junction and is given by

\[ w_{BE} = w_{BE0}(1 - V/V_{DE})^{z_e} \]

(2.1.10-8)

with the zero-bias value

\[ w_{BE0} = \begin{cases} \frac{\varepsilon_S A_{E0}}{C_{jEi0}} & \text{, bottom junction} \\ \frac{\varepsilon_S P_{E0}(0.8\frac{\pi}{2}x_{je})}{C_{jEp0}} & \text{, perimeter junction} \end{cases} \]

(2.1.10-9)

\( P_{E0} \) and \( A_{E0} \) are the emitter window perimeter and area, respectively, and \( x_{je} \) is the vertical junction depth. \( C_{jEi0} \) and \( C_{jEp0} \) are the zero-bias depletion capacitance of the bottom and perimeter junction, respectively. The factor \( 0.8(\pi/2)x_{je} \) approximates the perimeter junction curvature caused by lateral
outdiffusion of the emitter doping. Inserting (2.1.10-7 to 2.1.10-9) back into (2.1.10-6), defining a normalized voltage \( V_e = V/V_{DE} \), and multiplying with the respective area yields for the tunnelling current

\[
i_{BEt} = I_{BEtS}(-V_e)(1-V_e)^{1-z_E} \exp[-a_{BEt}(1-V_e)^{z_E-1}] .
\]  

(2.1.10-10)

For numerical reasons, the \( 1-V_e \) terms are converted to terms that contain the respective normalized bias dependent depletion capacitance \( C_e = C_{JE}(v)/C_{JE0} \), which has been made numerically stable at \( V_e = 1 \). Using the classical \( C_{JE}(v) \) relationship which is valid at the reverse bias of interest,

\[
(1-V_e)^{1-z_E} = C_e^{1-1/z_E} ,
\]

(2.1.10-11)

leads to the final formulation

\[
i_{BEt} = I_{BEtS}(-V_e)C_e^{1-1/z_E} \exp[-a_{BEt}C_e^{1/z_E-1}] .
\]

(2.1.10-12)

The "saturation" current

\[
I_{BEtS} = \frac{2\sqrt{2m^*/E_G} q^3 V_{DE}^2}{h^2 \varepsilon_{Si}} C_{JE0}
\]

(2.1.10-13)

and the coefficient

\[
a_{BEt} = \frac{8\pi \sqrt{2m^*E_G}E_G}{3qh} \frac{w_{BE0}}{2V_{DE}}
\]

(2.1.10-14)

are model parameters, that depend on physical and process data as well as on geometry. Note that \( i_{BEt} \) is a continuously differentiable expression since the depletion capacitance is continuously differentiable.

In most processes, the breakdown effect occurs first at the peripheral emitter junction, because the doping concentrations are highest there, and due to the curvature of that junction which leads to a narrower space-charge region and, thus, to a higher electric field. In this case, \( C_{JE0}, V_{DE}, z_E, \)
and $V_e$ in the above equations have to be replaced by $C_{jEp0}$, $V_{DEp}$, $z_{Ep}$ and $v_{B^*E'}/V_{DEp}$. However, in most SiGe (and also III-V) processes, the tunnelling occurs at the internal (bottom) BE junction. In this case, $C_{jEi0}$, $V_{DEi}$, $z_{Ei}$ and $v_{B'E'}/V_{DEi}$, respectively, need to be inserted instead. Also, the tunnelling current source in the HICUM equivalent circuit needs to be connected to either the perimeter or internal base node as shown in Fig. 2.1.10/2.

Thus, in order to provide a flexible description within HICUM and, also, to also allow proper geometry scaling, the parameter $TUNODE$ has been introduced that defines the (base) node at which the tunneling current source is supposed to be connected. Note, that the current source has to be connected either to the internal base node ($TUNODE = 0$) or to the perimeter base node ($TUNODE = 1$), but not to both. This modification is downwards compatible to version 2.1.

![Fig. 2.1.10/2: Possible locations of the BE tunnelling current source: $i_{BEL,p}$ or $i_{BEL,i}$.](image)

The above equation is based on a description of band-to-band tunneling, which dominates at reverse bias, and becomes less accurate for a forward biased junction, i.e. if trap-assisted tunneling dominates.
2.1.11 Substrate network

The substrate contact of a transistor may be at the bottom of the wafer only or, more preferably, at the surface. But even the surface contact is usually located relatively far away from the CS junction, so that a significant resistance $r_{Su}$ may exist in series to the CS depletion capacitance, due to the usually quite high substrate resistivity $\rho_{Su}$. In addition, the high permittivity of silicon, $\varepsilon_{Si}$, leads to a capacitance $C_{Su}$ in parallel to $r_{Su}$ that becomes important at high operating speed. Physically, the connection between the substrate contact and the CS depletion capacitance can be partitioned into a bulk (or bottom) and a periphery $RC$ network [21] (cf. also Fig. 2.1.17/4), each of which having the time constant $\tau_{Si}=\rho_{Su}\varepsilon_{Si}$. For practical applications in a compact model, however, a simplified network is employed that combines bottom and periphery components into one $RC$ equivalent circuit (cf. Fig. 2.1.1/1). The values of $r_{Su}$ and $C_{Su}$ are strongly geometry dependent.

Fig. 2.1.11/1 shows the impact of the substrate coupling on the frequency dependent output conductance of a 25GHz process (see also [16]).

![Fig. 2.1.11/1: Impact of intra-device substrate-coupling on transistor output conductance (real part of $y_{22}$) as function of frequency. Comparison of measurements (symbols) and HICUM (lines): (a) model without substrate network $r_{su}$, $C_{su}$; (b) model with substrate network. Emitter size: 0.4*14µm²; bias point: $I_{C}/A_{E}$=0.22 mA/µm², $V_{CE}$=0.8V.](image)
2.1.12 Parasitic substrate transistor

Under certain electrical circumstances, the parasitic substrate transistor can be turned on, depending also upon the processes and layout of the transistor. First of all, one can distinguish between a bulk substrate transistor given by the buried layer area and - dependent on the process - a peripheral substrate transistor. The most likely electrical condition for turning on the substrate transistor is a forward-biased BC junction which occurs either at high current densities under the emitter (internal BC junction) or if the transistor is operated in hard saturation (external and internal BC junction). An example for this are power amplifiers, in which the transistor is operated in hard saturation with $V_{CE} \rightarrow V_{CES}$ and strongly forward biased $V_{BC}$. Another condition for turning on the substrate transistor is a forward biased CS junction caused by voltage drops in the substrate (latch-up).

Since the bulk substrate transistor usually has a current gain of less than 1 due to the highly doped and wide buried layer, its influence is negligible and needs not to be considered at high collector current densities. Device simulations confirmed this for an advanced bipolar process. A peripheral substrate transistor action can be avoided by a surrounding collector sinker with high enough doping concentration at the buried layer depth. Also, this peripheral transistor does not exist at all in trench-isolated processes.

In (npn) transistors without surrounding collector sinker, however, the epitaxial collector acts as a lightly doped base between the external base (now the emitter) and the substrate (now the collector), resulting in a pnp transistor with considerable current gain that may be required to be modelled in addition to the vertical npn transistor. HICUM contains a simplified substrate transistor model in order to take the corresponding effects into account.

The parasitic substrate transistor consists of the elements $i_{TS}$, $i_{SC}$, $C_{JS}$, $i_{BCx}$ and $C_{BCx}$ in the equivalent circuit of Fig. 2.1.1/1. While $C_{JS}$, $i_{BCx}$ and $C_{BCx}$ already belong to the standard HICUM equivalent circuit, a substrate transistor action requires the addition of a substrate transfer current source. Since substrate transistor action is considered as second order effect, a simplified model has been chosen for $i_{TS}$:

$$i_{TS} = I_{TSf} - I_{TSr} = I_{TSS} \left[ \exp\left( \frac{V_{BCx}}{m_S V_T} \right) - \exp\left( \frac{V_{SCx}}{m_{Sr} V_T} \right) \right]$$  (2.1.12-1)
with the saturation current \( I_{TSS} \) and the emission coefficients \( m_{Sf} \) and \( m_{Sr} \) as model parameters. The second term is only relevant if the SC junction becomes forward biased which of little practical importance; therefore, to reduce the number of model parameters, \( m_{Sr} = m_{Sf} \) is assumed.

In case of a forward biased SC junction, also a "base" current component exists, that is modelled by the diode equation:

\[
i_{jSC} = I_{SCS} \left[ \exp\left(\frac{V_{SC}}{m_{SC}V_T}\right) - 1 \right] \quad (2.1.12-2)
\]

with the saturation current \( I_{SCS} \) and the emission coefficient \( m_{SC} \) as model parameters. Although this current (and its derivative) are usually of little practical relevance it is generally useful for simulator convergence.

The minority charge storage in the epitaxial region under the external base is taken into account by a diffusion charge

\[
Q_{dS} = \tau_{Sf} i_{TSf} \quad (2.1.12-3)
\]

with the forward transit time \( \tau_{Sf} \) as a model parameter of the substrate transistor. \( \tau_{Sf} \) depends on the average current path (neutral base width) under the external base and at the buried layer periphery. So far, the classical base transit time expression turned out to be a good approximation for estimating the value of \( \tau_{Sf} \). Also, device simulations have shown that for high-speed processes the stored charge represented by \( Q_{dS} \) has only negligible effect on transistor switching out of hard saturation.

Note, that in advanced bipolar processes the emitter terminal of the substrate transistor (B*) moves towards the (npn) base contact (B), which makes the external realization of such a parasitic transistor by a subcircuit even easier.
2.1.13 Small-signal Equivalent circuit

Fig. 2.1.13/1 shows the small-signal EC, that can be derived from the large-signal EC in Fig. 2.1.1/1. Nonlinear elements that depend on their branch voltage only, such as diodes, have been replaced by their conductances. Nonlinear elements that are controlled by other than their branch voltage, such as transfer current sources and the avalanche current source, are replaced by the respective controlled source and a possible conductance. The latter contains the direct dependence of the nonlinear current source on the branch voltage while the controlled source is designated by a complex current symbol. The respective derivatives for the nonlinear elements can be calculated (e.g. by symbolic tool or the respective simulator used with Verilog) once the currents and charges are available.

The capacitances $C_{BCCx}$, $C_{jEp}$, $C_{jEi}$, $C_{jCi}$ and $C_{jS}$, the parasitic isolation capacitances, and the (bias independent) series resistances have already been defined in the previous sections. From the diode
element current equations, respective conductances $g_{jBEp}$, $g_{jBEi}$, $g_{jBCi}$, $g_{jBCx}$, and $g_{jSC}$ can be found as follows:

$$g_{jn} = \frac{dI_{jn}}{dV_{jn}} \quad (2.1.13-1)$$

with $n = \{BE, BE', BCI, BCx, SC\}$, $V$ and $I$ being the respective branch voltage and diode current.

The conductance of the tunneling and avalanche current elements follow directly from eq. (2.1.10-10) and (2.1.10-2) respectively,

$$g_{BEt} = \frac{dI_{BEt}}{dV} \quad (2.1.13-2)$$

$$g_{AVL, b} = \frac{dI_{AVL}}{dV_{BE'}}_{v_{CE'}} \quad (2.1.13-3)$$

$$g_{AVL, c} = \frac{dI_{AVL}}{dV_{CE'}}_{V_{FE}} \quad (2.1.13-4)$$

The forward transfer $I_{TF}$ current depends on $V_{BE'}$ and $V_{BC'}$ (or $V_{CE'}$) and, therefore, leads to a voltage controlled current source $g_{mV_{BE'}}$ and the output conductance element $g_{o}$. The various conductances of the transfer current that are required for the small-signal equivalent circuit are calculated in HICUM/L2 as follows:

$$S_{jb} = \frac{dI_{TF}}{dV_{BE'}}_{v_{CE'}} \quad (2.1.13-5)$$

The forward component of the output conductance reads

$$S_{fc} = \frac{dI_{TF}}{dV_{CE'}}_{V_{FE}} \quad (2.1.13-6)$$
The corresponding inverse conductances are

\[
S_{rb} = \frac{dI_T}{dV_{BE} V_{CE}} \tag{2.1.13-7}
\]

and

\[
S_{rc} = \frac{dI_T}{dV_{CE} V_{BE}} \tag{2.1.13-8}
\]

From these derivatives follows the transconductance in common-emitter configuration \((dV_{BE}=dV_{BC})\)

\[
g_m = \left. \frac{dI_T}{dV_{BE} V_{CE}} \right|_{V_{CE}} = y_{21}(\omega=0) = S_{fb} + S_{rb} \tag{2.1.13-9}
\]

and the output conductance in common-emitter configuration

\[
g_o = \left. \frac{dI_T}{dV_{CE} V_{BE}} \right|_{V_{BE}} = y_{22}(\omega=0) = -(S_{fc} + S_{rc}) \tag{2.1.13-10}
\]

The resulting small-signal transfer current is then given by

\[
I_T = S_{fb} V_{BE} - S_{rb} V_{BC} \tag{2.1.13-11}
\]

If non-quasi-static effects are included, the transconductance \(S_{fb}\) becomes complex.

Since \(h_{fCl}<1\) for a (positive) bandgap grading in the base, an HBT has a higher Early voltage and lower output conductance than a homojunction transistor. For experimental examples of the bias and frequency dependence of the above conductances see chapter 6.

The transconductances of the parasitic substrate transistor, which is described by a simple transport model, are given by
resulting in the corresponding small-signal transfer current

\[ V_{Ts} = S_{Ts, b} V_{B C} - S_{Ts, s} V_{SC}. \]  

The BE diffusion capacitance is given by

\[ C_{dE} = \tau_f S_f. \]

while the BC diffusion capacitance is approximated by

\[ C_{dC} = \tau_r S_r. \]

The diffusion capacitance of the parasitic substrate transistors reads

\[ C_{dS} = \tau_f S_{Ts, b}. \]

and is connected in parallel to \( C''_{BCx} \).

Although the internal base resistance is bias dependent, the d.c. value is used also for the small-signal case,

\[ r^*_{bi} = r^*_{Bi}. \]

which so far turned out to be a reasonable approximation, while at the same time simplifying the implementation significantly.

If self-heating is turned on, the derivatives of the relevant equivalent circuit element variables with respect to the temperature caused by the dissipated power \( P \) are also taken into account. The most important derivatives are given below; justified simplifications have been made regarding the derivatives of certain components in order to obtain the fairly compact expression.
The derivatives below are defined for constant voltages at the nodes of the electrical equivalent circuit:

\[ S_{fT} = \left. \frac{dI_T}{dT} \right|_V, \]  
(2.1.13-18)

\[ S_{fTav} = \left. \frac{dI_{AVL}}{dT} \right|_V, \]  
(2.1.13-19)

\[ \left. \frac{dP}{dT} \right|_V = S_{pT} = V_{CE}S_{fT} + (V_{DCi} - V_{BC})S_{fTav}. \]  
(2.1.13-20)

In addition, the dissipated power requires derivatives with respect to node voltages, assuming a constant temperature (= voltage at the thermal node):

\[ \left. \frac{dP}{dV_B} \right|_{V, \Delta T} = V_{CE}(S_{fb} - S_{fr}) + [(V_{DCi} - V_{BC})S_{fbav} - I_{AVL}], \]  
(2.1.13-21)

\[ \left. \frac{dP}{dV_C} \right|_{V, \Delta T} = [V_{CE}(S_{fc} - S_{rc}) + I_T] + [(V_{DCi} - V_{BC})S_{fbav} + I_{AVL}]. \]  
(2.1.13-22)
2.1.14 Noise model

The noise behaviour is modelled by employing the small-signal equivalent circuit in Fig. 2.1.13/1 and adding to all series resistances, diodes, and to the transfer current source their corresponding equivalent noise current sources. Compared to the SGPM, the more sophisticated equivalent circuit and more accurate model equations of HICUM/L2 allow a more accurate overall description of the noise behaviour, especially at high frequencies (e.g. [42]).

In ohmic resistances thermal noise is taken into account by an equivalent noise current source

\[
\sqrt{I_r^2} = \frac{4k_B T \Delta f}{r}
\]

(2.1.14-1)

with \( r = r_E, r_C, r_{Be}, \) or \( r_{Bi} \). \( k_B \) is the Boltzmann constant, \( T \) is the device temperature, and \( \Delta f \) is the frequency interval. Investigations have shown that for certain processes a distributed model of the internal base yields an improved description of the high-frequency noise behaviour, which can only be achieved with a multi-transistor model.

Shot noise is assumed for transfer currents, such as

\[
\sqrt{I_T^2} = 2qI_T \Delta f
\]

(2.1.14-2)

as well as for the avalanche current \( I_{AVL} \) and for currents across junctions (diode currents),

\[
\sqrt{I_{diode}^2} = 2qI_{diode} \Delta f
\]

(2.1.14-3)

with the index \( diode = \{BEi, BCI, BEp, BCx, SC\} \). Note that eq. (2.1.14-3) is only a rough approximation.

The base current components injected across the BE junction also contain flicker noise, which depends inversely on the frequency \( f \). Investigations of flicker noise in polysilicon-emitter bipolar transistors seem to indicate that the flicker noise is generated at the poly-silicon to mono-silicon interface [6,7,9]. This corresponds to a strong correlation between the bottom and perimeter component. As a consequence, and for simplification of the noise model and its implementation, the present version contains only one flicker noise source in parallel to \( g_{jBEi} \) that combines the bottom and perimeter current,
with $k_F$ and $a_F$ as model parameters. Deviations from the $1/f$ behaviour, which can be caused by, e.g., random telegraph noise, cannot be taken into account by the employed model.
2.1.15 Temperature dependence

Temperature dependence is described in HICUM via those model parameters that are related to physical quantities like intrinsic carrier density or mobility. In the following formulas, $T_0$ is the reference temperature (e.g. 300K) for which the model parameters have been determined. The validity range of the equations depends somewhat on the technology considered. A more detailed description of the physical background of certain formulas employed in HICUM is given in [32, 33].

In most circuit simulators, though, a linear dependence of bandgap with temperature is assumed only for the saturation currents, which are most sensitive to temperature changes, while for the built-in voltages often a more complicated function $V_G(T)$ is used (e.g. [48]) which is valid down to quite low temperatures. However, since effects such as freeze-out are usually not taken into account by compact models, it is not recommended to use a model below about 250K unless its parameters have been extracted or at least verified especially for that temperature range.

For numerical reasons (over- or underflow), some of the original equations have to be modified, mostly towards extreme temperatures. The respective smoothing functions to be used for circuit simulator implementation are also given below. It is assumed that every circuit simulator prevents negative or zero temperature.

Relative temperature coefficients (TCs) are designated by the symbol $\alpha$ and temperature factors (no unit) are designated by $\zeta$.

2.1.15.1 Temperature dependent bandgap voltage

In order to allow simulations of devices fabricated in different materials and to make the model simulator-independent, a temperature dependent bandgap voltage has been added to the model equations. The formulation suggested in [65] has been selected,

$$ V_g(T) = V_g(0) + K_1 T \ln(T) + K_2 T $$

(2.1.15-1)

due to the following advantages:

- a higher accuracy w.r.t. measured data in the relevant temperature range compared to the classical formulation, and
- compatibility with existing temperature dependent current formulations in compact models that are based on the assumption of a simple linear temperature dependence $V_g(T) = V_{g,cl}(0) - a_g T$, but higher accuracy at the same time.
Note, that in (2.1.15-1) the temperature $T$ decreases faster towards zero than $ln(T)$ increases towards infinity, so that the equation assumes the finite value $V_g(0)$ at $T=0$. The original coefficient values are given in Table 1; the second row contains an improved set of parameters which is more accurate both at low temperatures and with respect to the classical formulation:

\[ V_g(T) = V_{g,cq}(0) - \frac{\alpha_g T^2}{T + T_g} \]  

(2.1.15-2)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>$K_1$ [V/K]</th>
<th>$K_2$ [V/K]</th>
<th>$V_g(0)$ [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[65]</td>
<td>-8.459 $10^{-5}$</td>
<td>3.042 $10^{-4}$</td>
<td>1.1774</td>
</tr>
<tr>
<td>[66]</td>
<td>-1.023 77 $10^{-4}$</td>
<td>4.321 5 $10^{-4}$</td>
<td>1.170</td>
</tr>
</tbody>
</table>

Table 2.1.15/1: Coefficients for calculating the bandgap voltage in silicon as a function of temperature from (2.1.15-1). In the range from 250 to 400K, a smaller error can be obtained by simply setting $V_g(0)=1.1777$V in the original parameter set.

For compact model and application purposes, it is sometimes more convenient to re-write above equation in terms of a reference temperature $T_0$ (e.g. for parameter extraction), which gives

\[ V_g(T) = V_g(T_0) + k_1 \frac{T}{T_0} \ln\left(\frac{T}{T_0}\right) + k_2 \left(\frac{T}{T_0} - 1\right) \]  

(2.1.15-3)

with the definitions

\[ k_1 = K_1 T_0 \quad k_2 = K_2 T_0 + k_1 \ln(T_0) \]  

(2.1.15-4)

and the bandgap voltage at the measurement reference temperature,

\[ V_g(T_0) = k_2 + V_g(0) \]  

(2.1.15-5)

Fig. 2.1.15/1 shows the temperature dependent bandgap voltage according to (2.1.15-1) compared to the most popular conventional formulations.
Fig. 2.1.15/1: Comparison of bandgap voltage approximations. The parameters used for (2.1.15-2) are \( V_g(0) = 1.170 \text{ V} \), \( \alpha_g = 4.73 \times 10^{-4} \text{ V/K} \), \( T_g = 636 \text{ K} \). The parameters for the (at \( T_0 \)) linearized equation are \( V_g(0) = 1.2009 \text{ V} \), \( \alpha_g = 2.5461 \times 10^{-4} \text{ V/K} \).

The choice of the bandgap description also influences the formulation of the effective intrinsic carrier density, which now reads

\[
n_{ie}^2(T) = n_{ie}^2(T_0) \left( \frac{T}{T_0} \right)^{m_g} \exp \left[ \frac{V_{geff}(0)}{V_T} \left( \frac{T}{T_0} - 1 \right) \right]
\]

(2.1.15-6)

with the constant

\[
m_g = 3 - \frac{k_1}{V_{T0}} = 3 - \frac{qK_1}{k_B}
\]

(2.1.15-7)

and \( K_1 \) from the bandgap voltage equation (2.1.15-1). Using the values in Table 2.1.15/1 for Si gives \( m_g = 4.188 \).
2.1.15.2 Transfer current

The transfer current is strongly temperature dependent via the intrinsic carrier density $n_i$. Since the square of $n_i$ is contained in the ICCR constant $c_{10}$, this leads to

$$c_{10}(T) = c_{10}(T_0) \left( \frac{T}{T_0} \right)^{\zeta_{CT}} \exp \left[ \frac{V_{Gb}(T)}{V_T(T)} \left( \frac{T}{T_0} - 1 \right) \right]$$ \hspace{1cm} (2.1.15-8)

The (over the base region) averaged bandgap voltage $V_{Gb}$ and the exponent factor $\zeta_{CT}$ are model parameters and

$$V_T(T) = \frac{k_B T}{q}$$ \hspace{1cm} (2.1.15-9)

is the temperature dependent value of the thermal voltage. Note that, $V_{Gb}$ can assume values smaller than in Table 2.1.15/1 due to high doping effects in the base region.

The zero-bias hole charge $Q_{p0}$ is only weakly temperature dependent via the influence of base width change with temperature, that is mainly caused by the change in depletion width of the BE junction. The temperature dependence can be approximated by the simple expression

$$Q_{p0}(T) = Q_{p0}(T_0) \left[ 2 - \left( \frac{V_{DEi}(T)}{V_{DEi}(T_0)} \right)^{\zeta_{Ei}} \right]$$ \hspace{1cm} (2.1.15-10)

No additional model parameters are required here. Also, the temperature derivative in the code is directly given by the already available derivative $dV_{DEi}/dT$. Also, for typical values of $V_{DEi}$ in the order of $V_{Gb}$ the value of $Q_{p0}$ will remain positive up to extremely high temperatures. Therefore, a smoothing function is omitted here to keep the computational effort minimal, particularly during self-heating calculations.

2.1.15.3 Base (junction) current components

Since in HICUM not the current gain but the physically independent base current is described, the respective saturation currents are modelled as a function of temperature

$$I_{BEIS}(T) = I_{BEIS}(T_0) \left( \frac{T}{T_0} \right)^{\zeta_{BE}} \exp \left[ \frac{V_{gEff}(0)}{V_T} \left( \frac{T}{T_0} - 1 \right) \right]$$ \hspace{1cm} (2.1.15-11)
with the new model parameters $\zeta_{BET}$ and the effective bandgap voltage $V_{gEeff}(0)$ in the emitter, which includes, e.g., high-doping effects. An estimate for $V_{gEeff}(0)$ can be calculated from the known effective bandgap voltage in the base and the measured relative TC $\alpha_{Bf}$ of the current gain:

$$V_{gEeff}(0) = V_{gBeff}(0) - \alpha_{Bf} T_0 \frac{V_T}{T_0} \tag{2.1.15-12}$$

This estimate can be used as default or preliminary value, e.g., when converting the HICUM v2.1 parameter $\alpha_{Bf}$ to $V_{gEeff}(0)$. In HICUM v2.2, $\alpha_{Bf}$ will be phased out as a model parameter in favour of the separate model parameters $\zeta_{BET}$ and $V_{gEeff}(0)$ in an equation form that is the same for all junction components (see below). Although defining the temperature dependence of the current gain at given collector bias current is more useful for circuit design than defining a bandgap voltage from a $V_{BE'} = 0$ extrapolated characteristic, the latter approach will be used in HICUM, starting from version 2.2 on in order to:

- provide a more flexible description of the current gain temperature dependence,
- be consistent with the independent modeling of the bias dependence of the base current components, and
- provide a clear definition of how to extract the corresponding model parameters.

As a consequence, HICUM employs for all junction related current components, except the transfer current, equations of the form

$$I_j = I_{jS} \exp\left(\frac{V}{mV_T}\right) \tag{2.1.15-13}$$

with the generic temperature dependent saturation current formulation

$$I_{jS}(T) = I_{jS}(T_0) \left(\frac{T}{T_0}\right)^{\zeta_T} \exp\left[\frac{V_{g-eff}(0)}{V_T} \left(\frac{T}{T_0} - 1\right)\right] \tag{2.1.15-14}$$

The corresponding variables that are inserted into above equation for each junction component are listed in Table 2. For the BE recombination components, in principle the average value

$$V_{gBBeff} = \frac{V_{gBBeff} + V_{gEeff}}{2} \tag{2.1.15-15}$$
that is already being used for the BE depletion capacitance components, should be inserted. However, since it is questionable whether the additional arithmetic operations are justified, the same parameters as for the back injection components are used.

<table>
<thead>
<tr>
<th>component</th>
<th>$V$</th>
<th>$I_s$</th>
<th>$m$</th>
<th>$V_{\text{geff}}$</th>
<th>$\zeta_T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{jBEi}$</td>
<td>$V_{B'E'}$</td>
<td>$I_{BEiS}$</td>
<td>$m_{BEi}$</td>
<td>$V_{gEi}$</td>
<td>$\zeta_{BET}$</td>
</tr>
<tr>
<td>$I_{jBEp}$</td>
<td>$V_{B*E'}$</td>
<td>$I_{BEpS}$</td>
<td>$m_{BEp}$</td>
<td>$V_{gEi}$</td>
<td>$\zeta_{BET}$</td>
</tr>
<tr>
<td>$I_{jREi}$</td>
<td>$V_{B'E'}$</td>
<td>$I_{REiS}$</td>
<td>$m_{REi}$</td>
<td>$V_{gEi}$</td>
<td>$\zeta_{BET}$</td>
</tr>
<tr>
<td>$I_{jREp}$</td>
<td>$V_{B*E'}$</td>
<td>$I_{REpS}$</td>
<td>$m_{REp}$</td>
<td>$V_{gEi}$</td>
<td>$\zeta_{BET}$</td>
</tr>
<tr>
<td>$I_{jBCi}$</td>
<td>$V_{B'C'}$</td>
<td>$I_{BCiS}$</td>
<td>$m_{BCi}$</td>
<td>$V_{gEi}$</td>
<td>$\zeta_{BCiT}$</td>
</tr>
<tr>
<td>$I_{jBCx}$</td>
<td>$V_{B*C'}$</td>
<td>$I_{BCxS}$</td>
<td>$m_{BCx}$</td>
<td>$V_{gEi}$</td>
<td>$\zeta_{BCxT}$</td>
</tr>
<tr>
<td>$I_{jSC}$</td>
<td>$V_{SC'}$</td>
<td>$I_{SCS}$</td>
<td>$m_{SC}$</td>
<td>$V_{gEi}$</td>
<td>$\zeta_{SC}$</td>
</tr>
</tbody>
</table>

Table 2.1.15/2: Junction current components and their corresponding parameters and controlling voltages

Commercially implemented SGP models contain the components $I_{jBEi}$, $I_{jBCi}$ (or $I_{jBCx}$) and $I_{jSC}$. In some variants, each of these components is assigned a different set ($V_{\text{geff}}, \zeta_T$) of parameters. Extending this to the additional components in HICUM would increase the number of parameters without significantly increasing accuracy and flexibility, or in other words: it is questionable from a practical application point of view for a compact model whether introducing separate model parameters for those base current components, that are of little importance for circuit design makes sense. Therefore, to keep the model as simple as possible (in terms of parameter determination), currents associated with same regions have been assigned the same parameters in Table 2. Furthermore, since the mobility exponent factor $\zeta_{Ci}$ of the internal collector region, defined by

$$
\mu_{Ci}(T) = \mu_{Ci}(T_0) \left( \frac{T}{T_0} \right)^{-\zeta_{Ci}}
$$

(2.1.15-16)
is already available as a model parameter, the respective exponent factor for $I_{jBCi}$ can be expressed as

$$\zeta_{BCiT} = m_g + 1 - \zeta_{Ci} \quad (2.1.15-17)$$

with $m_g$ from (2.1.15-7). Hence, $\zeta_{BCiT}$ does not need to be added as model parameter and is calculated internally. Similarly, the factor for the external collector current $I_{jBCx}$ reads

$$\zeta_{BCxT} = m_g + 1 - \zeta_{Cx} \quad (2.1.15-18)$$

with the mobility factor $\zeta_{Cx}$ of the external collector (epi-)region that is also being used for modeling the temperature dependence of the minority storage time of the parasitic substrate transistor.

Since the substrate doping is fairly low, the mobility exponent factor $\zeta_{\mu pS} = 2.5$ can be assumed as a good approximation, yielding

$$\zeta_{SCT} = m_g + 1 - \zeta_{\mu pS} \quad (2.1.15-19)$$

leaving the bandgap voltages as the only new model parameters for these regions. For silicon, the values of the above constants are: $m_g = 4.188$, $\zeta_{BCT} = 5.188 - \zeta_{Ci}$, $\zeta_{SCT} = 2.69$.

### 2.1.15.4 Transit time and minority charge

The critical current density $I_{CK}/A_E$ depends on temperature via physical parameters like mobility of the epitaxial collector and saturation velocity. The internal collector resistance contains the low-field electron mobility and reads

$$r_{CI}(T) = r_{CI}(T_0) \left( \frac{T}{T_0} \right)^{\zeta_{Ci}}. \quad (2.1.15-20)$$

The model parameter $\zeta_{Ci}$ is a function of the collector doping concentration (e.g., [32, 43]). The voltage $V_{lim}$ contains both collector mobility and saturation velocity,

$$V_{lim}(T) = \frac{v_s(T)}{\mu_{nC_i}(T)}. \quad (2.1.15-21)$$
According to [67], experimental results of the saturation velocity for \( T \geq 250\text{K} \) can be approximated by

\[
v_s(T) = v_{s0}(T_0)
\left(\frac{T}{T_0}\right)^{-a_{vs}}
\tag{2.1.15-22}
\]

with \( T_0 = 300\text{K} \), \( v_s(T_0) = 1.071 \times 10^7 \text{ cm/s} \) and \( a_{vs} = 0.87 \). The relation between \( a_{vs} \) and the existing HICUM model parameter \( a_{vs} \), which is the relative TC, can be calculated from the derivative of (2.5.3-2) at \( T_0 \) and is given by

\[
a_{vs} = a_{vs}T_0
\tag{2.1.15-23}
\]

The voltage \( V_{lim} \) contains both mobility and saturation velocity, resulting in

\[
V_{lim}(T) = V_{lim}(T_0)
\left(\frac{T}{T_0}\right)^{-a_{vs}}
\tag{2.1.15-24}
\]

which is simple and numerically stable, and does not require any additional model parameters. The equation is valid up to about 600K, which is the highest temperature of available experimental data for mobility and saturation velocity.

The CE saturation voltage can be modelled as a linear function of temperature,

\[
V_{CES}(T) = V_{CES}(T_0)[1 + \alpha_{CES}\Delta T]
, \tag{2.1.15-25}
\]

with \( \alpha_{CES} \) as a model parameter. Its value can be estimated from the difference between the respective relative temperature coefficients of the built-in voltages \( V_{DEi} \) and \( V_{DCi} \).

The temperature dependence of the transit time model is given in [43]. Except for the low-current transit time, no additional model parameters are required. The low-current portion of the transit time, \( \tau_f0 \), as a function of temperature is mainly determined by the quadratic temperature dependence of the parameter \( \tau_0 \):
The model parameters $\alpha_{0}$ and $k_{r0}$ can be expressed by physical quantities.

The time constants $\tau_{Bf}$ and $\tau_{pCs}$ depend on temperature via the same diffusivity (of the collector) and, therefore, the temperature dependence of the composite parameter $\tau_{hcs}$ can be expressed as

$$
\tau_{hcs}(T) = \tau_{hcs}(T_0) \left( \frac{T}{T_0} \right)^{(\zeta_{c} - 1)}. 
$$

(2.1.15-27)

The emitter time constant $\tau_{Ef0}$ depends on temperature via mainly the hole diffusivity in the neutral emitter and the current gain. Assuming a large emitter concentration with a negligible temperature dependence of the mobility (exponent coefficient $\approx 0.5$), the following expression can be obtained:

$$
\tau_{Ef0}(T) \approx \tau_{Ef0}(T_0) \left( \frac{T}{T_0} \right)^{\zeta_{e}^{\text{eff}}} \exp \left[ -\frac{\Delta V_{\text{geff}}(0)}{V_{T}} \left( \frac{T}{T_0} - 1 \right) \right].
$$

(2.1.15-28)

which is also numerically stable for all temperatures. Furthermore, above equation does not require any additional model parameters, since the bandgap difference (between base and emitter region) and exponent coefficient can be calculated from already existing model parameters,

$$
\Delta V_{\text{geff}}(0) = V_{g\text{Beff}}(0) - V_{g\text{Eeff}}(0)
$$

(2.1.15-29)

and

$$
\zeta_{\text{rEf}} = \zeta_{\text{BET}} - \zeta_{\text{CT}} - 0.5
$$

(2.1.15-30)

The temperature dependence of the minority charge and of the additional delay times, that model vertical NQS effects, follows automatically from that of the transit time using (2.1.3-2) and (2.1.9-1), respectively.
2.1.15.5 Temperature dependence of built-in voltages

In order to avoid the built-in voltages becoming negative at high temperatures, an empirical smoothing function was included in v2.1. This function has been replaced in v2.2 by a physics-based formulation, that can be derived from the behavior of the intrinsic carrier density at high temperatures [8].

At first, an auxiliary voltage is calculated at the reference temperature from the model parameter $V_D$ given at the reference (or nominal) temperature $T_0$

$$V_{Dj}(T_0) = 2V_{T0}\ln\left[\exp\left(\frac{V_D(T_0)}{2V_{T0}}\right) - \exp\left(-\frac{V_D(T_0)}{2V_{T0}}\right)\right] \tag{2.1.15-31}$$

with the thermal voltage $V_{T0} = k_BT_0/q$. Then, the respective value at the actual temperature is calculated using the temperature dependent effective bandgap voltage of the respective junction, resulting in

$$V_{Dj}(T) = V_{Dj}(T_0)\frac{T}{T_0} - 3V_T\ln\left(\frac{T}{T_0}\right) + V_{geff}(T) - V_{geff}(T_0)\frac{T}{T_0} \tag{2.1.15-32}$$

For the bandgap voltage formulation (2.1.15-1), above equation reads

$$V_{Dj}(T) = V_{Dj}(T_0)\left(\frac{T}{T_0}\right) - m_gV_T\ln\left(\frac{T}{T_0}\right) - V_{geff}(0)\left(\frac{T}{T_0} - 1\right) \tag{2.1.15-33}$$

which reduces to the classical equation (that assumes a linear temperature dependence of $V_{geff}$) if $m_g = 3$. Finally, the new built-in voltage is calculated as

$$V_D(T) = V_{Dj}(T) + 2V_T\ln\left(\frac{1}{2}\left[1 + \sqrt{1 + 4\exp\left(\frac{V_{Dj}(T)}{V_T}\right)}\right]\right) \tag{2.1.15-34}$$

Since $V_D$ is associated with the junction region, an average effective value is used for $V_g$, which is given by, e.g.,
\[ V_{g \text{eff}} \rightarrow V_{g(x,y) \text{eff}} = \frac{V_{g \text{eff}} + V_{g \text{eff}}}{2} \]  
\( (2.1.15-35) \)

with \((x,y) = (B,E), (B,C), (C,S)\).

For electro-thermal simulations as well as for calculating the temperature coefficient of \(Q_{p0}(T)\), the temperature derivative of the built-in voltage at the (parameter) reference temperature is required. In the code, the full expression for \(dV_D/dT\) as derived from (2.1.15-34) is used. However, since for \(Q_{p0}(T)\) only its value at the reference (extraction) temperature \(T_0\) is needed, the following expression can be used for parameter extraction:

\[ \left. \frac{dV_D(T)}{dT} \right|_{T_0} \approx \left. \frac{dV_{Dj}(T)}{dT} \right|_{T_0} \]  
\( (2.1.15-36) \)

Using the expression (2.1.15-1) for the bandgap voltage gives

\[ \left. \frac{dV_{Dj}(T)}{dT} \right|_{T_0} = \frac{V_{Dj}(T_0) - V_{g \text{eff}}(0) - m_g V_{T0}}{T_0} \]  
\( (2.1.15-37) \)

### 2.1.15.6 Depletion charges and capacitances

The key parameter for the temperature dependence of the depletion charges and capacitances is the diffusion (or built-in) voltage, temperature dependence of which is formulated in the previous section.

The zero-bias junction capacitance can be expressed generally as \(C_{j0} \sim V_D^{-z}\) so that its temperature dependence can be directly calculated from that of \(V_D\):

\[ C_{j0}(T) = C_{j0}(T_0) \left( \frac{V_D(T_0)}{V_D(T)} \right)^z. \]  
\( (2.1.15-38) \)

The temperature dependence of the depletion charge follows automatically from (2.1.4-1) by applying the above formulas and assuming that the exponent-factor \(z\) does not depend on temperature.

The parameter \(\alpha_j\) determining the maximum value of a depletion capacitance at forward bias decreases with increasing temperature and is (empirically) modified as follows:
As can be seen in Fig. 2.1.15/2, the zero-bias capacitance increases, while the voltage at the maximum and the maximum itself decrease with increasing temperature.

The parameter $C_{BE_{par}}$, $f_{BE_{par}}$ and $f_{BC_{par}}$ do not depend on temperature.

Fig. 2.1.15/2: Temperature dependence of the base-emitter depletion capacitance, normalized to its zero-bias value at 300K, vs. normalized applied voltage: comparison between 1D device simulation (symbols) and model equation (lines). The curves are for the temperatures $T/K = 300 (o)$, $350 (*)$, $400 (+)$.

2.1.15.7 Series resistances

The internal base resistance depends on temperature mainly via the mobility in the neutral base region, which is contained in the internal base sheet resistance. Thus, the zero-bias resistance is described as

$$r_{Bi0}(T) = r_{Bi0}(T_0) \left( \frac{T}{T_0} \right)^{\zeta_{rBi}}.$$  \hspace{1cm} (2.1.15-40)

The model parameter $\zeta_{rBi}$ is a function of the (average) base doping concentration (cf. $r_{Cl0}(T)$). Conductivity modulation and emitter current crowding in $r_{Bi}$ are automatically described as a func-
tion of $T$ by the corresponding charges and currents. The shunt capacitance $C_{rBi}$ is temperature dependent via the capacitances of the internal transistor.

External base resistance $r_{Bx}$, external collector resistance $r_{Cx}$, and emitter series resistance follow a similar relationship as $r_{Bi0}$. This requires the model parameters $\zeta_{rBx}$, $\zeta_{rCx}$ and $\zeta_{rE}$ which are a function of the (average) doping concentrations within the corresponding regions.

Fig. 2.1.15/3 shows the various types of temperature dependence that can be modelled with the above equation.

The temperature dependence of the substrate coupling resistance $r_{su}$ is presently not modeled but can easily be included employing the same formulation as (2.1.15-40) and the mobility factor $\zeta_{rsu} = 2.5$.

Fig. 2.1.15/3: Normalized resistance as a function of temperature according to eq. (2.1.15-40) for different values of $\zeta (= \zeta_{Cir}, \zeta_{rBi}, \zeta_{rBx}, \zeta_{rCx} \text{ or } \zeta_{rE})$ as parameter.
2.1.15.8 Breakdown

A. Base-collector junction (avalanche effect)

The temperature dependence of the coefficients describing avalanche breakdown can be described as [19]

\[ a_n(T) = a_n(T_0) \exp(\alpha_{na} \Delta T), \quad (2.1.15-41) \]

\[ b_n(T) = b_n(T_0) \exp(\alpha_{nb} \Delta T) \quad (2.1.15-42) \]

with \( \Delta T = T - T_0 \) and the temperature coefficients \( \alpha_{na} \) and \( \alpha_{nb} \). Insertion of these equations into (2.1.10-3,4) gives for the model parameters

\[ f_{AVL}(T) = f_{AVL}(T_0) \exp(\alpha_{fav} \Delta T) \quad \text{and} \quad q_{AVL}(T) = q_{AVL}(T_0) \exp(\alpha_{qav} \Delta T) \quad (2.1.15-43) \]

with the temperature coefficients \( \alpha_{fav} = \alpha_{na} - \alpha_{nb} \) and \( \alpha_{qav} = \alpha_{nb} \) which are considered as model parameters. According to a more recent study in [17], the temperature dependence of the parameter \( a_n \) is negligible while only \( b_n \) varies slightly with temperature. Therefore, the exp-function reduces to (or can be approximated by) its first series terms, i.e. \( \exp(\alpha_{nb} \Delta T) \approx 1 + \alpha_{nb} \Delta T \).

B. Base-emitter junction (tunnelling effect)

The temperature dependence of the parameters describing BE tunnelling is mainly determined by the bandgap’s temperature dependence. The saturation current is then given by [41]

\[ I_{BEiS}(T) = I_{BEiS}(T_0) \left[ \frac{V_G(T_0)}{V_G(T)} \left( \frac{V_{DE}(T)}{V_{DE}(T_0)} \right)^2 \frac{C_{jE0}(T)}{C_{jE0}(T_0)} \right]. \quad (2.1.15-44) \]

The exponent-coefficient as a function of temperature reads:

\[ a_{BEi}(T) = a_{BEi}(T_0) \left( \frac{V_g(T)}{V_g(T_0)} \right)^{3/2} \frac{V_{DE}(T_0)}{V_{DE}(T)} \frac{C_{jE0}(T)}{C_{jE0}(T)} \quad (2.1.15-45) \]

where either internal or perimeter related parameters have to be inserted for \( V_{DE} \) and \( C_{jE0} \) according to the node assignment of the tunnelling current source.
In the above equations, no additional model parameters are required since the model internal band-gap voltage (cf. eq. (2.1.15-1)) can be used. Employing the model internal band-gap voltage also enables the evaluation of the above parameters for different materials. Since the tunneling current is associated with the BE junction region, physically the bandgap voltage corresponds to the average value of the base and emitter bandgap voltage,

\[ V_g(T) = V_{gBE_{eff}}(T) = \frac{V_{gBE_{eff}}(T) + V_{gE_{eff}}(T)}{2} \]  
(2.1.15-46)

which is already available from the calculation of the BE depletion capacitance and junction saturation current component. However, only the ratio of the bandgap voltages enters the equations (2.1.15-44) and (2.1.15-45).

2.1.15.9 Parasitic substrate transistor

The temperature dependence of the transfer current of the parasitic substrate transistor is given by

\[ I_{TS}(T) = I_{TSS}(T_0) \left( \frac{T}{T_0} \right)^{\zeta_{BCx,T}} \exp \left[ \frac{V_{gCE_{eff}}(0)}{V_T} \left( \frac{T}{T_0} - 1 \right) \right] \]  
(2.1.15-47)

with the factor \( \zeta_{BCx,T} \) from (2.1.5-18).

In section 2.1.15-3, one can get the temperature dependence of the current across CS junction

The transit time of the parasitic substrate transistor is described as a function of temperature similar to (2.1.15-27),

\[ \tau_{Sf}(T) = \tau_{Sf}(T_0) \left( \frac{T}{T_0} \right)^{(\zeta_{Cx}-1)} \]  
(2.1.15-48)

with the temperature factor \( \zeta_{Cx} \) as additional model parameter, that can be determined from the mobility in the external collector region.

Note, that substrate transistor action can generally be avoided by a surrounding collector sinker.
2.1.16 Self-heating

The increase of the transistor's "junction" temperature \( T_j \) caused by self-heating is calculated using a thermal network as shown in Fig. 2.1.1/1b. The current source corresponds to the power dissipated in the device, and the node voltage corresponds to the junction temperature. The calculation requires the thermal resistance, \( R_{th} \), and thermal capacitance, \( C_{th} \), (of the particular transistor) as model parameters. The thermal network is solved together with each transistor model (provided \( R_{th}>0 \) and FLUSH (model parameter used as a flag for self-heating calculation)=1) for d.c. and transient operation. The node voltage is passed on to the model routine in order to calculate the temperature dependent model parameters.

The power is generally calculated from all relevant dissipative elements in the equivalent circuit, excluding any energy storage elements. However, since on one hand the accuracy of the single-pole network and, in particular, of the determination (and geometry scaling) of \( R_{th} \) and \( C_{th} \) are fairly limited, and on the other hand the consideration of all dissipative elements generates elaborate expressions for the derivatives in the Jacobian, only the most relevant dissipative elements are included in the power calculation:

\[
P = I_T V_C E' + I_{AVL}(V_{DCI} V_B C').
\]  

(2.1.16-1)

The purpose of this measure is to reduce the computational effort without sacrificing convergence.

Note that only self-heating is presently taken into account but not the thermal coupling between different devices on the chip, which is a much more complicated topic and does not belong directly into a transistor model formulation. However, the already existing temperature node of the model can be used for modelling thermal coupling in a circuit, like in HICUM/L4 [59].
2.1.17 Lateral scaling

This chapter contains a brief description of the geometry scaling used for HICUM in order to explain the general idea. An extensive set of scaling formulas for a variety of technologies is implemented in the program TRADICA [44] which is used to generate model parameters for a given transistor configuration (cf. chapter 4). The description of the full set of lateral scaling equations is beyond the scope of this text. Note, that due to many different processes the geometry scaling of bipolar transistors is generally much more complicated than for MOS transistors. However, during TRADICA’s use over more than 15 years, a quite general way of geometry scaling has been developed, that has proved to be applicable to a large variety of processes.

2.1.17.1 Transfer current

The geometry dependence of the parameters of the transfer current is given by the proportionality

\[ c_{10} \sim A_E^2, \quad Q_{p0} \sim A_E, \quad I_{Ch} \sim A_E \]

with \( A_E \) as the effective emitter area which is defined in [24, 40].

2.1.17.2 Base current components

The base current components can be split into a bottom and a periphery contribution. For the BE junction, the bottom component is scaled proportional to the effective emitter area. As a consequence, the periphery component has to be corrected by the amount of current already taken into account by widening the emitter to an effective area in order to keep the total BE base current same.

The base current across the internal base collector junction is scaled with the effective emitter area, while the current across the external BC junction is scaled with the external BC area minus the effective emitter area.

2.1.17.3 Minority charge and transit times

The formulas given in Chapter 2.1.3 for \( \tau_{f0}, \Delta \tau_{fh} \) and the corresponding charge \( Q_f \) were derived from one-dimensional (1D) considerations and can be employed if transistors with a fixed emitter width \( b_E \) are used, which is assumed to be much smaller than the emitter length \( l_E \). However, for
narrow or short emitter stripes, 2D and 3D effects occur that will result in less physical values for some of the parameters (such as $r_{Ci0}$) as well as in different “shapes” of the bias dependence of the transit time. Furthermore, if variable emitter widths and lengths down to the minimum allowed dimensions have to be modelled, the 1D equations would require a different set of model parameters for every size or at least for a certain set of sizes (“binning”). As a consequence, a scalable transit time model is preferred which is given below [40].

A. Low current densities

The transit time at low current densities can be expressed as a function of emitter dimensions through its model parameter

$$
\tau_0 = \tau_{f0i} \frac{1 + \left(\tau_{f0p}/\tau_{f0i}\right) \gamma C P_{E0}/A_{E0}}{1 + \gamma C P_{E0}/A_{E0}} = \tau_{f0i} f_{Ql}
$$

(2.1.17-1)

with $P_{E0}$ and $A_{E0}$, respectively, as emitter window perimeter-length and area, respectively. The transit time $\tau_{f0i}$ of the bottom transistor as well as the ratio of the transit time of the peripheral transistor to that of the bottom transistor, $\tau_{f0p}/\tau_{f0i}$, are TRADICA input parameters.

![Normalized low-current transit time as a function of emitter geometry for various ratios of $\tau_{f0p}/\tau_{f0i}$. Model parameter used: $\gamma C=0.05\mu m$.](image)

Fig. 2.1.17/1: Normalized low-current transit time as a function of emitter geometry for various ratios of $\tau_{f0p}/\tau_{f0i}$. Model parameter used: $\gamma C=0.05\mu m$. 
B. Critical current (density)

Collector current spreading leads to a lower effective current density and, as a result, a larger critical current density than the one scaled by the emitter area only. This can be described by

\[ I_{CK} = I_{CK,1D} f_{cs} \]  \hspace{1cm} (2.1.17-2)

with the collector current spreading factor

\[ f_{cs} = \begin{cases} \frac{\zeta_b - \zeta_l}{\ln[(1 + \zeta_b)/(1 + \zeta_l)]}, & l_{E0} > b_{E0} \quad (\zeta_b > \zeta_l) \\ 1 + \zeta_b, & l_{E0} = b_{E0} \quad (\zeta_l = \zeta_b) \end{cases} \]  \hspace{1cm} (2.1.17-3)

which becomes larger than 1 if current spreading occurs. The new model parameters that also determine the bias dependent lateral scaling (see below) are

\[ \zeta_b = 2 \frac{w_C}{b_E} \tan \delta_C \quad \text{and} \quad \zeta_l = 2 \frac{w_C}{l_E} \tan \delta_C \]  \hspace{1cm} (2.1.17-4)

They depend on the collector current spreading angle \( \delta_C \) which is a TRADICA parameter. The corresponding HICUM model parameters names are \( LATB \) (= \( \zeta_b \)) and \( LATL \) (= \( \zeta_l \)). Since the factor \( f_{cs} \) can be incorporated into the model parameter \( r_{Cj0} \) (cf. eq. (2.1.3-9)), it does not appear as additional parameter for HICUM. Fig. 2.1.17/2 shows the factor \( f_{cs} \) as a function of various parameters.
Fig. 2.172: Collector current spreading factor vs current spreading angle and ratio of emitter width to length, respectively, for a variety of parameters; upper left: emitter aspect ratio variation; upper right: variation of epi to emitter width for a long stripe transistor; lower left: same a before, but for a short transistor; lower right: variation of angle (in degrees).

C. High current densities

If the transistor enters the high-current region, minority charge is stored in the collector within the injection zone $w_i$ which is strongly bias dependent. This width also depends on the collector current spreading angle and can be calculated in normalized from as

$$\frac{w_i}{w_C} = \begin{cases} \frac{\kappa - 1}{\zeta_l - \kappa \zeta_b} , & l_{E0} > b_{E0} \\ \frac{1}{\zeta_b \left[ \frac{1 + \zeta_b}{1 + i_{ck} \zeta_b} - 1 \right]} , & l_{E0} = b_{E0} \end{cases}$$

(2.175)
and the normalized current

\[
\kappa = \frac{1 + \zeta_l}{1 + \zeta_b} \exp \left[ i_{ck} \ln \left( \frac{1 + \zeta_b}{1 + \zeta_l} \right) \right] = \left( \frac{1 + \zeta_b}{1 + \zeta_l} \right)^{i_{ck} - 1}
\]  

(2.1.17-6)

Fig. 2.1.17/3 shows the normalized injection width as a function of normalized (forward) collector current with the current spreading angle \( \delta_C \) as a parameter. \( \delta_C = 0 \) corresponds to the 1D case; with increasing spreading angle, the current density in the collector is reduced and, therefore, the extension of the injection width decreases relative to the 1D case. Compared to long transistors (Fig. (a)), which correspond to the 2D case with \( l_E >> b_E \), the impact of current spreading is smaller than for a square-emitter transistor (Fig. (b)), since in the latter current spreading in all four lateral directions becomes significant.

\[
i_{ck} = 1 - \frac{i + \sqrt{i^2 + a_{hc}}}{1 + \sqrt{1 + a_{hc}}} \quad \text{with} \quad i = 1 - \frac{I_{CK}}{I_{T_f}}
\]  

(2.1.17-7)

Fig. 2.1.17/3: Normalized injection width as a function of normalized (forward) collector current for various current spreading angles \( \delta_C \): (a) long emitter \( l_E >> b_E \); (b) square-emitter \( l_E = b_E \). Parameters: \( w_C/b_E = 1, a_{hc} = 0.05, w_C/l_E = 0.01 \) for (a) and \( w_C/l_E = 1 \) for (b).

Also, the equations for \( \tau_{fC} \) and \( Q_{fC} \) have to be extended in order to be able to describe the bias dependence of the occurring 2D and 3D current spreading effects [40]:

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with \( \tau_{pCS} = f_{\text{thc}} \tau_{\text{hcs}} \), and the auxiliary (bias dependent) functions

\[
QC_f = \tau_{pCS} I_T f \left\{ \frac{f_{Cl} \ln \left( \frac{1 + \zeta_b w}{1 + \zeta_l w} \right)}{2} - f_{Cb} + f_{Cl} \right\}, \quad I_{E0} > b_{E0} \tag{2.1.17-8}
\]

\[
QC_f = f_{Cl} \left( \frac{1 - \zeta_l}{1 - \zeta_b} \right) \left[ \frac{x^2 \ln x - 1}{4} + \frac{1}{1 - \zeta_b \zeta_l} \frac{x^3 \ln x - 1}{9} + \frac{\zeta_l}{w^3} \right], \quad I_{E0} = b_{E0} \tag{2.1.17-9}
\]

\[
f_{Cl} = w + \frac{\zeta_b + \zeta_l}{2} w^2 + \frac{\zeta_b \zeta_l}{3} w^3,
\]

\[
f_{Cb} = \frac{1}{\zeta_b} \left( 1 - \zeta_l \right) \left[ \frac{x^2 \ln x - 1}{4} + \frac{1}{\zeta_b \zeta_l} \frac{x^3 \ln x - 1}{9} \right] + \frac{\zeta_l}{w^3} \right], \quad I_{E0} = b_{E0} = \frac{1}{\zeta_b} \left( 1 - \zeta_l \right) \left[ \frac{x^2 \ln x - 1}{4} + \frac{1}{\zeta_b \zeta_l} \frac{x^3 \ln x - 1}{9} \right] + \frac{\zeta_l}{w^3} \right],
\]

with \( x = 1 + \zeta_b w \) and

\[
f_{Cl} = f_{Cb} (\zeta_b \leftrightarrow \zeta_l), \quad \tag{2.1.17-10}
\]

i.e. \( f_{Cl} \) has the same form as \( f_{Cb} \) but with \( \zeta_b \) and \( \zeta_l \) interchanged.

In the implementation of these equations, potential divisions by zero, that could occur for \( \zeta_b = 0 \) or \( \zeta_l = 0 \) or \( \zeta_b = \zeta_l = 0 \) (1D case), have been taken into account by appropriate series expansions, which then also include the 1D theory described before. For the 2D/3D case discussed above, the transit time is calculated as:

\[
\tau_{Cf} = \frac{dQ_{Cf}}{dI_T} \bigg|_{V_{CE}}.
\]

The base charge component at high current densities, \( \Delta Q_{Bf} \), is still calculated without current spreading, using the saturation storage time \( \tau_{Bf_{0s}} = \tau_{\text{hcs}}(1-f_{\text{thc}}) \) and the analytical expression of the corresponding transit time \( \Delta \tau_{Bf} \), while in (2.1.17-8) \( \tau_{pCS} = f_{\text{thc}} \tau_{\text{hcs}} \).
2.1.17.4 Depletion charges and capacitances

Internal capacitances and charges are scaled with the effective emitter area.

Scaling of external capacitances and charges depends on their physical origin:

- The geometry dependent peripheral BE depletion capacitance is calculated from the difference between the total and “effective” internal BE capacitance.
- The various components of the external BC depletion capacitance are calculated from the corresponding capacitance per area or perimeter (“specific” values) times the respective area or perimeter, with the latter one including corner contributions as well.
- The CS capacitance components are calculated from their respective specific values and the buried layer bottom area as well as from the dimensions of the peripheral substrate junction. Fig. 2.1.17/4 shows the various components that contribute to the peripheral CS depletion capacitance of a junction isolated bipolar transistor.

Also, BC and CS capacitance values can be predicted by TRADICA based on collector doping and specific substrate resistance.

![Fig. 2.1.17/4: Process variants of the CS junction, including components for modelling the depletion capacitance and intra-device substrate coupling.](image-url)
2.1.17.5 Series resistances

The series resistances of a bipolar transistor depend strongly on geometry and contact configuration of the respective transistor. The geometry scaling of the internal and external base resistance is described in [27, 34, 35]. The model parameter $f_{\text{geo}}$ occurring in the current crowding factor is given by

$$f_{\text{geo}} = \frac{1}{g_i g_\eta} \quad \text{(2.1.17-13)}$$

in which the geometry functions

$$g_\eta = 18.3 - \left[ 12.2 \frac{b_E}{l_E} - 19.6 \left( \frac{b_E}{l_E} \right)^2 \right] \quad \text{and} \quad g_i = \frac{1}{12} \left( \frac{1}{12} - \frac{1}{28.6} \right) \frac{b_E}{l_E} \quad \text{(2.1.17-14)}$$

depend on the emitter dimensions only and describe a smooth transition from long to short emitter windows. The variable $f_{Qi}$ in (2.1.6-11) is given by (2.1.17-1).

The external series resistances $r_E$ and $r_{Cx}$ can be calculated by TRADICA from specific resistances, sheet resistances and design rules, taking into account various transistor configurations. This method, which allows an independent determination of series resistances, is believed to be more accurate and flexible than (“direct”) extraction from measurements since reliable methods for measuring these resistances do not exist. Most measurement methods are either applicable to a particular process, a certain bias range, or a certain transistor operation (d.c. or small-signal), and validity limits are often unknown or difficult to assess.

2.1.17.6 Breakdown

The avalanche effect formulation contains only $q_{\text{AVL}}$ as directly area-dependent parameter, besides variables such as transfer current and the internal BC capacitance, scaling of which is already being taken care of.

Under the assumption that in a modern bipolar transistor tunnelling occurs at the emitter periphery junction, the geometry dependence is given by the perimeter $P_E$ of the emitter.
2.1.17.7 Parasitic substrate transistor

Since it is assumed that for most bipolar processes the substrate transistor is determined by its peripheral component, all current related parameters are presently scaled by the CS perimeter length. The CS depletion capacitance was already discussed before. The transit time scales vertically with the distance between the epi-substrate and the BC junction.

2.1.17.8 Self-heating

The most simple scaling of \( R_{th} \) and \( C_{th} \) with the effective emitter dimensions is as follows,

\[
R_{th} = r_{th} f_{th} \quad \text{and} \quad C_{th} = c_{th} / f_{th} ,
\]

(2.1.17-15)

with the geometry function \([12]\)

\[
f_{th} = \frac{\ln(4l_E/b_E)}{l_E} .
\]

(2.1.17-16)

\( r_{th} \) and \( c_{th} \) are TRADICA parameters, that are defined for a reference structure with \( b_{E,ref} \) and \( l_{E,ref} \). This scaling rule is certainly a rough approximation and has to be verified for a given process.

Fig. 2.1.17/5 shows the dependence of the thermal resistance on emitter width for constant emitter length. The variation is quite small and could also be described by a simple linear function. More measurement results are needed to establish a reliable geometry scaling rule for the thermal elements.
Fig. 2.1.17/5: Thermal resistance as a function of emitter width at constant emitter length: comparison between measurements (symbols) and analytical equation (line).

2.1.17.9 (Low-frequency) noise

Presently the low frequency flicker noise is modeled by the T-independent factors $AF$ and $KF$. The T-dependence is modeled by other existing parameters.
3 Parameters

This chapter contains a reference list of model parameters with a brief description. The provided default values should be used for model implementation in a circuit simulator; with these values, all but the absolutely necessary functions, that define a bipolar transistor, are turned off. This way, the user only needs to specify the parameters for those effects that are desired to be taken into account. Next to that column specifies the possible range of the parameter values, where according to the standard mathematical notation, brackets [ ] indicate that the range includes the endpoints, but parentheses ( ) signifies the exclusion of the endpoints. Few of the parameters (e.g. some flags) take only one of the two possible values and the corresponding ranges are given as [x/y], where the parameter takes the value of either x or y. Empty ‘range’ column signifies that the particular parameter can take any value. In addition to these, a second set of parameter values is provided for exercising the model with most of the physical effects being turned on. This set can be used for, e.g. model testing.

Finally, in the most right column, a multiplication factor is given, which represents the scaling of the respective parameter in case of M identical devices connected in parallel. Note though, that this scaling becomes inaccurate at high frequencies due to the missing interconnect elements that need to be accounted for separately for such device structures.

3.1 Parameter list for HICUM/Level2

The following list of model parameters is supposed to be available in all (commercial) implementations of the model. The list is divided into groups of parameters according to the elements in the HICUM equivalent circuit shown in Fig. 2.1.1 as well as those for additional physical effects such as noise and temperature dependence. Although the total number of model parameters appears to be large, less time and effort needs to be spent for model parameter extraction - assuming the same physical effects are considered as in the SGPM - due to (a) the physical nature and modularity of the model formulation and (b) the reliable and clearly defined extraction procedure. Note, that not every parameter always needs to be specified for a particular process or application in order to achieve the required accuracy. For example, certain parameters are related to HBTs only and, therefore, can be left at their default values for homojunction transistors.

Many HICUM parameters have been chosen as simple factors, that are related to physically meaningful basic parameters like a capacitance, charge or transit time. This choice significantly re-
duces changes (and the probability of errors) in the parameter list if the basic parameters are changed for, e.g., statistical simulation, because the factors often assume very similar values even for different process technologies.

Input for the factor M in the last column is interpreted as follows: multiplication of the parameter value is indicated by M while division is indicated by 1/M and no action by leaving the entry blank. Caution is required if the factor is applied to $r_{su}$, $C_{su}$, $R_{th}$ and $C_{th}$, in which no interaction between parallel devices is assumed.

For production-type parameter library releases, it is recommended to have self-heating and non-quasi-static effects turned off by their respective flags, since the effects may not be required for many design tasks, especially not for first phase design and feasibility studies. Including these effects will unnecessarily increase the simulation time for all users during the entire design phase. These effects can become important in the last phase for tuning the performance of certain types of circuits or for design verification before tape-out. It is suggested to make these flags available in the design system as options for circuit designers.

As reference temperature, 27°C has been chosen to remain compatible with other simulators and models. The value for “$\infty$” may be dependent on the simulator system. Therefore, the user is referred to the manual of the respective simulator.

### 3.1.1 Transfer current

<table>
<thead>
<tr>
<th>no</th>
<th>name</th>
<th>description</th>
<th>default</th>
<th>range</th>
<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>is</td>
<td>Saturation current (GICCR constant) (C10=IS*QP0)</td>
<td>1E-16 (2E-30)</td>
<td>[0:1]</td>
<td>1.35E-18 (3.76e-32)</td>
<td>A (AC)</td>
<td>M (M$^2$)</td>
</tr>
<tr>
<td>2</td>
<td>qp0</td>
<td>Zero-bias hole charge</td>
<td>2E-14</td>
<td>(0:1)</td>
<td>2.78e-14</td>
<td>C</td>
<td>M</td>
</tr>
<tr>
<td>3</td>
<td>ich</td>
<td>High-current correction for 2D and 3D effects</td>
<td>$\infty$</td>
<td>[0:inf]</td>
<td>2.09e-02</td>
<td>A</td>
<td>M</td>
</tr>
<tr>
<td>4</td>
<td>hfe</td>
<td>Emitter minority charge weighting factor in HBTs</td>
<td>1</td>
<td>[0:inf]</td>
<td>1.0</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>hfc</td>
<td>Collector minority charge weighting factor in HBTs</td>
<td>1</td>
<td>[0:inf]</td>
<td>1.0</td>
<td>-</td>
<td></td>
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<tr>
<td>6</td>
<td>hjei</td>
<td>B-E depletion charge weighting factor in HBTs</td>
<td>1</td>
<td>[0:100]</td>
<td>1.0</td>
<td>-</td>
<td></td>
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### 3.1.2 Base-emitter current components

<table>
<thead>
<tr>
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<th>name</th>
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<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ibeis</td>
<td>Internal B-E saturation current</td>
<td>1E-18</td>
<td>[0:1]</td>
<td>1.16e-20</td>
<td>A</td>
<td>M</td>
</tr>
<tr>
<td>2</td>
<td>mbei</td>
<td>Internal B-E current ideality factor</td>
<td>1</td>
<td>(0:10)</td>
<td>1.0150</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>ireis</td>
<td>Internal B-E recombination saturation current</td>
<td>0</td>
<td>[0:1]</td>
<td>1.16e-16</td>
<td>A</td>
<td>M</td>
</tr>
<tr>
<td>4</td>
<td>mrei</td>
<td>Internal B-E recombination current ideality factor</td>
<td>2</td>
<td>(0:10)</td>
<td>2.0</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>ibeps</td>
<td>Peripheral B-E saturation current</td>
<td>0</td>
<td>[0:1]</td>
<td>3.72e-21</td>
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<td>M</td>
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<tr>
<td>6</td>
<td>mbep</td>
<td>Peripheral B-E current ideality factor</td>
<td>1</td>
<td>(0:10)</td>
<td>1.0150</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>ireps</td>
<td>Peripheral B-E recombination saturation current</td>
<td>0</td>
<td>[0:1]</td>
<td>1.0e-30</td>
<td>A</td>
<td>M</td>
</tr>
<tr>
<td>8</td>
<td>mrep</td>
<td>Peripheral B-E recombination current ideality factor</td>
<td>2</td>
<td>(0:10)</td>
<td>2.0</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>tbhrec</td>
<td>base current recombination time constant at the BC barrier for high forward injection (default is v2.1 compatible)</td>
<td>0 (≡ ∞)</td>
<td>[0:inf]</td>
<td>250</td>
<td>ps</td>
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### 3.1.3 Base-collector current components

<table>
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<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>ibcis</td>
<td>Internal B-C saturation current</td>
<td>1E-16</td>
<td>[0:1]</td>
<td>1.16e-20</td>
<td>A</td>
<td>M</td>
</tr>
<tr>
<td>2</td>
<td>mbci</td>
<td>Internal B-C current ideality factor</td>
<td>1</td>
<td>(0:10)</td>
<td>1.0150</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>ibcxs</td>
<td>External B-C saturation current</td>
<td>0</td>
<td>[0:1]</td>
<td>4.39e-20</td>
<td>A</td>
<td>M</td>
</tr>
<tr>
<td>4</td>
<td>mbcx</td>
<td>External B-C current ideality factor</td>
<td>1</td>
<td>(0:10)</td>
<td>1.03</td>
<td>-</td>
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</table>
### 3.1.4 Base-emitter tunnelling current

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<th>unit</th>
<th>factor</th>
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<tbody>
<tr>
<td>1</td>
<td>ibets</td>
<td>B-E tunnelling saturation current</td>
<td>0</td>
<td>[0:1]</td>
<td>0.0</td>
<td>A</td>
<td>M</td>
</tr>
<tr>
<td>2</td>
<td>abet</td>
<td>Exponent factor for tunnelling current</td>
<td>40</td>
<td>[0:inf)</td>
<td>40</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>tunode</td>
<td>specifies the base node connection of the tunneling current source</td>
<td>1</td>
<td>[0/1]</td>
<td>0</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### 3.1.5 Base-collector avalanche current

<table>
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<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>favl</td>
<td>Avalanche current factor</td>
<td>0</td>
<td>[0:inf)</td>
<td>1.186</td>
<td>1/V</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>qavl</td>
<td>Exponent factor for avalanche current</td>
<td>0</td>
<td>[0:inf]</td>
<td>11.1e-15</td>
<td>C</td>
<td>M</td>
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</tbody>
</table>

### 3.1.6 Series resistances

<table>
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<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>rbi0</td>
<td>Zero-bias internal base resistance</td>
<td>0</td>
<td>[0:inf)</td>
<td>71.76</td>
<td>Ω</td>
<td>1/M</td>
</tr>
<tr>
<td>2</td>
<td>rbx</td>
<td>External base series resistance</td>
<td>0</td>
<td>[0:inf)</td>
<td>8.83</td>
<td>Ω</td>
<td>1/M</td>
</tr>
<tr>
<td>3</td>
<td>fgeo</td>
<td>Factor for geometry dependence of emitter current crowding (r_{Bi})</td>
<td>0.6557</td>
<td>[0:1]</td>
<td>0.73</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>fdqr0</td>
<td>Correction factor for modulation by B-E and B-C Space charge layer</td>
<td>0</td>
<td>[0:1]</td>
<td>0.2</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>fcrbi</td>
<td>Ratio of HF shunt to total internal capacitance (lateral NQS effect)</td>
<td>0</td>
<td>[0:1]</td>
<td>0.0</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>fqi</td>
<td>Ratio of internal to total minority charge</td>
<td>1.0</td>
<td>[0:1]</td>
<td>0.9055</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>re</td>
<td>Emitter series resistance</td>
<td>0</td>
<td>[0:inf)</td>
<td>12.534</td>
<td>Ω</td>
<td>1/M</td>
</tr>
<tr>
<td>8</td>
<td>rcx</td>
<td>External collector series resistance</td>
<td>0</td>
<td>[0:inf)</td>
<td>9.165</td>
<td>Ω</td>
<td>1/M</td>
</tr>
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</table>
3.1.7 Substrate transistor

<table>
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<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>itss</td>
<td>Saturation current of substrate transistor transfer current</td>
<td>0</td>
<td>[0:1]</td>
<td>1.0e-16</td>
<td>A</td>
<td>M</td>
</tr>
<tr>
<td>2</td>
<td>msf</td>
<td>Forward ideality factor of substrate transfer current (note: set (m_{sf} = m_{sf}^*) in (2.1.12-1))</td>
<td>1</td>
<td>(0:10]</td>
<td>1.05</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>iscs</td>
<td>Saturation current of C-S diode</td>
<td>0</td>
<td>[0:1]</td>
<td>1e-17</td>
<td>A</td>
<td>M</td>
</tr>
<tr>
<td>4</td>
<td>msc</td>
<td>Ideality factor of C-S diode</td>
<td>1</td>
<td>(0:10]</td>
<td>1.0</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>tsf</td>
<td>Transit time (forward operation)</td>
<td>0</td>
<td>[0:inf]</td>
<td>1.05</td>
<td>s</td>
<td>-</td>
</tr>
</tbody>
</table>

3.1.8 Intra-device substrate coupling

Note: using the M factor is dangerous in this case, unless the transistor cell is exactly replicated and no coupling exists between cells.

<table>
<thead>
<tr>
<th>no</th>
<th>name</th>
<th>description</th>
<th>default</th>
<th>range</th>
<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>rsu</td>
<td>Substrate series resistance</td>
<td>0</td>
<td>[0:inf]</td>
<td>0</td>
<td>Ω</td>
<td>1/M</td>
</tr>
<tr>
<td>2</td>
<td>csu</td>
<td>Shunt capacitance (caused by substrate permittivity)</td>
<td>0</td>
<td>[0:inf]</td>
<td>0</td>
<td>F</td>
<td>M</td>
</tr>
</tbody>
</table>

3.1.9 Depletion charge and capacitance components

To avoid any confusion with TCs, version 2.1 parameters \(ALJEI\) and \(ALJEP\) have been changed to \(AJEI\) and \(AJEP\).

<table>
<thead>
<tr>
<th>no</th>
<th>name</th>
<th>description</th>
<th>default</th>
<th>range</th>
<th>test</th>
<th>unit</th>
<th>factor</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>cjei0</td>
<td>Internal B-E zero-bias depletion capacitance</td>
<td>0</td>
<td>[0:inf]</td>
<td>8.11e-15</td>
<td>F</td>
<td>M</td>
</tr>
<tr>
<td>2</td>
<td>vdei</td>
<td>Internal B-E built-in potential</td>
<td>0.9</td>
<td>(0:10]</td>
<td>0.95</td>
<td>V</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>zei</td>
<td>Internal B-E grading coefficient</td>
<td>0.5</td>
<td>(0:1)</td>
<td>0.5</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>ajei</td>
<td>Ratio of maximum to zero-bias value of internal B-E capacitance</td>
<td>2.5</td>
<td>[0:inf]</td>
<td>1.8</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>no</td>
<td>name</td>
<td>description</td>
<td>default</td>
<td>range</td>
<td>test</td>
<td>unit</td>
<td>factor</td>
</tr>
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<td>----</td>
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<td>-----------------------------------------------------------------------------</td>
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<td>--------</td>
<td>------</td>
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<tr>
<td>5</td>
<td>cjep0</td>
<td>Peripheral B-E zero-bias depletion capacitance</td>
<td>0</td>
<td>[0:inf]</td>
<td>2.07e-15</td>
<td>F</td>
<td>M</td>
</tr>
<tr>
<td>6</td>
<td>vdep</td>
<td>Peripheral B-E built-in potential</td>
<td>0.9</td>
<td>(0:10]</td>
<td>1.05</td>
<td>V</td>
<td></td>
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<tr>
<td>7</td>
<td>zep</td>
<td>Peripheral B-E grading coefficient</td>
<td>0.5</td>
<td>(0:1]</td>
<td>0.4</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>ajep</td>
<td>Ratio of maximum to zero-bias value of peripheral B-E capacitance</td>
<td>2.5</td>
<td>[0:inf]</td>
<td>2.4</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>cji0</td>
<td>Internal B-C zero-bias depletion capacitance</td>
<td>0</td>
<td>[0:inf]</td>
<td>1.16e-15</td>
<td>F</td>
<td>M</td>
</tr>
<tr>
<td>10</td>
<td>vdc1</td>
<td>Internal B-C built-in potential</td>
<td>0.7</td>
<td>(0:10]</td>
<td>0.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>zci</td>
<td>Internal B-C grading coefficient</td>
<td>0.4</td>
<td>(0:1]</td>
<td>0.333</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>vptci</td>
<td>Internal B-C punch-through voltage</td>
<td>100</td>
<td>(0:100]</td>
<td>100</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>cjcx0</td>
<td>External B-C zero-bias depletion capacitance</td>
<td>0</td>
<td>[0:inf]</td>
<td>5.4e-15</td>
<td>F</td>
<td>M</td>
</tr>
<tr>
<td>14</td>
<td>vdcx</td>
<td>External B-C built-in potential</td>
<td>0.7</td>
<td>(0:10]</td>
<td>0.700</td>
<td>V</td>
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<tr>
<td>15</td>
<td>zcx</td>
<td>External B-C grading coefficient</td>
<td>0.4</td>
<td>(0:1]</td>
<td>0.333</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>vptcx</td>
<td>External B-C punch-through voltage</td>
<td>100</td>
<td>(0:100]</td>
<td>100</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>cjs0</td>
<td>C-S zero-bias depletion capacitance</td>
<td>0</td>
<td>[0:inf]</td>
<td>3.64e-14</td>
<td>F</td>
<td>M</td>
</tr>
<tr>
<td>18</td>
<td>vds</td>
<td>C-S built-in potential</td>
<td>0.6</td>
<td>(0:10]</td>
<td>0.6</td>
<td>V</td>
<td></td>
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<tr>
<td>19</td>
<td>zs</td>
<td>C-S grading coefficient</td>
<td>0.5</td>
<td>(0:1]</td>
<td>0.447</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>vpts</td>
<td>C-S punch-through voltage</td>
<td>100</td>
<td>(0:100]</td>
<td>100</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

Note: The punch-through voltages should be limited to values > 0.
### 3.1.10 Minority charge storage effects

<table>
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<th>name</th>
<th>description</th>
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<th>unit</th>
<th>factor</th>
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<tbody>
<tr>
<td>1</td>
<td>t0</td>
<td>Low-current forward transit time at VBC=0V</td>
<td>0</td>
<td>[0:inf)</td>
<td>4.75e-12</td>
<td>s</td>
<td></td>
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<tr>
<td>2</td>
<td>dt0h</td>
<td>Time constant for base and B-C space charge layer width modulation</td>
<td>0</td>
<td>[0:inf)</td>
<td>2.1e-12</td>
<td>s</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>tbvl</td>
<td>Time constant for modelling carrier jam at low VCE</td>
<td>0</td>
<td>[0:inf)</td>
<td>4.0e-12</td>
<td>s</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>tef0</td>
<td>neutral emitter storage time</td>
<td>0</td>
<td>[0:inf)</td>
<td>1.8e-12</td>
<td>s</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>gtfe</td>
<td>Exponent factor for current dependence of neutral emitter storage time</td>
<td>1</td>
<td>(0:10]</td>
<td>1.4</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>thcs</td>
<td>Saturation time constant at high current densities</td>
<td>0</td>
<td>[0:inf)</td>
<td>30e-12</td>
<td>s</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>alhc</td>
<td>Smoothing factor for current dependent of base and collector transit time</td>
<td>0.1</td>
<td>(0:10]</td>
<td>0.75</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>fthc</td>
<td>Partitioning factor for base and collector portion</td>
<td>0</td>
<td>[0:1]</td>
<td>0.6</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>rci0</td>
<td>Internal collector resistance at low electric field</td>
<td>150</td>
<td>(0:inf)</td>
<td>127.8</td>
<td>Ω</td>
<td>1/M</td>
</tr>
<tr>
<td>10</td>
<td>vlim</td>
<td>Voltage separating ohmic and saturation velocity regime</td>
<td>0.5</td>
<td>(0:10]</td>
<td>0.70</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>vces</td>
<td>Internal C-E saturation voltage</td>
<td>0.1</td>
<td>[0:1]</td>
<td>0.1</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>vpt</td>
<td>Collector punch-through voltage</td>
<td>0</td>
<td>(≡∞)</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>tr</td>
<td>Storage time for inverse operation</td>
<td>0</td>
<td>[0:inf)</td>
<td>0</td>
<td>s</td>
<td></td>
</tr>
</tbody>
</table>
3.1.11 Parasitic isolation capacitances
The version 2.1 names $CEOX$ and $Ccox$ will be phased out and replaced by the names below.

<table>
<thead>
<tr>
<th>no</th>
<th>name</th>
<th>description</th>
<th>default</th>
<th>range</th>
<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>cbepar</td>
<td>total parasitic BE capacitance (spacer and metal component)</td>
<td>0.0</td>
<td>[0:inf)</td>
<td>0.6E-15</td>
<td>F</td>
<td>M</td>
</tr>
<tr>
<td>2</td>
<td>fbepar</td>
<td>partitioning factor of parasitic BE cap (default is v2.1 compatible)</td>
<td>1.0</td>
<td>[0:1]</td>
<td>0.5</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>bcpcpar</td>
<td>total parasitic BC capacitance (trench and metal component)</td>
<td>0</td>
<td>[0:inf)</td>
<td>2.97e-15</td>
<td>F</td>
<td>M</td>
</tr>
<tr>
<td>4</td>
<td>fbcpar</td>
<td>partitioning factor of parasitic BC cap (default is v2.1 compatible)</td>
<td>1.0</td>
<td>[0:1]</td>
<td>0.5</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

3.1.12 Vertical non-quasi-static effects

<table>
<thead>
<tr>
<th>no</th>
<th>name</th>
<th>description</th>
<th>default</th>
<th>range</th>
<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>alqf</td>
<td>Factor for additional delay time of minority charge</td>
<td>0</td>
<td>[0:1]</td>
<td>0.225</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>alit</td>
<td>Factor for additional delay time of transfer current</td>
<td>0</td>
<td>[0:1]</td>
<td>0.45</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>flnqs</td>
<td>flag for turning on (1) or off (0) vertical NQS effects</td>
<td>0</td>
<td>[0:1]</td>
<td>1</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

3.1.13 Noise

<table>
<thead>
<tr>
<th>no</th>
<th>name</th>
<th>description</th>
<th>default</th>
<th>range</th>
<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>kf</td>
<td>Flicker noise coefficient (no unit only for AF=2)</td>
<td>0</td>
<td>[0:inf)</td>
<td>1.43e-8</td>
<td>-</td>
<td>$M^{1-AF}$</td>
</tr>
<tr>
<td>2</td>
<td>af</td>
<td>Flicker noise exponent factor</td>
<td>2</td>
<td>(0:10]</td>
<td>2</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>
### 3.1.14 Lateral geometry scaling (at high current densities)

<table>
<thead>
<tr>
<th>no</th>
<th>name</th>
<th>description</th>
<th>default</th>
<th>range</th>
<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>latb</td>
<td>Scaling factor for collector minority charge in direction of emitter width ( b_E )</td>
<td>0</td>
<td>[0:inf)</td>
<td>3.765</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>latl</td>
<td>Scaling factor for collector minority charge in direction of emitter length ( l_E )</td>
<td>0</td>
<td>[0:inf)</td>
<td>0.342</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

### 3.1.15 Temperature dependence

The parameter \( ALB \) (version 2.1) has been deleted; cf. release notes for version 2.2. Note that \( f1vg \) and \( f2vg \) are not HICUM specific, but can be made general parameters in a simulator.

<table>
<thead>
<tr>
<th>no</th>
<th>name</th>
<th>description</th>
<th>default</th>
<th>range</th>
<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>vgb</td>
<td>Bandgap-voltage extrapolated to 0K</td>
<td>1.17</td>
<td>(0:10]</td>
<td>1.17</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>f1vg</td>
<td>coefficient ( K_1 ) in T dependent bandgap equation</td>
<td>1.02377 ( 10^{-4} )</td>
<td></td>
<td>1.02377 ( 10^{-4} )</td>
<td>V/K</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>f2vg</td>
<td>coefficient ( K_2 ) in T dependent bandgap equation</td>
<td>4.3215 ( 10^{-4} )</td>
<td></td>
<td>4.3215 ( 10^{-4} )</td>
<td>V/K</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>zetact</td>
<td>exponent coefficient in transfer current temperature dependence</td>
<td>4.5</td>
<td></td>
<td>3.5</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>vge</td>
<td>effective emitter bandgap voltage ( V_{gEeff} )</td>
<td>VGB</td>
<td>(0:10]</td>
<td>1.07</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>zetabet</td>
<td>exponent coefficient in BE junction current temperature dependence</td>
<td>5</td>
<td></td>
<td>4</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>vge</td>
<td>eff. collector bandgap voltage ( V_{gCeff} )</td>
<td>VGB</td>
<td>(0:10]</td>
<td>1.14</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>vgs</td>
<td>eff. substrate bandgap voltage ( V_{gSeff} )</td>
<td>VGB</td>
<td>(0:10]</td>
<td>1.17</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>alt0</td>
<td>First-order relative temperature coefficient of parameter ( T_0 )</td>
<td>0</td>
<td></td>
<td>0</td>
<td>1/K</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>kt0</td>
<td>Second-order relative temperature coefficient of parameter ( T_0 )</td>
<td>0</td>
<td></td>
<td>0</td>
<td>1/K^2</td>
<td></td>
</tr>
</tbody>
</table>
### 3.1.16 Self-Heating

<table>
<thead>
<tr>
<th>no</th>
<th>name</th>
<th>description</th>
<th>default</th>
<th>range</th>
<th>test</th>
<th>unit</th>
<th>factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>rth</td>
<td>Thermal resistance</td>
<td>0</td>
<td>[0:inf]</td>
<td>0.0</td>
<td>K/W</td>
<td>1/M</td>
</tr>
<tr>
<td>2</td>
<td>cth</td>
<td>Thermal capacitance</td>
<td>0</td>
<td>[0:inf]</td>
<td>0.0</td>
<td>Ws/K</td>
<td>M</td>
</tr>
<tr>
<td>3</td>
<td>flsh</td>
<td>flag for turning on (1) or off (0) self-heating effects</td>
<td>0</td>
<td>[0/1]</td>
<td>1</td>
<td>-</td>
<td>M</td>
</tr>
</tbody>
</table>
### 3.1.17 Circuit simulator specific parameters

The parameters $T_{NOM}$ and $D_T$ are available in most simulators and are also mostly named the same. The “model version identifier” enables version control in simulators with different HICUM generations.

<table>
<thead>
<tr>
<th>no</th>
<th>name</th>
<th>description</th>
<th>default</th>
<th>unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$t_{nom}$</td>
<td>temperature at which parameters are specified</td>
<td>27</td>
<td>°C</td>
</tr>
<tr>
<td>2</td>
<td>$dt$</td>
<td>temperature change w.r.t. chip temperature for particular transistor</td>
<td>0</td>
<td>°C</td>
</tr>
<tr>
<td>3</td>
<td>version</td>
<td>model version identifier</td>
<td>2.2</td>
<td>-</td>
</tr>
</tbody>
</table>

The Table below contains the syntax for calling HICUM in various circuit simulators (listed in alphabetical order).

<table>
<thead>
<tr>
<th>simulator name</th>
<th>calling syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADS</td>
<td>HICUMM1</td>
</tr>
<tr>
<td>AnalogOffice</td>
<td>HICUM_L2 (npn), HICUM_L2_P (pnp)</td>
</tr>
<tr>
<td>APLAC</td>
<td>HICUM</td>
</tr>
<tr>
<td>ELDO</td>
<td>Level = 9</td>
</tr>
<tr>
<td>HSPICE</td>
<td>Level = 8</td>
</tr>
<tr>
<td>Silvaco SPICE</td>
<td>Level = 6</td>
</tr>
<tr>
<td>SPECTRE</td>
<td>bht</td>
</tr>
</tbody>
</table>
4 Parameter determination

HICUM/L2 has been developed to address modeling issues related to the design of integrated circuits. In this case, geometry and process information are generally available, that can be used to obtain as much as possible physics-based model parameters. Besides bias, frequency and temperature, the transistor geometry can be considered as an additional independent dimension for parameter extraction the use of which helps avoiding ambiguous values compared to just fitting the terminal characteristics of a single device. A discussion of the advantages of the multi-geometry-based parameter extraction recommended for HICUM (and being used in the MOS area for a long time) is given in, e.g., [44]. Therefore, the description below deals with the extracting sequence that is used for generating geometry scalable HICUM parameters. For additional information of the extraction procedure see also [15].

As described in [15], the extracted model parameters for HICUM (and also for the SPICE Gummel-Poon model) are converted into a geometry and layout independent form. These so-called specific data are then used in a special program (TRADICA) to generate model parameters for arbitrary transistor configurations.

For a given process, obtaining compact model parameters of a large variety of transistor configurations, using the recommended process-based scalable approach (PBSA), involves several major steps:

• wafer selection according to certain criteria;
• deriving the relevant transistor dimensions from design rules;
• measurement of the relevant characteristics of a certain set of test structures (incl. transistors) over bias, geometry, temperature and frequency;
• extraction of (geometry) specific model parameters;
• generation of the model parameters for desired transistor configurations (either as library or directly during the circuit design phase).

The various aspects related to the above steps are briefly discussed in this chapter. In addition, an overview on the recommended sequence of parameter extraction is given in a formal way in chapter 4.5 to provide the reader with basic information, such as measurement and data requirements as well as principle procedures employed. Another purpose of this overview is also to serve as a guideline for implementing the parameter extraction methodology.
4.1 Wafer selection

There are many criteria as to which wafer should be selected or which one rejected when it comes to model parameter extraction. Below, those criteria that proved to be useful for the process-based scalable approach pursued here are briefly discussed.

As already mentioned before, the PBSA relaxes the requirements for the wafer selection, since it allows to shift the (specific) parameters later on to their desired nominal values. However, the electrical performance of the transistors (and other parameters) should not be too far off from the target specifications. Also, it is important to evaluate the process regarding geometry scalability, since non-conventional scaling requires larger effort (and time) for parameter extraction. Therefore, before a wafer is accepted for parameter extraction purposes, the following tests are recommended to be performed and evaluated:

- Measurement of a tetrode structure (for each transistor type) at zero bias, yielding roughly the internal base sheet resistance $r_{SBi0}$;
- Measurement of a large area BC diode (i.e. without SIC) at zero bias and beyond punch through, yielding epi doping $N_C$ and thickness $w_C$;
- Measurement of the bias dependent S-parameters for a typical transistor (each type) at a single CE voltage and frequency, yielding the transit frequency $f_T$.

The first two measurements can be performed on PCM structures. The third one is more time consuming and can be done after the first two have been evaluated. In general, though, all of the above data are usually available during process development and evaluation.

It is recommended then to obtain a wafer map that shows the uniformity of the electrical parameters $r_{SBi0}$, $w_C$, $N_C$, and $f_T$. The correlation of the latter to the first three should be checked as well as, of course, the absolute values regarding their deviation with respect to the target values.

Next, an appropriate die for parameter extraction is selected as the centre of the area with the highest uniformity. As a consequence, the chance of deviations in electrical characteristics between different transistors of the selected die is likely to be minimized.

In addition to the electrical tests, it is highly recommended to obtain pictures of the cross-section and top view (SEM and TEM pictures) of the most important transistor configurations for both extractions and applications. These pictures are usually available during process development and not only provide an impression on the actual transistor structure but also serve for verifying the tran-
sistor dimensions assumed or calculated from design rules. In the experience of the author, the information obtained from the above pictures can avoid results, that appear to be non-physical, and geometry scaling problems, that cannot be explained otherwise just by electrical measurements.
4.2 Relevant transistor dimensions

Definitions of the relevant transistor dimensions used for calculating the area and perimeter length specific model parameters are given in Fig. 4.2.0/1 for a junction isolated silicon bipolar transistor fabricated in a self-aligning base-emitter process.

Fig. 4.2.0/1: Schematic cross-section and layout of a silicon bipolar transistor with junction isolation and self-aligned base-emitter formation.
The described parameter extraction procedure can also be applied to silicon epitaxial base transistors, including SiGe transistors. The corresponding schematic cross section and layout with the respective dimensions are shown in Fig. 4.2.0/2.

Fig. 4.2.0/2: Schematic cross-section and layout of an epitaxial base SiGe bipolar transistor with shallow and deep trench isolation.
4.3 Measurements

Parameter extraction for the PBSA relies on minimum requirements regarding measurement effort and equipment. While the set-up and detailed bias conditions (test plans) for a particular parameter determination procedure are given in the respective chapters, at this point a brief overview shall be provided on the basic and most important measurement methods, which are being employed for obtaining the data required for a variety of procedures. This chapter also serves for defining the "measurement" and "data" related terminology used throughout this documentation.

The measurements are taken on transistors and special test structures. Examples of the most important test structures suitable for PBSA are given in [15].

4.3.1 IV measurements and data

DC measurements taken, e.g., with a parameter analyser, on test structures and transistors are called IV measurements, resulting in the associated IV data. Examples are

- a forced current in a 3-terminal test structure for determining a sheet resistance and the corresponding measured voltage between the contacts or
- the collector and base current of a transistor as function of the applied voltage.

However, IV data also include the DC bias taken during S-parameter measurements (see below), while IV measurements always means a DC measurement and associated set up as defined above.

4.3.2 CV measurements and data

Capacitances with a sufficient large value can be measured with LCR or CV meters, thus the name CV measurements and CV data. This equipment usually operates at frequencies between 0.1...10 MHz. It is, therefore, only suited for measuring large size capacitances that are laid out as special test structures like in process monitors.

The designation CV data includes capacitance vs. voltage data from both CV measurements, as defined above, and from S-parameter measurements.

4.3.3 S-parameter measurements and data

Small-signal measurements at high frequencies are performed with a vector network analyser (VNA) and are taken as S-parameters, resulting in S-parameter data. Operating frequencies for obtaining accurate data are usually above 300 MHz, with an upper limit usually in the multi-10GHz range.
range, dependent on the respective equipment. For parameter extraction purposes, two types of S-measurement are often distinguished: (a) "cold" measurements during which the transistor is operated at reverse and very low forward bias with negligible carrier injection and current across the junctions; (b) "hot" measurements during which the transistor is operated under usual forward-bias conditions with significant carrier injection and non-negligible current across junction. The corresponding data are designated as, e.g. cold S-parameters or hot Y-parameters.

Although the operating frequencies of high-performance transistors in some of the present Si-based processes already exceed 100GHz, the corresponding parameters for modeling the high-frequency transistor can be determined at frequencies well below 100 GHz under so-called quasi-static conditions. The lower frequency limit for parameter extraction related S-parameter measurements is approximately given by the 3dB corner frequency of the common-emitter (CE) small-signal current gain. At current gains between 50 and 200, this corresponds to the range around 1GHz. One of the most important quasi-static small-signal transistor parameters for extracting model parameters is the transit frequency $f_T$. It has been shown in [10] that $f_T$ can be obtained from a single frequency measurement of the small-signal CE current gain.

A typical set of data from a single-frequency bias sweep measurement includes the terminal voltages and current as well as the frequency and the four S-parameters in either magnitude and phase or real and imaginary part representation. The S-parameters can then be converted into Y-parameters at the same bias points. Next, the Y-parameters need to be de-embedded in order to eliminate the influence of parasitic elements and obtain the Y-parameters of the device under test only. From the de-embedded Y-parameters as a function of bias, a large number of HICUM model parameters can be extracted.

Generally, the bias dependence of the small-signal behavior and parameters is of great interest for parameter extraction. In many circuit design applications, the dependence of small-signal parameters on the collector current $I_C$ at a given voltage $V_{CE}$ is of major importance. Unfortunately, it is found very often, that S-parameters as a function of frequency are taken for bias points, that are defined by the terminal voltages $V_{BE}$ and $V_{CE}$, while the terminal currents are not or cannot be monitored; the latter is often caused by, e.g., limitations of the data acquisition software or the equipment. Only with a separate DC measurement the terminal currents are then obtained, and the relationship between S-parameters and bias currents is attempted to be established. The great dan-
ger in this procedure is that the devices usually heat up differently (caused by self-heating) during the S-parameter and the pure DC measurement, leading to an incorrect relationship of the above mentioned variables. The consistent way of taking data is to monitor the current or, even better, to define the bias point by the collector current and $V_{CE}$. For some data acquisition software, the current can be monitored by reducing the small-signal measurements to a single frequency rather than a frequency sweep. Although in this case the "averaging" has to be increased, a somewhat shorter measurement time is often achieved (together with a large reduction in data) as well. Appropriate bias points for frequency sweep measurements can then be selected afterwards.

4.3.4 Sequence of measurements

In a production environment, measurement effort and time have to be minimized. This is done on one hand by using standard and established equipment set-ups and on the other hand by maximizing the equipment utilization in a given time frame.

Data acquisition for model parameter extraction starts at the reference temperature $T_0$ with simple and fast IV measurements of all special test structures used for determining sheet and contact resistances. Next, CV measurements are performed, followed by single-frequency cold and hot S-parameter measurements. The same device is probed for all bias conditions before moving the probes to the next device. These measurements provide already sufficient information for extracting more than 80% of the (specific) model parameters, the process of which can then start.

In the meantime, i.e. during parameter extraction, data acquisition continues with temperature dependent measurements, which are quite time consuming. By the time the latter measurements are completed, parameter extraction has provided an overview on the process and its actual performance, so that those bias range and points can be determined which are of interest for frequency sweeps. Frequency sweep measurements are usually required and taken only at the reference temperature. Based on the temperature and frequency dependent data, the remaining model parameters (except those for low-frequency $1/f$ noise) can be extracted, and model verification can already start.

Finally, special measurements, such as those for noise and distortion, can be performed at $T_0$. 
4.4 Flowchart and comparison to SGPM

The PBSA allows to combine the parameter extraction of different compact models with a minimum of additional effort. Fig. 4.4.0/1 visualizes the overall extraction flow including the modules that are model independent ("general") and those that are specific to the SGPM and HICUM. This provides a rough overview on the effort required to add a new model such as HICUM to an existing parameter extraction for the SGPM and vice versa (i.e. keeping the SGPM in the loop as a backup). The program TRADICA allows to generate both types of models as well as a hierarchy of SGPMs with different complexity from a single set of extracted geometry specific parameters.
Fig. 4.4.0/1: Rough overview on the flow and modules for a combined geometry scalable parameter extraction for both SGPM and HICUM. SGPM/L2 corresponds to a similar equivalent circuit as HICUM, including, e.g., separate elements for the emitter perimeter injection and a partitioning of the base resistance and external BC capacitance.
4.5 A step by step procedure

The goal of this chapter is to give a "formal" overview on the sequence for extracting geometry scalable HICUM parameters. To keep this overview efficient, for each step only a brief description of the applied extraction procedure is provided, while for a detailed description (incl. equations) and the origin of the respective procedure, the reader is referred to one of the subsequent chapters of this documentation. One important boundary condition for developing HICUM was to enable a parameter extraction procedure in which as many as possible steps can be performed linearly independently or with only a weak interdependence, particularly for determining parameters describing first-order effects. For commercially available implementations see [61,62].

In modern bipolar technologies, often at least two types of transistors are offered: a high-performance (HP) transistor and a high-voltage (HV) transistor, that are defined by same process flow and with just one additional mask. The HP transistor is usually realized with a selectively implanted collector (SIC). It is recommended to extract first the parameters of the HV transistors and then the parameters of the HP transistors, since the HV transistor’s collector is typically realized with the background doping that is also present under the external base of the HP device. If HV transistors are not available, those ones required for extraction can usually be easily realized and should be included on a test chip. If parameters for a HV transistor without SIC have to be extracted, no respective HP device is needed.

A couple of assumptions are being made in order to apply the procedures in practice:

- A suitable wafer with the appropriate test structures and transistors has been selected that has passed the recommended acceptance check mentioned in chapter 4.1.
- All measurements that are required for a particular extraction step are available and have been properly de-embedded. It is generally preferable to convert S-parameters to Y-parameters (to be done during de-embedding in any way) and use the latter data for parameter extraction.
- The design rules and dimensions of all test structures and transistors are known and have been verified, so that all necessary geometry calculations can be performed.
- The process is geometry scalable, i.e. the profile under the emitter does not depend significantly on the emitter width. This can be checked by measuring the internal base sheet resistance as a function of emitter width (cf. [28,15]).

The information about each extraction step is contained in a small table. The meaning of the key words on the right-hand-side and the terminology used shall be briefly explained below.
• "Measurement data" characterizes the type of data required for the particular step. Acronyms such as CV, IV or cold measurements have already been defined in chapter 4.3.
• "Required model parameters" specify those ones that have to be extracted in an earlier step and are needed for the present step. They do not include dimensions, which are specified under "required geometry data".
• "Procedure" refers to the main extraction steps; the detailed background is described elsewhere.
• Under "Extracted specific parameters" those parameters are listed that are geometry independent. These parameters are used in the program TRADICA to generate geometry scalable libraries for model parameters. Of course, certain HICUM parameters, such as ratios, are geometry independent in the first place and do not need to be scaled with geometry. However, since it is useful to determined a full set of (geometry) specific parameters first and keep the data in one place before subsequent parameter (library) generation, all extracted parameters are listed here.
• "Related HICUM parameters" are those that eventually are written into a library (as model card) and are generated for a particular transistor configuration, employing a program like TRADICA.

Fig. 4.5/02 shows a rough overview of the impact of the most important model parameters on the DC characteristics.
Fig. 4.5.0/2: Overview of the impact of the most important model parameters on HICUM’s forward DC characteristics.

Below, the extraction sequence is outlined. Linearly independent steps are indicated by the entry "none" under "Required model parameters".
### 4.5.1 BC depletion and isolation capacitance

| Measurement data | • cold Y-parameters of different transistor configurations  
|                  | • CV data of large area HV structure (optional)  
|                  | • CV data of large area HP structure  

| Required model parameters | none (optional: $C_{BCpar}$ calculated from TRADICA for each transistor configuration)  

| Required geometry data | • area $A_{BC}$ and perimeter $P_{BC}$ of BC junction (HV transistor)  
|                       | • area $A_{SIC}$ of SIC region (HP transistor)  

| Procedure: | • HV data: separation into bias dependent bottom and perimeter specific components of the depletion capacitance via different geometries; also, determination of specific isolation capacitance possible.  
|           | • Extraction of parameters for modeling the bias dependence of above depletion capacitances.  
|           | • HP CV data: extraction of SIC related parameters.  

| Extracted (specific) parameters | • HV data: $C_{jCb}^0, V_{DCb}, z_{Cb}, V_{PTCb}, C_{jCp0}^r, V_{DCp}, z_{Cp}, V_{PTCp}, [C_{Cox}]$  
|                               | • HP data: $C_{jCi0}, V_{DCi}, z_{Ci}, V_{PTCi}$  

| Related HICUM parameters | $C_{jCx0}, V_{DCx}, z_{Cx}, V_{PTCx}, C_{BCoar}, f_{BCpar}, C_{jCi0}, V_{DCi}, z_{Ci}, V_{PTCi}$  

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### 4.5.2 BE depletion and isolation capacitance

| Measurement data and test structures | • cold and hot Y-parameters of different transistor configurations  
• CV data of large area structure (optional) |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>none (optional: $C_{BEpar}$ calculated from TRADICA for each transistor configuration)</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>area $A_{E0}$ and perimeter $P_{E0}$ of emitter window</td>
</tr>
</tbody>
</table>
| Procedure                          | • Determination of $C_{BE}$ from $1/(2\pi f_T)$ at a forward bias point.  
• Separation into bias dependent bottom and perimeter specific components of the depletion capacitance via different geometries; also, determination of specific isolation capacitance possible.  
• Extraction of parameters for modeling the bias dependence of above depletion capacitances |
| Extracted (specific) parameters    | $\bar{C}_{jEi0}$, $V_{DEi}$, $z_{Ei}$, $a_{jEi}$; $C_{jEp0}$, $V_{DEp}$, $z_{Ep}$, $a_{jEp}$; $C_{Eox}$ |
| Related HICUM parameters           | $C_{jEi0}$, $V_{DEi}$, $z_{Ei}$, $a_{jEi}$; $C_{jEp0}$, $V_{DEp}$, $z_{Ep}$, $a_{jEp}$; $C_{BEpar}$ |

### 4.5.3 CS depletion capacitance

| Measurement data and test structures | • cold Y-parameters of different transistor configurations  
• CV data of large area structure (optional, but recommended) |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>none</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>area $A_{CS}$ and perimeter $P_{CS}$ of CS junction</td>
</tr>
</tbody>
</table>
| Procedure                          | • Separation into bias dependent bottom and perimeter specific components of the depletion capacitance via different geometries.  
• Extraction of parameters for modeling the bias dependence of above depletion capacitances. |
| Extracted (specific) parameters    | $\bar{C}_{jSb0}$, $V_{DSb}$, $z_{Sb}$, $V_{PTSb}$; $C_{jSp0}$, $V_{DSp}$, $z_{Sp}$, $V_{PTSp}$ |
| Related HICUM parameters           | $C_{jSb0}$, $V_{DS}$, $z_{S}$, $V_{PTS}$ |
4.5.4 Internal base (sheet) resistance

**Measurement data**
- IV data on transistor tetrodes with different emitter widths:
  - sweep of $V_{BE} = V_{BC}$ ($V_{CE} = 0$)
  - sweep of $V_{BE} @ V_{BC} = 0$

**Required model parameters**
- $C_{JEi0}$, $V_{DEi}$, $z_{EI}$; $C_{JCi0}$, $V_{DCi}$, $z_{CI}$ (or numerical integration of associated depletion charges)

**Required geometry data**
- width $b_{E0}$ and length $l_{E0}$ of emitter windows

**Procedure:**
- Determine internal base sheet resistance $r_{SBi}(V_{BE}, V_{BC})$ from corrected data.
- Extraction of parameters for modeling the bias dependence of $r_{SBi}$.
- Determination of the link and total external resistance (used for next step)

**Extracted (specific) parameters**
- $r_{SBi0}$, $Q_{p0}$, $f_{dQr0}$, $r_{Ss}$

**Related HICUM parameters**
- $r_{Bi0}$, $Q_{p0}$, $f_{dQr0}$

Note, that the model parameter $f_{geo}$ can be (and has been) directly calculated from the transistor configuration.

4.5.5 Components of external base resistance

**Measurement data**
- IV data of various resistance test structures
- link and total external resistance from transistor tetrodes

**Required model parameters**
- None

**Required geometry data**
- dimensions of the relevant regions of the test structures

**Procedure:**
- Determine resistance(s) from IV data and perform current spreading correction (depending on resistance type).
- Extract sheet or specific contact resistance from each structure

**Extracted (specific) parameters**
- $\rho_{KB}$, $r_{Spo}$, $r_{Sm}$, $r_{Sil}$

**Related HICUM parameter**
- $r_{Bx}$

For single device extraction, this module has to be replaced by a procedure for extracting $r_{Bx}$. 
4.5.6 Emitter resistance

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>open collector IV data from transistor structures with different emitter size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>None</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>total emitter window width $A_{E0}$ of each transistor</td>
</tr>
</tbody>
</table>
| Procedure: | • for each transistor: fit modified open-collector model equation to measured data  
• extract specific contact resistance from $r_E(1/A_{E0})$ |
| Extracted (specific) parameter | $\rho_{KE}$ |
| Related HICUM parameter | $r_E$ |

The open-collector method has been found to give reasonable and reliable results, although the current flow through the emitter window deviates from the one in usual transistor operation.

4.5.7 Components of external collector resistance

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>IV data of special resistance test structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>None</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>dimensions of the relevant regions of the test structure</td>
</tr>
</tbody>
</table>
| Procedure: | • Determine resistance from IV data and perform current spreading correction (if required).  
• Extract buried layer sheet and specific contact plus sinker resistance |
| Extracted (specific) parameters | $\rho_{KC}, r_{Shl}$ |
| Related HICUM parameter | $r_{Cx}$ |
4.5.8 Collector current at low bias

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>IV data from transistors with different emitter size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>most processes: $C_{jEi0}$, $V_{DEi}$, $z_{Ei}$, $a_{jEi}$ (not for &quot;real&quot; HBTs) optional: $Q_{p0}$; $[C_{jCi0}$, $V_{DCi}$, $z_{Ci}$, if $V_{CE} =$ const)</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>emitter window area of the transistors</td>
</tr>
<tr>
<td>Procedure:</td>
<td>• Separation into bias dependent bottom and perimeter specific current components via different geometries. • Extraction of parameters related to bias dependence from least-squares fit of $\log(I_C/A_E)$ vs. $V_{BE} @ V_{BC}=0$ (procedure is partially dependent on process):</td>
</tr>
<tr>
<td>Extracted (specific) parameters</td>
<td>$\gamma_C$, $I_S$, $[Q_{p0}$, $m_{Cj}]$</td>
</tr>
<tr>
<td>Related HICUM parameters</td>
<td>$I_S$ (or $c_{10}$), $[Q_{p0}$, $m_{Cj}]$</td>
</tr>
</tbody>
</table>

4.5.9 Current across BE junction at low bias

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>IV data from transistors with different emitter size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>none</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>emitter window area of the transistors</td>
</tr>
<tr>
<td>Procedure:</td>
<td>• Separation into bias dependent bottom and perimeter specific current components via different geometries. • Extraction of saturation current (density) and non-ideality coefficient of each component from least-squares fit of $\log(I)$ vs. $V_{BE} @ V_{BC}=0$</td>
</tr>
<tr>
<td>Extracted (specific) parameters</td>
<td>$\gamma_B$, $I_{BEiS}$, $m_{BEi}$, $I_{BEpS}$, $m_{BEp}$; $I_{REiS}$, $m_{REi}$, $I_{REpS}$, $m_{REp}$</td>
</tr>
<tr>
<td>Related HICUM parameters</td>
<td>$I_{BEiS}$, $m_{BEi}$, $I_{BEpS}$, $m_{BEp}$; $I_{REiS}$, $m_{REi}$, $I_{REpS}$, $m_{REp}$</td>
</tr>
</tbody>
</table>
4.5.10 Current across BC junction at low bias

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>IV data from transistors with different size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>none</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>collector-base junction area $A_{BC}$ and emitter window area $A_{E0}$ of the transistors</td>
</tr>
</tbody>
</table>
| Procedure: | • Separation into bias dependent bottom and perimeter specific current components via different geometries.  
• Extraction of saturation current (density) and non-ideality coefficient for each component from least-squares fit of log($I$) vs. $V_{BC}$ @ $V_{BE}=0$ |
| Extracted (specific) parameters | $I_{BCxS}, m_{BCx}; \bar{I}_{BCiS}, m_{BCi}$ |
| Related HICUM parameters | $I_{BCxS}, m_{BCx}; I_{BCiS}, m_{BCi}$ |

4.5.11 Thermal resistance

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>IV data of transistors used for extraction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>$r_E, r_{Bx}, r_{Bi}$</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>emitter window area $A_{E0}$ of the transistors</td>
</tr>
<tr>
<td>Procedure:</td>
<td>• Extraction of $R_{th}$ of each transistor from $I_B$ as a function of dissipated power according to [50], but with known $r_E$.</td>
</tr>
<tr>
<td>Extracted (specific) parameter</td>
<td>$r_{th}$</td>
</tr>
<tr>
<td>Related HICUM parameter</td>
<td>$R_{th}$</td>
</tr>
</tbody>
</table>
### 4.5.12 Forward transit time

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>Hot Y-parameters of different transistor configurations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>( C_{jC0}, V_{DC0}, z_{Cj}, V_{PTCj}, C_{jCx0}, V_{DCx}, z_{Cx}, V_{PTCx}, C_{BCpar}; r_{E}, r_{Cx}; \gamma_{C}; [R_{th}] )</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>Emitter window dimensions ( b_{E0} ) and ( l_{E0} ) of the transistors</td>
</tr>
</tbody>
</table>

**Procedure:**
- Determine transit frequency \( f_T \) from Y-parameters and determine transit time \( \tau_f \) from \((1/(2\pi f_T)) \) vs \( I_C \).
- **Low-current range:**
  - From \( \tau_{00}(V_{BC}) \) data, extract parameters describing the bias dependence.
  - Determine bottom and perimeter related component and associated geometry factor from \( \tau_{00}(V_{BC}=0) \) of transistors with different emitter size.
- **Medium current range**
  - From \( I_{CK}(V_{CE} \text{ or } V_{BC}) \) data, extract parameters describing the bias dependence.
  - Extract current spreading angle from \( I_{CK}(V_{CE}=0.8V \text{ or } V_{BC}=0V) \)
- **High-current region:** extract relevant parameters describing the bias dependence.

**Extracted (specific) parameters**
- \( \tau_{00}, \tau_{tpi}, \tau_{0p}/\tau_{0i}, \Delta \tau_{0h}, \tau_{Bfv}, r_{Cj0}, V_{lim}, V_{PT}, V_{CES}; a_{hc}, \tau_{hcs}, \tau_{Ef0}, g_{te}; f_{thc} \)

**Related HICUM parameters**
- \( \tau_{0}, \Delta \tau_{0h}, \tau_{Bfv}, r_{Cj0}, V_{lim}, V_{PT}, V_{CES}; a_{hc}, \tau_{hcs}, \tau_{Ef0}, g_{te}; f_{thc} \)
## 4.5.13 Collector current at high injection

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>IV data from transistors with different emitter size</th>
</tr>
</thead>
</table>
| Required model parameters | - those for $I_T$ and $I_{BE}$ extracted at low injection  
- depletion capacitances and transit time (to calculate $Q_{p,T}$)  
- $r_E$, $r_{Bx}$, $r_{Bi}$, $r_{Cx}$  
- $R_{jh}$ |

<table>
<thead>
<tr>
<th>Required geometry data</th>
<th>emitter window area of the transistors</th>
</tr>
</thead>
</table>

### Procedure:
- Extraction in high current region via non-linear optimization of $\log(I_C/A_E)$ vs. $V_{BE}$ at sufficiently low $V_{CE}$ (to minimize impact of self-heating).
- Optimization can be performed simultaneously on transistors with different emitter sizes.

<table>
<thead>
<tr>
<th>Extracted (specific) parameter</th>
<th>$I_{Ch}$</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Related HICUM parameter</th>
<th>$I_{Ch}$</th>
</tr>
</thead>
</table>

## 4.5.14 Base-collector Breakdown

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>$I_B(V_{CB}$ or $V_{CE}$) data from transistors with different size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>$C_{ji0}$, $V_{DCi}$, $z_{Ci}$, $V_{PTCi}$, $\gamma_C$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Required geometry data</th>
<th>emitter window area $A_{E0}$ of the transistors</th>
</tr>
</thead>
</table>

### Procedure:
- Determination of avalanche current $I_{AVL}(V_{CB})$ from measured $I_B(V_{CB})$ data at sufficiently low forward bias $V_{BE}$.
- Extraction of parameters describing the bias dependence via non-linear optimization of $I_{AVL}(V_{CB})$.

<table>
<thead>
<tr>
<th>Extracted (specific) parameters</th>
<th>$f_{AVL}$, $\bar{q}_{AVL}$</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Related HICUM parameters</th>
<th>$f_{AVL}$, $q_{AVL}$</th>
</tr>
</thead>
</table>
4.5.15 High-Frequency effects

4.5.15.1 Non-quasi-static effects

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>hot Y-parameters of a typical transistor configuration</th>
</tr>
</thead>
</table>
| Required model parameters | • those for $I_T$ and $I_{BE}$ extracted at low injection
| | • all capacitances and transit time
| | • $r_E$, $r_{Bx}$, $r_{Bi}$, $r_{Cx}$ |
| Required geometry data | None |
| Procedure: | • Extraction of $\alpha_{iT}$ by fitting Im{$y_{21}$} at high frequencies for various bias points below peak $f_T$;
| | • Extraction of $\alpha_{Qf}$ by fitting Re{$y_{11}$} at high frequencies for various bias points beyond peak $f_T$. |
| Extracted (specific) parameters | $\alpha_{iT}$, $\alpha_{Qf}$ |
| Related HICUM parameters | $\alpha_{iT}$, $\alpha_{Qf}$ |

4.5.15.2 Partitioning of the external BC capacitance

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>None</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>specific BC capacitances and sheet/contact resistances of the external base</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>dimensions of the various regions of the external base</td>
</tr>
<tr>
<td>Procedure:</td>
<td>Calculation of the partitioning factor by TRADICA for each geometry during parameter (library) generation</td>
</tr>
<tr>
<td>Extracted (specific) parameter</td>
<td></td>
</tr>
<tr>
<td>Related HICUM parameter</td>
<td>$f_{BCpar}$</td>
</tr>
</tbody>
</table>

Presently existing methods, that are based on experimental data, only allow to extract the partitioning factor for a single geometry, but do not offer a generic description for geometry scaling.
### 4.5.16 Intra-device substrate coupling

Presently existing methods only allow to extract the substrate resistance for a single geometry, but do not offer a generic description for geometry scaling.

#### Measurement data
- cold Y-parameters of relevant transistor configurations

#### Required model parameters
- \( r_E \) (is of minor importance though)

#### Required geometry data
- None

#### Procedure:
- Determine the impedance \( Z_{su} \) of the substrate coupling network and extract \( r_{su} \) and \( C_{su} \) from real and imaginary part of \( 1/Z_{su} \).
- Alternative (also for parameter library generation): calculation from simulation after experimental calibration.

#### Extracted (specific) parameters
- \( r_{su}, C_{su} \)

#### Related HICUM parameters
- \( r_{su}, C_{su} \)

### 4.5.17 High-frequency emitter current crowding

Presently existing methods only allow to extract \( f_{CrBi} \) from experimental data of a single geometry, but do not offer a generic description for geometry scaling. In addition, the modeling approach can only be applied to the small-signal case.

#### Measurement data
- hot Y-parameters of different transistor configurations

#### Required model parameters
- those of \( i_T \) and \( i_{BE} \)
- all capacitances (incl. transit time) at the base node
- \( r_E, r_{Bx}, r_{Bi} \)

#### Required geometry data
- None

#### Procedure:
- \( f_{CrBi} \) can be determined from optimizing the model’s \( y_{11} \) at high frequencies to the results of a transistor with the largest emitter width offered in a process.
- Alternative (also for parameter library generation): use \( f_{CrBi} = 0.2 \)

#### Extracted (specific) parameter
- \( f_{CrBi} \)

#### Related HICUM parameter
- \( f_{CrBi} \)
4.5.18 Parasitic substrate transistor elements

Geometry scaling of the substrate junction related currents depends on the process. For practical applications, the minimum effort is assumed to be spent on modeling and parameter extraction of the substrate transistor.

4.5.18.1 Transfer current

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>transistor configurations with different substrate size</th>
</tr>
</thead>
</table>
| Required model parameters | • if separate substrate pad is available: none  
  • if in HF pads: base current components |
| Required geometry data | substrate perimeter length and/or area |
| Procedure: | • Separation into bias dependent bottom and/or perimeter specific current components via different geometries.  
  • Extraction of parameters related to bias dependence from least-squares fit of \( \log(I_{Ts}) \) vs. \( V_{SC} \). |
| Extracted (specific) parameters | \( I_{TsS} \) or \( I_{TsS} \), \( m_{sf} \) |
| Related HICUM parameters | \( I_{TsS}, m_{sf} \) |

4.5.18.2 Charge storage time

| Measurement data | hot Y-parameters for a critical transistor configuration at (very) low \( V_{CE} \)  
  (optional: different transistor configurations) |
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>transit time, ( C_{BE}, C_{BC} )</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>none</td>
</tr>
<tr>
<td>Procedure:</td>
<td>adjust ( \tau_{sf} ) to fit ( f_T ) at low ( V_{CE} ).</td>
</tr>
<tr>
<td>Extracted (specific) parameter</td>
<td>( \tau_{sf} )</td>
</tr>
<tr>
<td>Related HICUM parameter</td>
<td>( \tau_{sf} )</td>
</tr>
</tbody>
</table>

It is assumed that no separate substrate test transistor is available in HF pads to directly measure the S-parameters of the substrate transistor.
4.5.19 Temperature dependence

$T_0$ is the (reference) temperature at which the parameter extraction for modeling the bias and frequency dependent transistor behavior is performed. For extracting the relevant model parameters, the same measurements as for $T_0$ are repeated for different temperatures $T$.

4.5.19.1 Series resistances

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>IV data at different temperatures $T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>series resistances and/or their components at $T_0$</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>None</td>
</tr>
</tbody>
</table>
| Procedure: | • determine the respective resistance $r$ for each $T$  
  • fitting of the ratio $\log[r(T)/r(T_0)]$ vs. $(T/T_0)$ with the respective exponent factor $\zeta$ as parameter. |
| Extracted (specific) parameters | $\zeta_{C_i}, \zeta_{r_{Bi}}, \zeta_{r_{Bx}}, \zeta_{r_{Cx}}, \zeta_{r_E}$ |
| Related HICUM parameters | $\zeta_{C_i}, \zeta_{r_{Bi}}, \zeta_{r_{Bx}}, \zeta_{r_{Cx}}, \zeta_{r_E}$ |

4.5.19.2 Bandgap voltage

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>$I_C(V_{BE})$ data at $V_{BC}=0$ for different temperatures $T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>none</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>none</td>
</tr>
</tbody>
</table>
| Procedure: | • Determine the saturation current $I_S$ and the non-ideality coefficient at various temperatures.  
  • Extract $V_{gB}$ from a least-squares fit based on $I_S(T)$ |
| Extracted (specific) parameter | $V_{gB}$ |
| Related HICUM parameter | $V_{gB}$ |
### 4.5.19.3 TC of the forward current gain

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>$I_C(V_{BE}), I_B(V_{BE})$ data at $V_{BC}=0$ for different temperatures $T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>none</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>none</td>
</tr>
</tbody>
</table>
| Procedure: | • Determine $B(I_C)$ at various temperatures.  
  • Extract $\alpha_{Bf}$ from $B(I_C=\text{const})$ vs. $T-T_0$ via least-squares fit |
| Extracted (specific) parameter | $\alpha_{Bf}$ |
| Related HICUM parameter | $\alpha_{Bf}$ |

### 4.5.19.4 Transit time at low current densities

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>hot Y-parameters vs bias (at $V_{BC}=0$) for different temperatures $T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>none</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>none</td>
</tr>
</tbody>
</table>
| Procedure: | • Determine the low-current transit time $\tau_{0}$ for each $T$  
  • Extract $\alpha_{\tau0}$ and $k_{\tau0}$ from $\tau_{0}(T)$ via non-linear optimization |
| Extracted (specific) parameters | $\alpha_{\tau0}, k_{\tau0}$ |
| Related HICUM parameters | $\alpha_{\tau0}, k_{\tau0}$ |
### 4.5.19.5 Critical current

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>hot Y-parameters vs bias (at $V_{BC}=0$) for different temperatures $T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>none</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>none</td>
</tr>
</tbody>
</table>
| Procedure: | • Determine the transit time $\tau_f$ and the critical current $I_{CK}$ for each $T$
  • Extract $\alpha_{CEs}$ from re-fitting $I_{CK}$ at each $T$ with $V_{CEs}(T)$ as a parameter.
  • $\alpha_{vs}$ can be taken from literature |
| Extracted (specific) parameters | $\alpha_{vs}$, $\alpha_{CEs}$ |
| Related HICUM parameters | $\alpha_{vs}$, $\alpha_{CEs}$ |

### 4.5.19.6 BC breakdown

<table>
<thead>
<tr>
<th>Measurement data</th>
<th>$I_B(V_{CB}$ or $V_{CE}$) data for different temperatures $T$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Required model parameters</td>
<td>none</td>
</tr>
<tr>
<td>Required geometry data</td>
<td>none</td>
</tr>
</tbody>
</table>
| Procedure: | • Determine the avalanche current $I_{AVL}$ from $I_B$ for each $T$
  • With $\alpha_{fav}$ and $\alpha_{qav}$ as variables, perform a nonlinear optimization on the measured data for $I_{AVL}$ by exercising the compact model with fixed values for $f_{AVL}$ and $q_{AVL}$, that were determined at the reference temperature $T_0$. |
| Extracted (specific) parameters | $\alpha_{fav}$, $\alpha_{qav}$ |
| Related HICUM parameters | $\alpha_{fav}$, $\alpha_{qav}$ |
### 4.6 Measurement conditions

The table below contains an overview on the most important measurements to be performed and the associated bias conditions. The values are examples and given for Si-based processes. Only a minimum number of measurements is specified (i.e. more data is always useful).

<table>
<thead>
<tr>
<th>measurement type and bias conditions</th>
<th>data</th>
<th>result</th>
</tr>
</thead>
</table>
| • internal base pinch resistance data from at least 3 structures with different $b_E$;  
  $V_{BE}=[-0.5,0.5]V \quad @ \quad V_{CE}=0$, $\Delta V_{BE}=0.1V$, $\Delta V_{BB}=0.01V$  
• sheet and contact resistances of ext. base region, buried layer, collector (sinker, contact)  
  $\Delta V=0.01...0.1V$, depending on resistance value | $V_{BE} I_{B1} I_{B2}$ | base and collector series resistance components |
| | $\Delta V \ I$ (or $r_s, r_{con} \ldots$) | |
| • C-V on large area transistor  
  $V_{BE}=[-0.5,0.5]V$, $V_{BC}=V_{SC}=0$, $\Delta V_{BE}=0.1V$  
• $V_{BC}=[-BV_{CEO},0.5]V$, $V_{BE}=V_{BC}=0$, $\Delta V_{BC}=0.1V$  
• $V_{SC}=[-BV_{CEO},0.5]V$, $V_{BE}=V_{SC}=0$, $\Delta V_{SC}=0.1V$  
• C-V on large area BC diode (only for transistors with selectively implanted collector)  
  $V_{BC}=[-BV_{CEO},0.5]V$, $V_{BE}=V_{SC}=0$, $\Delta V_{BC}=0.1V$ | $V_{BE} C_{JE}$  
$V_{BC} C_{JC}$  
$V_{SC} C_{JS}$  
$V_{BC} C_{JC}(\text{epi})$ | depletion and isolation capacitance components |
| • cold S-parameters as a function of bias on $\geq 3$ transistors with different $b_E (<< l_E)$  
  $V_{BE}=[-0.5, 0.5]V$, $V_{BC}=0$, $\Delta V_{BE}=0.1V$  
• $V_{BC}=[-BV_{CEO}, 0.5]V$, $V_{BE}=0$, $\Delta V_{BC}=0.1V$ | $V_{BE} \ S$  
$V_{BC} \ S$ | depletion and isolation capacitance components |
| • S-parameters as a function of bias on at least 3 transistors with different $b_E (<< l_E)$ :  
  $I_{C/AE}=[0.01, 2]mA/\mu m^2$ (depends on process)  
for at least 3 $V_{CE}$, e.g. $V_{CE}/V=0.5, 1.5, BV_{CEO}$ | $V_{BE} V_{CE} I_{C} I_{B} \ S$  
| | $f_T, \ \tau_f, \ \text{certain forward I-V parameters; verification}$ |
| • d.c. output characteristics (reference transistor only)  
  $V_{CE}=[0V, V_{CE,max}] @ I_{B}=\text{const} / V_{BE}=\text{const}$  
  ($V_{CE,max}<BV_{CEO}$ (high $I_{C/AE}$))  
• $I_{C/AE}=[0.01,2]mA/\mu m^2$ (depends on process !!) | $V_{CE} I_{C} I_{B} V_{BE}$ | Avalanche, certain $I_{C}$ parameters; verification |

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**HICUM Parameter determination**

- d.c. reverse characteristic (reference transistor only)
  - $V_{BC}=[0.4, 0.7] \text{V} @ V_{BE}=0\text{V}$

- Temperature dependence: e.g. $T=[-40, 75, 125] ^\circ\text{C}$
  - repeat above measurements
  - shift $V_{BE}$ bias according to temperature, assuming a TC of about -1.5mV/K

<table>
<thead>
<tr>
<th>measurement type and bias conditions</th>
<th>data</th>
<th>result</th>
</tr>
</thead>
<tbody>
<tr>
<td>d.c. reverse characteristic (reference transistor only)</td>
<td>$V_{BC} I_B [I_C]$</td>
<td>BC diode current</td>
</tr>
<tr>
<td>Temperature dependence: e.g. $T=[-40, 75, 125] ^\circ\text{C}$</td>
<td>$T$, ...</td>
<td>TCs</td>
</tr>
</tbody>
</table>
5 Operating Point Information from Circuit Simulators

Below is a list of those quantities that should be provided by the circuit simulator to the model user as “operating point information”. The voltages in the expressions are defined as follows:

\[
\begin{align*}
V_{BEi} &= V_{B'} - V_{E'} \\
V_{BEx} &= V_{B*} - V_{E'} \\
V_{BCi} &= V_{B'} - V_{C'} \\
V_{BCx} &= V_{B*} - V_{C'} \\
V_{SCI} &= V_{S'} - V_{C'} \\
\end{align*}
\]

<table>
<thead>
<tr>
<th>Variable</th>
<th>Unit</th>
<th>Description</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>IB</td>
<td>A</td>
<td>Base terminal current</td>
<td>as calculated in the model</td>
</tr>
<tr>
<td>IC</td>
<td>A</td>
<td>Collector terminal current</td>
<td>as calculated in the model</td>
</tr>
<tr>
<td>IS</td>
<td>A</td>
<td>Substrate terminal current</td>
<td>as calculated in the model</td>
</tr>
<tr>
<td>VBE</td>
<td>V</td>
<td>External $BE$ voltage</td>
<td>as calculated in the model</td>
</tr>
<tr>
<td>VBC</td>
<td>V</td>
<td>External $BC$ voltage</td>
<td>as calculated in the model</td>
</tr>
<tr>
<td>VCE</td>
<td>V</td>
<td>External $CE$ voltage</td>
<td>as calculated in the model</td>
</tr>
<tr>
<td>VSC</td>
<td>V</td>
<td>External $SC$ voltage</td>
<td>as calculated in the model</td>
</tr>
<tr>
<td>BETADC</td>
<td></td>
<td>Common emitter forward current gain</td>
<td>(\frac{I_C}{I_B})</td>
</tr>
<tr>
<td>GM</td>
<td>A/V</td>
<td>Transconductance (Same definition as for SGPM) (\frac{\partial I_T}{\partial V_{BEi}})</td>
<td>(\frac{\partial I_T}{\partial V_{BEi}})</td>
</tr>
<tr>
<td>GMAVL</td>
<td>A/V</td>
<td>Transconductance for avalanche current</td>
<td>(\frac{\partial I_{AVL}}{\partial V_{BCi}})</td>
</tr>
<tr>
<td>GMS</td>
<td>A/V</td>
<td>Transconductance of the parasitic substrate PNP</td>
<td>(\frac{\partial I_{TS}}{\partial V_{BCx}})</td>
</tr>
<tr>
<td>RPIi</td>
<td>Ω</td>
<td>Intrinsic input resistance</td>
<td>(\frac{1}{r_{\pi i}} = \frac{\partial I_{BEi}}{\partial V_{BEi}})</td>
</tr>
<tr>
<td>Variable</td>
<td>Unit</td>
<td>Description</td>
<td>Definition</td>
</tr>
<tr>
<td>----------</td>
<td>------</td>
<td>-------------</td>
<td>------------</td>
</tr>
<tr>
<td>RPIx</td>
<td>Ω</td>
<td>Extrinsic input resistance</td>
<td>$\frac{1}{r_{\pi x}} = \frac{\partial I_{BEp}}{\partial V_{BEEx}} - \frac{\partial I_{BEi}}{\partial V_{BEEx}}$ (second term is due to tunnelling current)</td>
</tr>
<tr>
<td>RMUi</td>
<td>Ω</td>
<td>Intrinsic feedback resistance</td>
<td>$\frac{1}{r_{\mu i}} = \frac{\partial I_{BCi}}{\partial V_{BCi}} - \frac{\partial I_{AVL}}{\partial V_{BCi}}</td>
</tr>
<tr>
<td>RMUx</td>
<td>Ω</td>
<td>Extrinsic feedback resistance</td>
<td>$\frac{1}{r_{\mu x}} = \frac{\partial I_{BCx}}{\partial V_{BCx}}$</td>
</tr>
<tr>
<td>RMUs</td>
<td>Ω</td>
<td>Intrinsic substrate feedback resistance</td>
<td>$\frac{1}{r_{\mu s}} = \frac{\partial I_{SC}}{\partial V_{SCI}}$</td>
</tr>
<tr>
<td>RO</td>
<td>Ω</td>
<td>Output resistance (same definition as for SGPM)</td>
<td>$\frac{1}{r_o} = -\frac{\partial I_T}{\partial V_{BCi}}</td>
</tr>
<tr>
<td>ROs</td>
<td>Ω</td>
<td>Output resistance for the parasitic substrate PNP</td>
<td>$\frac{1}{r_{os}} = -\frac{\partial I_{TS}}{\partial V_{SCI}}$</td>
</tr>
<tr>
<td>CPIi</td>
<td>F</td>
<td>Total intrinsic $BE$ capacitance</td>
<td>$C_{\pi i} = C_{jEi} + C_{dE}$</td>
</tr>
<tr>
<td>CPIx</td>
<td>F</td>
<td>Total extrinsic $BE$ capacitance</td>
<td>$C_{\pi x} = C_{iEp} + C_{Epar}$</td>
</tr>
<tr>
<td>CMUi</td>
<td>F</td>
<td>Total intrinsic $BC$ capacitance</td>
<td>$C_{\mu i} = C_{jCi} + C_{dC}$</td>
</tr>
<tr>
<td>CMUx</td>
<td>F</td>
<td>Total extrinsic $BC$ capacitance</td>
<td>$C_{\mu x} = C_{jCx} + C_{Cpar} + C_{dS}$</td>
</tr>
<tr>
<td>CCS</td>
<td>F</td>
<td>CS junction capacitance</td>
<td>$C_{jS}$</td>
</tr>
<tr>
<td>RBI</td>
<td>Ω</td>
<td>Internal base resistance</td>
<td>as calculated in the model</td>
</tr>
<tr>
<td>CRBI</td>
<td>F</td>
<td>Shunt capacitance across RBI</td>
<td>as calculated in the model</td>
</tr>
<tr>
<td>TF</td>
<td>s</td>
<td>Total forward transit time</td>
<td>as calculated in the model</td>
</tr>
<tr>
<td>FT</td>
<td>Hz</td>
<td>Transit frequency (still simplified expression, but improved vs. SGPM)</td>
<td>$\frac{g_m}{C_{BE} + C_{BC} + (\tau_f + r C_{BC})g_m}$, $C_{BE} = C_{\pi i} + C_{\pi x}$, $C_{BC} = C_{\mu i} + C_{\mu x}$, $r = r_{Cx} + r_{E} + r_{B}/\beta_0$</td>
</tr>
<tr>
<td>Variable</td>
<td>Unit</td>
<td>Description</td>
<td>Definition</td>
</tr>
<tr>
<td>----------</td>
<td>------</td>
<td>-----------------------------</td>
<td>---------------------------------------------------------------------------</td>
</tr>
<tr>
<td>VEF</td>
<td>V</td>
<td>Effective forward Early voltage</td>
<td>$I_T \left( \frac{\partial I_T}{\partial V_{CEi}} \right)<em>{V</em>{BEi}}^{-1} - V_{CEi}$</td>
</tr>
<tr>
<td>VER</td>
<td>V</td>
<td>Effective inverse Early voltage</td>
<td>$I_T \left( \frac{\partial I_T}{\partial V_{BEi}} \right)<em>{V</em>{BCi}}^{-1} - V_{BEi}$</td>
</tr>
</tbody>
</table>
6 Experimental Results

This chapter contains selected examples that demonstrate HICUM’s capabilities of modelling bias, frequency, geometry and temperature dependent transistor behaviour. If not specified otherwise, all results were obtained using a scalable single basic parameter set (cf. chapter 3 and 4). The results cover not only a large variety of processes, ranging from low-speed (6 GHz) to high-speed (50 GHz SiGe) processes and even an example for a vertical pnp, but also various modes of operation (d.c. small-signal, large-signal). The major emphasis is on high-frequency (h.f.) characteristics and figures of merit that are related to h.f. (circuit) applications. Considering the above mentioned variables (bias, geometry, temperature, frequency), model verification is becoming a quite difficult task, the effort of which is often severely underestimated.

Wherever possible, the following comparisons are performed in normalized form and in variables that are related to circuit design; for instance, often the current density $I_C/A_E$ is employed (to allow process comparisons), and the bias points are defined by $(I_C/A_E,V_{CE})$. The results do not contain examples for junction capacitance modelling, which has already been shown to be accurate. The experimental results given below cover the following areas:

- d.c. characteristics including I-V and current gain curves as well as conductances vs. bias.
- Bias dependence of transit time $\tau_f$ and transit frequency $f_T$. An accurate approximation of the transit time and the junction capacitances, which are a fundamental (linearly independent) variables in HICUM, guarantee an accurate modelling of composite parameters, such as $f_T$ and $\gamma$-parameters.
- For small-signal characteristics, $\gamma$-parameters are preferred, since they can be easier linked directly to elements in the transistor equivalent circuit (e.g. [14,29,38]). The examples contain comparisons of all four $\gamma$-parameters vs. frequency, bias, and geometry.
- High-speed switching is difficult to measure directly and accurately for today’s fast transistors; therefore, HICUM was verified by 2D and 3D mixed-mode device/circuit simulation [39]. For older (slower) processes, however, HICUM could be verified experimentally [26,32].
- Temperature dependent modelling has been pursued and compared to experimental data for several process generations (e.g. [32,33,43]), leading to reliable model formulations.
- Noise: both $1/f$ and high-frequency noise have been investigated as a function of bias, frequency and geometry (cf. [5,6,7,9]) and have been compared to measurements.
• Non-linear h.f. distortion can be considered as another way to verify a model’s large-signal behaviour. In the presented examples, the output power $P_{out}$ as response to a single-tone input power $P_{in}$ is compared to measurements over frequency, bias and geometry for different types of transistors.

• Predictive and statistical modelling capability is important for reducing design cycle time, but have not been included for bipolar applications in commercial simulators and design tools in a physics-based and generic way. The given examples show $f_T$ as one of several useful figures of merit (FoM) for high frequency applications; compared to other h.f. FoMs, $f_T$ is clearly defined and can most easily be measured, although its measurement time is still not suitable for statistical data acquisition.

• Circuit results have been included for a CML ring-oscillator as standard benchmark circuit for digital applications. Sufficiently simple benchmark circuits for wireless applications are more difficult to obtain.
6.1 DC characteristics

Comparison between measurement (symbols) and HICUM (solid lines) from a single transistor parameter extraction for a 12 GHz bipolar transistor [4]: (a) Gummel plot; (b) current gain. $V_{BC}/V = 0,-2,-4$; emitter size: $0.6*4.8\mu m^2$
Comparison between measurement (symbols) and HICUM (solid lines) from a single transistor parameter extraction for a 12 GHz bipolar transistor [4]: (a) output characteristics for $I_B=$const; (b) output conductance $dI_C/dV_{CE}$; emitter size: 0.6*4.8µm²
Comparison between measurement (symbols) and HICUM (solid lines) for a 25 GHz bipolar transistor: (a) Gummel plot; (b) normalized transconductance. $V_{CE}/V=0.5, 0.8, 1.5, 3$; emitter size: $0.4 \times 14 \mu m^2$
Comparison between measurement (symbols) and HICUM (solid lines) for a 25 GHz bipolar transistor: (a) output characteristics for $V_{BE}=\text{const}$; (b) output conductance $dI_C/dV_{CE}$; emitter size: $0.4*14\mu m^2$. 
Comparison between measurement (symbols) and HICUM (solid lines) for a 45 GHz IBM SiGe bipolar transistor [49,50]: (a) collector current density; (b) base current density.

$V_{CE} = 0.8, 1.6, 2.4$; emitter size: $0.5 \times 10 \mu m^2$. Self-heating and avalanche breakdown are quite pronounced for this transistor.
6.2 Transit frequency and transit time

Transit frequency vs. collector current density \((V_{BC}=\text{const})\) for different bipolar processes. Comparison between measurement (symbols) and HICUM (solid lines) from single transistor parameter extraction: (a) emitter size \(0.5*10^2\mu m^2\); \(V_{BC}/V=0,-5,-10\) (the dashed lines are the results of the SPGM) \([18,43]\); (b) emitter size \(0.6*4.8\mu m^2\); \(V_{BC}/V = 0.5, 0, -0.5, -2, -4\) \([4,18]\).
Comparison between measurement (symbols) and HICUM (solid lines) for a 25GHz bipolar process [43]: (a) transit frequency; (b) transit time. Emitter size 0.4*14µm², $V_{CE}/V=0.5,0.8,1.5,3$. 

(c) M. Schroter & A. Chakravorty
Comparison for the bias dependent transit frequency between measurement (symbols) and HICUM (solid lines) for a 25GHz bipolar process. Transistor size: (a) 1.2*14 µm²; (b) 0.4*1.4 µm². $V_{CE}$/V = 0.5, 0.8, 1.5, 3.
Bias dependent transit frequency of an IBM SiGe bipolar transistor. Comparison between measurement (symbols) and HICUM (solid lines) [50]; emitter size 0.5*10\(\mu\)m\(^2\); \(V_{CE}/V=0.8,1.6,2.4\).

Bias dependent transit frequency of a SiGe bipolar process [4]. Comparison between measurement (symbols) and HICUM (solid lines); emitter size 0.4*2\(\mu\)m\(^2\); \(V_{BC}/V = 0.5, 0, -0.5, -1, -1.5\).
6.3 High-frequency small-signal characteristics

Note: \( \text{real}\{y_{12}\} \) is very small and usually of little practical interest, but can cause the modelled phase of \( y_{12} \) to deviate from measurements.

Frequency dependence of \( Y \)-parameters for a 12 GHz transistor (0.6*4.8 \( \mu \)m\(^2\)) at \( I_C/A_E = 0.1 \text{mA}/\mu \text{m}^2 \), \( V_{BC} = 0.5 \text{V} \) (cf. \( f_T \) curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8 \mu m^2) at $I_C/A_E = 0.34$ mA/\mu m^2, $V_{BC} = 0.5$ V (cf. $f_T$ curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8 µm²) at $I_C/A_E = 0.38$ mA/µm², $V_{BC} = -1$ V (cf. $f_T$ curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.
Frequency dependence of S-parameters (in Smith and polar chart) for a 12 GHz transistor (0.6*4.8\(\mu\)m\(^2\)) at \(I_C/A_E = 0.38\) mA/\(\mu\)m\(^2\), \(V_{BC} = -1\) V (cf. \(f_T\) curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.
Frequency dependence of S-parameters (in magnitude and phase) for a 12 GHz transistor (0.6*4.8 µm²) at $I_C/A_E = 0.38$ mA/µm², $V_{BC} = -1$ V (cf. $f_T$ curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.
Frequency dependence of H-parameters for a 12 GHz transistor (0.6*4.8 $\mu$m$^2$) at $I_{C/A_E} = 0.38$ mA/$\mu$m$^2$, $V_{BC} = -1$ V (cf. $f_T$ curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8 $\mu m^2$) at $I_C/A_E = 0.12$ mA/$\mu m^2$, $V_{BC} = -3$ V (cf. $f_T$ curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8 µm²) at \( I_C/A_E = 0.425 \text{ mA/µm}^2 \), \( V_{BC} = -3 \text{ V} \) (cf. \( f_T \) curves): comparison between measurement (symbols) [4] and HICUM (lines). Single transistor parameter extraction.
Y-parameters as a function of collector current density for a 12 GHz transistor (0.6*4.8 µm²) at \( f = 1 \) GHz: comparison between measurement (symbols) and HICUM (lines). \( V_{CB}/V = -0.5, 0, 0.5, 2, 4 \).
Frequency dependence of Y-parameters for a 25 GHz transistor (0.4*14µm²) at $I_{CE}/A_{E} = 0.1$ mA/µm², $V_{CE} = 0.5$ V (cf. $f_T$ curves): comparison between measurement (symbols) and HICUM (lines).
Frequency dependence of Y-parameters for a 25 GHz transistor (0.4*14 µm²) at $I_C/A_E = 0.56$ mA/µm², $V_{CE} = 0.5$ V (cf. $f_T$ curves): comparison between measurement (symbols) and HICUM (lines).
Frequency dependence of Y-parameters for a 25 GHz transistor (0.4*14µm²) at $I_{C/AE} = 0.67$ mA/µm², $V_{CE} = 3$ V (cf. $f_T$ curves): comparison between measurement (symbols) and HICUM (lines).
Y-parameters as a function of collector current density ($V_{CE} = $ const.) for a 25 GHz transistor (0.4*14µm$^2$) at $f = 1$ GHz: comparison between measurement (symbols) and HICUM (lines). $V_{CE}/V = 0.5, 0.8, 1.5, 3$. 
Y-parameters as a function of collector current density ($V_{CE}$ = const.) for a 25 GHz transistor ($1.2*14\mu m^2$) at $f$ = 1 GHz: comparison between measurement (symbols) and HICUM (lines). $V_{CE}$/V = 0.5, 0.8, 1.5, 3.
Unilateral gain $G_U$ as a function of frequency for a 12 GHz transistor (0.6*4.8µm²) at various bias points. Comparison between measurement (symbols) and HICUM (lines): (a) $V_{BC} = -1$ V; (b) $V_{BC} = -2$ V. Note the high accuracy even at current densities far beyond $I_C/A_E(@peak f_T)$. 
Unilateral gain $G_U$ as a function of frequency for a 25 GHz transistor ($0.4\times14\mu m^2$) at various bias points. Comparison between measurement (symbols) and HICUM (lines): (a) $V_{CE} = 0.5$ V; (b) $V_{CE} = 0.8$ V. Note the high accuracy even at current densities far beyond $I_C/A_E (@peak f_T)$. 
6.4 High-speed transient (switching) operation

(2D mixed-mode device/circuit simulation [39]; for experimental results of an older process see [26])

(a) Transistor inverter (worst-case for switching behaviour comparison). (b) Transit time vs. collector current density of a 14 GHz bipolar transistor. (c) Switching-on and -off behavior for $i_C$ (top) and $i_B$ (bottom) into and out of, respectively, the bias point $A_2$ in Fig. (b). Comparison between device simulation (solid lines), HICUM with NQS effects (dash-dotted lines), and HICUM without NQS effects (dashed lines) [39].
6.5 Temperature dependence

6.5.1 DC characteristics

Comparison between measurement (symbols) and HICUM (solid lines) for a 25 GHz bipolar transistor: collector current density $I_C/A_E$ vs. $V_{BE}$ for different temperatures. Emitter size: 0.4*14 $\mu$m$^2$; $V_{BC} = 0$ V.
6.5.2 AC characteristics

(a) Transit time and (b) transit frequency vs. $I_{C}/A_{E}$ for $T = 125$ C: comparison between measurement (symbols) and HICUM (solid lines) [43]. Emitter size: $0.4*14 \, \mu m^2$; $V_{CE}/V = 0.5,0.8,1.5,3$. Note, that the results were generated with a single model parameter set, except for the temperature coefficients of $\tau_0$. 
6.6 Low-frequency noise

Collector current noise spectral density $S_{ic}$ vs. frequency $f$ for 25 GHz transistors at $T = 25$ C and various bias points $I_C$ (cf. insert) and $V_{CE} = 1$ V. Comparison between measurement (symbols) and HICUM (lines): (a) $A_{E0} = 0.4*14 \mu m^2$, (b) $A_{E0} = 0.8*14 \mu m^2$. 
6.7 High-frequency noise

Minimum noise figure $F_{\text{min}}$ vs. frequency $f$ for a 25 GHz transistor. Comparison between measurement (symbols) and HICUM (lines): (a) emitter size is $4 \times 0.4 \times 21 \mu m^2$, $I_C/A_E = 0.405 mA/\mu m^2$, $V_{CE} = 1V$; (b) emitter size is $0.8 \times 14 \mu m^2$, $I_C/A_E = 0.03 mA/\mu m^2$, $V_{CE} = 1V$.

Comparison between measurement (symbols) and HICUM (lines) for a 25 GHz transistor ($4 \times 0.4 \times 21 \mu m^2$): (a) Minimum noise figure $F_{\text{min}}$ vs. collector current density $I_C/A_E$; (b) equivalent noise resistance $R_n$ vs. collector current density. $f/\text{GHz} = 1, 2, 3$; $V_{CE} = 1V$. 
6.8 High-frequency distortion

Some general remarks are required for explaining and understanding the distortion results.

The transistors were measured on-wafer in a 50Ω system using the same h.f. pad configuration that is employed for small-signal S-parameter measurements. An automated measurement system was set-up which facilitates bias point sweeps [20,45,46]. The system was carefully calibrated in order to take into account all losses up to the device and to accurately obtain both output power $P_{in}$ and input power $P_{out}$ at the transistor terminals for all relevant frequencies. Single-tone measurements were performed at four different fundamental frequencies $f_1/\text{GHz} = (0.05, 0.1, 0.9, 1.8)$. The two low frequencies at 50 and 100 MHz were chosen to be able to separate later the cause of non-linearities during model comparison. The following table shows the relation between $P_{in}$ specified in dBm by the power sweeper (defined for a 50Ω load) and the respective voltage amplitude.

<table>
<thead>
<tr>
<th>$P_{\text{dBm}}$</th>
<th>-40</th>
<th>-30</th>
<th>-20</th>
<th>-10</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\hat{v}$ [V]</td>
<td>6.4</td>
<td>20</td>
<td>64</td>
<td>200</td>
</tr>
</tbody>
</table>

As response at the output, the signals at the respective fundamental frequency as well as the second and third harmonic frequency ($f_2$ and $f_3$) were measured with a spectrum analyser for different transistor types. The table below lists the frequencies that belong together. The resulting $P_{out}$ at the various frequencies can then be compared to model characteristics as a function of d.c. bias and geometry. Figures of merit, such as the 1dB compression point and harmonic distortion, can also be calculated.

<table>
<thead>
<tr>
<th>$f_1$/GHz</th>
<th>0.05</th>
<th>0.1</th>
<th>0.9</th>
<th>1.8</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_2$/GHz</td>
<td>0.1</td>
<td>0.2</td>
<td>1.9</td>
<td>3.6</td>
</tr>
<tr>
<td>$f_3$/GHz</td>
<td>0.15</td>
<td>0.3</td>
<td>2.7</td>
<td>5.4</td>
</tr>
</tbody>
</table>

For circuit simulation, the periodic steady-state method available in SPECTRE-RF was used. However, time-domain based simulators seem to generate an incorrect d.c. component (probably converted from the second harmonic) at the transistor input, which causes the d.c. bias point to run
away at high input power. This (probably) numerical effect, which should not occur according to the measurement set-up, was not observed during harmonic balance simulations (using HP-MDS) with the same circuit and parameters. A corresponding correction algorithm was developed and implemented in MATLAB, the results of which were verified by HP-MDS.

For logistical reasons the measurements were carried out on a different die of the same wafer the parameter extraction was performed on. Process variations across the wafer might cause slightly increased deviations between model and measurements. Nevertheless, the model still turned out to be quite accurate.
$P_{out}$ vs. $P_{in}$ for $f_0 = 0.9$ GHz; comparison between measurement (symbols) and HICUM (lines):
(a) 10 GHz (power) transistor (0.4*14$\mu$m$^2$) at $I_C/A_E = 0.05$ mA/$\mu$m$^2$, $V_{CE} = 0.8$ V;
(b) 25 GHz transistor (0.4*14$\mu$m$^2$) at $I_C/A_E = 0.13$ mA/$\mu$m$^2$, $V_{CE} = 3$ V.
$P_{out}$ vs. collector current density $I_C A_E$ at $f_0 = 0.9$ GHz for a 10 GHz (power) transistor ($0.4 \times 14 \mu m^2$); comparison between measurement (symbols) and HICUM (lines):
(a) $P_{in} = -20$ dBm; (b) $P_{in} = -10$ dBm. $V_{CE} = 0.8$ V.
$P_{out}$ vs. collector current density $I_C/A_E$ at $f_0 = 0.9$ GHz for a 25 GHz transistor ($0.4*14\mu m^2$); comparison between measurement (symbols) and HICUM (lines):

(a) $P_{in} = -20$ dBm; (b) $P_{in} = -10$ dBm. $V_{CE} = 0.5$ V.
$P_{out}$ vs. collector current density $I_{C}/A_{E}$ at $f_0 = 0.9$ GHz for a 25 GHz transistor (0.4*14µm²); comparison between measurement (symbols) and HICUM (lines):
(a) $P_{in} = -20$ dBm; (b) $P_{in} = -10$ dBm. $V_{CE} = 3$ V.
$P_{out}$ vs. collector current density $J_C/A_E$ at $f_0 = 1.8$ GHz for a 25 GHz transistor (0.4*14$\mu$m$^2$); comparison between measurement (symbols) and HICUM (lines):
(a) $P_{in} = -20$ dBm, $V_{CE} = 0.5$ V; (b) $P_{in} = -10$ dBm, $V_{CE} = 3$ V.
**6.9 Predictive modelling**

Transit frequency vs. collector current density for several process variations: base line (circles), 10% decrease of selectively implanted collector dose (squares), 25% increase of epi width $w_C$ (diamonds). Comparison between measurement (symbols) and HICUM predictions (solid lines). $V_{CE} = 0.8$ V; emitter size: $0.4 \times 14 \, \mu \text{m}^2$.

Collector current density at fixed $V_{BE} = 0.8$V for the same process variants as above; comparison between measurement (o) and HICUM predictions (-). $V_{CE} = 0.8$ V; Emitter size: $0.4 \times 14 \, \mu \text{m}^2$
Transit frequency vs. collector current density for several variations of a “high-voltage” process: base line (circles), ≈5% increase of epi collector doping (squares), 25% increase of epi width $w_C$ (diamonds). Comparison between measurement (symbols) and HICUM predictions (solid lines). $V_{CE} = 0.8$ V; emitter size: 0.4*14 µm².
6.10 Statistical modelling

Statistical distribution curves of peak $f_T$ for a “high-speed” process. Comparison between (a) measurements and (b) HICUM predictions from process monitors. $V_{CE} = 2$ V; emitter size: $0.4 \times 14 \mu m^2$. The results were obtained from 5 different lots.
Statistical distribution curves of peak $f_T$ for transistors with 0.4*14µm$^2$ emitter size. Comparison between measurements (histogram and solid lines) and HICUM predictions from process monitors (dashed lines): (a) “high-speed” process; (b) “high-voltage” process. The results were obtained from 5 different lots.
6.11 Circuit results

A few remarks are required here. In principle, there is agreement between design and modelling engineers that model validation on benchmark circuits is beneficial for both sides (cf chapter 4). However, this validation loop is rarely closed in an industrial environment for various reasons, such as simply the large schedule and product pressure on one hand and the very limited resources on the other hand. In addition, it is difficult to obtain agreement on which benchmark circuits satisfy at least the majority of design applications. For digital applications, often frequency dividers and ringoscillators consisting of CML or ECL gates are employed; experimental results for the latter will be shown below. For h.f. analog (e.g., wireless) applications, not only the selection but also the design and testing itself is much more difficult. A larger variety of designs that are suited for on-wafer testing are required. As of now, results of only few production circuits are available that agree well with model “predictions”, but which have not been included here due to proprietary reasons.
Oscillation frequency $f_{osc}$ vs. current density ($I_{tail}/A_E$) per stage for a CML ring-oscillator fabricated in a 25 GHz process; comparison between measurement (symbols) and HICUM (lines). Due to power considerations, the smallest manufacturable emitter size (0.4*0.7μm$^2$) has been used; no specific or other model parameters were adjusted for this example.
7 Appendix: Derivation of some important model equations

The derivation of the basic formulation of the generalized ICCR (GICCR) [36] requires the following assumptions:

- A one-dimensional transistor structure is considered, with the emitter contact at the monosilicon surface and the collector contact at the transition from the “lightly”-doped collector region to the buried layer. The vertical ordinate is designated with \( x \) and is omitted in the following derivation from the indices for reasons of better legibility and understanding.
- The volume recombination in above region is negligible.
- The time derivative is zero; in general, it is sufficient though to assume quasi-static operation.
- Effects such as thermionic emission and tunneling across the junctions are neglected; they need to be accounted for by separate terms and can - in principle - be combined with the GICCR solution.

It can be shown that a GICCR can also be derived for the a three-dimensional case, so that the assumption of a one-dimensional region can be dropped for a actual applications.

First, consider the electron continuity equation which, together with the second and third assumption, reads

\[
\frac{dJ_n}{dx} = q \left( R + \frac{\partial n}{\partial t} \right) = 0 .
\]  

(7.0.0-1)

This corresponds to a spatially independent electron current density,

\[
I_n = \text{const}(x) = -J_T = \frac{-I_T}{A_E} ,
\]

(7.0.0-2)

which can be expressed by the transfer current and area of the (1D) transistor. Note, that under DC operation, \( I_T = I_C \).

The derivation starts with the electron transport equation:

\[
J_n = -q \mu n \frac{d\phi_n}{dx}
\]

(7.0.0-3)

Inserting the electron density,
\[ n = n_i \exp \left( \frac{\psi - \phi_n}{V_T} \right) \]  

(7.0.0-4)

gives

\[ J_n = -q \mu_n n_i \exp \left( \frac{\psi - \phi_n}{V_T} \right) \frac{d\phi_n}{dx} = -q \mu_n n_i \exp \left( \frac{\psi}{V_T} \right) \exp \left( \frac{-\phi_n}{V_T} \right) \frac{d\phi_n}{dx}. \]  

(7.0.0-5)

Note, that \( n_i \) is the effective intrinsic carrier density; it contains for the various transistor regions possible bandgap differences, that are caused by high-doping effects and bandgap-engineering. This topic will be discussed later.

Using

\[ \frac{d\left( \exp \left( \frac{-\phi_n}{V_T} \right) \right)}{dx} = -\frac{1}{V_T} \exp \left( \frac{\phi_n}{V_T} \right) \frac{d\phi_n}{dx} \]  

(7.0.0-6)

leads to

\[ J_n = q V_T \mu_n n_i \exp \left( \frac{\psi}{V_T} \right) \frac{d\left( \exp \left( \frac{-\phi_n}{V_T} \right) \right)}{dx}. \]  

(7.0.0-7)

Separation of the differential terms gives

\[ \frac{J_n}{q V_T \mu_n n_i} \exp \left( -\frac{\psi}{V_T} \right) dx = d \left( \exp \left( -\frac{\phi_n}{V_T} \right) \right). \]  

(7.0.0-8)

The inconvenient term \( \exp(-\psi/V_T) \) can be replaced by more useful variables such as the hole density and an \( \exp(\phi_p/V_T) \) term via the transformation,

\[ \exp \left( -\frac{\psi}{V_T} \right) = \frac{n_i \exp \left( \frac{\phi_p - \psi}{V_T} \right)}{n_i \exp \left( \frac{\phi_p}{V_T} \right)} = \frac{p}{n_i \exp \left( \frac{\phi_p}{V_T} \right)}, \]  

(7.0.0-9)
yielding

\[ \frac{J_n}{q V_T} \frac{p}{\mu_n n_i^2 \exp \left(\frac{\varphi_p}{V_T}\right)} \int_{x_l}^{x_u} d\varphi_n = d \left( \exp \left( -\frac{\varphi_n}{V_T} \right) \right) \]  \hspace{1cm} (7.0.0-10)

Integration of the above equation over the interval \([x_l, x_u]\) gives:

\[ \int_{x_l}^{x_u} \frac{J_n}{q V_T} \frac{p}{\mu_n n_i^2 \exp \left(\frac{\varphi_p}{V_T}\right)} d\varphi_n = \int_{\exp(\varphi_p(x_l)/V_T)}^{\exp(\varphi_p(x_u)/V_T)} d \left( \exp \left( -\frac{\varphi_n}{V_T} \right) \right) \]  \hspace{1cm} (7.0.0-11)

The result for the right-hand-side is

\[ \int_{\exp(\varphi_p(x_l)/V_T)}^{\exp(\varphi_p(x_u)/V_T)} d \left( \exp \left( -\frac{\varphi_n}{V_T} \right) \right) = - \left[ \exp \left( -\frac{\varphi_n(x_u)}{V_T} \right) - \exp \left( -\frac{\varphi_n(x_l)}{V_T} \right) \right]. \]  \hspace{1cm} (7.0.0-12)

The exact value of the electron quasi-fermi potentials depends on the choice of the integration limits and will be discussed later. First, the left-hand-side of (7.0.0-12) is integrated, giving after extension with the exp of the controlling (internal) base-emitter voltage, \(\exp(-V_{BEi}/V_T)\), and with the transfer current density as defined in (7.0.0-2) the general expression

\[ \int_{x_l}^{x_u} \frac{J_n}{q V_T} \frac{p}{\mu_n n_i^2 \exp \left(\frac{\varphi_p}{V_T}\right)} d\varphi_n = \int_{x_l}^{x_u} \frac{J_n}{q V_T} \frac{p}{\mu_n n_i^2 J_T \exp \left(\frac{V_{BEi} - \varphi_p}{V_T}\right)} d\varphi_p \]  \hspace{1cm} (7.0.0-13)

that contains the desired terminal variables of the 1D transistor. The reason for not using (7.0.0-2) and \(\varphi_p = V_{BEi}\) directly is the yet undefined integration interval. Equating again (7.0.0-13) and (7.0.0-12), and keeping only the desired variable \(J_T\) on the l.h.s., results in the general basic formulation
from which different forms of the ICCR can be derived. At this point, the various terms and variables as well as the choice of the integration limits need to be discussed in order to enable the derivation of a practically more applicable relation than the above one.

The electron fermi-potentials in the numerator assume their known 1D terminal values only at the contacts, i.e. if the entire 1D transistor region \([x_E, x_C]\) is chosen as integration interval,

\[
\varphi_n(x_l) = \varphi_n(x_E) = 0 \quad \text{and} \quad \varphi_n(x_u) = \varphi_n(x_C) = V_{CEi} ,
\]

making this an attractive choice, the effect of which on the denominator is discussed next.

Defining the spatially dependent weighting function in normalized form,

\[
h(x) = \frac{\mu_{n0r}n_{ir}^2}{\mu_n(x)n_i^2(x)} \frac{J_n(x)}{J_T} \frac{\exp\left(\frac{V_{BEi} - \varphi_p(x)}{V_T}\right)}{\frac{1}{h_g} h_i h_v} = h_g h_i h_v g
\]

with \(\mu_{n0r}\) and \(n_{ir}\) as mobility and intrinsic carrier density, respectively, of a reference material (e.g. the base or a point in the base region), permits to write the denominator as

\[
\int_{x_E}^{x_C} \frac{p}{\mu_n n_i^2 J_T} \exp\left(\frac{V_{BEi} - \varphi_p}{V_T}\right) dx = \frac{1}{\mu_{n0r} n_{ir} x_E} \int_{x_E}^{x_C} h(x) p(x) dx .
\]

For any bias point, the integral on the r.h.s., multiplied by \(q\), can always be written as

\[
q \int_{x_E}^{x_C} h(x) p(x) dx = \tilde{h} \bar{Q}_p ,
\]

with \(\tilde{h}\) as an average value of the weighting function and
is the 1D (i.e. per area) hole charge stored in the selected integration interval. The latter can be measured via the terminals if the integration interval is chosen properly.

A brief discussion of the weighting function follows in order to provide a better idea of the assumptions made for the ICCR and GICCR.

The weighting function $h_v$

The hole quasi-fermi potential is equal to $V_{BEi}$ at least over the base and its adjacent space charge regions as well as far into the emitter and collector region, resulting in $h_v = 1$ within the respective integration interval. This is also true in the very thin emitter region of advanced transistors. In conventional processes with larger emitter junction depth though, a significant portion of the holes injected back into the neutral emitter recombine there, leading to a slight decrease of $\phi_p$. However, the resulting deviation of $h_v$ from 1 within this region coincides with a rapid decrease of holes, so that the contribution of the product $h_v p$ to the integral is negligible. Therefore, $h_v = 1$ is a very good assumption under all relevant bias conditions.

The weighting function $h_i$

The transfer current density (at the 1D collector contact) equals the electron current density in the base and collector region. Only in the BE space-charge region and the neutral emitter region, $J_n$ can increase slightly as a result of the back injection of holes and the corresponding recombination. The maximum increase occurs at the emitter contact $x_E$:

$$J_n(x_E) = J_T + J_p(x_E).$$

(7.0.0-20)

The maximum possible increase occurs for opaque emitters, where $J_p(x_E) = J_B$, and is given by

$$\max\{ h_i \} = h_i(x_E) = 1 + \frac{J_B}{J_T} = 1 + \frac{1}{B}$$

(7.0.0-21)
with B as the DC current gain. As a consequence, for the vast majority and, particularly advanced bipolar transistors, \( h_i = 1 \) is a good assumption under all relevant bias conditions.

**The weighting function \( h_g \)**

High-doping effects as well as intentional bandgap grading in heterojunction transistors can cause \( n_i^2 \) values to differ by orders of magnitude in the various transistor regions. In addition, also the mobility varies significantly within the transistor as a function of both doping and bias (via the electric field). The variation caused by the latter is most pronounced in the BC junction and collector region. In general though, \( \mu_n \) and \( n_i \) possess an opposite dependence on doping, leading to a partial compensation within \( h_g \). However, the influence of \( n_i \) still remains much stronger than that of \( \mu_n \). As a consequence, the weighting function \( h_g \) deviates strongly from 1 and has to be considered for all processes. Note, that the index "\( g \)" has been chosen to indicate the major factor of influence, namely the bandgap in the effective intrinsic carrier concentration. Nevertheless, a spatially dependent function \( h_g \) can still be accommodated in a compact model formulation as shown below.

Overall, for properly designed transistors the weighting function \( h \) consists only of the contribution of \( h_g \), so that the average value in (7.0.0-18) is given by

\[
\bar{h} = \bar{h}_g = \frac{\mu_n n_{ir} n_i^2}{\mu_n n_i^2}.
\]

(7.0.0-22)

Note that the bias dependence of \( \bar{h} \) can also be caused by a bias dependent hole distribution within the transistor, even if \( h(x) \) does not depend on bias; e.g., at high current densities, \( p(x) \) can spread into the collector in which \( n_i^2 \) might be few orders of magnitude smaller than in the base, so that the collector portion of the hole charge has to be weighted much stronger than the base portion and can, therefore, still cause a significant contribution to the overall integral, although the charge in the collector might still be very small [36]!

Since the major contribution to the integral comes from the base region, where the hole density is largest, the only other relevant contributions will come from those regions, where the hole den-
sity has not dropped to insignificant values. In other words, the regions towards the contacts do not contribute to the integral and are irrelevant for the discussion on how to chose the integration interval for the denominator of (7.0.0-14). Of the infinite number of possible integration intervals, the two most important choices are:

- If the base region is chosen as integration interval, \( \bar{h} \) can be shown to be only very weakly bias dependent for homojunction transistors. The main disadvantages, however, are (i) the unknown and strongly bias dependent values for the electron quasi-fermi potentials at the base region boundaries, which are not easily accessible by measurements, and (ii) the difficulty to measure the base hole charge separately (and to extract the corresponding model parameters). In addition, the bias dependence of \( \bar{h} \) will not be as weakly dependent anymore for drift HBTs.

- If the entire 1D transistor region is chosen as integration interval, \( \bar{h} \) is expected to exhibit a larger bias dependence than for homojunction transistors. It has been shown though for bipolar technologies over (at least) the past 25 years that the bias dependence of \( \bar{h} \) is negligible in the bias region of practical interest. As an advantage of choosing the 1D contacts for boundary conditions, the electron quasi-fermi potentials are well-known and given by (7.0.0-15).

For the reasons given above, the entire (1D) transistor region has been chosen as integration interval. The resulting transfer current expression then reads

\[
J_T = q V_T \frac{\exp \left( \frac{V_{BEi}}{V_T} \right) - \exp \left( \frac{V_{BCi}}{V_T} \right)}{x_C},
\]

(7.0.0-23)

\[
\int \frac{p}{\mu_n n_i^2} dx
\]

\[
\int \frac{\mu_n n_i^2}{\mu_n n_i^2} p dx
\]

or after introducing the weighting function \( h_g \) according to (7.0.0-16)

\[
J_T = q^2 V_T \mu_{n0} n_i^2 \frac{\exp \left( \frac{V_{BEi}}{V_T} \right) - \exp \left( \frac{V_{BCi}}{V_T} \right)}{x_C},
\]

(7.0.0-24)
7.1 The ICCR (homojunction transistors)

Inserting (7.0.0-15), (7.0.0-18) with \( h = \bar{h}_{g} \) as well as \( V_{BCi} = V_{BET}V_{CEi} \) into (7.0.0-14) yields

\[
J_T = q^2 V_T \mu_n n_i^2 \left( \exp\left( \frac{V_{BEi}}{V_T} \right) - \exp\left( \frac{V_{BCi}}{V_T} \right) \right) \frac{Q_p}{c_{10}} .
\] (7.1.0-25)

This equation, with

\[
c_{10} = q^2 V_T \mu_n n_i^2
\] (7.1.0-26)

is the well-known ICCR, which is very accurate for most homojunction transistors, provided that the hole charge (density),

\[
\bar{Q}_p = \bar{Q}_{p0} + \bar{Q}_{jEi} + \bar{Q}_{jCi} + \bar{Q}_f + \bar{Q}_r
\] (7.1.0-27)

is accurately modeled as a function of bias. The latter is a prerequisite for the description of high-speed applications in any way. Also, since the hole charge has to be continuously differentiable with respect to bias, the transfer current is also automatically continuously differentiable over all bias regions and is modeled via a single-piece formulation.

Fig. illustrates the impact of the various hole charges on the transfer current during a sweep of the BE voltage. At low current densities, the depletion charges \( Q_{jEi} \) and \( Q_{jCi} \) are the only bias dependent contributors to \( Q_p \). For constant \( V_{BC} \), the bias dependence of the BE depletion charge determines the ideality of the transfer current characteristic; for constant \( V_{BC} \), the bias dependence of the BC depletion charge determines the slope of the output characteristics and, thus, automatically takes into account the bias dependent Early voltage. At high current densities, the minority charge \( Q_f \) starts to increase rapidly exceeding the depletion charges around peak \( f_T \) and then dominating the bias dependence of \( Q_p \) beyond peak \( f_T \). As a consequence, the ideality factor of the transfer current characteristic also increases rapidly leading to a string decrease in the transcondutance. A detailed discussion of the ICCR for BJT processes can be found in, e.g., [32].
7.2 The GICCR (heterojunction transistors)

In homojunction transistors bandgap differences are caused by high-doping effects only, so that the variation in \( n_i^2 \) over the integration interval \([x_E, x_C]\) is moderate. In contrast, large bandgap differences are intentional in HBTs, leading to \( n_i^2 \) variations of orders of magnitude. As demonstrated in [36], the transfer current of (SiGe) HBTs cannot be described anymore with the ICCR. The latter can be extended though, resulting in the generalized ICCR (GICCR) which maintains the advantages of a single-piece continuously differentiable description of the main transistor current. While the integration interval and, thus, the numerator of (7.0.0-14) remain the same, the denominator of (7.0.0-14) has to be considered more carefully for HBTs.

The starting point for the extension is eq. (7.0.0-17), with \( h(x) \approx h_g(x) \) for the same reasons as discussed before, resulting in

\[
\int_{x_E}^{x_C} \frac{p}{\mu_n n_i^2} dx = \frac{1}{\mu_{n0} n_{ir}^2} \int_{x_E}^{x_C} \frac{\mu_{n0} n_{ir}^2}{\mu_n n_i^2} p(x) dx .
\]  

\[ (7.2.0-28) \]
The choice of the reference material (or reference transistor region) and its associated parameter values for $\mu_{n0r}n_{ir}^2$ is arbitrary and will be discussed later. Due to the large variation of $n_i^2$ between emitter, base and collector region, the definition of a sufficiently bias independent average value $\overline{h}_g$ is not always possible and might lead to unacceptable errors in modeling the transfer current high current densities. The goal is, therefore, to formulate the integral in terms of single charges in particular transistor regions, multiplied with proper average values of the respective weighting functions, that are both suitable for compact modeling.

In HBTs, the bandgap is significantly different in the emitter, base and collector region, while the transition from one bandgap to another usually takes place around the junction. As a consequence, partitioning of the integral into the neutral emitter, base and collector region as well as into depletion regions looks like a reasonable choice in order to obtain separate integrals in which the weighting functions are sufficiently independent on location and bias. Defining the respective average values,

$$\overline{h}_k = \overline{h}_{gk} = \int \frac{h_{gk}p(x)dx}{\int p(x)dx} = \frac{\mu_{n0r}n_{ir}^2}{\mu_{nk}n_{ik}^2}$$

with $k = (e, jei, b, jci, c)$, (7.2.0-29)

the denominator integral of the ICCR reads after multiplying with $q$

$$\overline{P}_{p,T} = \int_{x_E}^{x_C} \frac{\mu_{n0r}n_{ir}^2}{\mu_{n_i}^2}p(x)dx = \overline{P}_{p0} + h_{jEi}\overline{Q}_{jEi} + h_{jCi}\overline{Q}_{jCi} + \overline{Q}_{f,T} + \overline{Q}_{r,T} \cdot$$

(7.2.0-30)

where the base region has been chosen as reference, i.e. $\mu_{n0r}n_{ir}^2 = \mu_{nb}n_{ib}^2$. According to [36], assuming bias independent average values for the separate weighting functions leads to a significant improvement over the conventional ICCR with a sufficiently accurate description of the transfer current characteristics and the respective derivatives over the entire bias range of interest (up to very high current densities). The average weighting factors are new model parameters.

Application of the GICCR also requires the modeling of the separate portions, $\overline{Q}_{pE}$ and $\overline{Q}_{pC}$, of the total hole charge. The GICCR has been evaluated for many advanced SiGe bipolar technolo-
gies. It has been found that a constant factor $\tilde{h}$ can in fact be used for more than one bias point up to quite high current densities, thus maintaining all the advantages of the ICCR with the added benefit of being able to model HBTs in physics-based way.

For a 2D/3D GICCR, see [64].
References

[38] M. Schröter, (a) "Physical models for high-speed silicon bipolar transistors - A comparison and overview", (in German), Habilitation thesis, 1994 (excerpts are available on request);
(b) "Bipolar transistor modelling for integrated circuit design", Graduate Course, Carleton University, Ottawa, 1995 (contains large portions of (a) in English).


[54] C. McAndrew, private communication.


