4 Parameter determination

HICUM/L2 has been developed to address modeling issues related to the design of *integrated* circuits. In this case, geometry and process information are generally available, that can be used to obtain as much as possible physics-based model parameters. Besides bias, frequency and temperature, the transistor geometry can be considered as an additional independent dimension for parameter extraction the use of which helps avoiding ambiguous values compared to just fitting the terminal characteristics of a *single* device. A discussion of the advantages of the multi-geometry-based parameter extraction recommended for HICUM (and being used in the MOS area for a long time) is given in, e.g., [44]. Therefore, the description below deals with the extracting sequence that is used for generating geometry scalable HICUM parameters. For additional information of the extraction procedure see also [15].

As described in [15], the extracted model parameters for HICUM (and also for the SPICE Gummel-Poon model) are converted into a geometry and layout independent form. These so-called specific data are then used in a special program (TRADICA) to generate model parameters for arbitrary transistor configurations.

For a given process, obtaining compact model parameters of a large variety of transistor configurations, using the recommended process-based scalable approach (PBSA), involves several major steps:

- wafer selection according to certain criteria;
- deriving the relevant transistor dimensions from design rules;
- measurement of the relevant characteristics of a certain set of test structures (incl. transistors) over bias, geometry, temperature and frequency;
- extraction of (geometry) specific model parameters;
- generation of the model parameters for desired transistor configurations (either as library or directly during the circuit design phase).

The various aspects related to the above steps are briefly discussed in this chapter. In addition, an overview on the recommended sequence of parameter extraction is given in a formal way in chapter 4.5 to provide the reader with basic information, such as measurement and data requirements as well as principle procedures employed. Another purpose of this overview is also to serve as a guide line for implementing the parameter extraction methodology.

4.1 Wafer selection

There are many criteria as to which wafer should be selected or which one rejected when it comes to model parameter extraction. Below, those criteria that proved to be useful for the process-based scalable approach pursued here are briefly discussed.

As already mentioned before, the PBSA relaxes the requirements for the wafer selection, since it allows to shift the (specific) parameters later on to their desired nominal values. However, the electrical performance of the transistors (and other parameters) should not be too far off from the target specifications. Also, it is important to evaluate the process regarding geometry scalability, since non-conventional scaling requires larger effort (and time) for parameter extraction. Therefore, before a wafer is accepted for parameter extraction purposes, the following tests are recommended to be performed and evaluated:

- Measurement of a tetrode structure (for each transistor type) at zero bias, yielding roughly the internal base sheet resistance r_{SBi0};
- Measurement of a large area BC diode (i.e. without SIC) at zero bias and beyond punch through, yielding epi doping N_C and thickness w_C;
- Measurement of the bias dependent S-parameters for a typical transistor (each type) at a single CE voltage and frequency, yielding the transit frequency f_T.

The first two measurements can be performed on PCM structures. The third one is more time consuming and can be done after the first two have been evaluated. In general, though, all of the above data are usually available during process development and evaluation.

It is recommended then to obtain a wafer map that shows the uniformity of the electrical parameters r_{SBi0}, w_C, N_C, and f_T. The correlation of the latter to the first three should be checked as well as, of course, the absolute values regarding their deviation with respect to the target values.

Next, an appropriate die for parameter extraction is selected as the centre of the area with the highest uniformity. As a consequence, the chance of deviations in electrical characteristics between different transistors of the selected die is likely to be minimized.

In addition to the electrical tests, it is highly recommended to obtain pictures of the cross-section and top view (SEM and TEM pictures) of the most important transistor configurations for both extractions and applications. These pictures are usually available during process development and not only provide an impression on the actual transistor structure but also serve for verifying the tran-

sistor dimensions assumed or calculated from design rules. In the experience of the author, the information obtained from the above pictures can avoid results, that appear to be non-physical, and geometry scaling problems, that cannot be explained otherwise just by electrical measurements.

4.2 Relevant transistor dimensions

Definitions of the relevant transistor dimensions used for calculating the area and perimeter length specific model parameters are given in Fig. 4.2.0/1 for a junction isolated silicon bipolar transistor fabricated in a self-aligning base-emitter process.

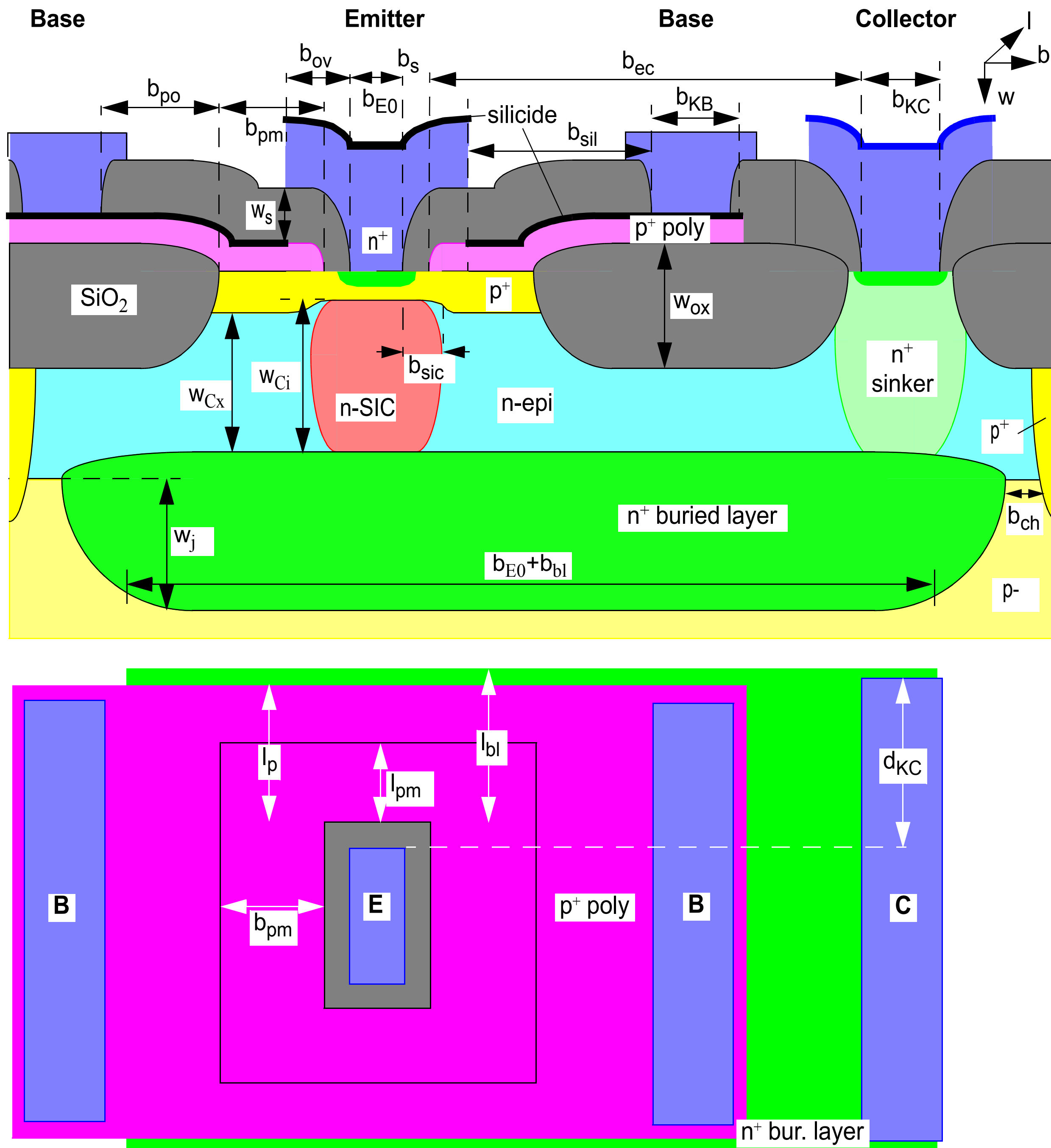

Fig. 4.2.0/1: Schematic cross-section and layout of a silicon bipolar transistor with junction isolation and self-aligned base-emitter formation.

The described parameter extraction procedure can also be applied to silicon epitaxial base transistors, including SiGe transistors. The corresponding schematic cross section and layout with the respective dimensions are shown in Fig. 4.2.0/2.

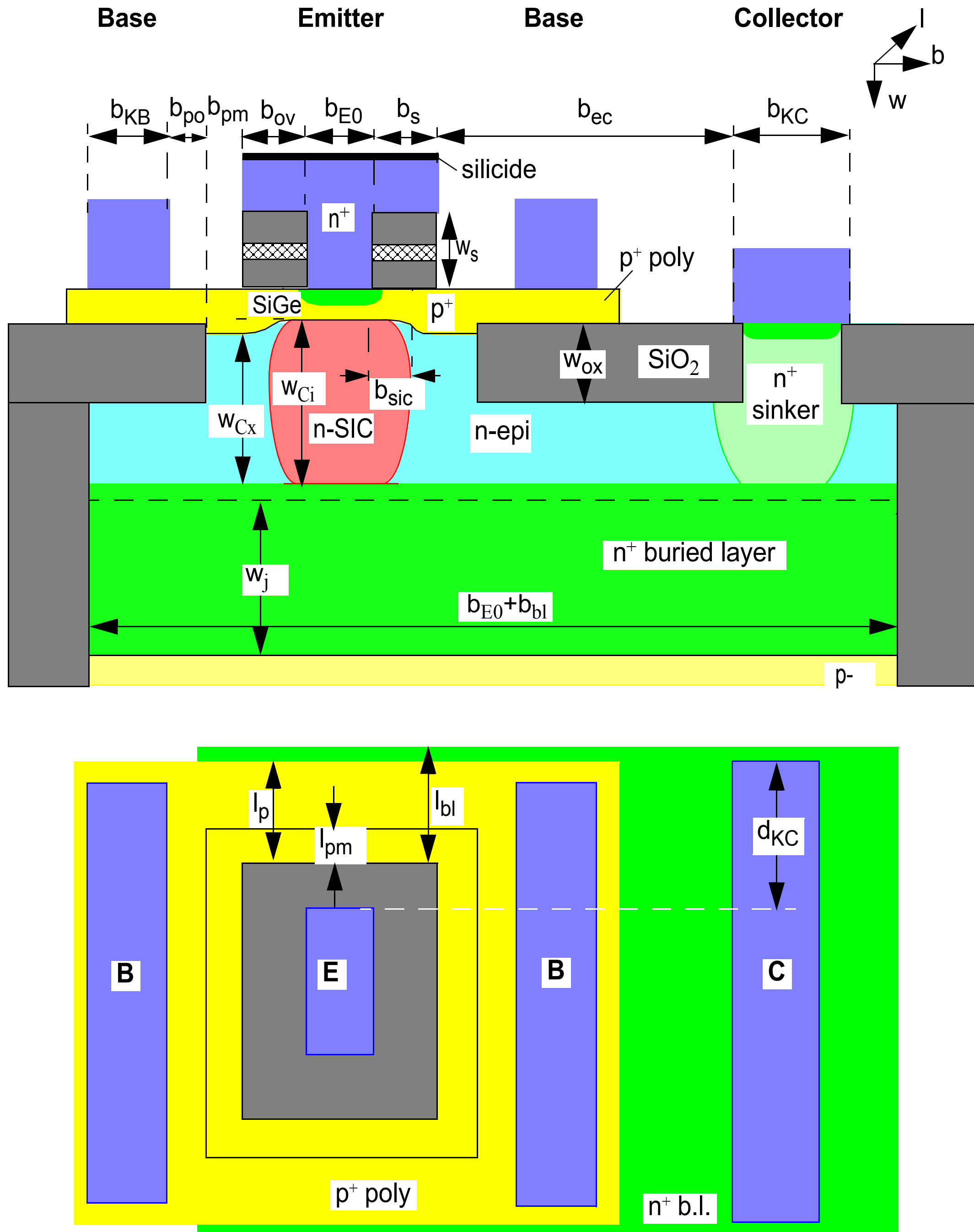

Fig. 4.2.0/2: Schematic cross-section and layout of an epitaxial base SiGe bipolar transistor with shallow and deep trench isolation.

4.3 Measurements

Parameter extraction for the PBSA relies on minimum requirements regarding measurement effort and equipment. While the set-up and detailed bias conditions (test plans) for a particular parameter determination procedure are given in the respective chapters, at this point a brief overview shall be provided on the basic and most important measurement methods, which are being employed for obtaining the data required for a variety of procedures. This chapter also serves for defining the "measurement" and "data" related terminology used throughout this documentation.

The measurements are taken on transistors and special test structures. Examples of the most important test structures suitable for PBSA are given in [15].

4.3.1 IV measurements and data

DC measurements taken, e.g., with a parameter analyser, on test structures and transistors are called IV measurements, resulting in the associated IV data. Examples are

- a forced current in a 3-terminal test structure for determining a sheet resistance and the corresponding measured voltage between the contacts or
- the collector and base current of a transistor as function of the applied voltage.

However, IV data also include the DC bias taken during S-parameter measurements (see below), while IV measurements always means a DC measurement and associated set up as defined above.

4.3.2 CV measurements and data

Capacitances with a sufficient large value can be measured with LCR or CV meters, thus the name CV measurements and CV data. This equipment usually operates at frequencies between 0.1...10 MHz. It is, therefore, only suited for measuring large size capacitances that are laid out as special test structures like in process monitors.

The designation CV data includes capacitance vs. voltage data from both CV measurements, as defined above, and from S-parameter measurements.

4.3.3 S-parameter measurements and data

Small-signal measurements at high frequencies are performed with a vector network analyser (VNA) and are taken as S-parameters, resulting in S-parameter data. Operating frequencies for obtaining accurate data are usually above 300 MHz, with an upper limit usually in the multi-10GHz

range, dependent on the respective equipment. For parameter extraction purposes, two types of S-measurement are often distinguished: (a) "cold" measurements during which the transistor is operated at reverse and very low forward bias with negligible carrier injection and current across the junctions; (b) "hot" measurements during which the transistor is operated under usual forward-bias conditions with significant carrier injection and non-negligible current across junction. The corresponding data are designated as, e.g. cold S-parameters or hot Y-parameters.

Although the operating frequencies of high-performance transistors in some of the present Si-based processes already exceed 100GHz, the corresponding parameters for modeling the high-frequency transistor can be determined at frequencies well below 100 GHz under so-called quasi-static conditions. The lower frequency limit for parameter extraction related S-parameter measurements is approximately given by the 3dB corner frequency of the common-emitter (CE) small-signal current gain. At current gains between 50 and 200, this corresponds to the range around 1GHz. One of the most important quasi-static small-signal transistor parameters for extracting model parameters is the transit frequency f_T. It has been shown in [10] that f_T can be obtained from a single frequency measurement of the small-signal CE current gain.

A typical set of data from a single-frequency bias sweep measurement includes the terminal voltages and current as well as the frequency and the four S-parameters in either magnitude and phase or real and imaginary part representation. The S-parameters can then be converted into Y-parameters at the same bias points. Next, the Y-parameters need to be de-embedded in order to eliminate the influence of parasitic elements and obtain the Y-parameters of the device under test only. From the de-embedded Y-parameters as a function of bias, a large number of HICUM model parameters can be extracted.

Generally, the bias dependence of the small-signal behavior and parameters is of great interest for parameter extraction. In many circuit design applications, the dependence of small-signal parameters on the collector current I_C at a given voltage V_{CE} is of major importance. Unfortunately, it is found very often, that S-parameters as a function of frequency are taken for bias points, that are defined by the terminal voltages V_{BE} and V_{CE}, while the terminal currents are not or cannot be monitored; the latter is often caused by, e.g., limitations of the data acquisition software or the equipment. Only with a separate DC measurement the terminal currents are then obtained, and the relationship between S-parameters and bias currents is attempted to be established. The great dan-

ger in this procedure is that the devices usually heat up differently (caused by self-heating) during the S-parameter and the pure DC measurement, leading to an incorrect relationship of the above mentioned variables. The consistent way of taking data is to monitor the current or, even better, to define the bias point by the collector current and V_{CE}. For some data acquisition software, the current can be monitored by reducing the small-signal measurements to a single frequency rather than a frequency sweep. Although in this case the "averaging" has to be increased, a somewhat shorter measurement time is often achieved (together with a large reduction in data) as well. Appropriate bias points for frequency sweep measurements can then be selected afterwards.

4.3.4 Sequence of measurements

In a production environment, measurement effort and time have to be minimized. This is done on one hand by using standard and established equipment set-ups and on the other hand by maximizing the equipment utilization in a given time frame.

Data acquisition for model parameter extraction starts at the reference temperature T_0 with simple and fast IV measurements of all special test structures used for determining sheet and contact resistances. Next, CV measurements are performed, followed by single-frequency cold and hot S-parameter measurements. The same device is probed for all bias conditions before moving the probes to the next device. These measurements provide already sufficient information for extracting more than 80% of the (specific) model parameters, the process of which can then start.

In the meantime, i.e. during parameter extraction, data acquisition continues with temperature dependent measurements, which are quite time consuming. By the time the latter measurements are completed, parameter extraction has provided an overview on the process and its actual performance, so that those bias range and points can be determined which are of interest for frequency sweeps. Frequency sweep measurements are usually required and taken only at the reference temperature. Based on the temperature and frequency dependent data, the remaining model parameters (except those for low-frequency *1/f* noise) can be extracted, and model verification can already start.

Finally, special measurements, such as those for noise and distortion, can be performed at T_0.

4.4 Flowchart and comparison to SGPM

The PBSA allows to combine the parameter extraction of different compact models with a minimum of additional effort. Fig. 4.4.0/1 visualizes the overall extraction flow including the modules that are model independent ("general") and those that are specific to the SGPM and HICUM. This provides a rough overview on the effort required to add a new model such as HICUM to an existing parameter extraction for the SGPM and vice versa (i.e. keeping the SGPM in the loop as a backup). The program TRADICA allows to generate both types of models as well as a hierarchy of SGPMs with different complexity from a single set of extracted geometry specific parameters.

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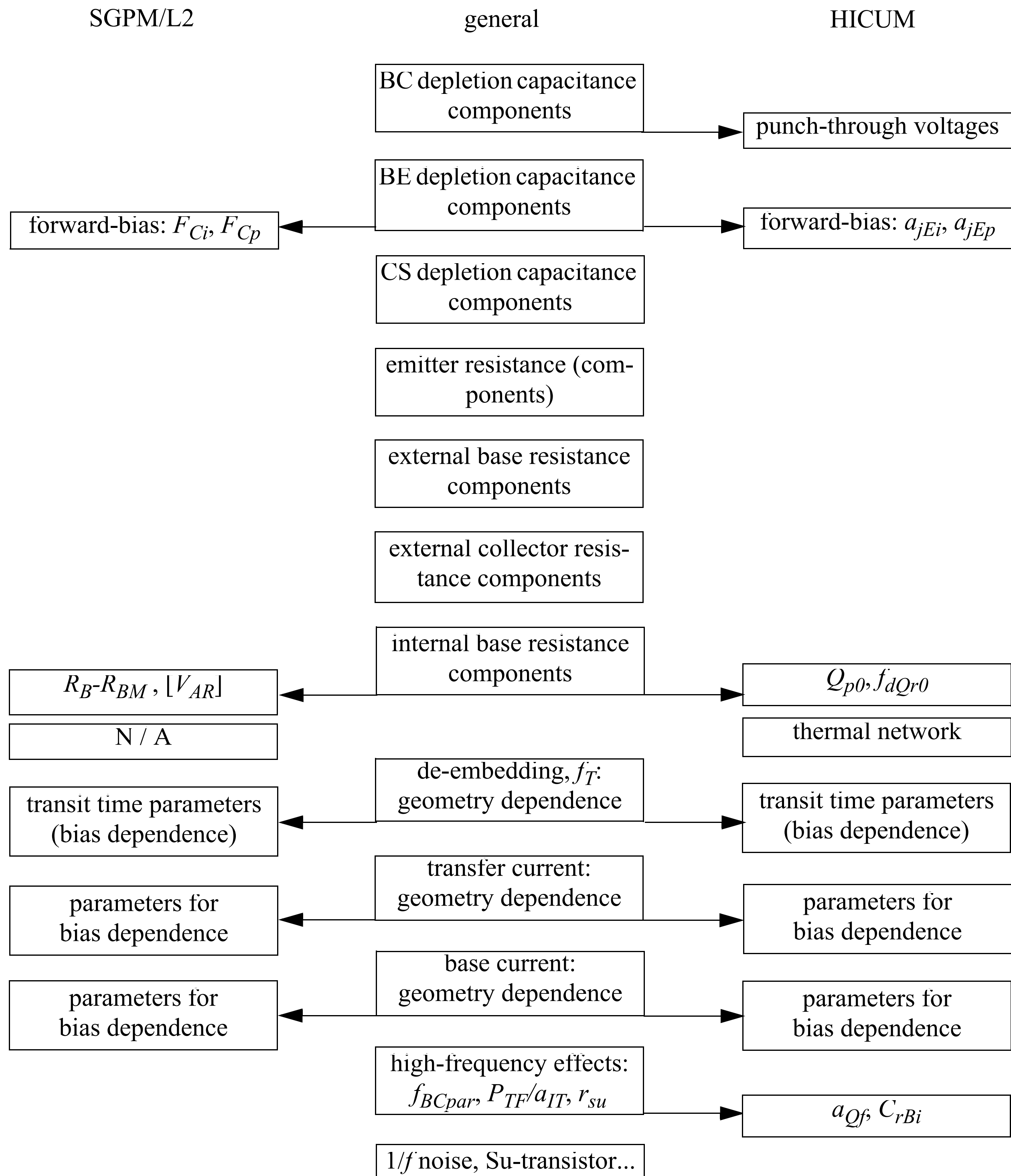

Fig. 4.4.0/1: Rough overview on the flow and modules for a combined geometry scalable parameter extraction for both SGPM and HICUM. SGPM/L2 corresponds to a similar equivalent circuit as HICUM, including, e.g., separate elements for the emitter perimeter injection and a partitioning of the base resistance and external BC capacitance.

4.5 A step by step procedure

The goal of this chapter is to give a "formal" overview on the sequence for extracting geometry scalable HICUM parameters. To keep this overview efficient, for each step only a brief description of the applied extraction procedure is provided, while for a detailed description (incl. equations) and the origin of the respective procedure, the reader is referred to one of the subsequent chapters of this documentation. One important boundary condition for developing HICUM was to enable a parameter extraction procedure in which as many as possible steps can be performed linearly independently or with only a weak interdependence, particularly for determining parameters describing first-order effects. For commercially available implementations see [61,62].

In modern bipolar technologies, often at least two types of transistors are offered: a high-performance (HP) transistor and a high-voltage (HV) transistor, that are defined by same process flow and with just one additional mask. The HP transistor is usually realized with a selectively implanted collector (SIC). It is recommended to extract first the parameters of the HV transistors and then the parameters of the HP transistors, since the HV transistor’s collector is typically realized with the background doping that is also present under the external base of the HP device. If HV transistors are not available, those ones required for extraction can usually be easily realized and should be included on a test chip. If parameters for a HV transistor without SIC have to be extracted, no respective HP device is needed.

A couple of assumptions are being made in order to apply the procedures in practice:

- A suitable wafer with the appropriate test structures and transistors has been selected that has passed the recommended acceptance check mentioned in chapter 4.1.
- All measurements that are required for a particular extraction step are available and have been properly de-embedded. It is generally preferable to convert S-parameters to Y-parameters (to be done during de-embedding in any way) and use the latter data for parameter extraction.
- The design rules and dimensions of all test structures and transistors are known and have been verified, so that all necessary geometry calculations can be performed.
- The process is geometry scalable, i.e. the profile under the emitter does not depend significantly on the emitter width. This can be checked by measuring the internal base sheet resistance as a function of emitter width (cf. [28,15]).

The information about each extraction step is contained in a small table. The meaning of the key words on the right-hand-side and the terminology used shall be briefly explained below.

- "Measurement data" characterizes the type of data required for the particular step. Acronyms such as CV, IV or cold measurements have already been defined in chapter 4.3.
- "Required model parameters" specify those ones that have to be extracted in an earlier step and are needed for the present step. They do not include dimensions, which are specified under "required geometry data".
- "Procedure" refers to the main extraction steps; the detailed background is described elsewhere.
- Under "Extracted specific parameters" those parameters are listed that are geometry independent. These parameters are used in the program TRADICA to generate geometry scalable libraries for model parameters. Of course, certain HICUM parameters, such as ratios, are geometry independent in the first place and do not need to be scaled with geometry. However, since it is useful to determined a full set of (geometry) specific parameters first and keep the data in one place before subsequent parameter (library) generation, all extracted parameters are listed here.
- "Related HICUM parameters" are those that eventually are written into a library (as model card) and are generated for a particular transistor configuration, employing a program like TRADICA.

Fig.4.5.0/2 shows a rough overview of the impact of the most important model parameters on the DC characteristics.

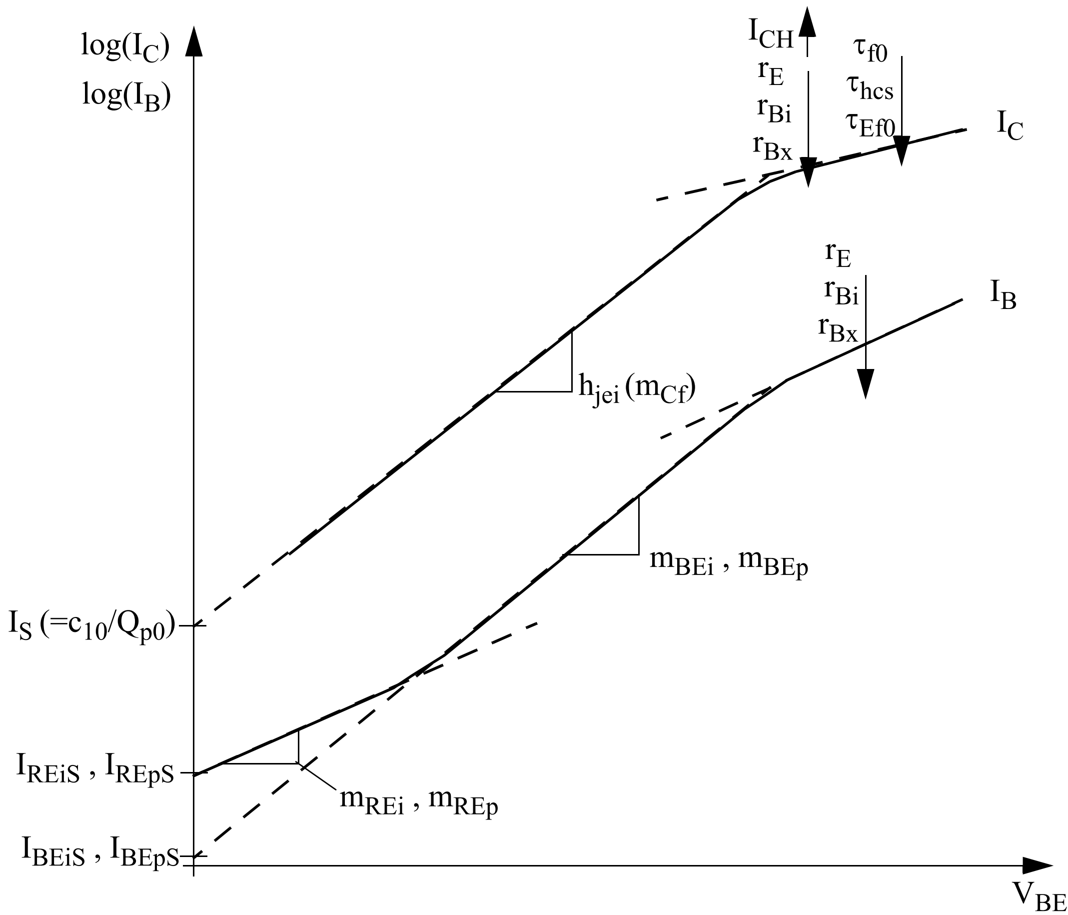

Fig. 4.5.0/2: Overview of the impact of the most important model parameters on HICUM's forward DC characteristics.

Below, the extraction sequence is outlined. Linearly independent steps are indicated by the entry "none" under "Required model parameters".

4.5.1 BC depletion and isolation capacitance

Measurement data	• cold Y-parameters of different transistor configurations • CV data of large area HV structure (optional) • CV data of large area HP structure
Required model parameters	none (optional: C_{BCpar} calculated from TRADICA for each transistor configuration)
Required geometry data	• area A_{BC} and perimeter P_{BC} of BC junction (HV transistor) • area A_{SIC} of SIC region (HP transistor)
Procedure:	• HV data: separation into bias dependent bottom and perimeter specific components of the depletion capacitance via different geometries; also, determination of specific isolation capacitance possible. • Extraction of parameters for modeling the bias dependence of above depletion capacitances. • HP CV data: extraction of SIC related parameters.
Extracted (specific) parameters	• HV data: $\bar{C}_{jCb0}$, V_{DCb}, z_{Cb}, V_{PTCb}; C'_{jCp0}, V_{DCp}, z_{Cp}, V_{PTCp}, [C'_{Cox}] • HP data: $\bar{C}_{jCi0}$, V_{DCi}, z_{Ci},V_{PTCi}
Related HICUM parameters	C_{jCx0}, V_{DCx}, z_{Cx}, V_{PTCx}, C_{BCoar},f_{BCpar}; C_{jCi0}, V_{DCi}, z_{Ci},V_{PTCi}

4.5.2 BE depletion and isolation capacitance

Measurement data and test structures	• cold and hot Y-parameters of different transistor configurations • CV data of large area structure (optional)
Required model parameters	none (optional: C_{BEpar} calculated from TRADICA for each transistor configuration)
Required geometry data	area A_{E0} and perimeter P_{E0} of emitter window
Procedure:	• Determination of C_{BE} from $1/(2\pi f_T)$ at a forward bias point. • Separation into bias dependent bottom and perimeter specific components of the depletion capacitance via different geometries; also, determination of specific isolation capacitance possible. • Extraction of parameters for modeling the bias dependence of above depletion capacitances
Extracted (specific) parameters	$\bar{C}_{jEi0}$, V_{DEi}, z_{Ei}, a_{jEi}; C'_{jEp0}, V_{DEp}, z_{Ep}, a_{jEp}, [C'_{Eox}]
Related HICUM parameters	C_{jEi0}, V_{DEi}, z_{Ei}, a_{jEi}; C_{jEp0}, V_{DEp}, z_{Ep}, a_{jEp}; C_{BEpar}

4.5.3 CS depletion capacitance

Measurement data and test structures	• cold Y-parameters of different transistor configurations • CV data of large area structure (optional, but recommended)
Required model parameters	none
Required geometry data	area A_{CS} and perimeter P_{CS} of CS junction
Procedure:	• Separation into bias dependent bottom and perimeter specific components of the depletion capacitance via different geometries. • Extraction of parameters for modeling the bias dependence of above depletion capacitances.
Extracted (specific) parameters	$\bar{C}_{jSb0}$, V_{DSb}, z_{Sb}, V_{PTSb}; C'_{jSp0}, V_{DSp}, z_{Sp}, V_{PTSp}
Related HICUM parameters	C_{jS0}, V_{DS}, z_S, V_{PTS}

4.5.4 Internal base (sheet) resistance

Measurement data	IV data on transistor tetrodes with different emitter widths: • sweep of $V_{BE} = V_{BC}$ ($V_{CE} = 0$) • sweep of V_{BE} @ $V_{BC} = 0$
Required model parameters	C_{jEi0}, V_{DEi}, z_{Ei}; C_{jCi0}, V_{DCi}, z_{Ci} (or numerical integration of associated depletion charges)
Required geometry data	width b_{E0} and length l_{E0} of emitter windows
Procedure:	• Determine internal base sheet resistance $r_{SBi}(V_{BE},V_{BC})$ from corrected data. • Extraction of parameters for modeling the bias dependence of r_{SBi}. • Determination of the link and total external resistance (used for next step)
Extracted (specific) parameters	r_{SBi0}, $\overline{Q}_{p0}$, f_{dQr0}, r_{Ss}
Related HICUM parameters	r_{Bi0}, Q_{p0}, f_{dQr0}

Note, that the model parameter f_{geo} can be (and has been) directly calculated from the transistor configuration.

4.5.5 Components of external base resistance

Measurement data	• IV data of various resistance test structures • link and total external resistance from transistor tetrodes
Required model parameters	None
Required geometry data	dimensions of the relevant regions of the test structures
Procedure:	• Determine resistance(s) from IV data and perform current spreading correction (depending on resistance type). • Extract sheet or specific contact resistance from each structure
Extracted (specific) parameters	ρ_{KB} , r_{Spo}, r_{Spm}, r_{Ssil}
Related HICUM parameter	r_{Bx}

For single device extraction, this module has to be replaced by a procedure for extracting r_{Bx}.

4.5.6 Emitter resistance

Measurement data	open collector IV data from transistor structures with different emitter size
Required model parameters	None
Required geometry data	total emitter window width A_{E0} of each transistor
Procedure:	• for each transistor: fit modified open-collector model equation to measured data • extract specific contact resistance from $r_E(1/A_{E0})$
Extracted (specific) parameter	ρ_{KE}
Related HICUM parameter	r_E

The open-collector method has been found to give reasonable and reliable results, although the current flow through the emitter window deviates from the one in usual transistor operation.

4.5.7 Components of external collector resistance

Measurement data	IV data of special resistance test structure
Required model parameters	None
Required geometry data	dimensions of the relevant regions of the test structure
Procedure:	• Determine resistance from IV data and perform current spreading correction (if required). • Extract buried layer sheet and specific contact plus sinker resistance
Extracted (specific) parameters	ρ_{KC}, r_{Sbl}
Related HICUM parameter	r_{Cx}

4.5.8 Collector current at low bias

Measurement data	IV data from transistors with different emitter size
Required model parameters	most processes: C_{jEi0}, V_{DEi}, z_{Ei}, a_{jEi} (not for "real" HBTs) optional: Q_{p0}; [C_{jCi0}, V_{DCi}, z_{Ci}, if V_{CE} = const)
Required geometry data	emitter window area of the transistors
Procedure:	• Separation into bias dependent bottom and perimeter specific current components via different geometries. • Extraction of parameters related to bias dependence from least-squares fit of log(I_C/A_E) vs. V_{BE} @ V_{BC}=0 (procedure is partially dependent on process):
Extracted (specific) parameters	γ_C, $\overline{I}_S$, [$\overline{Q}_{p0}$, m_{Cf}]
Related HICUM parameters	I_S (or c_{10}), [Q_{p0}, m_{Cf}]

4.5.9 Current across BE junction at low bias

Measurement data	IV data from transistors with different emitter size
Required model parameters	none
Required geometry data	emitter window area of the transistors
Procedure:	• Separation into bias dependent bottom and perimeter specific current components via different geometries. • Extraction of saturation current (density) and non-ideality coefficient of each component from least-squares fit of log(I) vs. V_{BE} @ V_{BC}=0
Extracted (specific) parameters	γ_B; $\overline{I}_{BEiS}$, m_{BEi}, I'_{BEpS}, m_{BEp}; $\overline{I}_{REiS}$, m_{REi}, I'_{REpS}, m_{REp}
Related HICUM parameters	I_{BEiS}, m_{BEi}, I_{BEpS}, m_{BEp}; I_{REiS}, m_{REi}, I_{REpS}, m_{REp}

4.5.10 Current across BC junction at low bias

Measurement data	IV data from transistors with different size
Required model parameters	none
Required geometry data	collector-base junction area A_{BC} and emitter window area A_{E0} of the transistors
Procedure:	• Separation into bias dependent bottom and perimeter specific current components via different geometries. • Extraction of saturation current (density) and non-ideality coefficient for each component from least-squares fit of log(I) vs. V_{BC} @ V_{BE}=0
Extracted (specific) parameters	$\overline{I}_{BCxS}$, m_{BCx}; $\overline{I}_{BCiS}$, m_{BCi}
Related HICUM parameters	I_{BCxS}, m_{BCx}; I_{BCiS}, m_{BCi}

4.5.11 Thermal resistance

Measurement data	IV data of transistors used for extraction
Required model parameters	r_E, r_{Bx}, r_{Bi}
Required geometry data	emitter window area A_{E0} of the transistors
Procedure:	• Extraction of R_{th} of each transistor from I_B as a function of dissipated power according to [50], but with known r_E.
Extracted (specific) parameter	r_{th}
Related HICUM parameter	R_{th}

4.5.12 Forward transit time

Measurement data	hot Y-parameters of different transistor configurations
Required model parameters	C_{jCi0}, V_{DCi}, z_{Ci},V_{PTCi}; C_{jCx0}, V_{DCx}, z_{Cx}, V_{PTCx}, C_{BCpar}; r_E, r_{Cx}; γ_C; [R_{th}]
Required geometry data	emitter window dimensions b_{E0} and l_{E0} of the transistors

Procedure:	• Determine transit frequency f_T from Y-parameters and determine transit time τ_f from $1/(2\pi f_T)$ vs $1/I_C$.
	• Low-current range:
	  • From $\tau_{f0}(V_{BC})$ data, extract parameters describing the bias dependence.
	  • Determine bottom and perimeter related component and associated geometry factor from $\tau_{f0}(V_{BC}{=}0)$ of transistors with different emitter size.
	• Medium current range
	  • From $I_{CK}(V_{CE}$ or $V_{BC})$ data, extract parameters describing the bias dependence
	  • Extract current spreading angle from $I_{CK}(V_{CE}{=}0.8\text{V}$ or $V_{BC}{=}0\text{V})$
	• High-current region: extract relevant parameters describing the bias dependence.

Extracted (specific) parameters	τ_{f0i}, $f_{tpi} = \tau_{f0p}/\tau_{f0i}$, $\Delta\tau_{0h}$, τ_{Bfvl}; $\overline{r_{Ci0}}$, V_{lim}, V_{PT}, V_{CEs}; a_{hc}, τ_{hcs}, τ_{Ef0}, $g_{\tau E}$,$f_{\tau hc}$
Related HICUM parameters	τ_0, $\Delta\tau_{0h}$, τ_{Bfvl}; r_{Ci0}, V_{lim}, V_{PT}, V_{CEs}; a_{hc}, τ_{hcs}, τ_{Ef0}, $g_{\tau E}$,$f_{\tau hc}$

4.5.13 Collector current at high injection

Measurement data	IV data from transistors with different emitter size
Required model parameters	• those for I_T and I_{BE} extracted at low injection • depletion capacitances and transit time (to calculate $Q_{p,T}$) • r_E, r_{Bx}, r_{Bi}, r_{Cx} • R_{th}
Required geometry data	emitter window area of the transistors
Procedure:	• Extraction in high current region via non-linear optimization of $\log(I_C/A_E)$ vs. V_{BE} at sufficiently low V_{CE} (to minimize impact of self-heating). • Optimization can be performed simultaneously on transistors with different emitter sizes.
Extracted (specific) parameter	$\overline{I_{Ch}}$
Related HICUM parameter	I_{Ch}

4.5.14 Base-collector Breakdown

Measurement data	I_B(V_{CB} or V_{CE}) data from transistors with different size
Required model parameters	C_{jCi0}, V_{DCi}, z_{Ci},V_{PTCi}; γ_C
Required geometry data	emitter window area A_{E0} of the transistors
Procedure:	• Determination of avalanche current $I_{AVL}(V_{CB})$ from measured $I_B(V_{CB})$ data at sufficiently low forward bias V_{BE}. • Extraction of parameters describing the bias dependence via non-linear optimization of $I_{AVL}(V_{CB})$.
Extracted (specific) parameters	f_{AVL}, $\bar{q}_{AVL}$
Related HICUM parameters	f_{AVL}, q_{AVL}

4.5.15 High-Frequency effects

4.5.15.1 Non-quasi-static effects

Measurement data	hot Y-parameters of a typical transistor configuration
Required model parameters	• those for I_T and I_{BE} extracted at low injection • all capacitances and transit time • r_E, r_{Bx}, r_{Bi}, r_{Cx}
Required geometry data	None
Procedure:	• Extraction of α_{iT} by fitting $\mathrm{Im}\{y_{21}\}$ at high frequencies for various bias points below peak f_T. • Extraction of α_{Qf} by fitting $\mathrm{Re}\{y_{11}\}$ at high frequencies for various bias points beyond peak f_T.
Extracted (specific) parameters	α_{iT}, α_{Qf}
Related HICUM parameters	α_{iT}, α_{Qf}

4.5.15.2 Partitioning of the external BC capacitance

Measurement data	None
Required model parameters	specific BC capacitances and sheet/contact resistances of the external base
Required geometry data	dimensions of the various regions of the external base
Procedure:	Calculation of the partitioning factor by TRADICA for each geometry during parameter (library) generation
Extracted (specific) parameter	
Related HICUM parameter	f_{BCpar}

Presently existing methods, that are based on experimental data, only allow to extract the partitioning factor for a single geometry, but do not offer a generic description for geometry scaling.

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4.5.16 Intra-device substrate coupling

Measurement data	cold Y-parameters of relevant transistor configurations
Required model parameters	r_E (is of minor importance though)
Required geometry data	None
Procedure:	• Determine the impedance Z_{su} of the substrate coupling network and extract r_{su} and C_{su} from real and imaginary part of $1/Z_{su}$. • Alternative (also for parameter library generation): calculation from simulation after experimental calibration.
Extracted (specific) parameters	
Related HICUM parameters	r_{su}, C_{su}

Presently existing methods only allow to extract the substrate resistance for a single geometry, but do not offer a generic description for geometry scaling.

4.5.17 High-frequency emitter current crowding

Measurement data	hot Y-parameters of different transistor configurations
Required model parameters	• those of i_T and i_{BE} • all capacitances (incl. transit time) at the base node • r_E, r_{Bx}, r_{Bi}
Required geometry data	None
Procedure:	• f_{CrBi} can be determined from optimizing the model's y_{11} at high frequencies to the results of a transistor with the largest emitter width offered in a process. • Alternative (also for parameter library generation): use $f_{CrBi} = 0.2$
Extracted (specific) parameter	f_{CrBi}
Related HICUM parameter	f_{CrBi}

Presently existing methods only allow to extract f_{CrBi} from experimental data of a single geometry, but do not offer a generic description for geometry scaling. In addition, the modeling approach can only be applied to the small-signal case.

4.5.18 Parasitic substrate transistor elements

Geometry scaling of the substrate junction related currents depends on the process. For practical applications, the minimum effort is assumed to be spent on modeling and parameter extraction of the substrate transistor.

4.5.18.1 Transfer current

Measurement data	transistor configurations with different substrate size
Required model parameters	• if separate substrate pad is available: none • if in HF pads: base current components
Required geometry data	substrate perimeter length and/or area
Procedure:	• Separation into bias dependent bottom and/or perimeter specific current components via different geometries. • Extraction of parameters related to bias dependence from least-squares fit of log(I_{Ts}) vs. V_{SC}.
Extracted (specific) parameters	I'_{TsS} or $\overline{I}_{TsS}$, m_{sf}
Related HICUM parameters	I_{TsS}, m_{sf}

4.5.18.2 Charge storage time

Measurement data	hot Y-parameters for a critical transistor configuration at (very) low V_{CE} (optional: different transistor configurations)
Required model parameters	transit time, C_{BE}, C_{BC}
Required geometry data	none
Procedure:	adjust τ_{sf} to fit f_T at low V_{CE}.
Extracted (specific) parameter	τ_{sf}
Related HICUM parameter	τ_{sf}

It is assumed that no separate substrate test transistor is available in HF pads to directly measure the S-parameters of the substrate transistor.

4.5.19 Temperature dependence

T_0 is the (reference) temperature at which the parameter extraction for modeling the bias and frequency dependent transistor behavior is performed. For extracting the relevant model parameters, the same measurements as for T_0 are repeated for different temperatures T.

4.5.19.1 Series resistances

Measurement data	IV data at different temperatures T
Required model parameters	series resistances and/or their components at T_0
Required geometry data	None
Procedure:	• determine the respective resistance r for each T • fitting of the ratio $\log[r(T)/r(T_0)]$ vs. (T/T_0) with the respective exponent factor ζ as parameter.
Extracted (specific) parameters	ζ_{Ci}, ζ_{rBi}, ζ_{rBx}, ζ_{rCx}, ζ_{rE}
Related HICUM parameters	ζ_{Ci}, ζ_{rBi}, ζ_{rBx}, ζ_{rCx}, ζ_{rE}

4.5.19.2 Bandgap voltage

Measurement data	$I_C(V_{BE})$ data at V_{BC}=0 for different temperatures T
Required model parameters	none
Required geometry data	none
Procedure:	• Determine the saturation current I_S and the non-ideality coefficient at various temperatures. • Extract V_{gB} from a least-squares fit based on $I_S(T)$
Extracted (specific) parameter	V_{gB}
Related HICUM parameter	V_{gB}

4.5.19.3 TC of the forward current gain

Measurement data	$I_C(V_{BE})$, $I_B(V_{BE})$ data at V_{BC}=0 for different temperatures T
Required model parameters	none
Required geometry data	none
Procedure:	• Determine B(I_C) at various temperatures. • Extract α_{Bf} from B(I_C=const) vs. T-T_0 via least-squares fit
Extracted (specific) parameter	α_{Bf}
Related HICUM parameter	α_{Bf}

4.5.19.4 Transit time at low current densities

Measurement data	hot Y-parameters vs bias (at V_{BC}=0) for different temperatures T
Required model parameters	none
Required geometry data	none
Procedure:	• Determine the low-current transit time τ_{f0} for each T • Extract $\alpha_{\tau 0}$ and $k_{\tau 0}$ from $\tau_{f0}(T)$ via non-linear optimization
Extracted (specific) parameters	$\alpha_{\tau 0}$, $k_{\tau 0}$
Related HICUM parameters	$\alpha_{\tau 0}$, $k_{\tau 0}$

4.5.19.5 Critical current

Measurement data	hot Y-parameters vs bias (at V_{BC}=0) for different temperatures T
Required model parameters	none
Required geometry data	none
Procedure:	• Determine the transit time τ_f and the critical current I_{CK} for each T • Extract α_{CEs} from re-fitting I_{CK} at each T with $V_{CEs}(T)$ as a parameter. • α_{vs} can be taken from literature
Extracted (specific) parameters	α_{vs} , α_{CEs}
Related HICUM parameters	α_{vs} , α_{CEs}

4.5.19.6 BC breakdown

Measurement data	I_B(V_{CB} or V_{CE}) data for different temperatures T
Required model parameters	none
Required geometry data	none
Procedure:	• Determine the avalanche current I_{AVL} from I_B for each T • With α_{fav} and α_{qav} as variables, perform a nonlinear optimization on the measured data for I_{AVL} by exercising the compact model with fixed values for f_{AVL} and q_{AVL}, that were determined at the reference temperature T_0.
Extracted (specific) parameters	α_{fav} , α_{qav}
Related HICUM parameters	α_{fav} , α_{qav}

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4.6 Measurement conditions

The table below contains an overview on the most important measurements to be performed and the associated bias conditions. The values are examples and given for Si-based processes. Only a minimum number of measurements is specified (i.e. more data is always useful).

measurement type and bias conditions	data	result
• internal base pinch resistance data from at least 3 structures with different b_E; • V_{BE}=[-0.5,0.5]V @ V_{CE}=0, ΔV_{BE}=0.1V, ΔV_{BB}=0.01V • sheet and contact resistances of ext. base region, buried layer, collector (sinker, contact) • ΔV=0.01...0.1V, depending on resistance value	V_{BE} I_{B1} I_{B2} ΔV I (or r_S, r_{con} ...)	base and collector series resistance components
• C-V on large area transistor • V_{BE}=[-0.5,0.5]V, V_{BC}=V_{SC}=0, ΔV_{BE}=0.1V • V_{BC}=[-BV_{CEO},0.5]V,V_{BE}=V_{SC}=0, ΔV_{BC}=0.1V • V_{SC}=[-BV_{CEO},0.5]V,V_{BE}=V_{BC}=0, ΔV_{SC}=0.1V • C-V on large area BC diode (only for transistors with selectively implanted collector) • V_{BC}=[-BV_{CEO},0.5]V,V_{BE}=V_{SC}=0, ΔV_{BC}=0.1V	V_{BE} C_{jE} V_{BC} C_{jC} V_{SC} C_{jS} V_{BC} C_{jC}(epi)	depletion and isolation capacitance components
• cold S-parameters as a function of bias on ≥ 3 transistors with different b_E (<< l_E) • V_{BE}=[-0.5, 0.5]V, V_{BC}=0, ΔV_{BE}=0.1V • V_{BC}=[-BV_{CEO}, 0.5]V, V_{BE}=0, ΔV_{BC}=0.1V	V_{BE} $\underline{S}$ V_{BC} $\underline{S}$	depletion and isolation capacitance components
• S-parameters as a function of bias on at least 3 transistors with different b_E (<<l_E) : • I_C/A_E=[0.01, 2]mA/µm^2 (depends on process) for at least 3 V_{CE}, e.g. V_{CE}/V=0.5, 1.5, BV_{CEO}	V_{BE} V_{CE} I_C I_B $\underline{S}$	f_T, τ_f, certain forward I-V parameters; verification
• d.c. output characteristics (reference transistor only) • V_{CE}=[0V, $V_{CE,max}$] @ I_B=const / V_{BE}=const ($V_{CE,max}$<BV_{CEO}(high I_C/A_E)) • I_C/A_E=[0.01,2]mA/µm^2 (depends on process !!)	V_{CE} I_C I_B V_{BE}	Avalanche, certain I_C parameters; verification

measurement type and bias conditions	data	result
• d.c. reverse characteristic (reference transistor only) • V_{BC}=[0.4, 0.7]V @ V_{BE}=0V	V_{BC} I_B [I_C]	BC diode current
• Temperature dependence: e.g. T=[-40, 75, 125] ^{o}C • repeat above measurements • shift V_{BE} bias according to temperature, assuming a TC of about -1.5mV/K	T, ...	TCs