

# **HICUM**

-

## **A Geometry Scalable Physics-Based Compact Bipolar Transistor model**

**Michael Schroter and Anindya Mukherjee**

**ECE Dept**

**University of California San Diego, CA**

**Chair for Electron Devices and Integrated Circuits**

**University of Technology Dresden, Germany**

Documentation of model level 2 version 2.23

December, 2008

<b>1 Introduction</b>	<b>6</b>
1.1 Preliminary remarks	6
1.2 Model features overview	8
<b>2 Model equations</b>	<b>12</b>
2.1 HICUM/Level2	13
2.1.1 Equivalent circuit	13
2.1.2 Quasi-static transfer current	15
2.1.3 Minority charge, transit times, and diffusion capacitances	22
2.1.3.1 Minority charge component controlled by the forward transfer current	22
2.1.3.2 Minority charge component controlled by the inverse transfer current	33
2.1.4 Depletion charges and capacitances	34
2.1.4.1 Base-emitter junction	34
2.1.4.2 Internal base-collector junction	37
2.1.4.3 External base-collector junction	41
2.1.4.4 Collector-substrate junction	43
2.1.5 Static base current components	44
2.1.6 Internal base resistance	47
2.1.7 External (parasitic) bias independent capacitances	52
2.1.8 External series resistances	56
2.1.9 Non-quasi-static effects	60
2.1.10 Breakdown	63
2.1.10.1 Collector-Base Breakdown	63
2.1.10.2 Emitter-base breakdown	65
2.1.11 Substrate network	68
2.1.12 Parasitic substrate transistor	69
2.1.13 Noise model	71
2.1.13.1 Correlation between base and collector noise	72
2.1.14 Temperature dependence	76
2.1.14.1 Temperature dependent bandgap voltage	76
2.1.14.2 Transfer currents	79
2.1.14.3 Zero bias hole charge	80
2.1.15.4 Base (junction) current components	81
2.1.15.5 Transit time and minority charge	84
2.1.15.6 Temperature dependence of built-in voltages	87
2.1.15.7 Depletion charges and capacitances	89
2.1.15.8 Series resistances	91
2.1.15.9 Breakdown	92
2.1.15.10 Parasitic substrate transistor	94
2.1.15 Self-heating	96
2.1.16 Lateral scaling	97
2.1.16.1 Transfer current	97
2.1.16.2 Base current components	97
2.1.16.3 Minority charge and transit times	97
2.1.16.4 Depletion charges and capacitances	105
2.1.16.5 Series resistances	106

2.1.16.6 Breakdown	106
2.1.16.7 Parasitic substrate transistor	107
2.1.16.8 Self-heating	107
<b>3 Parameters</b> .....	<b>109</b>
3.1 Parameter list for HICUM/Level2	109
3.1.1 Transfer current	110
3.1.2 Base-emitter current components	111
3.1.3 Base-collector current components	111
3.1.4 Base-emitter tunnelling current	112
3.1.5 Base-collector avalanche current	112
3.1.6 Series resistances	112
3.1.7 Substrate transistor	113
3.1.8 Intra-device substrate coupling	113
3.1.9 Depletion charge and capacitance components	113
3.1.10 Minority charge storage effects	115
3.1.11 Parasitic isolation capacitances	116
3.1.12 Vertical non-quasi-static effects	116
3.1.13 Noise	116
3.1.14 Lateral geometry scaling (at high current densities)	117
3.1.15 Temperature dependence	117
3.1.16 Self-Heating	118
3.1.17 Circuit simulator specific parameters	119
<b>4 Parameter determination</b> .....	<b>120</b>
4.1 Wafer selection	121
4.2 Relevant transistor dimensions	123
4.3 Measurements	125
4.3.1 IV measurements and data	125
4.3.2 CV measurements and data	125
4.3.3 S-parameter measurements and data	125
4.3.4 Sequence of measurements	127
4.4 Flowchart and comparison to SGPM	128
4.5 A step by step procedure	130
4.5.1 BC depletion and isolation capacitance	133
4.5.2 BE depletion and isolation capacitance	134
4.5.3 CS depletion capacitance	134
4.5.4 Internal base (sheet) resistance	135
4.5.5 Components of external base resistance	135
4.5.6 Emitter resistance	136
4.5.7 Components of external collector resistance	136
4.5.8 Collector current at low bias	137
4.5.9 Current across BE junction at low bias	137
4.5.10 Current across BC junction at low bias	138
4.5.11 Thermal resistance	138
4.5.12 Forward transit time	139
4.5.13 Collector current at high injection	140

---

4.5.14	Base-collector Breakdown	140
4.5.15	High-Frequency effects	141
4.5.15.1	Non-quasi-static effects	141
4.5.15.2	Partitioning of the external BC capacitance	141
4.5.16	Intra-device substrate coupling	142
4.5.17	High-frequency emitter current crowding	142
4.5.18	Parasitic substrate transistor elements	143
4.5.18.1	Transfer current	143
4.5.18.2	Charge storage time	143
4.5.19	Temperature dependence	144
4.5.19.1	Series resistances	144
4.5.19.2	Bandgap voltage	144
4.5.19.3	TC of the forward current gain	145
4.5.19.4	Transit time at low current densities	145
4.5.19.5	Critical current	146
4.5.19.6	BC breakdown	146
4.6	Measurement conditions	147
<b>5</b>	<b>Operating Point Information from Circuit Simulators</b>	<b>149</b>
<b>6</b>	<b>Experimental Results</b>	<b>152</b>
6.1	DC characteristics	154
6.2	Transit frequency and transit time	159
6.3	High-frequency small-signal characteristics	163
6.4	High-speed transient (switching) operation	179
6.5	Temperature dependence	180
6.5.1	DC characteristics	180
6.5.2	AC characteristics	181
6.6	Low-frequency noise	182
6.7	High-frequency noise	183
6.8	High-frequency distortion	184
6.9	Predictive modelling	191
6.10	Statistical modelling	193
6.11	Circuit results	195
<b>7</b>	<b>Appendix: Derivation of some important model equations</b>	<b>197</b>
7.1	The ICCR (homojunction transistors)	204
7.2	The GICCR (heterojunction transistors)	205
7.3	Vertical NQS effects implementation	207
7.4	Lateral NQS effects	214
7.5	Correlated noise implementation	214
	<b>References</b>	<b>219</b>

**List of often used symbols and abbreviations**

$A_{E0}, L_{E0}$	emitter window area and perimeter
$A_E, L_E$	effective (electrical) emitter area and perimeter
$b_{E0}, l_{E0}$	emitter window width and length
$b_E, l_E$	effective (electrical) emitter width and length (for definition see [24, 40])
$\gamma_C$	ratio of periphery to area specific collector current; equal to emitter width increase due to periphery injection, e.g. $b_E = b_{E0} + 2\gamma_C$
$I_T, i_T$	DC and time dependent transfer current of the vertical npn transistor structure
$I_{CK}$	critical current (indicating onset of high-current effects)
$\mu_n, \mu_p$	electron (hole) mobility
$N_{Ci}$	(average) collector doping under emitter
$N_{Cx}$	collector doping under external base
$Q_p$	hole charge
$\tau_f$	forward transit time
$w_B, w_{B0}$	neutral/metallurgical base width
$w_{Ci}$	(effective) collector width under emitter
$w_{Cx}$	(effective) collector width under external base
$w_i$	width of collector injection zone (for charge storage calculation in collector region)
GICCR	Generalized Integral Charge-Control Relation [36]
TRADICA	TRAnsistor DIMensioning and CALculation program [44]

# 1 Introduction

## 1.1 Preliminary remarks

The purpose of the following remarks is to provide (i) a motivation behind the compact modeling approach pursued with HICUM, (ii) an overview on its targeted application area, and (iii) a list of requirements for a compact model from different point of views.

Bipolar technology has recently seen a tremendous growth, fuelled mostly by applications that require high speed and driving power on one hand and low noise and distortion on the other hand.

Presently, major applications of bipolar technology are:

- Wireless communications in the 0.9 to 5.6 GHz range for, e.g. GSM, Bluetooth, DECT, in the 4-12 GHz range for, e.g. satellite TV, WLAN, and in the 20 to 60GHz range for short range communications, with the first application dominating.
- Fiber-optic communications in the 10 to 60 Gb/s range for, e.g. fast internet access and data transfer (LAN, WAN) as well as TV/HDTV (FTTC, FTTH); production and related design has started for systems up to 10Gb/s, seeing a significant push also for higher integration, such as cross-point switches in BiCMOS processes with emphasis on low-power high-speed bipolar circuits.
- “Linear analog” circuits for, e.g. disc drives, consumer electronics in general, power and automotive electronics. Many of these components require reliable and well-established processes with higher breakdown voltages rather than advanced high-speed bipolar processes.
- Fast data acquisition and conversion (ADCs) for, e.g., instrumentation and measurement equipment.
- Advanced automotive components at very high frequencies in the range of 24 to 100 GHz for, e.g. collision warning and avoidance. The respective circuits so far have been realized mostly with III-V processes, such as HBTs.

The above sequence is assumed to be roughly in the order of present importance from a business point of view; exact breakdowns are difficult to find, and the ranking can change quickly in areas of rapid growth. The first two applications are perceived to comprise the largest number of designs. As a consequence, compact bipolar transistor modeling should focus on these areas which, fortunately, include most of the critical issues of the other applications.

Compact modeling is also strongly connected to development and deployment of process technologies. A physics-based compact model together with the related parameter extraction and generation methodology can contribute significantly to improve the alignment of process development with product design requirements by enabling quick evaluations of the impact of process changes

on device and circuit performance. Compact modeling basically provides a link between processing and design.

In general, bipolar processes span over quite a variation in device structure as well as device type. It is recommended to split compact bipolar models into at least two categories:

- vertical devices including high-speed npn and pnp transistors
- lateral devices, mostly pnp transistors.

HICUM is targeted towards the first category. It might be necessary though to divide the first category again into “low-power” ( $BV_{CEO} < 10\text{V}$ ) and “high-power” ( $BV_{CEO} > 10\text{V}$ ) transistors if the difference in device design and the electrical application range turns out to be too large for a single model. So far, HICUM has been verified to be accurate for transistors with  $BV_{CEO}$  values up to about 15V, but there is no reason why the model should not work for higher voltages.

From the above, the following requirements for a compact model can be derived from an industrial point of view:

- high accuracy over a wide electrical (and temperature) range;
- laterally scalable parameter calculation, including variable contact configurations, in order to allow circuit optimization;
- numerical stability and fast execution time, although this is somewhat dependent on the application.
- physics-based formulation, allowing predictive and statistical modeling;
- reliable and well-defined extraction procedure should be available together with test structures; also, the use of standard equipment and set-ups are only important for, e.g., fast throughput.
- modular formulation of the model equations, minimizing interrelations between different electrical regions and facilitating simple implementation into circuit simulators.

Since the limitations of the standard SPICE Gummel-Poon model (SGPM), especially for designing high-speed circuits, have been well-known for many years (cf. examples in [62]), the advanced model HICUM has been developed to address the above mentioned requirements.

## 1.2 Model features overview

HICUM is a semi-physical compact bipolar transistor model. Semi-physical means that for arbitrary transistor configurations, defined by emitter size as well as number and location of base, emitter and collector fingers (or contacts, respectively), a complete set of model parameters can be calculated from a single set of technology specific electrical and technological data (cf. [1]). For this, the value of each element in the equivalent circuit is related to a function describing the dependence on so-called specific electrical data (such as sheet resistances and capacitances per unit area or length), technological data (such as width and doping of the collector region underneath the emitter), physical data (like mobilities), transistor dimensions (such as design rules), operating point, and temperature. The availability of such a semi-physical compact model is an important precondition for circuit optimization with respect to, e.g., maximum speed and low power consumption as well as for including process variations in the design.

The name HICUM was derived from *HIgh-CUrrrent Model*, indicating that HICUM initially was developed with special emphasis on modelling the operating region at high current densities which is very important for certain high-speed applications. The first version was described in detail in [2,3,4,5,6] and was verified for digital applications based on a conventional technology. Later, formulas for the calculation of the base resistance were developed [7,8,9] which include three-dimensional effects occurring in short transistors with an emitter length approaching the emitter width. The latter sizes are important for low-power designs. The introduction of self-aligning poly-silicon technologies as well as the extension of the model to high-frequency analog operation led to improvements [10,11] w.r.t. the first version, which were also verified for very fast large-signal digital-type applications [12].

HICUM is based on an extended and Generalized Integral Charge-Control Relation (GICCR) [13,14,15,16]. However, in contrast to the (original) Gummel-Poon model (GPM) [17] as well as the SPICE-GPM (SGPM) [18] and its variants, in HICUM the (G)ICCR concept is applied consistently without inadequate simplifications and additional fitting parameters (such as the Early voltages). Since reliable design and optimization of high-speed circuits requires accurate modeling mainly of the dynamic transistor behavior, quantities like depletion capacitances and the transit time of mobile carriers as well as the associated charges, which determine the dynamic behaviour, are considered as basic quantities of the model. An accurate approximation of these basic quantities as a function of bias yields, thus, not only an accurate description of the small-signal and dynamic



large-signal behaviour but also - via the (G)ICCR [19] - of the d.c. behaviour. This coupling between static and dynamic description leads, moreover, to a reduction of "artificial" model parameters like Early voltages and knee currents. Furthermore, the above mentioned basic quantities can be easily and accurately determined by standard small-signal measurement methods.

The modularity and physics-based approach of HICUM allows the construction of a model hierarchy without additional effort in parameter extraction. Based on HICUM Level2 (HICUM/L2) and its corresponding set of specific electrical parameters, the simplified version HICUM Level0 (HICUM/L0) with the same equivalent circuit as the SGPM as well as an electrically and thermally distributed model, HICUM Level4 [20], can be generated. In contrast to the SGPM though, HICUM/L0 eliminates many problems while maintaining similar overall simplicity. The HICUM/Level0 model is presently being implemented in commercial simulators.

The important physical and electrical effects taken into account by HICUM/L2, which is described in Chapter 2.1, are briefly summarized below:

- high-current effects (incl. quasi-saturation)
- distributed high-frequency model for the external base-collector region
- emitter periphery injection and associated charge storage
- emitter current crowding (through a bias dependent internal base resistance)
- two- and three-dimensional collector current spreading
- parasitic (bias independent) capacitances between base-emitter and base-collector terminal
- vertical non-quasi-static (NQS) effects for transfer current *and* minority charge
- temperature dependence and self-heating
- weak avalanche breakdown at the base-collector junction
- tunneling in the base-emitter junction
- parasitic substrate transistor
- bandgap differences (occurring in HBTs)
- lateral (geometry) scalability

Modelling of these effects is reflected not only in the model equations but also in the topology of the equivalent circuit. Although the above listed effects are taken into account, the standard HICUM/L2 equivalent circuit still corresponds to a one-transistor model (see Fig. 2.1.1/1), which has turned out as sufficiently accurate for the vast majority of circuit applications. HICUM/L2 contains elements for describing the internal transistor (index  $i$ ), the emitter periphery (index  $p$ ) and the external transistor regions (index  $x$ ). The internal transistor is defined by the region under the emitter which is assigned an effective emitter width [21,22] and area, respectively, in order to retain a one-

transistor model with an as simple as possible equivalent circuit topology as well as a sound physical background. In contrast to MOS transistor models, the geometry dependent calculations have been implemented in a separate program (TRADICA, cf. [1]) for various reasons ( e.g. [23]).

Due to its semi-physical nature HICUM/L2 possesses geometry scaling capabilities up to high current densities [21]. In order to make use of these scaling capabilities specific parameters have to be determined from measurements, for which instructions have been developed (e.g., [23,4,24,25, 26]). Parameter extraction as well as generation of model parameters for different transistor configurations will be addressed in Chapter 4. Notes on operating point information that need to be available in (commercial) circuit simulators are provided in Chapter 5.

As the experimental results in chapter 6 show, the accuracy and applicability of HICUM has been demonstrated for a variety of different technologies, ranging from a low-speed and relatively high-voltage process to present SiGe production processes, as well as for many different operating modes.

This documentation includes the contents of change notes up to the version specified on the title page. The differences of new model releases will be documented first separately in order to simplify code updates, and will then be incorporated into this documentation.

## **Acknowledgments**

Many individuals have contributed to the development of HICUM through various activities such as valuable feedback and model testing. It is impossible to list everybody who in some way participated in the model related development, but I feel that it is appropriate and important to name at least the most important contributors.

A number of the changes described have been suggested by and/or already implemented in various commercial simulators. In this respect, we very much appreciate the valuable feedback and suggestions particularly from Yo-Chien Yuan, Rosana Perez and Rick Poore (Agilent), Mohamed Selim and Joel Besnard (Mentor Graphics), B. Ardouin (XMOD), Thierry Burdeaux and Didier Celi, F. Pourchon (STM), M. Racanelli, P. Kempf and H. Jiang (JazzSemi), W. Kraus (Atmel), R. Murty and D. Hame (IBM), P. Brenner and J. Berkner (Infinion), P. Kolev (RFMD), E. Gerhardt (Alcatel), T.-Y. Lee (formerly at Conexant), P. Zampardi (Skyworks Inc.), Jean-Paul Malzac (Silvaco), and Adam Divergilio (Tektronix), A. Chakravorty (IIT-M) and P. Sakalas, S. Lehmann, H. Tran, Y. Zimmermann, H. Wittkopf, K.-E. Moebus, S. Komarow (all with Chair for Electron Devices and Integrated Circuits, Dresden University of Technology). Many thanks go also to Marek Mierzwinski (Tiburon) and Geoffrey Coram (Analog Devices) for discussions about and help with the Verilog-A implementation, to Prof. J.-C. Perraud (CAEN) for feedback regarding the prototype implementation in SPICE3F test simulations.

The HICUM group would like to thank especially ATMEL Germany (Heilbronn), STM (Grenoble, France), IBM (Burlington, USA) and Jazz Semiconductor (Newport Beach, USA) for financial support. We also appreciate the software donations from Agilent, Applied Wave Research, Cadence, Mentor Graphics and XMOD Technologies as well as wafer access from Atmel Germany, Infineon (Munich, Germany), Jazz Semiconductor (Newport Beach, USA), Skyworks (Newbury Park, USA), STM (Crolles, Grenoble, France), TSMC (Hsinchu, Taiwan) and IHP (Frankfurt/Oder, Germany) for measurements and experimental model verification.

Finally, Michael Schroter wishes to express his sincere gratitude to Prof. H.-M. Rein for providing the encouragement and knowledge-base that started the early model development and laid the foundation for the present state.