HICUM / L2
A physics-based compact heterojunction bipolar transistor model

Technical documentation of model version 3.0.0

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List of often used symbols and abbreviations

A_{E0} , L_{E0}	emitter window area and perimeter
A_E , L_E	effective (electrical) emitter area and perimeter
b_{E0} , l_{E0}	emitter window width and length
b_E , l_E	effective (electrical) emitter width and length
I_T , i_T	DC and time dependent transfer current of the vertical npn transistor structure
I_{CK}	critical current (indicating onset of high-current effects)
μ_n, μ_p	electron (hole) mobility
N_{Ci}	(average) collector doping under emitter
N_{Cx}	collector doping under external base
Q_p	hole charge
τ_f	forward transit time
w_B ,w_{B0}	neutral/metallurgical base width
w_{Ci}	(effective) collector width under emitter
w_{Cx}	(effective) collector width under external base
w_i	width of collector injection zone (for charge storage calculation in collector region)

GICCR	Generalized Integral Charge-Control Relation
SGPM	SPICE Gummel-Poon model

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1 Introduction

A compact model represents the link between process technology and circuit design. The physics-based HIgh-CUrrent Model (HICUM) Level2 (L2) has been a standard compact model for bipolar junction transistors (BJTs) and heterojunction bipolar transistors (HBTs) for many years. The model has been shown to be applicable to many process generations of SiGe HBTs [1] and also to InP HBTs [36-39], including high-speed and high-voltage device designs. This manual documents the latest release of HICUM/L2. Changes with respect to previous versions have been summarized during meetings of the Compact Model Coalition and are available on the corresponding slide sets.

The physical background of HICUM/L2 and the derivation of its equations up to version 2.30 have been described in detail in [1], while mjor extensions beyond v2.30 are described in [31, 32, 70]. Therefore, this manual presents just the (bias and temperature dependent) equations that have been implemented into the latest release of the Verilog-A (VA) model code* without going into the details of or assumptions for their derivation. The model equations are discussed on the basis of a vertical npn transistor. A vertical pnp transistor requires for most processes the addition of a parasitic n-well transistor (e.g. in a subcircuit). Since HICUM has been developed for high-speed applications, in the public domain version described in this document only minimal effort has been undertaken to *very* accurately describe the inverse (or reverse) operating region defined by $V_{CE}<0$. The model formulations are extended in a simple way into that bias region in order to mainly ensure numerical stability.

HICUM/L2 is a physics-based compact transistor model in which the value of each element in the equivalent circuit is a function of so-called specific electrical data (such as sheet resistances and capacitances per area or length), technological data (such as width and doping of the collector region underneath the emitter), physical data (like mobilities), transistor dimensions (such as design rules), operating point, and temperature. As a consequence, for arbitrary transistor configurations, defined by emitter size as well as number and location of base, emitter and collector contacts, a complete set of model parameters can be calculated from a single set of technology specific electrical and technological data (cf. [23, 1]). This feature enables circuit optimization as well as statistical modelling and circuit design. In combination with device simulation, even the physical limits of SiGe HBT technology [33, 34] and its technology roadmap can be predicted using the model

*.In the following text the actually implemented model equations are marked by a frame.

[35]. Note that geometry scaling equations are not part of the model implementation and this manual since they need to be implemented in a preprocessor in order to be sufficiently accurate and flexible for a large variety of transistor configurations and process technologies.

Parameter extraction as well as generation of model parameters for different transistor configurations are not part of this manual since they depend on user preferences. There are two alternatives for parameter extraction. Users may build their own parameter extraction infrastructure by implementing methods gathered from literature. Publications related to extracting HICUM/L2 parameters are, e.g., [40-61]. In particular, a parameter exctraction flow has been discussed in [41, 61].

The history of HICUM/L2 is described in [1]. Its development has so far continued for over 30 years. Over its long period of existence, HICUM has been verified for a large variety of bipolar technologies and circuits. For comparisons of the model with experimental results and applications to (production) circuit design, the reader is referred to the literature (e.g. in [1] and more recent work (e.g. [63])), including benchmark circuits for model verification and low-power mm-wave circuits with HBTs operating in the saturation region [64-68]. Considering the present direction of SiGe and InP HBT technology towards mm-wave and THz applications as well as the involvement of the HICUM/L2 team in the corresponding major flagship projects, it is expected that the model development will continue for a significant time along with HBT process development.

For information on the exact version of HICUM/L2 that is available in (commercial) circuit simulators the reader is referred to the respective EDA company websites.

Acknowledgments

Many individuals have contributed to the development of HICUM through various activities such as valuable feedback and model testing. It is impossible to list everybody who in some way participated in the model related development over the past 30 years. A long list of contributors can be found though in [1].

2 Model equations

2.1 Equivalent circuit

Compared to the SGPM the equivalent circuit (EC) of HICUM/Level2 contains two additional circuit nodes, namely B* and S' in Fig. 2.1.0/1. The node B*, which separates the operating point dependent internal base resistance from the operating point independent external component, is required to take into account emitter periphery effects, which can play a significant role in modern transistors. This node is also employed for an improved modelling of the distributed nature of the external base-collector (BC) region by splitting the external BC capacitance C_{BCx} over r_{Bx} in the form of a π-type equivalent circuit for the corresponding *RC* transmission line(s). As a further advantage of introducing the node B*, high-frequency small-signal emitter current crowding can be correctly taken into account by the capacitance C_{rBi}. An emitter-base isolation capacitance C_{BEpar}, that becomes significant for advanced technologies with thin spacer or link regions, as well as a BC oxide capacitance C_{BCpar}, which is included in the C_{BCx} element, are taken into account.

In contrast to other models, the influence of the internal collector series resistance is taken into account by the model equations for the transfer current i_{T} and the minority charge which is represented by the elements C_{dE} and C_{dC} in Fig. 2.1.0/1. As a consequence, the collector terminal C' of the internal transistor is (physically) located at the end of the epitaxial (or n-well) collector region. This approach not only avoids additional complicated and computationally expensive model equations for an "internal collector resistance" but also saves one node. The chosen approach has been demonstrated to be accurate for a wide range of existing bipolar technologies (cf. [1]). Mathematical proof and TCAD based verification for including the internal collector resistance in the GICCR has been provided in [4].

The reliable design of high-speed circuits often requires the consideration of the coupling between the buried layer and the substrate terminal S. Since the substrate material consists of both a resistive and capacitive component, as a first (rough) approach a substrate network with a resistance r_{Su} and a capacitance C_{Su} is introduced, leading to the “internal” substrate node S*. Note that an accurate description of intra-device substrate usually requires a more sophisticated equivalent circuit which depends on the transistor configuration, employed technology and frequency range, and in particular on the actual transistor layout being used in circuit design.

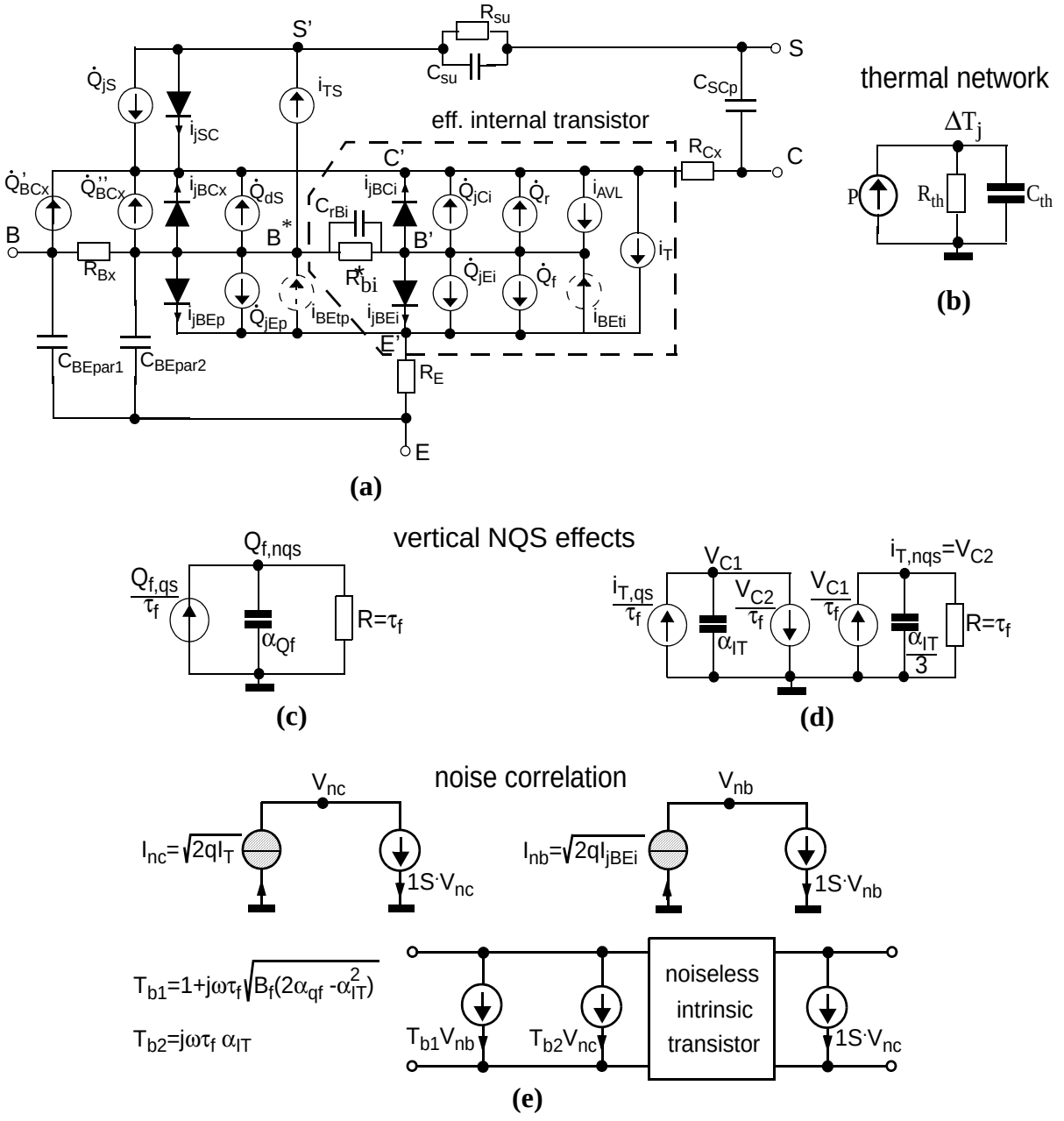

Fig. 2.1.0/1: Complete HICUM/L2 equivalent circuit as implemented in Verilog-A. (a) Large-signal equivalent circuit. The external BC capacitance consists of a depletion and a bias independent parasitic capacitance with the ratio C'_{BCx}/C''_{BCx} being adjusted with respect to proper modelling of the h.f. behavior. (b) Thermal network used for self-heating calculation. (c), (d) Adjunct networks for vertical NQS effects. (e) Adjunct networks for correlated high-frequency noise. The internal transistor (index i) is defined by the region under the emitter which is assigned an effective emitter width and area, respectively, in order to retain a one-transistor model with an as simple as possible equivalent circuit to-

pology as well as a sound physical background. The index “p” (“x”) indicates elements representing the perimeter (external) transistor region(s).

A possibly existing substrate transistor has been taken into account by using a simple transport model. Like in the SGPM, this can also be realized by a subcircuit (cf. Section 2.12) and setting r_{Su} and C_{jS} to zero in the HICUM equivalent circuit. In advanced bipolar processes, the emitter terminal of the substrate transistor (B*) moves towards the (npn) base contact (B) which makes the external realization of such a parasitic transistor by a subcircuit even easier. The substrate transistor - if it is not avoided by proper layout measures - only turns on for operation at very low CE voltages (“very” hard saturation).

The physical meaning and modelling of all EC elements in Fig. 2.1.0/1 is discussed below in more detail. The description in the following text is given for an npn transistor, which is the most widely used type of bipolar transistors. For vertical pnp transistors, the model can be applied by interchanging the signs of terminal voltages and currents. Lateral pnp transistors can be described by a composition of HICUM/L2 models but usually a subcircuit consisting of three simple transport models (e.g. HICUM/L0) is considered to be more appropriate.

2.2 Quasi-static transfer current

The transfer current of a vertical homo- and hetero-junction bipolar transistor can be described by a generalized form of the ICCR that can also be extended to 2D and 3D transistor structures with narrow emitter stripes or very small contact windows. The various steps to arrive at the final equation for the transfer current i_T are outlined below, demonstrating the modular structure of the model equations. For a detailed derivation of the GICCR the reader is referred to [3, 1].

A. Basic formulation

The result of the one-dimensional (1D) GICCR is

$$\boxed{i_T = \frac{c_{10}}{Q_{p,T}}\left[\exp\left(\frac{v_{B'E'}}{V_T}\right) - \exp\left(\frac{v_{B'C'}}{V_T}\right)\right]} \tag{2.2.0-1}$$

with the constant

$$c_{10} = (qA_E)^2 V_T \overline{\mu_{nB} n_{iB}^2}. \tag{2.2.0-2}$$

$v_{B'E'}$ and $v_{B'C'}$ are the (time dependent) terminal voltages of the 1D transistor if the integration leading to the modified hole charge, $Q_{p,T}$, is performed throughout the total 1D transistor, i.e. between its emitter and collector contact. The term $\overline{\mu_{nB} n_{iB}^2}$ is an average value for the base region.

$Q_{p,T}$ consists of a *weighted* sum of charges,

$$\boxed{Q_{p,T} = Q_{p0} + h_{jEi} Q_{jEi} + h_{jCi} Q_{jCi} + Q_{f,T} + Q_{r,T}}, \tag{2.2.0-3}$$

The charge formulations designated with the index "*T*" result when the transfer current is derived from the transport equation and hetero-junctions as well as current spreading are included. The hole charge at thermal equilibrium, Q_{p0}, is a model parameter. Q_{jEi} and Q_{jCi} are the depletion charges stored within the BE and BC junction. $Q_{f,T}$ and $Q_{r,T}$ are (weighted) forward and reverse minority charges stored in the total (1D) transistor. The various components in the minority charges and the weighting factors will be discussed in more detail later.

The correspondence to the conventional model formulation can be maintained by realizing that the usual collector saturation current is simply given by

$$I_S = \frac{c_{10}}{Q_{p0}} , \tag{2.2.0-4}$$

so that (2.2.0-1) can also be written in normalized form:

$$i_T = \frac{I_S}{Q_{p,T}/Q_{p0}} \left[\exp\left(\frac{v_{B'E'}}{V_T}\right) - \exp\left(\frac{v_{B'C'}}{V_T}\right) \right] . \tag{2.2.0-5}$$

Mathematically, i_T in (2.2.0-1) can be split into a "forward" component,

$$i_{Tf} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{v_{B'E'}}{V_T}\right) \tag{2.2.0-6}$$

and a "reverse" (better to say inverse) component,

$$i_{Tr} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{v_{B'C'}}{V_T}\right) , \tag{2.2.0-7}$$

which will be referred to in the discussion below. Physically, i_{Tf} represents the electron current flowing from emitter to collector at forward operation at $\exp(V_{C'E'}/V_T) >> 1$. Analogously, i_{Tr} represents the electron current flowing from collector to emitter at inverse operation with $\exp(-V_{C'E'}/V_T) >> 1$. This separation of i_T simplifies both the implementation of the solution of the non-linear transfer current formulation as well as the modelling of the minority charge components.

B. Extension to the 2D (3D) case and influence of internal base resistance

The 1D transistor structure can be transformed into a 2D or 3D structure by multiplying all area specific 1D model parameters with the emitter area of the transistor. This defines the internal transistor, i.e. the structure under the emitter window. As a result, the lateral voltage drop caused by the base current has to be taken into account for calculating $v_{B'E'}$ and $v_{B'C'}$ in (2.2.0-1). This requires an appropriate definition and model for the internal base resistance by which then $v_{B'E'}$ and $v_{B'C'}$ are becoming "averaged" terminal voltages to ensure a correct description of the electrical (terminal) characteristics of the internal transistor.

C. Emitter periphery injection

The carrier injection at the emitter periphery junction and the corresponding transfer current component through the external base can be taken into account by defining an effective electrical emitter width b_E and length l_E, which are usually larger than the emitter window dimensions. This results in an effective size for the internal transistor in the 2D and 3D case with the effective emitter area A_E. By multiplication of all area specific 1D model parameters with A_E (rather than A_{E0}) it can be shown, that (2.2.0-1) can then be directly applied without any loss of accuracy at low current densities. At high current densities, however, this approach can become less accurate, and another extension is usually required which will be discussed later. $v_{B'E'}$ and $v_{B'C'}$ are now the terminal voltages of the effective internal transistor (cf. Fig. 2.1.0/1), and the components Q_{jEi} and Q_{jCi} in the charge $Q_{p,T}$ are now defined for the effective internal transistor.

Besides the lateral scalability of the model, the major advantages of this approach are that (i) a single equation can be used throughout the total operating region and (ii) a single transfer current source element can be used in the EC (Fig. 2.1.0/1) to describe even transistors with strong 2D and 3D effects.

D. Heterojunction bipolar transistors (HBTs)

The generalized ICCR results in the following expression for the *weighted* minority charge

$$\boxed{Q_{f,T} = h_{f0}Q_{f0} + h_{fE}\Delta Q_{Ef} + \Delta Q_{Bf} + h_{fC}\Delta Q_{Cf}} \tag{2.2.0-8}$$

with Q_{f0} as low-current charge component, and ΔQ_{Ef}, ΔQ_{Bf}, ΔQ_{Cf} as the actual minority charges in the neutral emitter, base, collector. ΔQ_{Cf} can include bias dependent lateral current spreading (see later). The weighing factors h_{f0}, h_{fE} and h_{fC} as well as h_{jEi} and h_{jCi} in (2.2.0-3) are given by the differences and grading of the bandgap between the various transistor regions in a HBT. Note, that $Q_{f,T}$ is generally *not equal to the stored minority charge* Q_f used during dynamic operation. The charge components of $Q_{f,T}$ are discussed in ch. 2.3.

Assuming a linear bandgap change in the base with the grading coefficient a_G, the model parameter h_{jci} can be expressed analytically as

$$h_{jCi} \approx \exp\left(-\frac{a_G w_{B0}}{V_T}\right) \tag{2.2.0-9}$$

with w_{B0} as the neutral base width in equilibrium. The corresponding factor for the BE charge, h_{jEi}, is close to 1 for Si-based processes, but is usually larger than 1 for (SiGe) HBTs.

Bandgap grading in the base emitter space charge region and the corresponding reduction of the transconductance is modeled by a bias dependence of h_{jEi} [32]

$$\boxed{h_{jEi}(v_{B'E'}) = h_{jEi0}\frac{\exp(u)-1}{u}} \tag{2.2.0-10}$$

with the auxiliary variable

$$\boxed{u = a_{hjEi}\left[1-\left(1-\frac{v_{j,u}}{V_{DEi}}\right)^{z_{Ei}}\right]}. \tag{2.2.0-11}$$

Here, h_{jEi0}* and a_{hjEi} are model parameters for the value for the weight factor at zero bias and the slope of the bias dependence. V_{DEi} and z_{Ei} are already existing parameters describing the bias dependence of the corresponding capacitance C_{jEi} (cf. 2.4.1).

The parameter a_{hjEi} is related to the grading in the base. It can be approximated by

$$a_{hjEi} = \frac{w_{BE,0}}{a_{ni}} \tag{2.2.0-12}$$

with the BE SCR at equilibrium,

$$w_{BE,0} = x_{p0} - x_{jE} = \sqrt{\frac{2\varepsilon}{q}\frac{N_E V_{DEi}}{N_B(N_B + N_E)}}, \tag{2.2.0-13}$$

based on the parameters given in Fig. 2.2.0/2 and $a_{\mathrm{ni}} = \Delta x_{\mathrm{Ge}} V_{\mathrm{T}}/\Delta V_{\mathrm{Ge}}$.

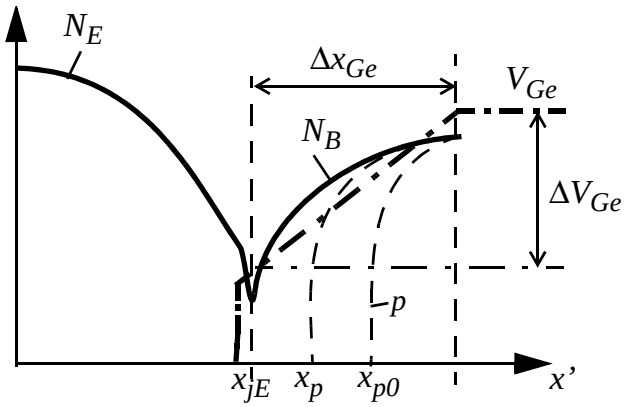

Fig. 2.2.0/2:Sketch of the internal base emitter region of a HBT with graded bandgap.

Towards and beyond V_{DEi}, the voltage $v_{\mathrm{B'E'}}$ is limited smoothly by

$$\boxed{v_{j,u} = V_{DEi} - r_{h_{jEi}} V_T \frac{x_u + \sqrt{x_u^2 + a_{fi}}}{2}} \text{ with } x_u = \frac{V_{DEi} - v_{B'E'}}{r_{h_{jEi}} V_T}, \tag{2.2.0-14}$$

*.In order the allow backward compatibility, the parameter h_{jEi0} is still called h_{jEi} in the model card.

with the model parameter r_{hjEi} and the smoothing constant a_{fi}= 1.921812. The latter also smoothes the onset of $Q_{f,T}$. A possible division by zero in the Bernoulli function $B(u) = [\exp(u) - 1]/u$ in (2.2.0-10) at $v_{B'E'}$=0 is avoided by a series expansion and with the following implementation:

$$B(u) = \begin{cases} \dfrac{\exp(u)-1}{u} & \text{for } |u| \geq u_{min} \\ 1 + \dfrac{u}{2} & \text{for } |u| < u_{min} \end{cases}. \qquad (2.2.0\text{-}15)$$

The boundary for the series expansion has been set to u_{min} = 0.001 and is not critical since h_{jEi} is multiplied with a vanishing BE depletion charge in the corresponding bias region. The behavior of the functions discussed above for h_{jEi} is shown in Fig. 2.2.0/3. With u_{min} = 0.001, the relative error at u_{min} is for the absolute value below 0.2% and for the derivative below 0.14%.

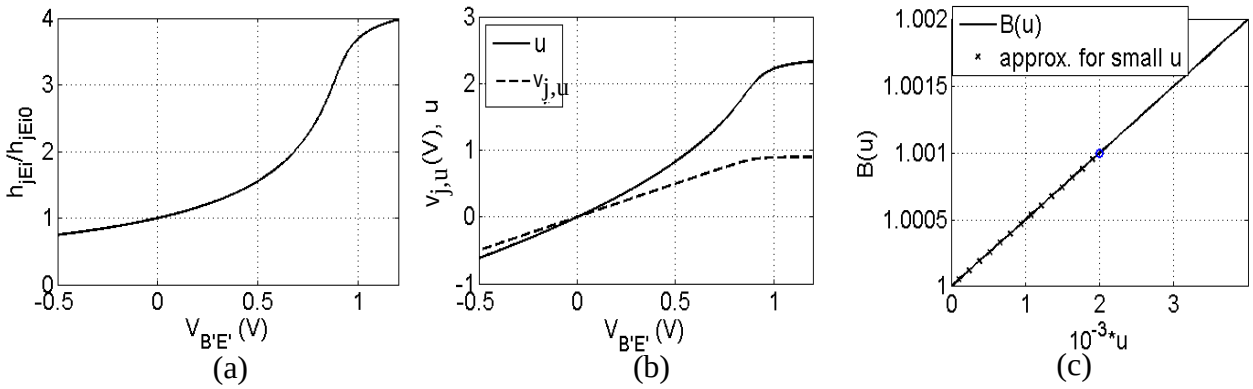

Fig. 2.2.0/3: (a) Normalized h_{jEi} and (b) u and $v_{\mathrm{j,u}}$ as function of $V_{\mathrm{B'E'}}$. (c) Bernoulli function and series expansion approximation for small values of u; the circle indicates u_{min}.

The weight factors [1]

$$h_{fE} = \frac{\overline{\mu_{nB} n_{iB}^2}}{\mu_{nE} n_{iE}^2} \quad \text{and} \quad h_{fC} = \frac{\overline{\mu_{nB} n_{iB}^2}}{\mu_{nC} n_{iC}^2} \qquad (2.2.0\text{-}16)$$

are model parameters that take into account the different values for effective intrinsic carrier concentration n_{i} and mobility μ_{n} of the neutral transistor regions. The factors h_{jCi}, h_{fE}, and h_{fC} are con-

sidered to be model parameters in order to make the model applicable also in cases where the doping concentrations and other physical values are unknown.

For SiGe heterojunction transistors, h_{fC} can be significantly larger than 1 while h_{jCi} is less than 1, explaining the larger Early voltages measured in those transistors. In contrast, for most homojunction transistors these parameters assume values close to 1 although they are becoming more relevant, too, in advanced homojunction transistors due to high-doping effects.

For HBTs, such as those fabricated in III-V semiconductors, that contain a significant energy difference in the conduction band, transport effects such as thermionic emission and tunneling may have to be accounted for. There are various ways of doing this which differ in complexity and, therefore, convergence rate and simulation time. For the present model, the most simple approach has been adopted by introducing a non-ideality coefficient m_{Cf} in the forward component of the transfer current:

$$i_{Tf} = \frac{c_{10}}{Q_{p,T}} \exp\left(\frac{v_{B'E'}}{m_{Cf} V_T}\right). \tag{2.2.0-17}$$

This approach is believed to offer sufficient flexibility for practical purposes, while keeping down additional computational burden.

F. Final transfer current model formulation

The total transfer current is then

$$\boxed{i_T = i_{Tf} - i_{Tr}}. \tag{2.2.0-18}$$

At high reverse bias across either junction, the respective space-charge region can extend throughout the whole base region (base punch-through or reach-through effect). As a result, $Q_{\mathrm{p,T}}$ would become zero or even less than zero which would cause numerical problems. This situation is most likely to occur at low current densities, where the (always positive) minority charge is negligible. Therefore, in HICUM the hole charge at low current densities,

$$\boxed{Q_{pT,j} = Q_{p0} + h_{jEi} Q_{jEi} + h_{jCi} Q_{jCi}}, \tag{2.2.0-19}$$

is limited to a positive value $Q_{\mathrm{B,rt}} = 0.05 Q_{\mathrm{p0}}$, using a smoothing function, and is replaced by

$$\boxed{Q_{pT,\,low} \;=\; Q_{B,\,rt}\left(1+\frac{x+\sqrt{x^2+a}}{2}\right)} \;\; with \;\; \boxed{x \;=\; \frac{Q_{pT,\,j}}{Q_{B,\,rt}}-1} \qquad (2.2.0\text{-}20)$$

and a=1.921812 which reproduces the values of the exponential smoothing function in the early version 2.1. For the usual operating range with $Q_{pT,j}/Q_{p0} > 1$, the difference $Q_{pT,low}$-$Q_{p,j}$ is much smaller than $10^{-6}Q_{p0}$, so the smoothing and the associated computational effort could be skipped in the code. Also note that the effect of base reach-through is extremely unlikely, so that any additional (numerical) effort to take into account the physical mechanisms occurring under these circumstances does not seem to be justified for a compact model.

In general, the GICCR is a non-linear implicit equation for either i_T or $Q_{p,T}$, respectively. Since $Q_{p,T}$ is the common variable in both current components i_{Tf} and i_{Tr}, the GICCR is solved in HICUM for $Q_{p,T}$ by employing Newton-Raphson iteration*. However, as long as $Q_{f,T}$ and Q_r are linearly varying functions of the respective current, i.e. the transit times are current *independent*, the GICCR reduces to a quadratic equation, with an explicit solution for $Q_{p,T}$ (assuming $c_1 = c_{10}$ at low current densities)

$$\boxed{Q_{p,\,T} \;=\; \frac{Q_{pT,\,low}}{2}+\sqrt{\left(\frac{Q_{pT,\,low}}{2}\right)^2+\tau_{f0}c_{10}\exp\left(\frac{v_{B'E'}}{m_{cf}V_T}\right)+\tau_r c_{10}\exp\left(\frac{v_{B'C'}}{V_T}\right)}} \qquad (2.2.0\text{-}21)$$

with $Q_{p,low}$ from (2.2.0-20). Inserting the above solution into i_{Tf} and i_{Tr} and adding the minority charge terms provide quite a useful *initial guess* for the Newton iteration at higher current densities:

$$Q_{p,T,initial} = Q_{pT,low} + \tau_{f0}\, i_{Tf} + \tau_r\, i_{Tr} \;. \qquad (2.2.0\text{-}22)$$

For the practical implementation of the GICCR the reader is referred to the model code.

*. In the SGPM, the solution is obtained by significant simplifications of the minority charge terms, leading to an (explicit) quadratic equation. Such an approach is physically consistent and accurate only at low current densities.

2.3 Minority charge, transit times, and diffusion capacitances

The minority charge is divided into a "forward" and a "reverse" (or inverse) component. The forward component, Q_f, is considered to be dependent on the forward transfer current, i_{Tf}, while the reverse component, Q_r, is considered to be dependent on the reverse transfer current, i_{Tr}. The large-signal charge components can be determined by integrating the respective small-signal transit times, defined as

$$\tau = \frac{dQ}{dI} \tag{2.3.0-23}$$

rather than $\tau = Q/I$.

2.3.1 Minority charge component controlled by the forward transfer current

The operating point dependent minority charge stored in a forward biased (vertical) transistor can be determined from the transit time τ_f by simple integration (cf. Fig. 2.3.1/1),

$$Q_f = \int_0^{i_{Tf}} \tau_f \, di \quad . \tag{2.3.1-1}$$

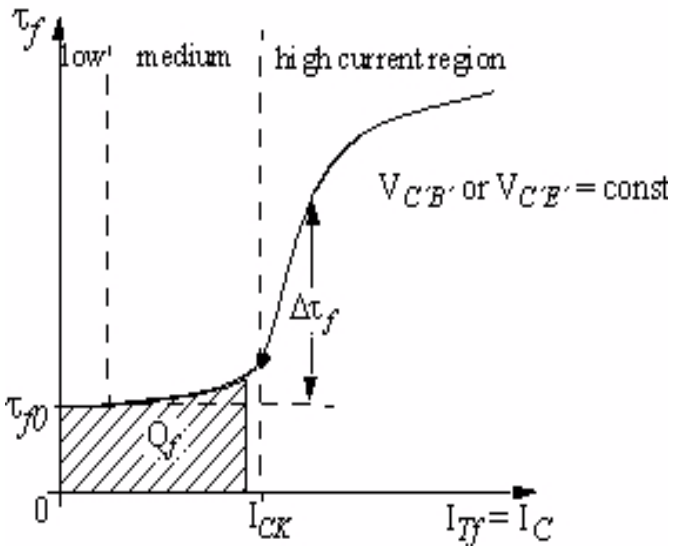

Fig. 2.3.1/1: Illustration of the forward minority charge and transit time as a function of current and definition of the bias regions.

τ_f can be extracted from the measured transit frequency vs. d.c. collector current I_C (=I_T) at forward operation for different voltages v_{CE} or v_{BC} as a parameter. The current and voltage dependent transit time is modelled in HICUM by two components,

$$\boxed{\tau_f(v_{C'E'}, i_{Tf}) = \tau_{f0}(v_{B'C'}) + \Delta\tau_f(v_{C'E'}, i_{Tf})}\,, \qquad (2.3.1\text{-}2)$$

where τ_{f0} is the low-current transit time, and $\Delta\tau_f$ represents the increase of the transit time at high collector current densities. Fig. 2.3.1/2 shows the typically observed behavior of τ_f and its various components, for which physics-based equations will be given later in this chapter. It is important to note, that the sum of all physically (from carrier densities) calculated storage times, τ_{mS}, equals the transit time τ_f, that is extracted from small-signal results using the measurement method.

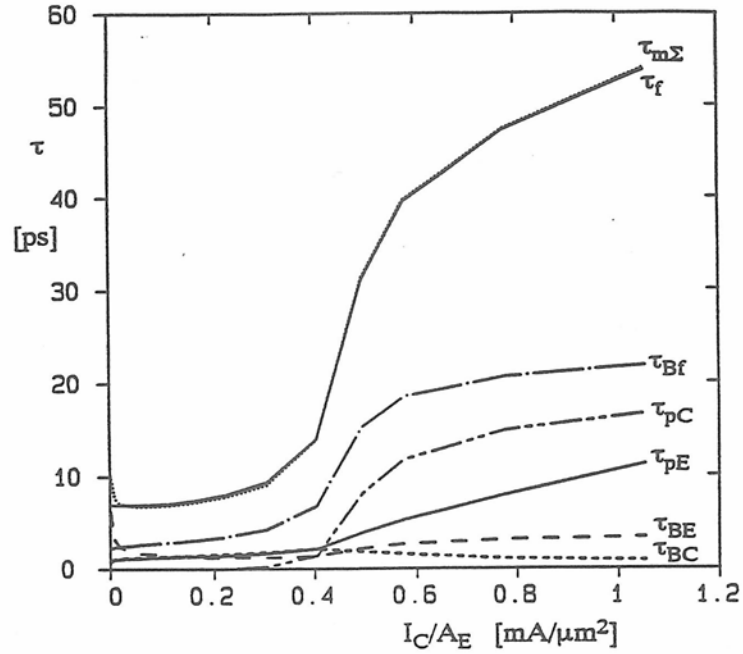

Fig. 2.3.1/2: Charge storage and transit time components vs. collector current density. The components τ_{Bf}, τ_{pC}, τ_{pE}, τ_{BE}, τ_{BC}, and τ_{mS} were calculated from 1D device simulation, while τ_B was extracted from small-signal simulations and f_T using the measurement method.

The minority charge model in HICUM uses an “effective” collector voltage

$$\boxed{v_{ceff} = V_T\left[1 + \frac{u + \sqrt{u^2 + a_{vceff}}}{2}\right]} \text{ with the argument } u = \frac{v_c - V_T}{V_T} \qquad (2.3.1\text{-}3)$$

with the constant a_{vceff} (= 1.921812), which is not a model parameter, and

$$v_c = v_{C'E'} - V_{C'E's} \quad \text{or} \quad v_c = V_{DCk} - v_{B'C'} \ . \tag{2.3.1-4}$$

The internal CE saturation voltage $V_{C'E's}$ ($\approx V_{DEi}$-V_{DCi}) is a model parameter. From v3.0 on, either one of the above options for v_c above can be selected by specifying V_{DCk} (> 0) regardless of the value for $V_{C'E's}$. Ideally, $V_{DCk} = V_{DCi}$, but this couples the critical current modeling with the C_{jCi} modeling and becomes inaccurate (for I_{CK}) especially for a forward biased internal BC junction. The smoothing function for v_{ceff} has been implemented in order to provide a continuous behavior of the critical current (see later) and the forward minority charge for very small and negative values of v_c. As Fig. 2.3.1/3 shows, v_{ceff} is equal to v_c for values larger than about $2V_{C'E's}$ and approaches the thermal voltage V_T as the limit for negative values.

The transit time and minority charge model used in HICUM and its derivation are discussed in detail in [1]. In this text, the most important equations and their physical meaning are summarized.

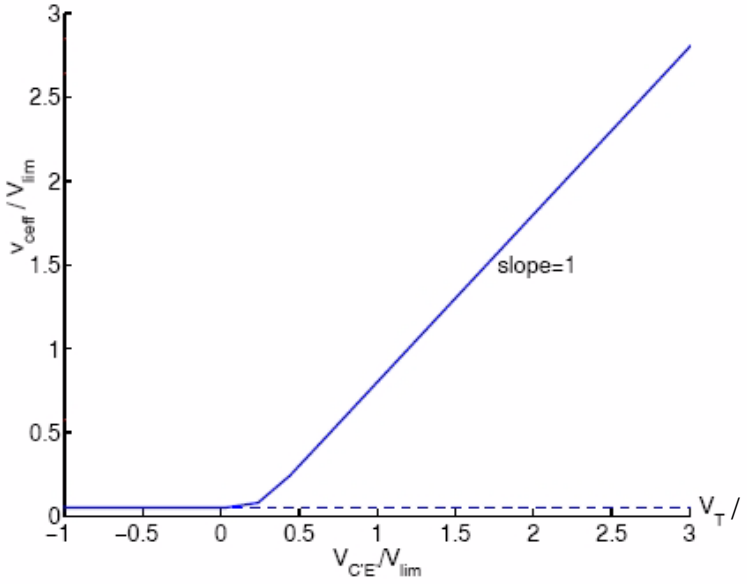

Fig. 2.3.1/3: Normalized effective collector voltage vs. normalized (internal) collector voltage showing the behaviour of the smoothing function.

A. Low-current densities

The low-current component τ_{f0} depends on the collector-base (or collector-emitter voltage) only,

$$\tau_{f0}(v_{B'C'}) = \tau_0 + \Delta\tau_{0h}(c-1) + \tau_{Bvl}\left(\frac{1}{c}-1\right) \tag{2.3.1-5}$$

with the normalized internal BC depletion capacitance $1/c = C_{jCi,t}(V_{B'C'})/C_{jCi0}$. Note, that $C_{jCi,t}$ is evaluated for the same model parameters as the internal BC depletion capacitance C_{jCi}, but with infinite punch-through voltage in order to roughly take into account the impact of the bias dependent space-charge region moving into the base and buried layer beyond the punch-through voltage.

The first time constant in (2.3.1-5), τ_0, represents the sum of voltage independent components of various transistor regions at $V_{B'C'} = 0$; this condition already defines how to extract its value. The second term represents the net voltage dependent change caused by the Early-effect and the transit time through the BC space charge region: for $\Delta\tau_{0h}<0$ the Early effect dominates while for $\Delta\tau_{0h}>0$ the transit time increase caused by the widening of the BC space charge region at large voltages dominates. The third term takes into account the finite carrier velocity in the BC space charge region resulting in a carrier jam at low $V_{C'E'}$ voltages.

Fig. 2.3.1/4 shows two examples for the voltage dependence of the low-current transit time and its two voltage dependent components. The axis values have been normalized to the model parameters τ_0 and V_{DCi}, respectively. The upper figure (a) contains a behavior that is (more) typical for a relatively slow high-voltage transistor, which is characterized by a relatively wide and low-doped collector region under the emitter. In this case, τ_{f0} increases with increasing $V_{C'E'}$ ($=V_{B'E'}-V_{B'C'}$) due to the widening of the BC space charge region. Towards very low $V_{C'E'}$ the drift velocity within the BC space charge region decreases, and the respective (third) term in (2.3.1-5) dominates the voltage dependence, which leads again to an increase of τ_{f0} and to a minimum around $V_{B'C'}=0$.

The lower figure (b) shows the typical behaviour for a high-speed transistor with, e.g., a selectively implanted collector and a thin base. With increasing reverse bias, the BC space charge region does extend noticeably also into the base, resulting in a (slightly) negative value of $\Delta\tau_{0h}$ and a decrease of the respective component. Therefore, τ_{f0} decreases with increasing $V_{C'E'}$.

The respective low-current forward minority charge is simply given by

$$\boxed{Q_{f0} = \tau_{f0}\, i_{Tf}} \quad . \tag{2.3.1-6}$$

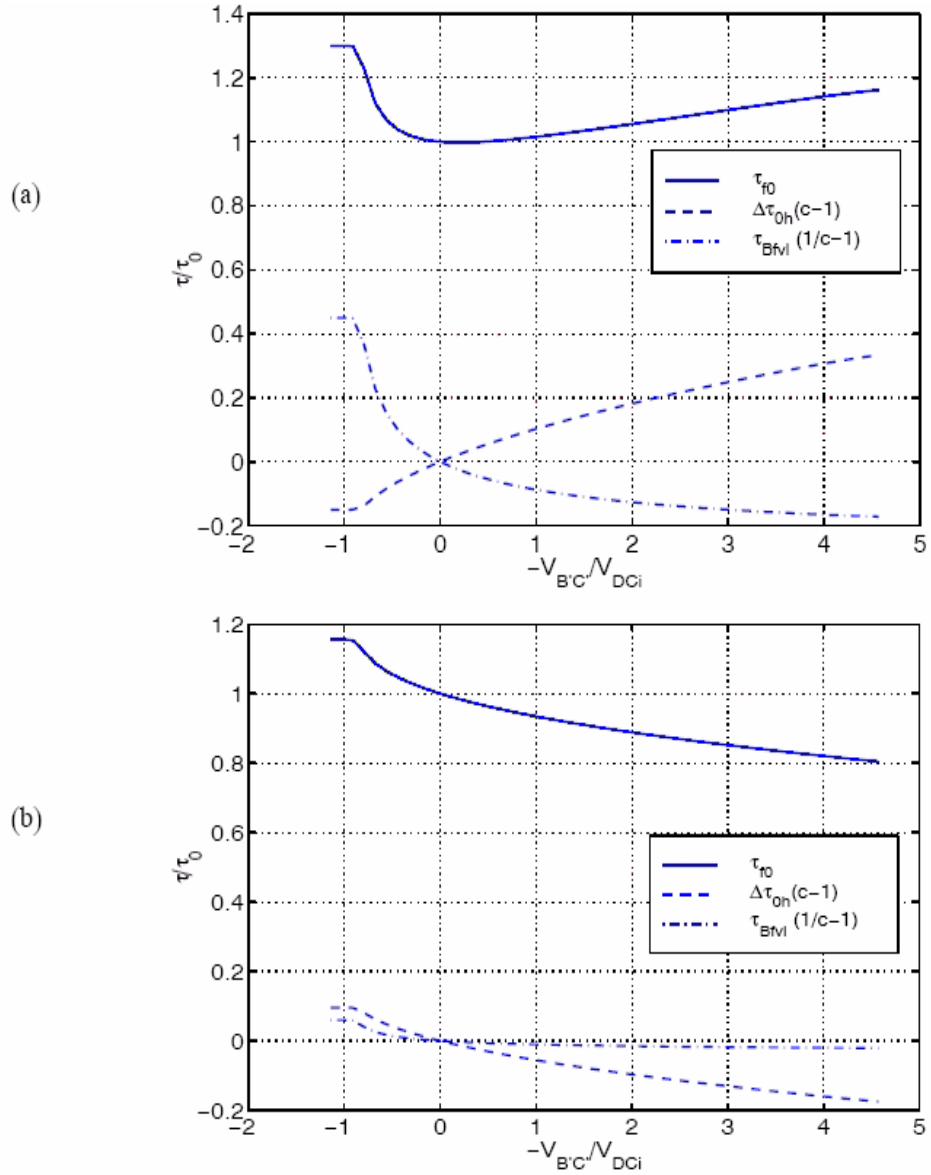

Fig. 2.3.1/4: Normalized low-current transit time and its components as a function of normalized (internal) BC voltage: (a) for a "high-voltage" transistor (τ_0=10ps, $\Delta\tau_{0h}$=2.5ps, τ_{Bfvl}=3ps), (b) for a "high-speed" transistor (τ_0=2.5ps, $\Delta\tau_{0h}$=-0.4ps, τ_{Bfvl}=0.1ps).

B. Medium and high current densities

At medium current densities, the electric field at the BC junction starts to decrease, and the BC junction region becomes quasi-neutral at high current densities. This is often called Kirk-effect [6, 72]. In HICUM, the onset of high-current effects is characterized by the critical current

$$I_{CK} = \frac{v_{ceff}}{r_{Ci0}} \frac{1}{\left(1 + \left(\frac{v_{ceff}}{V_{lim}}\right)^{\delta_{ck}}\right)^{1/\delta_{ck}}} \left[1 + \frac{x + \sqrt{x^2 + a_{ick}}}{2}\right] \qquad (2.3.1\text{-}7)$$

with $x = (v_{ceff}\text{-}V_{lim})/V_{PT}$ in the smoothing function that connects the cases of low and high electric fields in the collector, and with the smoothing parameter a_{ick}(= 10^{-3})*.

The other (model) parameters are the internal collector resistance at low electric fields,

$$r_{Ci0} = \frac{w_C}{q\mu_{nC0}N_{Ci}A_E} \frac{1}{f_{cs}} , \qquad (2.3.1\text{-}8)$$

the voltage defining the boundary between low and high electric fields in the collector,

$$V_{lim} = \frac{v_{sn}}{\mu_{nC0}} w_C , \qquad (2.3.1\text{-}9)$$

and the (collector) punch-through voltage

$$V_{PT} = \frac{qN_{Ci}}{2\varepsilon} w_C^2 . \qquad (2.3.1\text{-}10)$$

As the above relations show, I_{CK} depends on the electron saturation drift velocity, v_{sn}, and the electron low-field mobility, μ_{nC0}, as well as on width w_C and (average) doping N_{Ci} of the internal collector. The current spreading factor f_{cs}, which is discussed in chapter 2.16, facilitates lateral scaling and is calculated by TRADICA [23] (or any other parameter generation program). Despite their physical relationship, r_{Ci0}, V_{lim} and V_{PT} are considered to be model parameters in order to offer a

*.The default value given in parentheses is the constant value used in versions prior to v2.34.

more flexible parameter extraction and broader application of the model. However, their physics-based relationship is very useful for temperature and statistical modelling.

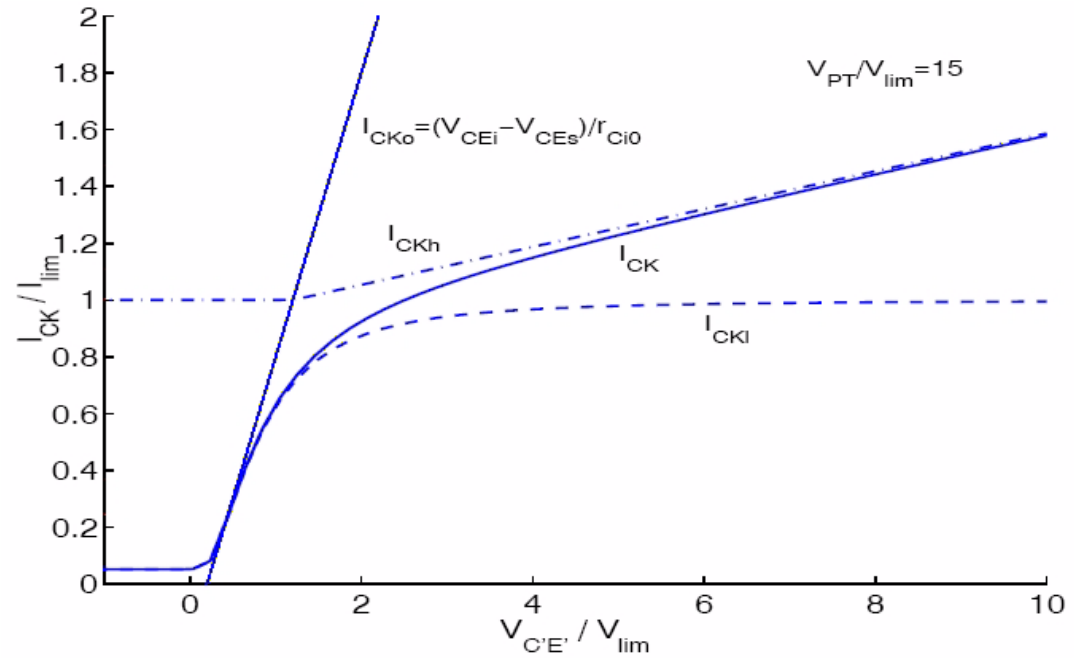

Fig. 2.3.1/5: Normalized critical current I_{CK} vs. normalized internal CE voltage and related single components: $I_{CKl} = (v_{ceff}/r_{Ci0})/\sqrt{1+(v_{ceff}/V_{lim})^2}$ from low-voltage theory;
$I_{CKh} = I_{lim}\,[1+(v_{ceff}-V_{lim})/V_{PT}]$ from high-voltage theory with $I_{lim}=V_{lim}/r_{Ci0}$.

The parameter δ_{ck} in (2.3.1-7) can be used for a more flexible description of the field dependent mobility in the collector (e.g. for pnp transistors as shown in Fig. 2.3.1/6).

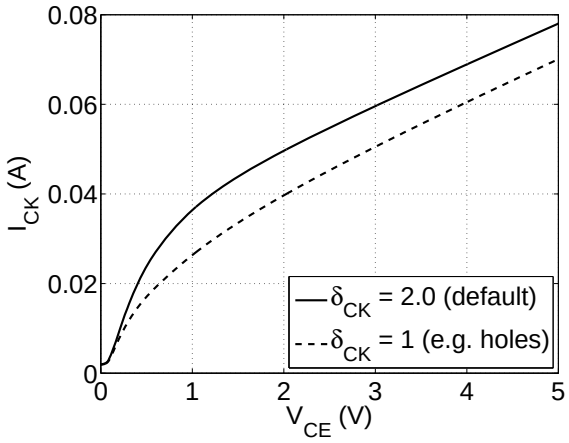

Fig. 2.3.1/6: Different models for I_{CK} using the parameter δ_{ck}.

The consequence of the changing electric field in the BC junction at medium current densities is, first of all, an increase in the neutral base width and, therefore, in the base component of the transit time; secondly, also the transit time through the BC space charge region may increase, depending on how large the electric field is. Thirdly, the corresponding decrease of the small-signal current gain leads to an increase of the emitter component. Since the current independent part of this component has already been taken into account in τ_{f0} only the change (increase) has to be modelled,

$$\boxed{\Delta\tau_{Ef} = \tau_{Ef0}\left(\frac{i_{Tf}}{I_{CK}}\right)^{g_{\tau E}}} \tag{2.3.1-11}$$

with the model parameters g_{tE} and the storage time

$$\tau_{Ef0} = \frac{\tau_{pE0}}{\beta_0} \approx \frac{1}{\beta_0}\left(\frac{w_E}{v_{Ke}} + \frac{w_E^2}{2\mu_{pE}V_T}\right) \tag{2.3.1-12}$$

which depends on the low-frequency common-emitter small-signal current gain β_0 and the hole transit time τ_{pE0} in which w_E, μ_{pE}, and v_{Ke} are the width, hole mobility, and the effective hole contact recombination velocity of the neutral emitter, respectively. The corresponding charge stored in the neutral emitter is:

$$\boxed{\Delta Q_{Ef} = \Delta\tau_{Ef}\frac{i_{Tf}}{1+g_{\tau E}}} \ . \tag{2.3.1-13}$$

In the neutral collector, minority (hole) charge storage starts only at high current densities. Therefore, the charge difference to its negligible low-current contribution is equal to the total hole charge Q_{pC} in the collector:

$$\boxed{\Delta Q_{Cf} = Q_{Cf} = Q_{pC} = \tau_{pCs} i_{Tf} w^2} \tag{2.3.1-14}$$

with the saturation storage time of the neutral collector,

$$\tau_{pCs} = \frac{w_C^2}{4\mu_{nC0}V_T} \ . \tag{2.3.1-15}$$

The normalized injection width,

$$\boxed{w = \frac{w_i}{w_C} = \frac{i + \sqrt{i^2 + a_{hc}}}{1 + \sqrt{1 + a_{hc}}}} \tag{2.3.1-16}$$

is bias dependent via the variable

$$\boxed{i = 1 - \frac{I_{CK}}{i_{Tf}}} \tag{2.3.1-17}$$

while a_{hc} is considered to be a model parameter. By using a smoothing function for w rather than the original expression i in (2.3.1-16), the collector charge is made continuously differentiable over the whole bias region. The corresponding collector storage time is given by

$$\Delta\tau_{Cf} = \tau_{Cf} = \tau_{pC} = \frac{dQ_{pC}}{dI_{Tf}} = \tau_{pCs}\, w^2 \left[1 + \frac{2}{\frac{i_{Tf}}{I_{CK}}\sqrt{i^2 + a_{hc}}}\right] \tag{2.3.1-18}$$

Device simulations for many different processes have shown that the shape of the current dependence of the neutral base component τ_{Bf}, is very similar to that of the collector portion τ_{pC} due to the coupling of these regions by the carrier density at the BC junction. As a consequence, the bias dependent increase of the base charge at high-current densities is similarly expressed as

$$\boxed{\Delta Q_{Bf} = \tau_{Bfvs} i_{Tf}\, w^2} \tag{2.3.1-19}$$

with the saturation storage time reached at high current densities,

$$\tau_{Bfvs} = \frac{w_{Bm} w_C}{2 G_{\zeta i} \mu_{nC0} V_T}. \tag{2.3.1-20}$$

w_{Bm} is the metallurgical base width, and G_{zi} (≥1) is a factor that depends on the drift field in the neutral base. The corresponding additional base transit time reads

$$\Delta\tau_{Bf} = \frac{d\Delta Q_{Bf}}{dI_{Tf}} = \tau_{Bfvs}\, w^2 \left[1 + \frac{2}{\frac{i_{Tf}}{I_{CK}} \sqrt{i^2 + a_{hc}}} \right] . \qquad (2.3.1\text{-}21)$$

In HICUM, the total storage time constant,

$$\tau_{hcs} = \tau_{pCs} + \tau_{Bfvs} = \frac{w_C^2}{4\mu_{nC0} V_T} + \frac{w_{Bm} w_C}{2 G_{\zeta i} \mu_{nC0} V_T} , \qquad (2.3.1\text{-}22)$$

is used as a model parameter to make the model application more flexible and easy to use. As discussed in chapter 2.16, the accurate and physics-based description of collector current spreading and associated lateral scaling at high current densities require a partitioning between base and collector component. For this, the partitioning constant

$$f_{\tau hc} = \frac{\tau_{pCs}}{\tau_{hcs}} = \frac{w_C}{w_C + 2 w_{Bm}} \qquad (2.3.1\text{-}23)$$

is introduced as model parameter. A value of f_{thc} between 0 and 1 allows a gradual partitioning, with the 1D expressions given above (i.e. no collector current spreading) being employed for $f_{thc} = 0$, while a dominating influence of the collector term (including current spreading) can be taken into account by $f_{thc} \to 1$.

Fig. 2.3.1/7 shows a sketch of the current dependence of the *additional* transit time $\Delta\tau_f$ and its various components, calculated with the equations given above and using model parameters that are typical for a high-speed process.

In case of negligible collector current spreading (corresponding to 1D current flow), the collector and base component can be lumped together ($f_{thc} = 0$), leading to the expression for the additionally stored minority charge in the base and collector region at high current densities,

$$\boxed{\Delta Q_{fh} = \Delta Q_{Bf} + Q_{Cf} = \tau_{hcs} i_{Tf} w^2} . \qquad (2.3.1\text{-}24)$$

The corresponding increase of the transit time at high-current densities is then given by

$$\Delta\tau_{fh} = \Delta\tau_{Bf} + \tau_{Cf} = \tau_{hcs}\, w^2 \left[1 + \frac{2}{\frac{i_{Tf}}{I_{CK}}\sqrt{i^2 + a_{hc}}} \right] . \qquad (2.3.1\text{-}25)$$

The 1D current flow is detected by the model if the model parameters LATB and LATL (cf. chapter 2.16) are zero.

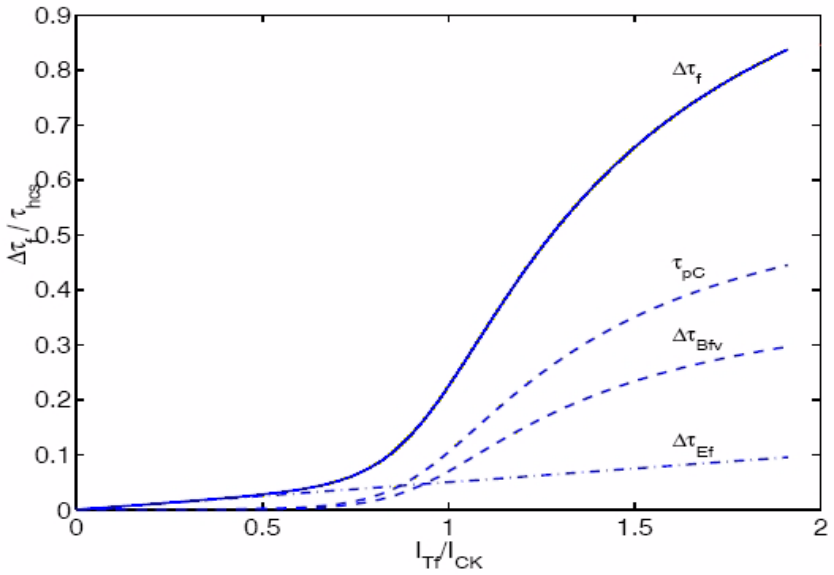

Fig. 2.3.1/7: Sketch of normalized transit time $\Delta\tau_f$ vs. normalized forward collector current I_{Tf}, including the various components: collector component τ_{pC}, additional base component $\Delta\tau_{Bf}$, and additional emitter contribution $\Delta\tau_{Ef}$.

The total minority charge in the various operating regions, that is used for transient or high-frequency analysis, is then calculated according to (2.3.0-23) and it consists of the following contributions:

$$Q_f = Q_{f0} + \Delta Q_{Ef} + \Delta Q_{fh} \qquad (2.3.1\text{-}26)$$

while the total forward transit time (or storage time) is given by

$$\tau_f = \tau_{f0} + \Delta\tau_{Ef} + \Delta\tau_{fh} \ . \qquad (2.3.1\text{-}27)$$

If the lateral scaling capability is used, ΔQ_{fh} and $\Delta\tau_{fh}$ are composed of their separately calculated base and collector contribution (cf. chapter 2.16). The above equations contain physical and proc-

ess parameters that facilitate the predictions of the electrical characteristics as a function of process variations.

In SiGe HBTs (and other HBTs with a heterojunction in the BC SCR), a strong increase of the transit time may be observed at the onset of high current effects depending on the location of the heterojunction relative to the junction. The associated BC barrier effect is modeled in HICUM by the current and voltage dependent barrier voltage

$$\Delta V_{cB} = V_{cBar} \exp\left(-\frac{2}{i_{Bar} + \sqrt{i_{Bar}^2 + a_{cBar}}}\right) \tag{2.3.1-28}$$

with the smoothing variable

$$i_{Bar} = \frac{i_{Tf} - I_{CK}}{i_{cBar}} \tag{2.3.1-29}$$

and the model parameters V_{cBar}, a_{cBar} and i_{cBar}. As shown in Fig. 2.3.1/8, the barrier voltage as obtained by 1D device simulation is modeled very accurately by this equation. Setting $V_{cBar} = 0$ turns off the entire barrier effect formulation.

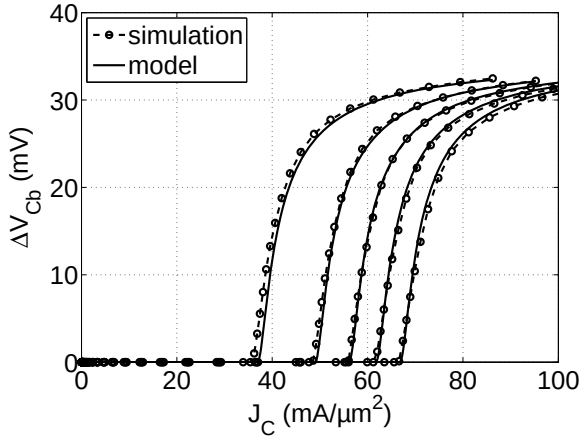

Fig. 2.3.1/8: Modeling of the barrier voltage.

Due to the barrier, the charge and transit time of (2.3.1-26) and (2.3.1-27) change to

$$Q_f = Q_{f0} + \Delta Q_{Ef} + \Delta Q_{fh,c+} \Delta Q_{Bf,b} \tag{2.3.1-30}$$

and

$$\tau_f = \tau_{f0} + \Delta\tau_{Ef} + \Delta\tau_{fh,c+}\,\Delta\tau_{Bf,b}. \tag{2.3.1-31}$$

The impact of the BC barrier effect on the base region related mobile charge component is described by

$$\boxed{\Delta Q_{Bf,\,b} = \tau_{Bfvs} i_{Tf}\left[\exp\left(\frac{\Delta V_{cB}}{V_T}\right) - 1\right]} \tag{2.3.1-32}$$

with $\tau_{Bfvs} = (1\text{-}f_{\tau hc})\tau_{hCs}$. The Kirk-effect related collector charge and transit time increase is delayed by the barrier voltage according to

$$\boxed{\Delta Q_{fh,\,c} = \tau_{hCs} i_{Tf} w^2 \exp\left(\frac{\Delta V_{cB} - V_{cBar}}{V_T}\right)}. \tag{2.3.1-33}$$

Using above equations, the strong increase of the transit time as well as a possible overshoot is modeled as shown in Fig. 2.3.1/9 for a comparison with 1D device simulation.

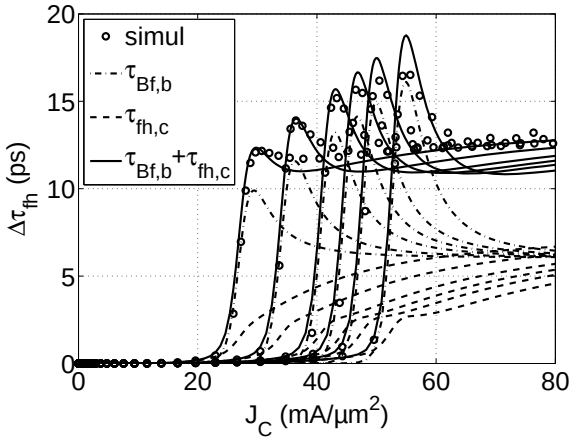

Fig. 2.3.1/9: Modeling of the transit time taking the heterojunction effect into account.

Modeling collector current spreading requires the modification of only the collector component $\Delta Q_{Cf,c}$ of $\Delta Q_{fh,c}$, while modeling the barrier related recombination in the base (and associated additional base current) requires an expression for the total additional base charge

$$\Delta Q_{Bf} = \Delta Q_{Bf,b} + \Delta Q_{Bf,c}. \tag{2.3.1-34}$$

Using the parameter $f_{\tau hc}$ allows to split $\Delta Q_{fh,c}$ into the two desired components

$$\boxed{\Delta Q_{Cf,\,c} = f_{\tau hc}\Delta Q_{fh,\,c}}, \tag{2.3.1-35}$$

$$\boxed{\Delta Q_{Bf,\,c} = (1 - f_{\tau hc})\Delta Q_{fh,\,c}}, \tag{2.3.1-36}$$

while the sum of the original charges still remains the same:

$$\Delta Q_{\mathrm{fh,c+}}\, \Delta Q_{\mathrm{Bf,b}} = \Delta Q_{Cf,c} + \Delta Q_{Bf}. \tag{2.3.1-37}$$

A detailed explanation of these components can be found in [1].

2.3.2 Minority charge component controlled by the inverse transfer current

For forward transistor operation in high-speed applications, the portion of the minority charge which is exclusively controlled by the base-collector voltage is often negligible or only a small fraction of the total minority charge. Therefore, including this charge in Q_f causes only negligible error in transient operation of transistors in high-speed circuits. For small-signal high-frequency operation in the high-current region, which is a very unusual case, the base-collector voltage controlled charge may be taken into account by including its diffusion capacitance in the total internal base collector capacitance.

Alternatively, the BC diffusion charge can be modelled by the simple relation

$$Q_\mathrm{r} = \tau_\mathrm{r}\, i_\mathrm{Tr} \tag{2.3.2-1}$$

with the inverse transit time τ_r as a model parameter.

2.4 Depletion charges and capacitances

Modelling of depletion charges (Q_j) and capacitances (C_j) as a function of the voltage v across the respective junction is partially based on classical theory that gives within a certain operating range

$$Q_j = \int_0^v C_j dv' = \frac{C_{j0} V_D}{1-z}\left[1-\left(1-\frac{v}{V_D}\right)^{(1-z)}\right] \qquad (2.4.0\text{-}2)$$

and

$$C_j = \frac{C_{j0}}{\left(1-\frac{v}{V_D}\right)^z} \quad . \qquad (2.4.0\text{-}3)$$

The zero bias capacitance C_{j0}, the diffusion (or built-in) voltage V_D as well as the exponent coefficient z are the model parameters. Due to the pole at forward bias, i.e. at $v = V_D$, however, the above formula is not yet suited for a compact model from both a numerical and physics-based point of view. The respective modification will be described for the BE depletion capacitance.

At high reverse voltages the epitaxial collector can become fully depleted up to the buried layer. This punch- (or reach-)through effect is also not included in the classical equation above (and in the SGPM). The corresponding extension will be discussed for the BC depletion capacitance.

2.4.1 Base-emitter junction

Fig. 2.4.1/1 shows the voltage dependence of a BE depletion capacitance at forward bias. The symbols were obtained from 1D device simulation. The depletion capacitance follows quite well the classical equation up to a certain voltage, which is close to the turn-on voltage of a transistor used for switching applications. In contrast to the classical equation, the capacitance then reaches a maximum within the “practical” operation range of a transistor. Towards very high forward bias, the capacitance even decreases to zero, since the total depletion charge has to be limited from a physical point of view.

The modified equation employed in HICUM is described below for the example of the internal BE depletion capacitance with the (classical) model parameters C_{jEi0}, V_{DEi}, z_{Ei}, and the additional model parameter a_{jEi}. The latter is defined in Fig. 2.4.1/1 as the ratio of the maximum value to the

zero-bias value and can directly be extracted from f_T measurements at low current densities (e.g. [5, 1]). As a consequence, C_{jEi} is kept at its maximum value in HICUM to maintain consistency between measurement and model. Keeping C_{jEi} constant is also justified, because at high forward bias, i.e. beyond the maximum, the diffusion capacitance becomes orders of magnitude larger than C_{jEi}. The reverse bias region of the BE depletion capacitance and charge is described by the classical equations.

For modeling the peripheral BE depletion charge and capacitance, the corresponding model parameters C_{jEp0}, V_{DEp}, z_{Ep}, a_{jEp} as well as the voltage and $v_{B*E'}$ have to be inserted.

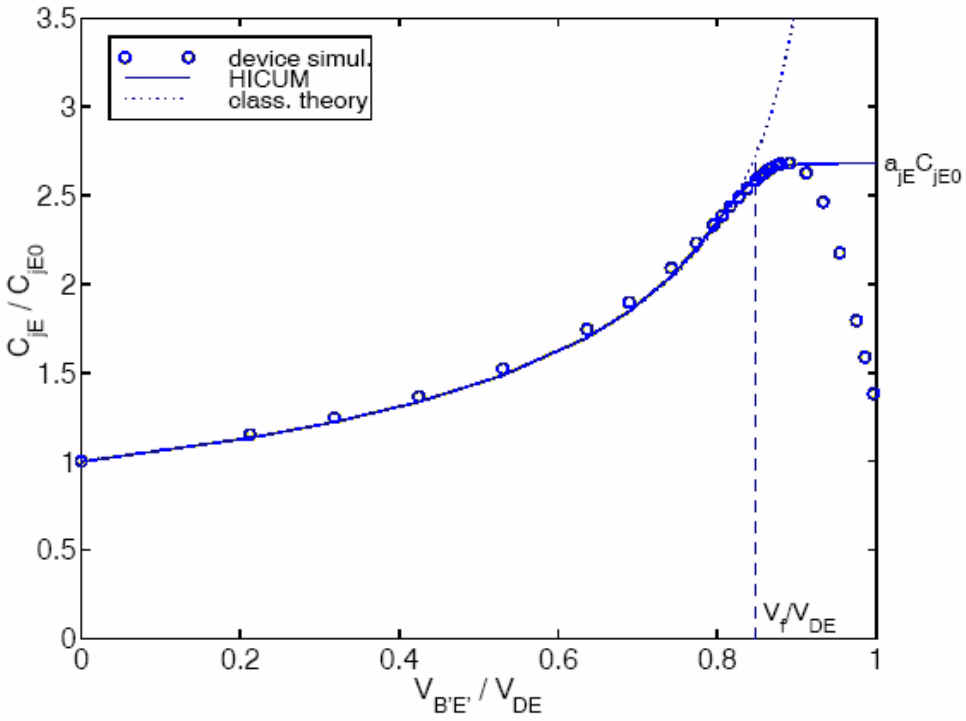

Fig. 2.4.1/1: Typical dependence of BE depletion capacitance on junction voltage at forward bias: comparison between 1D device simulation, HICUM, classical theory. In addition, characteristic variables used in the model equations have been inserted.

From Fig. 2.4.1/1, the forward bias depletion charge can be composed of a classical portion and a component for medium and large forward bias:

$$Q_{jEi} = \frac{C_{jEi0}V_{DEi}}{1-z_{Ei}}\left[1-\left(1-\frac{v_j}{V_{DEi}}\right)^{(1-z_{Ei})}\right] + a_{jEi}C_{jEi0}(v_{B'E'}-v_j). \qquad (2.4.1\text{-}1)$$

The arithmetic overflow at V_{DEi} is avoided by replacing the junction voltage $V_{\mathrm{B'E'}}$ with the auxiliary voltage

$$v_j = V_f - V_T \frac{x + \sqrt{x^2 + a_{fj}}}{2} < V_f \tag{2.4.1-2}$$

using hyperbolic smoothing and the argument

$$x = \frac{V_f - v_{B'E'}}{V_T}. \tag{2.4.1-3}$$

V_{f} is the voltage at large forward bias, at which the capacitance of the classical expression intercepts the maximum constant value (cf. Fig. 2.4.1/1):

$$\boxed{V_f = V_{DEi}[1 - a_{jEi}^{-(1/z_{Ei})}]}. \tag{2.4.1-4}$$

Q_{jEp} is calculated similarly.

The depletion capacitance is then calculated from the derivative of the charge yielding

$$C_{jEi} = \frac{C_{jEi0}}{(1 - v_j / V_{DEi})^{z_{Ei}}} \cdot \frac{dv_j}{dv_{B'E'}} + a_{jEi} C_{jEi0} \left(1 - \frac{dv_j}{dv_{B'E'}}\right) \tag{2.4.1-5}$$

with the derivative of v_j,

$$\frac{dv_j}{dv_{B'E'}} = \frac{x + \sqrt{x^2 + a_{fj}}}{2\sqrt{x^2 + a_{fj}}}. \tag{2.4.1-6}$$

The capacitance is not explicitly coded in the Verilog-A implementation. Instead the derivative of the depletion charge is calculated automatically (symbolically and numerically) where required.
In (2.4.1-6), the value of a_{fj} can be adjusted to yield results equivalent to an exponential smoothing function formulation in the original version 2.1. If at $x = 0$, which corresponds to $v_{B'E'} = V_f$, the exponential and hyperbolic function values for v_j are forced to be the same, and one obtains

$$a_{fj} = 4\ ln^2(2) = 1.921812\,. \qquad (2.4.1\text{-}7)$$

This is not a model parameter, but a fixed constant within the code. Fig. 2.4.1/2 shows a comparison of the (2.4.1-2) with the original equation in version 2.1. There is no visible difference; the numerically calculated error is below 1.4% for a_{jEi} = 3, and below 1% for values of 2.4 or lower.

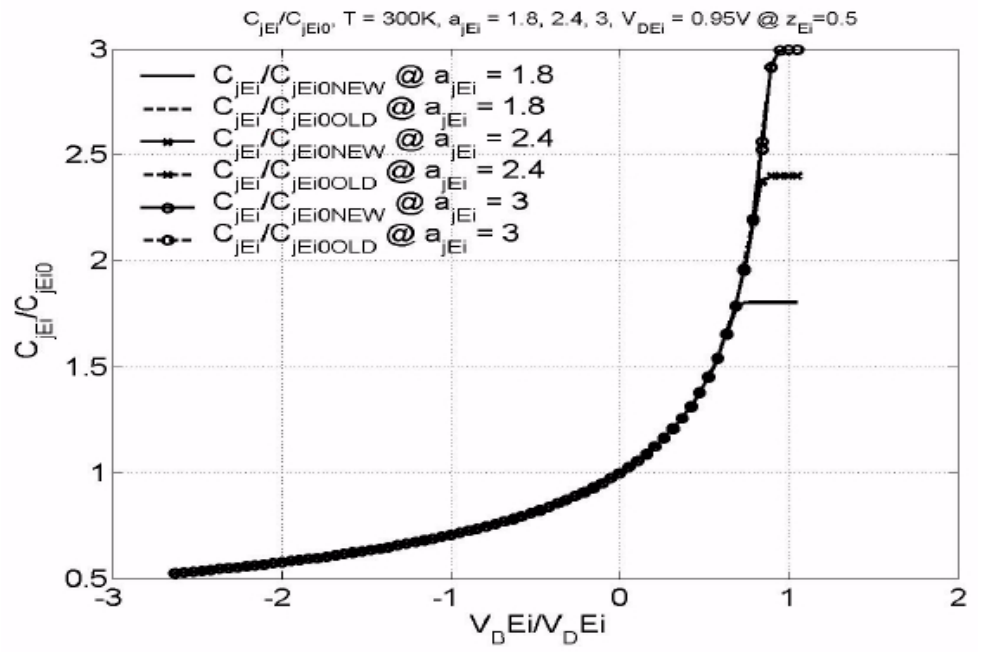

Fig. 2.4.1/2: Base-emitter depletion capacitance calculated with equation (2.4.1-2) with a_{jEi} as parameter.

2.4.2 Internal base-collector junction

The BC junction is usually operated at reverse bias. If the internal voltage $v_{C'B'}$ exceeds the effective punch-through voltage (see later), the epitaxial collector region becomes fully depleted. For an ideal step-like transition from the epitaxial collector to the buried-layer the corresponding capacitance would remain constant (like a plate capacitance). However, in reality the doping concentration increases with only a finite slope towards the maximum buried layer concentration. As a consequence, C_{jCi} still decreases even beyond punch-through, but with a weaker voltage dependence.

Before the capacitance equation is explained in detail, it is helpful to define a number of variables that are needed in the equations. The effective punch-through voltage is given by

$$V_{jPCi} = V_{PTCi} - V_{DCi} = \frac{qN_{Ci}}{2\varepsilon} w_{Ci}^2 - V_{DCi} \quad , \tag{2.4.2-1}$$

which is shown in Fig. 2.4.2/1. For flexibility and accuracy reasons as well as in order to simplify and decouple parameter extraction, V_{PTCi} is considered as a separate model parameter rather than using V_{PT} from the I_{CK} formulation. For predictive modeling V_{PTCi}=V_{PT} is certainly a good initial guess.

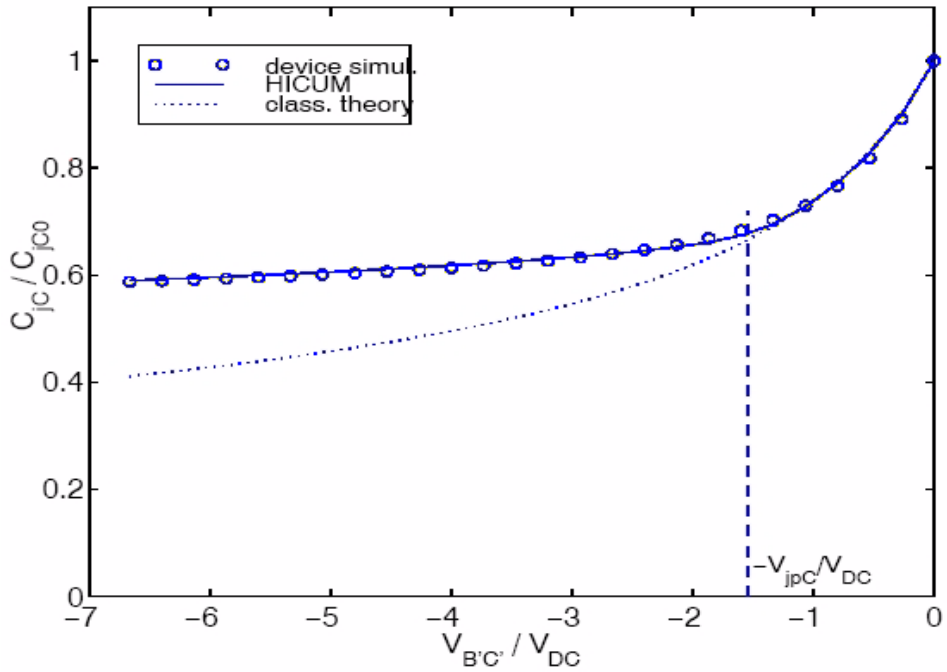

Fig. 2.4.2/1: Typical dependence of BC depletion capacitance on junction voltage at reverse bias: comparison between 1D device simulation (symbols), HICUM (solid line), classical theory (dashed line). In addition, characteristic variables used in the model equations have been inserted.

The voltage defining the boundary between the classical expression and the maximum (constant) value at large forward bias was already defined for the BE junction capacitance (cf. Fig. 2.4.1/1); in terms of the respective BC model parameters it reads here as:

$$\boxed{V_{fCi} = V_{DCi}[1 - a_{jCi}^{-(1/z_{Ci})}]} \quad . \tag{2.4.2-2}$$

The voltage, at which the transition from medium to large reverse bias (slowly) starts, is defined as

$$\boxed{V_r = 0.1V_{jPCi} + 4V_T}\,. \tag{2.4.2-3}$$

In the following, "large reverse" bias is defined as $v_{\mathrm{BCi}} \le -V_{\mathrm{jPCi}}$, "medium" bias is defined as $V_{\mathrm{jPCi}} < v_{\mathrm{BCi}} < V_{\mathrm{fCi}}$, and "large forward" bias is defined as $v_{\mathrm{BCi}} \ge V_{\mathrm{fCi}}$.

The depletion capacitance consists of three components,

$$\boxed{C_{jCi} = C_{jCi,\,cl} + C_{jCi,\,PT} + C_{jCi,\,fb}}\,, \tag{2.4.2-4}$$

which are discussed below in more detail.

$C_{\mathrm{jCi,cl}}$ represents the contribution at medium bias,

$$\boxed{C_{jCi,cl} = \frac{C_{jCi0}}{(1 - v_{j,m}/V_{DCi})^{z_{Ci}}} \cdot \frac{e_{j,r}}{1 + e_{j,r}} \frac{e_{j,m}}{1 + e_{j,m}}} \tag{2.4.2-5}$$

which contains the classical equation as the first term. The last two product terms result from smoothing functions for the respective BC junction voltage, that enable a continuously differentiable transition to the two adjacent bias regions. Like for the BE depletion capacitance, the numerical overflow at large forward bias is avoided by replacing $v_{\mathrm{B'C'}}$ with the auxiliary (smoothed) voltage, $v_{j,m}$, defined in (2.4.1-2). The collector punch-through at reverse bias is included by an additional smoothing term,

$$\boxed{v_{j,r} = V_{fCi} - V_T \ln[1 + e_{j,r}]} \quad \text{with} \quad \boxed{e_{j,r} = \exp\left(\frac{V_{fCi} - v_{B'C'}}{V_T}\right)}, \tag{2.4.2-6}$$

which also contains the actual junction voltage $v_{\mathrm{B'C'}}$. Analogously to C_{jE}, the forward bias value (for $e(v_{j,r}) = 0$) is limited to a maximum,

$$\boxed{C_{jCi,fb} = a_{jCi} C_{jCi0} \frac{1}{1 + e_{j,r}}}\,, \tag{2.4.2-7}$$

with a_{jCi} as a constant. The last term is again a continuously differentiable function that enables a smooth transition between medium and large forward bias. Since C_{jCi} is of little practical relevance

at high forward bias, a_{jCi} is set to 2.4 in the code, rather than being a model parameter in order to keep the number of parameters as low as possible.

Finally, $C_{\mathrm{jCi,PT}}$ represents the large reverse bias region around and beyond punch-through,

$$\boxed{C_{jCi,PT} = \frac{C_{jCi0,r}}{(1 - v_{j,r}/V_{DCi})^{z_{Ci,r}}} \cdot \frac{1}{1 + e_{j,m}}} \quad . \tag{2.4.2-8}$$

Here, the first term contains the classical voltage dependence, but now with different parameters $C_{\mathrm{jCi0,r}}$ and $z_{\mathrm{Ci,r}}$, which model the weak bias dependence under punch-through conditions, and will be discussed later. In this case, the auxiliary voltage is given by the smoothing function

$$\boxed{v_{j,m} = -V_{jPCi} + V_r\left[\ln(1 + e_{j,m}) - \exp\left(-\frac{V_{jPCi} + V_{fCi}}{V_r}\right)\right]} \quad \text{with}$$

$$\boxed{e_{j,m} = \exp\left(\frac{V_{jPCi} + v_{j,r}}{V_r}\right)} \tag{2.4.2-9}$$

which now depends on the auxiliary voltage $v_{\mathrm{j,r}}$ in order to enable a smooth capacitance and charge behavior over all bias regions. Note, that $v_{\mathrm{j,r}}$ equals $v_{\mathrm{B'C'}}$ at large reverse bias. The last term in $v_{j,m}$ avoids a possible numerical overflow ($v_{\mathrm{j,m}} > V_{\mathrm{DCi}}$) for very small values of z_{Ci} at high forward bias.

The corresponding depletion charge is then obtained by integration of C_{jCi},

$$\boxed{Q_{jCi} = \underbrace{Q_{jCi,m}}_{\text{medium}} + \underbrace{Q_{jCi,r}}_{\text{reverse}} - \underbrace{Q_{jCi,c}}_{\text{correction}} + \underbrace{a_{jCi}C_{jCi0}(v_{B'C'} - v_{j,r})}_{\text{large forward}}} \tag{2.4.2-10}$$

with the component at medium bias,

$$\boxed{Q_{jCi,m} = \frac{C_{jCi0}V_{DCi}}{1 - z_{Ci}}\left[1 - \left(1 - \frac{v_{j,m}}{V_{DCi}}\right)^{1 - z_{Ci}}\right]} \ , \tag{2.4.2-11}$$

the component at large reverse bias,

$$\boxed{Q_{jCi,r} = \frac{C_{jCi0,r}V_{DCi}}{1 - z_{Ci,r}}\left[1 - \left(1 - \frac{v_{j,r}}{V_{DCi}}\right)^{1 - z_{Ci,r}}\right]} \ , \tag{2.4.2-12}$$

and a “correction” component,

$$\boxed{Q_{jCi,c} = \frac{C_{jCi0,r} V_{DCi}}{1 - z_{Ci,r}} \left[1 - \left(1 - \frac{v_{j,m}}{V_{DCi}} \right)^{1 - z_{Ci,r}} \right]} \quad , \tag{2.4.2-13}$$

that results from the integration process. The parameters $C_{\mathrm{jCi0,r}}$ and $z_{\mathrm{Ci,r}}$ in the last two components are required to model the weaker voltage dependence under punch-through conditions, compared to the voltage dependence at medium bias. $C_{\mathrm{jCi0,r}}$ can be calculated from the punch-through voltage as

$$\boxed{C_{jCi0,r} = C_{jCi0} \cdot \left(\frac{V_{DCi}}{V_{PTCi}} \right)^{(z_{Ci} - z_{Ci,r})}} \quad , \tag{2.4.2-14}$$

while $z_{\mathrm{Ci,r}}$ is internally set to $z_{\mathrm{Ci}}/4$. The latter turned out to be a good compromise for the investigated cases. As consequence, both $C_{\mathrm{jCi0,r}}$ and $z_{\mathrm{Ci,r}}$ are only internal parameters and do not have to be extracted and externally specified. If required, however, it would be sufficient to make $z_{\mathrm{Ci,r}}$ a user model parameter.

At high current densities C_{jCi} becomes also current dependent as discussed, e.g., in [1]. The respective (smooth) expressions for both capacitance and charge require complicated expressions which can increase simulation time significantly. For small-signal applications, a pure voltage dependent model for C_{jCi} is usually sufficient, since transistors in (small-signal) analog circuits are not operated at high current densities. For large-signal transient applications, however, the influence of a current dependent C_{jCi} is negligible, especially at higher current densities. Therefore, the current dependence of C_{jCi} has been neglected so far.

2.4.3 External base-collector junction

The total BC capacitance consists of a bias dependent external depletion capacitance, C_{jCx}, and a bias independent parasitic capacitance C_{BCpar} (see also Section 2.7). The depletion portion in turn contains a SIC related bottom component, a background doping related bottom component and a perimeter component, that all usually have different voltage dependence and, hence, model parameters. For a compact model, the depletion components are merged into a single element by fitting a single set of model parameters to the overall voltage dependence (e.g. using TRADICA). The re-

sulting capacitance (and charge), $C_{BCx} = C_{jCx}(v) + C_{BCpar}$, is then partitioned across the external base resistance r_{Bx} (cf. Fig. 2.1.0/1) according to a first-order high-frequency approximation of the RC transmission line behaviour of the external base. This merging procedure, which is also required for simpler equivalent circuit structures, reduces the number of model parameters to be specified for the circuit simulator. A possible alternative is to determine the partitioning from measurements of, e.g., high-frequency S-parameters; however, it was found that such a partitioning factor (strongly) depends on the measurement method and conditions used and, therefore, can assume non-physical values.

The partitioning of the total capacitance C_{BCx} across r_{Bx} requires an additional model parameter,

$$f_{BCpar} = \frac{C_{BCx2}}{C_{BCx}} \quad . \tag{2.4.3-1}$$

and defines the ratio of the portion at the perimeter base node ("behind" r_{Bx}) to the total capacitance. The factor f_{BCpar} depends on geometry and technology specific parameters (and can be calculated by, e.g., TRADICA). According to (2.4.3-1) the capacitances are split as follows in the present HICUM implementation (cf. Fig. 2.1.0/1):

$$C_{BCx} = C_{BCx1} + C_{BCx2} = (1\text{-}f_{BCpar})\, C_{BCx} + f_{BCpar}\, C_{BCx} \; . \tag{2.4.3-2}$$

Depending on the values for f_{BCpar}, C_{BCpar} and C_{jCx} as well as according to the nature of the capacitance components, different cases have to be distinguished. For instance, if $f_{BCpar} > C_{BCpar}/C_{BCx}$ then part of C_{BCpar} has to be connected to node B* (i.e. *behind* r_{Bx}). Since C_{BCpar} is closest to the base contact, usually the major portion or even its total value has to be connected to the base terminal B. The various cases are taken into account based on the zero-bias depletion capacitance rather than the voltage dependent value in order to reduce arithmetic operation count. The implementation is as shown in Fig. 2.1.4/4.

$C_{BCx01} = (1\text{-}f_{BCpar})\, C_{BCx0}$

if$(C_{BCx01} \geq C_{BCpar})$ *then*

$C_{BCpar1} = C_{BCpar}$

$C_{BCpar2} = 0$

$C_{jCx01} = C_{BCx01} - C_{BCpar}$

$C_{jCx02} = C_{jCx0} - C_{jCx01}$
else
$C_{BCpar1} = C_{BCx01}$
$C_{BCpar2} = C_{BCpar} - C_{BCpar1}$
$C_{jCx01} = 0$
$C_{jCx02} = C_{jCx0}$
endif

Fig. 2.4.3/1: Implementation of BC capacitance partitioning

Since the depletion charge of the external BC junction does not depend on the transfer current, the purely voltage dependent expressions given for C_{jCi} and Q_{jCi} can be employed for C_{jCx} and Q_{jCx} by simply inserting the model parameters C_{jCx0}, V_{DCx}, z_{Cx}, and V_{PTCx}. The punch-through voltage (and capacitance) of the external collector region is usually different from that of the internal region due to their different epi widths and - in case of a selectively implanted collector - the different doping concentrations in the internal and external region.

2.4.4 Collector-substrate junction

The CS depletion charge and capacitance consist of a bottom and a perimeter component, which were merged into a single element in model versions up to v2.33. From model version 2.34 on, both components are available separately in order to improve the description of the output admittance at high frequencies. The two components are modelled by the same formulation as employed for the external BC depletion charge and capacitance. The corresponding model parameters are C_{jS0}, V_{DS}, z_S, and V_{PTS} for the bottom component and C_{SCp0}, V_{DSp}, z_{Sp} and V_{PTSp} for the perimeter component in a junction isolated technology. Taking into account the punch-through effect may be necessary for technologies containing a semi-insulating substrate (layer). For most technologies, however, there is no punch-through effect at the CS junction, and V_{PTS} can be set to "infinity". For deep trench isolation (DTI) the perimeter component may become voltage independent. This case can be modelled by setting $V_{dSp} = 0$. In this case, $C_{SCp} = C_{SCp0}$ for all voltages and temperatures.

For certain applications and processes, an additional substrate coupling network in series to C_{jS} (i.e. the bottom component) as well as a substrate transistor may be necessary. These extensions are discussed later in ch. 2.11.

2.5 Static base current components

The base current flowing into the emitter can be separated into a bottom and peripheral component. The bottom portion models the current injected across the (*effective*) emitter area, and the peripheral component models the current injected across the peripheral BE junction. Each of these components contains the current contributions caused by volume (SRH and Auger) recombination, by surface recombination, by tunneling, and by an (effective) interface recombination velocity at the emitter "contact". The physical modelling of all these effects, including e.g. the modulation of the neutral emitter width in advanced and heterojunction bipolar transistors, would require a complicated and computationally time expensive description as well as a significantly increased effort in parameter determination. From a practical application point of view, however, a simpler approach for most of the above mentioned components does exist that is sufficiently accurate.

The following equations describe the d.c. and quasi-static component of the base current, which are applicable also at high frequencies. Note, that at high switching speeds or frequencies, the dynamic (capacitive) component of the base current becomes much larger than the d.c./quasi-static component, so that its correct modeling is of higher importance for those applications.

The quasi-static internal base current, which represents injection across the bottom emitter area, is modelled in HICUM as

$$\boxed{i_{jBEi} = I_{BEiS}\left[\exp\left(\frac{v_{B'E'}}{m_{BEi}V_T}\right)-1\right] + I_{REiS}\left[\exp\left(\frac{v_{B'E'}}{m_{REi}V_T}\right)-1\right]} \qquad (2.5.0\text{-}1)$$

The saturation currents I_{BEiS} and I_{REiS} as well as the non-ideality coefficients m_{BEi} and m_{REi} are model parameters. The first component in the above formula represents the current injected into the neutral emitter; a corresponding $m_{\mathrm{BEi}}>1$ represents effects such as Auger recombination and the (very small) modulation of the width of the neutral emitter region. The second component represents the loss in the space charge region due to volume and surface recombination; the value of m_{REi} is usually in the range of 1.5 to 2 so that this component only plays a role at low injection. It is used to model the decrease of the current gain at low current densities.

Analogously, the quasi-static base current injected across the emitter periphery is given by

$$i_{jBEp} = I_{BEpS}\left[\exp\left(\frac{v_{B^*E'}}{m_{BEp}V_T}\right)-1\right] + I_{REpS}\left[\exp\left(\frac{v_{B^*E'}}{m_{REp}V_T}\right)-1\right]. \qquad (2.5.0\text{-}2)$$

The saturation currents I_{BEpS} and I_{REpS} as well as the non-ideality factors m_{BEp} and m_{REp} are model parameters.

Since the recombination at low forward bias is more pronounced at the emitter periphery compared to the bottom, its contribution (I_{REiS} ...) to the internal base current component may often be omitted in order to simplify the model and the parameter determination.

In hard-saturation or for inverse operation the current contributions across the base-collector junction become significant. The component of the internal BC junction is

$$i_{jBCi} = I_{BCiS}\left[\exp\left(\frac{v_{B'C'}}{m_{BCi}V_T}\right)-1\right] . \qquad (2.5.0\text{-}3)$$

The component for the external BC junction reads correspondingly

$$i_{jBCx} = I_{BCxS}\left[\exp\left(\frac{v_{B^*C'}}{m_{BCx}V_T}\right)-1\right] . \qquad (2.5.0\text{-}4)$$

In many practical cases, both components can be combined into one, i_{jBC}, between B* and C', without loss of accuracy (in, e.g., the output characteristics). This simplifies parameter extraction and reduces the number of model parameters.

In various SiGe-HBT processes, an additional base current is observable that mostly results from the additional minority charge storage in the base at the barrier caused by the Ge drop within the BC junction [7]. The typical behavior is shown in Fig. 2.1.5/1 for the base current of a SiGe-DHBT. Triggered by the collapse of the electric field in the collector at high current densities, which can be described by the critical current I_{CK}, the conduction band barrier for electrons starts to form at about V_{BE} = 0.8V for the transistor under consideration. The resulting accumulation of electrons on the base side of the BC junction is compensated by an accumulation of holes, which leads to an excess recombination rate. As a consequence, the corresponding current can be approximated to a first order by

$$i_{Bhrec} = \frac{\Delta Q_{Bf}}{\tau_{Bhrec}} \tag{2.5.0-5}$$

with ΔQ_{Bf} from (2.3.1-34) as the additional minority charge in the base, which increases rapidly above I_{CK}; the corresponding recombination constant τ_{Bhrec} is a model parameter. The current has been taken into account by adding a (controlled) current source in parallel to i_{jBEi}.

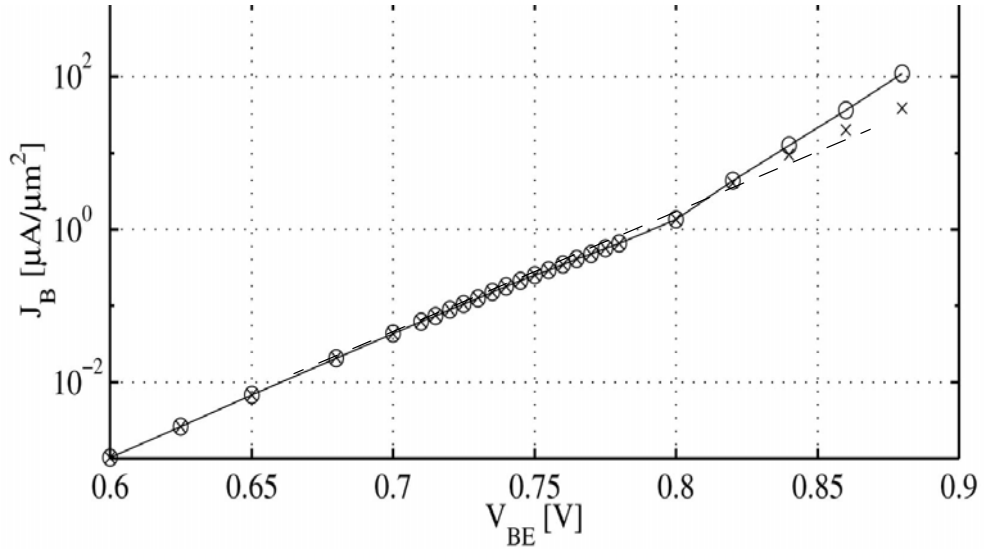

Fig. 2.5.0/1: Base current vs. base-emitter voltage for a SiGe-DHBT. Comparison between device simulation (circles), model without additional recombination component (dashed line) and model with additional recombination component (crosses).

2.6 Internal base resistance

In HICUM, the internal and external base resistance are separately treated. The value of the internal base resistance r_{Bi} depends strongly on operating point, temperature, and mode of transistor operation (d.c., transient, h.f. small-signal). Especially the last mentioned dependence is a very complicated issue for high-speed large-signal switching processes.

The d.c. internal base resistance is modelled as

$$r_{Bi} = r_i \psi(\eta) \tag{2.6.0-6}$$

and is in HICUM/Level2 defined by the *effective* emitter dimensions b_E and l_E. Both the resistance r_i and the emitter current crowding function $\psi(\eta)$ are bias and geometry dependent. The effect of conductivity modulation is being discussed first.

Conductivity modulation is described by the expression

$$r_i = r_{Bi0} \frac{Q_0}{Q_0 + \Delta Q_p} , \tag{2.6.0-7}$$

with r_{Bi0} as zero-bias internal base resistance, and the bias dependent portion ΔQ_p of the stored hole charge,

$$\boxed{\Delta Q_p = Q_{jEi} + Q_{jCi} + Q_f + Q_r \approx Q_{jEi} + Q_{jCi} + Q_f}, \tag{2.6.0-8}$$

Q_r is generally very small and hence is being neglected. Q_0 is a model parameter that is physically related and often is close to the zero-bias hole charge Q_{p0}. Therefore, Q_0 is calculated from Q_{p0} as,

$$\boxed{Q_0 = (1 + f_{DQr0}) Q_{p0}} \tag{2.6.0-9}$$

with the factor f_{dQr0} as model parameter.

Under extreme bias conditions (such as base “reach-through” with $Q_{jEi} + Q_{jCi}$ approaching $-Q_{p0}$) or with odd combination of model parameters, (2.6.0-7) can cause a numerical instability due to division by zero or a negative resistance value, which is not physical. This can be avoided by en-

suring that the denominator remains larger than zero for all conditions. Defining the normalized charge $q_r = 1 + \Delta Q_p / Q_0$, (2.6.0-7) is rewritten as

$$r_i = r_{Bi0} \frac{1}{f(q_r)}, \tag{2.6.0-10}$$

where the smoothing function

$$f(q_r) = \frac{q_r + \sqrt{q_r^2 + a_{qr}}}{2} \quad \text{with} \quad a_{qr} = 0.01 , \tag{2.6.0-11}$$

reaches the value 0.05 if q_r approaches -1. In a real transistor, reverse depletion charges lower than $-Q_{p0}$ (> $-Q_0$) are not impossible but extremely unlikely. Although this case is not avoided in the model for the charges themselves, the corresponding instability in r_i is avoided.

Fig. 2.6.0/2 shows the typical bias dependence of the (normalized) internal base sheet resistance due to conductivity modulation; the ratio r_{SBi}/r_{SBi0} is proportional to r_i/r_{Bi0}.

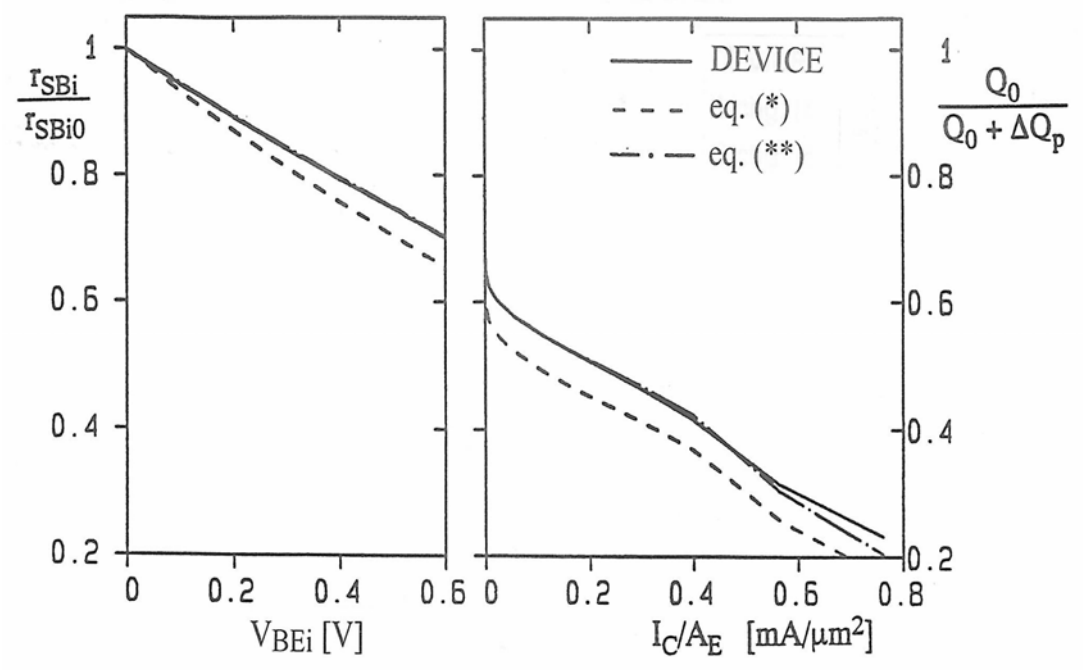

Fig. 2.6.0/2: Typical bias dependence of the normalized internal base sheet resistance and comparison to eq. (2.6.0-7) with f_{dQr0}=0 (labeled eq. (*)) and f_{dQr0}>0 (labeled eq. (**)) [1]. DEVICE corresponds to (1D) numerical device simulation; (V_{BEi}=$V_{B'E'}$).

The zero-bias resistance r_{Bi0} is a model parameter which can be calculated (e.g., by TRADICA) as a function of emitter geometry and zero-bias internal base sheet resistance r_{SBi0}. For a transistor with n_E emitter contacts (or stripes) and arbitrary aspect ratio $l_E/b_E \geq 1$:

$$r_{Bi0} = r_{SBi0} \frac{b_E}{l_E n_E} g_i \tag{2.6.0-12}$$

with the geometry function for n_E+1 base contacts

$$g_i = \frac{1}{12} - \left(\frac{1}{12} - \frac{1}{28.6}\right)\frac{b_E}{l_E} \quad . \tag{2.6.0-13}$$

The effect of emitter current crowding is described for all aspect ratios $l_E/b_E \geq 1$ by the function

$$\boxed{\psi(\eta) = \frac{\ln(1+\eta)}{\eta}} \tag{2.6.0-14}$$

with the current crowding factor

$$\boxed{\eta = f_{geo} \frac{r_i i_{jBEi}}{V_T}} \quad . \tag{2.6.0-15}$$

The factor f_{geo} is a model parameter which takes into account the geometry dependence of emitter current crowding (cf. Chapter 2.16). Hence, the final expression for the internal base resistance is

$$\boxed{r_{Bi} = r_i \cdot \frac{\ln(1+\eta)}{\eta}} \tag{2.6.0-16}$$

For transistors with narrow emitter contacts (or stripes) the influence of the charge storage at the emitter periphery on the dynamic transistor behaviour can significantly increase. In order to obtain acceptable computation times and to keep the extraction effort reasonable, the HICUM/LEVEL2 equivalent circuit does not contain a complete peripheral transistor element. Therefore, the peripheral charge has to be taken into account by modifying existing elements. The internal base impedance seen between the terminals B*-E' is decreased by the (effective) peripheral charge Q_{fp} to

$$r_{Bi}^{*} = r_{Bi}\frac{\Delta Q_i}{\Delta Q_p} = r_{Bi}\frac{\Delta Q_i}{\Delta Q_i + Q_{fp}} \quad . \tag{2.6.0-17}$$

ΔQ_i is the change of the hole charge in the internal transistor during a switching process. For model implementation, however, ΔQ_i is approximated by the change of only the *major* charge contributions w.r.t. equilibrium,

$$\boxed{\Delta Q_i = Q_{jEi} + Q_{fi}} \tag{2.6.0-18}$$

with Q_fi as the internal *minority* charge. The latter as well as the peripheral minority charge Q_fp can be calculated from the total minority charge Q_f, that is analytically described in the model, using the model parameter f_Qi,

$$\boxed{Q_{fi} = f_{Qi}Q_f} \quad \text{and} \quad \boxed{Q_{fp} = (1-f_{Qi})Q_f} \tag{2.6.0-19}$$

The parameter f_Qi depends on geometry and can be determined from the transit time of transistors with, e.g., different emitter widths. Note, the denominator of (2.6.0-17) contains Q_f directly so that Q_fp is not required to be explicitly known or calculated. Thus, the implemented equation reads

$$\boxed{r_{Bi}^{*} = r_{Bi}\frac{Q_{jEi} + f_{Qi}Q_f}{Q_{jEi} + Q_f}} \; . \tag{2.6.0-20}$$

For the (high-frequency) small-signal case a similar expression can be derived [1],

$$r_{Bi}^{*} = r_{Bi}\frac{C_i}{C_i + C_{dEp}} \tag{2.6.0-21}$$

with $C_\mathrm{dEp} = C_\mathrm{dE}(1\text{-}f_\mathrm{Qi})$ as the peripheral diffusion capacitance and

$$\boxed{C_i = C_{jEi} + C_{dEi}} \tag{2.6.0-22}$$

as the total capacitance connected to the *internal* base node B'. The use of r_{Bi}^{*} from (2.6.0-17) gives for slow transients or low frequencies a (small) difference compared to the actual d.c. value of r_Bi.

However, that deviation is usually insignificant because the influence of the peripheral charge or capacitance is large only for narrow emitter stripes where the d.c. internal base resistance is comparatively small. Note again, that for calculating the denominator of (2.6.0-21) C_{dEp} does not need to be known explicitly, but only C_{dE}:

$$r_{Bi}^{*} = r_{Bi}\frac{C_{jEi} + f_{Qi}C_{dE}}{C_{jEi} + C_{dE}}. \tag{2.6.0-23}$$

2.7 External (parasitic) bias independent capacitances

In addition to junction and diffusion capacitances, that are both operating point dependent, there may exist constant parasitic capacitances between base and emitter as well as base and collector. The parasitic base-emitter capacitance C_{BEpar} is caused by the spacer region and overlap of emitter poly over base poly. The parasitic base collector capacitance C_{BCpar} is caused by the overlap of base poly and contact region over the buried layer (or the epi collector). The significance of theses capacitances depends on the technology considered. In order to make HICUM applicable for an as large as possible variety of technologies, two parasitic capacitances are included in the equivalent circuit of Fig. 2.1.0/1.

C_{BEpar} takes into account the overlap of emitter and base connection, e.g., n^+ poly-silicon separated from p^+ poly-silicon by the thin spacer (cf. Fig. 2.7.0/3) as well as the (metal) capacitance caused by the proximity of the via studs on top of the contacts, which is required to connect the latter to a metal layer.

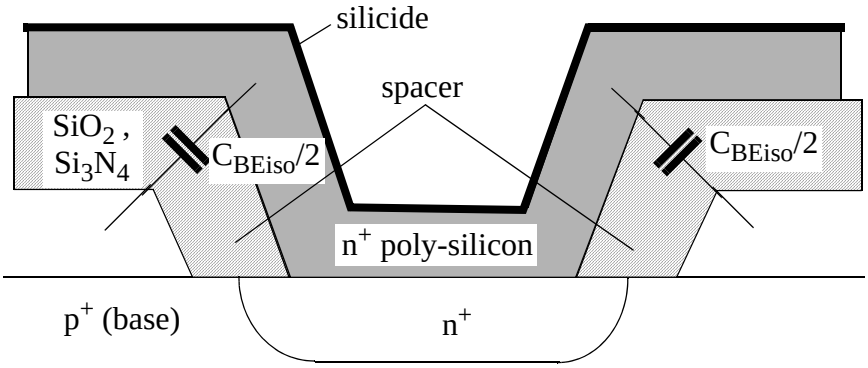

Fig. 2.7.0/3: Physical origin of the BE isolation capacitance C_{BEiso}, which is part of the C_{BEpar}.

Physically, the BE isolation capacitance C_{BEiso}, which is caused by the base-emitter spacer region, and the external base resistance may have a distributed character, as shown in Fig. 2.7.0/4(a). Moreover, in advanced processes, the isolation capacitance increases due to a smaller spacer thickness, while the base-emitter perimeter junction capacitance C_{jEp}, represented by its charge element charge Q_{jEp} in Fig. 2.7.0/4(b), is decreasing due to shallower emitter junction depths. The exact representation of these elements in a compact model for an accurate high-frequency description depends on the contributions of the various base resistance and capacitance portions and the geometry

of the BE spacer isolation region. In addition to the BE spacer related capacitance C_{BEiso}, the parasitic capacitance $C_{BE,metal}$ (and its associated charge $Q_{BE,metal}$) from the metal contact studs on top of the base and emitter poly-silicon increases with shrinking design rules. This capacitance, which belongs to the layout (p-cell) and thus to the transistor model, is connected directly between the base and emitter terminals.

For a compact model, a lumped representation of both the external base resistance and the parasitic capacitances is required. For this, a p-equivalent circuit is the best first-order compromise (cf. Fig. 2.7.0/4(b)) that allows an improved high-frequency modeling. Therefore, the distributed isolation capacitance is partitioned between the perimeter and external base node to make the model more flexible for a larger variety of processes. For instance, if the resistance contribution of the spacer region to the total external base resistance dominates, most of C_{BEiso} needs to be assigned to the internal base node ($C_{BEiso,2}$). The partitioning of C_{BEiso} in form of a π-equivalent circuit also allows to include the metal capacitance without any additional effort.

The partitioning option requires as model parameters the specification of either the partial capacitance components at each node or the total parasitic BE capacitance,

$$C_{BEpar} = C_{BEiso} + C_{BE,\,metal} \tag{2.7.0-24}$$

and a partitioning factor. The latter option is more convenient from a user's point of view and, hence, employed in HICUM. The respective model parameter

$$f_{BEpar} = \frac{C_{BEpar,\,2}}{C_{BEpar}} = \frac{C_{BEiso,\,2} + C_{BE,\,metal}}{C_{BEiso} + C_{BE,\,metal}} \tag{2.7.0-25}$$

is defined as the ratio of the "inner" to the total (measured) parasitic capacitance. Thus, the value $f_{BEpar} = 0$ indicates that the whole parasitic capacitance is connected between the transistor terminals.

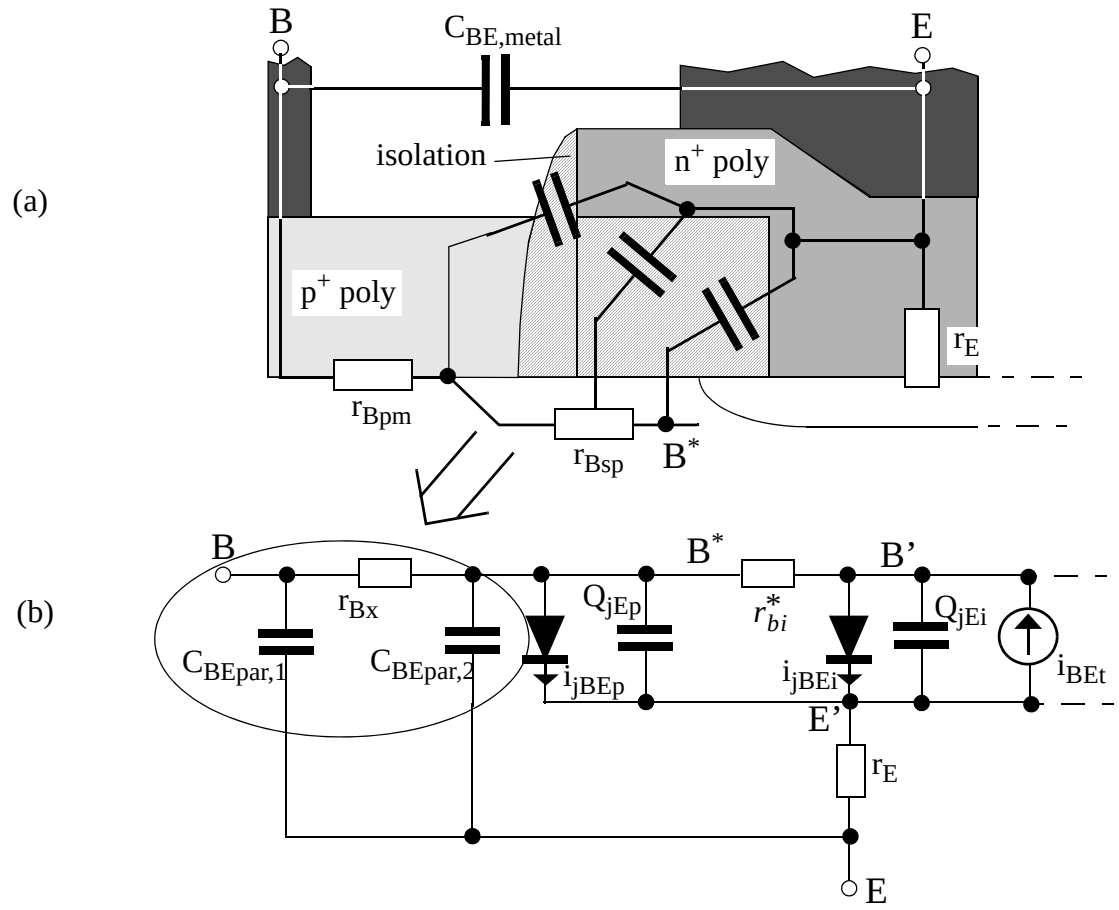

Fig. 2.7.0/4: External and internal base-emitter region: (a) schematic cross-section of left half of base-emitter region with physical series resistance and distributed isolation capacitance components; (b) equivalent circuit with lumped isolation charge (and capacitance) partitioning.

In many modern bipolar technologies the base contact is located on a field oxide and causes an additional isolation capacitance C_{BCpar} between base and collector terminal (cf. Fig. 2.7.0/5). This capacitance is included in the equivalent circuit within C_{BCx} since its partitioning across r_{Bx} depends on the technology. The parameter f_{BCpar} determines the actual partitioning of C_{BCpar}, too, as was shown earlier in Fig. 2.4.2/1.

Both the parasitic capacitances are strongly geometry dependent and either have to be measured using proper test structures or can be calculated by TRADICA [23].

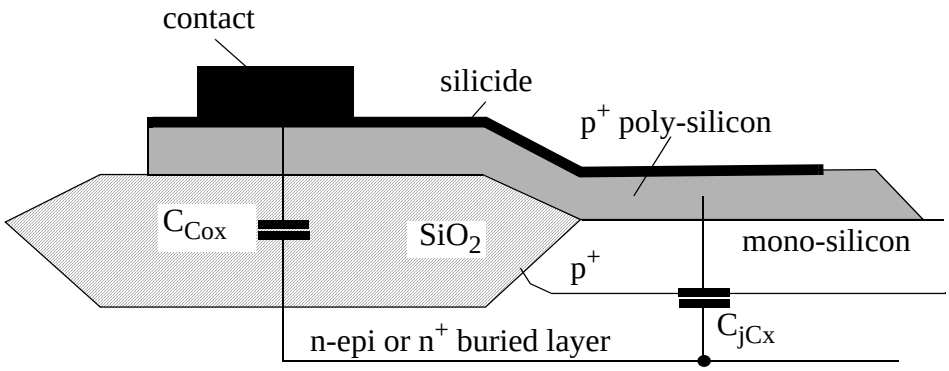

Fig. 2.7.0/5: Physical origin of BC isolation (overlap) capacitance C_{Cox}, which is part of C_{BCpar}.

2.8 External series resistances

The resistive regions of the external transistor and the emitter contact are represented in the equivalent circuit of Fig. 2.1.0/1 by bias independent series resistances. The reason for including a substrate resistance in the equivalent circuit will be discussed in Section 2.11.

2.8.1 External base resistance

Fig. 2.8.1/1 contains a cross section through the external base region of a double-poly self-aligned bipolar transistor. The external base resistance r_{Bx} consists of the following components:

- base contact resistance, r_{KB};
- resistance of the poly-silicon on the field oxide, r_{po};
- resistance of the poly-silicon on the mono-silicon, r_{pm};
- (link) resistance under the spacer, r_{sp}.

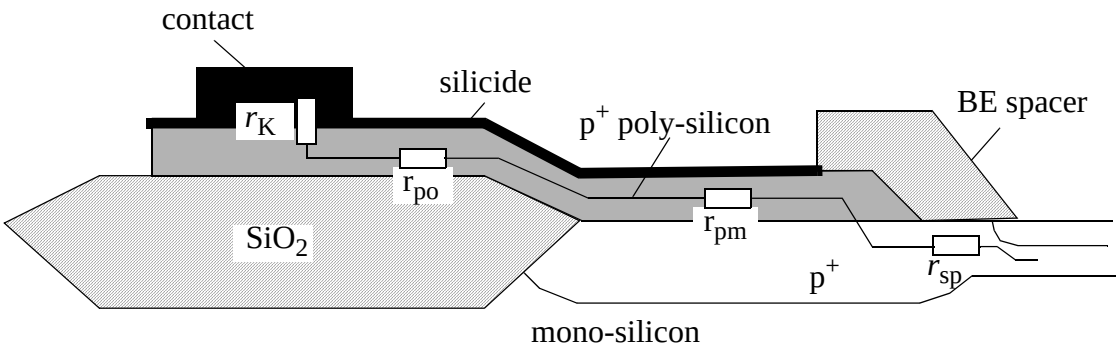

Fig. 2.8.1/1: The various components of the external base resistance.

The value of each of these components depends on the dimensions of the region and the corresponding sheet resistance or specific resistivity. The external base resistance is then given by:

$$r_{Bx} = r_{KB} + r_{po} + r_{pm} + r_{sp} \qquad (2.8.1\text{-}1)$$

Many advanced processes use a silicide with a sheet resistance of typically 2...10 Ω/sq. As a consequence, r_{po} and a portion of r_{pm} are significantly reduced and become small compared to the contact and, especially, the link resistance.

For short emitters and transistors with a one-sided base contact only, 3D effects become important that are taken into account by TRADICA's resistance calculations.

Methods for determining r_{Bx} have been reviewed in [55].

2.8.2 External collector resistance

Fig. 2.8.2/1 contains a cross section through the buried layer and collector region of a bipolar transistor. The external collector resistance r_{Cx} consists of the following components:

- collector contact resistance, r_{KC};
- resistance of the sinker region, r_{sink}, connecting contact and buried layer;
- resistance of the buried layer, r_{bl}.

The value of each of these components depends on the dimensions of the region and the corresponding sheet resistance or specific resistivity. The external collector resistance is then given by:

$$r_{Cx} = r_{KC} + r_{sink} + r_{bl} \tag{2.8.2-1}$$

The external collector resistance does not contain any resistance component from the epitaxial layer under the emitter. If r_{KC} is determined by the poly-mono-silicon interface resistance, it would be about the same as the emitter contact resistance.

The distributed collector current flow in multi-emitter transistors as well as a different number and location of collector stripes (or contacts) is taken into account in TRADICA by using special formulas. Also, for short emitter (and collector) stripes, current spreading in the buried layer is included in the resistance calculations.

Methods for determining r_{Bx} have been reviewed in [58, 60].

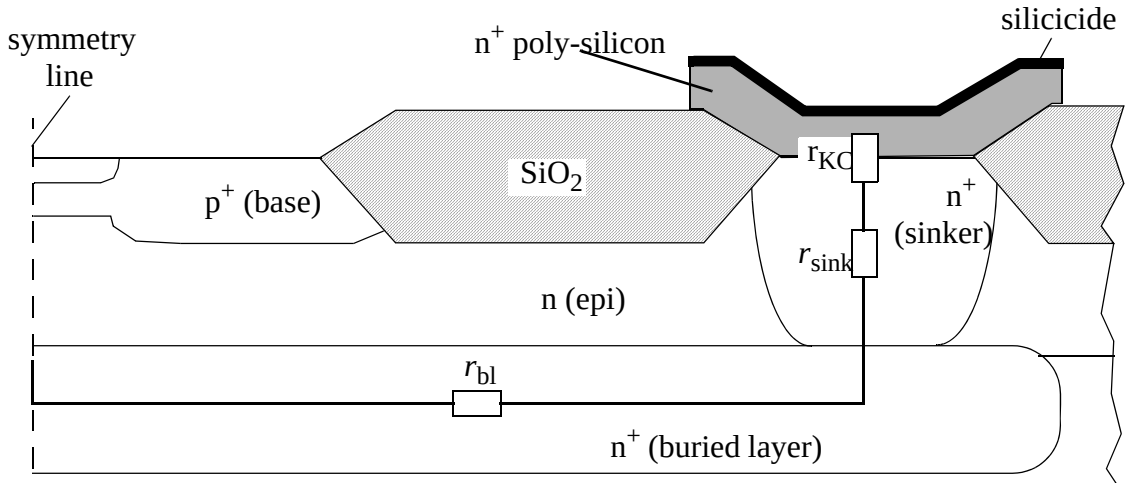

Fig. 2.8.2/1: The various components of the external collector resistance.

2.8.3 Emitter resistance

The emitter resistance r_E consists of the following (major) components:

- metallization resistance, r_{Em};
- poly-silicon resistance, r_{Ep};
- resistance of the interface between poly-silicon and mono-silicon, r_{Ei};
- resistance of the mono-silicon bulk region, r_{Eb}.

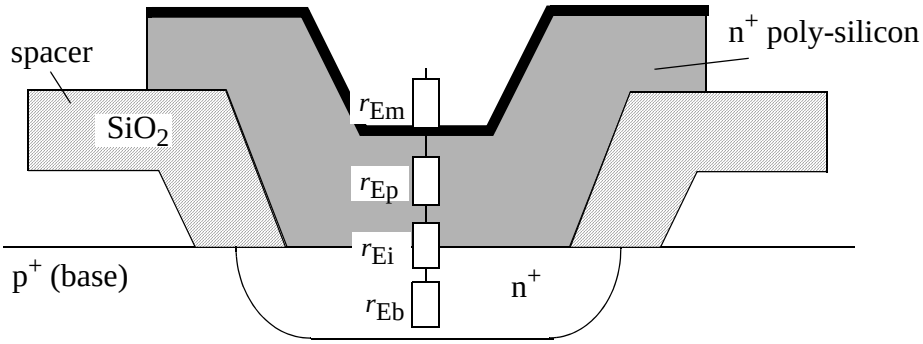

Fig. 2.8.3/1: The various components of the emitter resistance.

For many processes, measurements have been showing a direct proportionality of r_E with the reciprocal emitter window area [30]. As a consequence, it is assumed that the emitter resistance for technologies with poly-silicon emitter is mainly determined by the resistance r_i at the interface between poly- and mono-silicon, and that contributions from the other regions are of minor importance. However, this has to be verified for each particular process. Methods for determining r_E have been reviewed in [49].

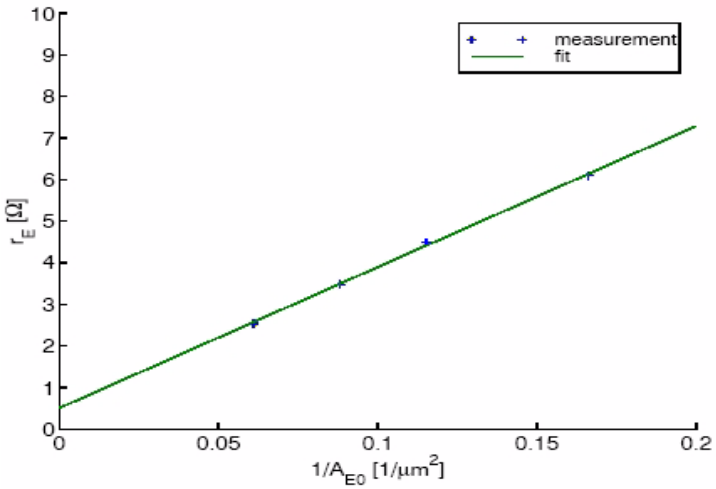

Fig. 2.8.3/2: Measured emitter resistance vs. reciprocal emitter window area and comparison to the scaling equation $r_E = \bar{r}_E / A_E + r_0$ with $\bar{r}_E$ as area specific emitter resistance in [$\Omega\mu m^2$] and r_0 as residual (parasitic) probe resistance.

2.9 Non-quasi-static effects

Non-quasi-static (NQS) effects are occurring at high-frequencies or fast switching processes. Note, that the designation "high" or "fast" is relative and depends on the technology employed. NQS effects exist in both vertical and lateral spatial direction.

2.9.1 Vertical NQS effects

It is well-known from “classical” transistor theory that at high frequencies the minority charge Q_f and the transfer current i_T are reacting delayed w.r.t. the voltages across both pn-junction. This effect is taken into account in HICUM by introducing additional delay times for both Q_f and I_{Tf}. These additional delay times are modelled as a function of bias by relating them to the transit time:

$$\boxed{\tau_2 = \alpha_{Qf}\tau_f \qquad \text{and} \qquad \tau_m = \alpha_{iT}\tau_f} \ . \tag{2.9.1-1}$$

The factors α_{Qf} and α_{iT} are model parameters. The assumption of a stiff coupling between the additional delay times and the transit time has to be regarded as a first order approximation, especially at high current densities where a certain current dependence of α_{Qf} and α_{iT} has been observed. However, it is questionable whether a more complicated modelling of τ_2 and τ_m is justified from an application point of view. Note, that the SGPM only allows τ_m to be specified for *one* (fixed) operating point. Fig. 2.9.1/1 shows the NQS delay times as a function of collector current density for.

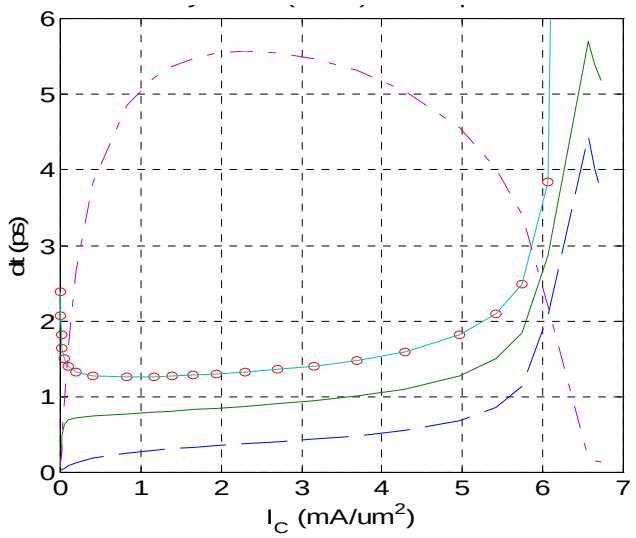

Fig. 2.9.1/1: NQS delay times τ_{IT} (solid green line) and τ_{Qf} (dashed blue line) vs. bias current for a 100GHz SiGe HBT. For reference, the accumulated transit time $\tau_{m\Sigma}$ (line with circles) from Regional Analysis as well as f_T (dash-dotted red line) have been inserted.

The additional time "delay", which results mostly in an excess phase in the frequency domain, is implemented in HICUM using a second order Bessel polynomial for ***both time and frequency domain analysis*** in order to maintain consistency of the respective results. The ideal delay proposed in [8] is only a crude approximation of the actual physics-based solution would and, in addition, cause implementation problems in a circuit simulator for time domain analysis. The use of a Bessel polynomial avoids those problems and leads to the same results in the frequency range of practical interest.

Up to version 2.1 NQS effects were implemented using Weil's approach [9]. However, Verilog-A based implementations used for subsequent releases does not allow access to the previous internal time steps of the simulator. The alternative of realizing the second-order differential equation is through an LCR or gyrator adjunct network. But unlike in other compact models, HICUM takes into account the bias dependence of the delay times. To avoid undesired derivatives generated that were shown by device simulation to be non-physical, the adjunct network is implemented with a normalization to the transit time [10, 1]. It was shown that this approach accurately matches the small-signal results obtained from the Bessel polynomial in the original formulation (v2.1 and earlier ones). In HICUM/L2 v2.24 and beyond the implementation of the input NQS effect has been further simplified to just a first-order RC adjunct network instead of a second-order LCR network. This simplification, which reduces one node was found to be adequate based on device simulations.

2.9.2 Lateral NQS effect

Dynamic emitter current crowding causes at high frequencies (or fast transients) a reduction of the impedance seen into the internal base node compared to d.c. or low-frequency conditions.

For the small-signal case, the distributed character of the internal base region can be modelled by shunting an adequate capacitance C_{rBi} in parallel to the d.c. resistance r_{Bi}. An analytical treatment of the small-signal input impedance of a stripe emitter transistor with $l_E/b_E>>1$ results for not too high frequencies in

$$\boxed{C_{rBi} = f_{CrBi} C_i} \tag{2.9.2-1}$$

with C_i as the total capacitance connected to the internal base node B',

$$\boxed{C_i = C_{jEi} + C_{jci} + C_{dE} + C_{dC}}\,. \tag{2.9.2-2}$$

From theory $f_\mathrm{CrBi} = 0.2$ for a long rectangular emitter stripe [10]. In general though, f_CrBi depends on the emitter geometry; for instance, it increases (slightly) for smaller emitter aspect ratios. Therefore and to provide maximum flexibility, f_CrBi is considered as a model parameter.

It turned out that the parallel capacitance C_rBi increases the computational effort significantly due to the large number of derivatives caused by C_i. With only a minor impact on accuracy, a computationally much more efficient solution has been achieved in v2.3 and beyond by simplifying the diffusion capacitances C_{dE} and C_{dC} from (2.9.2-2) to

$$\boxed{C_{dE} = \frac{i_{Tf}}{V_T}\tau_{f0} \quad \text{and} \quad C_{dC} = \frac{i_{Tr}}{V_T}\tau_r}. \tag{2.9.2-3}$$

Here, τ_{f0} was used for C_{dE} instead of τ_f in order to compensate the overestimation of g_m by i_{Tf}/V_T.

The derivation of (2.9.2-1) is based on the assumption of negligible emitter current crowding. Therefore, if this assumption is violated, (2.9.2-1) must not be used. Note, that for fast large-signal transient applications, where lateral NQS effects are most pronounced, strong transient current emitter crowding may occur. Furthermore, the theory leading to (2.9.2-1) is entirely based on a small-signal consideration and does not provide any clue regarding the charge stored on the capacitor. In fact, due to the bias dependence of C_rBi according to (2.9.2-2), there is no simple charge representation in time domain that would produce just the parallel capacitor across r_Bi without any additional derivatives (i.e. trans-capacitances).

As a consequence, it is strongly recommended ***not*** to use C_rBi for any type of *transient* analysis and to consider C_rBi only as a means for improving the model for *small-signal* circuit design. If for time-domain simulation the associated charge needs to be implemented, it is given by

$$Q_{rBi} = C_{rBi} V_{B^*B'} \tag{2.9.2-4}$$

and not by $Q_{rBi} = f_{CrBi}(Q_{jEi} + Q_{jCi} + Q_f + Q_r)$, which yields a completely different current. (Due to unavailability of "*ddx*" operator in v2.24, only the "Q_{rBi}" value, given by the above equation, can be calculated but not the C_{rBi} value.)

For a discussion on modeling the lateral NQS effect, refer e.g. to [71].

2.10 Breakdown

2.10.1 Collector-Base Breakdown

HICUM contains a breakdown model for the base-collector junction that is valid for a planar breakdown occurring in the internal transistor, i.e. below the emitter. The latter is a reasonable assumption because published measurements for production BJTs and HBTs show such a planar breakdown rather than a breakdown at the periphery of the external BC-junction. A compact model is mainly intended to indicate the onset of breakdown. In how far it is suited for a simulation and design of circuits within the breakdown regime depends partially also on the numerical robustness of the particular circuit simulator. The present model also includes current dependent breakdown, where the maximum electric field changes in magnitude and its location from the BC junction to the buried layer. On combination with other effects, such as self-heating, instabilities (such as snap-back) may occur that could cause convergence problems for most circuit simulators.

The model equation for the element I_{AVL} in Fig. 2.1.0/1 is based on the well-known relationship

$$i_{AVL} = I_{Tf} \int_0^{w_{BC}} a_n \exp(-b_n/|E|)\,\mathrm{dx} \tag{2.10.1-1}$$

The ionization rate a_{n} and the field b_{n} are coefficients describing the Avalanche process, E is the electric field within the junction region, x is the ordinate in vertical direction, and w_{BC} is the width of the BC depletion region. From this, the avalanche generation current can be approximated by

$$\boxed{i_{AVL} = i_{Tf}(M-1) = i_{Tf}\frac{g_{AVL}}{1-k_{AVL}g_{AVL}}} \tag{2.10.1-2}$$

with the avalanche multiplication factor M and

$$g_{AVL} = f_{AVL}(V_{DCi} - v_{B'C'}) \exp\left(-\frac{q_{AVL}}{C_{jCi}(V_{DCi} - v_{B'C'})}\right) \tag{2.10.1-3}$$

and the model parameters

$$f_{\mathrm{AVL}} = 2a_{\mathrm{n}}/b_{\mathrm{n}} \quad , \tag{2.10.1-4}$$

$$q_{AVL} = b_n \varepsilon A_E / 2 \,, \tag{2.10.1-5}$$

which depend on emitter area, physical data and temperature (via a_n and b_n). The term in the denominator of (2.10.1-2) allows the simulation of strong avalanche breakdown up to BV_{CBO}. Strong avalanche can be turned on by the parameter k_{AVL}, the physics-based value of which is one. However, due to the simplifications made in the derivation of the equation, the value may differ from one after a parameter extraction.

To avoid the possible discontinuity at $v_{B'C'}=V_{DCi}$, i_{AVL} is simply set to zero for $v_{B'C'} \geq V_{DCi}$. At large reverse bias $(V_{DCi}-v_{B'C'}) < -q_{AVL}/C_{jCi0}$, i_{AVL} is linearized to avoid too rapid current increases and the associated potential convergence problem.

Fig. 2.10.1/1 shows the ratio i_{AVL}/I_T, which is proportional to the multiplication factor, as function of the normalized BC voltage for different values of the exponent coefficient $q_{AVL}/(C_{jCi0}V_{DCi})$.

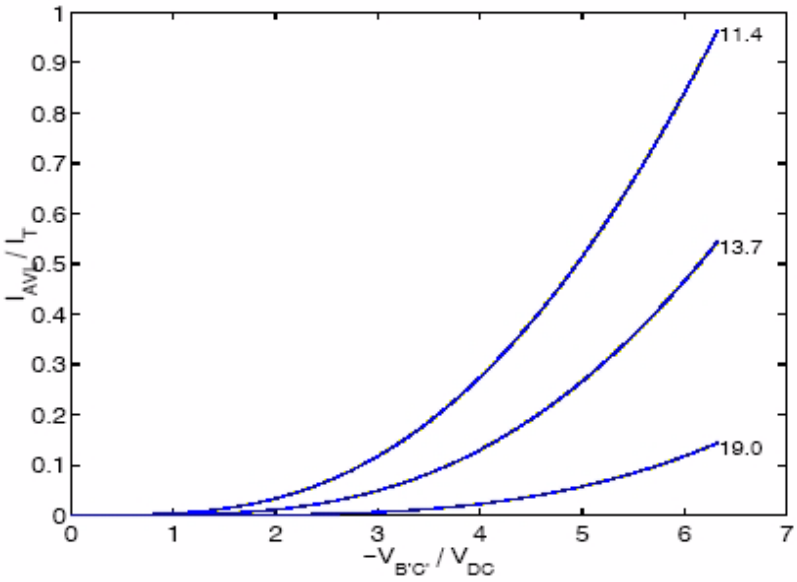

Fig. 2.10.1/1: Avalanche current i_{AVL}, normalized to I_T ($=I_{Tf}$), as a function of the normalized BC voltage for various values of the exponent coefficient $q_{AVL}/(C_{jCi0}V_{DCi})$ (see labels). Model parameters used: C_{jCi0}=0.56fF/µm^2, V_{DCi}=0.79V, z_{Ci}=0.307.

The electric field in the collector changes with current density. Thus, the ionization integral and the avalanche current via (2.10.1-3) also change with the transfer current. This effect can be taken into account by modifying (2.10.1-3) as follows [70]

$$g_{AVL} = f_{AVL}(V_{DCi} - v_{B'C'}) \exp\left(-\frac{q_{AVL}}{C_{jCi}(V_{DCi} - v_{B'C'})f_{avi}}\right), \tag{2.10.1-6}$$

where

$$f_{avi} = \sqrt{s_{mavl}\ln\left(\exp\left(\frac{c_{mavl}C_{jCi}}{s_{mavl}C_{jCi0}}\right) - 2 + 2\cosh\left(\frac{1 - I_{Tf}/I_{lim,\,avl}}{s_{mavl}}\right)\right)} \tag{2.10.1-7}$$

is a function that smoothly models the change of the electric field distribution in the collector with current from low to very high current densities. The smoothing parameters s_{Mavl} (= 0.1) and c_{Mavl} (= 1) are fixed and not available as model parameters. The variable

$$I_{lim,\,avl} = h_{CAVL}I_{lim} + h_{VDAVL}I_{Tf} \tag{2.10.1-8}$$

with $I_{\mathrm{lim}} = V_{\mathrm{lim}}/r_{\mathrm{Ci0}}$ models the changing condition of a horizontal field distribution in a spatially variable collector doping with the model parameters h_{CAVL} and h_{VDAVL}. For a spatially constant (epi) collector doping profile, the horizontal electric field distribution occurs at I_{lim} so that the model parameter h_{CAVL} is expected to be one in that case. Setting $h_{\mathrm{CAVL}} = 0$ turns of the current dependent formulation and sets $f_{\mathrm{avi}} = 1$.

2.10.2 Emitter-base junction breakdown

In advanced bipolar transistors the EB breakdown voltage is usually around 1...3V due to the high doping concentrations. As a result, the breakdown effect in advanced (high-speed) transistors corresponds to a tunnelling mechanism.

The model equation employed in HICUM is based on the expression for the tunnelling current density [13]

$$J_{BEt} = \frac{\sqrt{2m^*/E_G}\, q^3(-V)}{h^2} E_{BEj} \exp\left[-\frac{8\pi\sqrt{2m^*E_G}E_G}{3qhE_{BEj}}\right] \quad . \tag{2.10.2-1}$$

Here E_G is the bandgap energy, m^* is the effective electron mass, h is the Planck constant, and V is the voltage across the respective BE junction; i.e. $V=V_{B',E'}$ for the bottom junction or $V=V_{B^*E'}$ for the perimeter junction. E_{BEj} is the electric field at the junction which - according to the theory of abrupt junctions - can be expressed as

$$E_{BEj} = 2\frac{V_{DE}-V}{w_{BE}} \tag{2.10.2-2}$$

with V_{DE} as the built-in voltage of the respective junction. w_{BE} is the space charge region width of that junction and is given by

$$w_{BE} = w_{BE0}(1-V/V_{DE})^{z_E} \tag{2.10.2-3}$$

with the zero-bias value

$$w_{BE0} = \begin{cases} \varepsilon_{Si}A_{E0}/C_{jEi0} & \text{, bottom junction} \\ \varepsilon_{Si}P_{E0}\left(0.8\frac{\pi}{2}x_{je}\right)/C_{jEp0} & \text{, perimeter junction} \end{cases} \tag{2.10.2-4}$$

P_{E0} and A_{E0} are the emitter window perimeter and area, respectively, and x_{je} is the vertical junction depth. C_{jEi0} and C_{jEp0} are the zero-bias depletion capacitance of the bottom and perimeter junction, respectively. The factor $0.8(\pi/2)x_{je}$ approximates the perimeter junction curvature caused by lateral

out diffusion of the emitter doping. Inserting (2.10.2-2 to 2.10.2-4) back into (2.10.2-1), defining a normalized voltage $V_e=V/V_{DE}$, and multiplying with the respective area yields for the tunnelling current

$$i_{BEt} = I_{BEtS}(-V_e)(1-V_e)^{1-z_E}\exp[-a_{BEt}(1-V_e)^{z_E-1}] \quad . \tag{2.10.2-5}$$

For numerical reasons, the $1-V_e$ terms are converted to terms that contain the respective normalized bias dependent depletion capacitance $C_e=C_{jE}(v)/C_{jE0}$, which has been made numerically stable at $V_e=1$. Using the classical $C_{jE}(v)$ relationship which is valid at the reverse bias of interest,

$$(1-V_e)^{1-z_E} = C_e^{1-1/z_E} \quad , \tag{2.10.2-6}$$

leads to the final formulation

$$\boxed{i_{BEt} = I_{BEtS}(-V_e)C_e^{1-1/z_E}\exp[-a_{BEt}C_e^{1/z_E-1}]} \quad . \tag{2.10.2-7}$$

The "saturation" current

$$I_{BEtS} = 2\frac{\sqrt{2m^*/E_G}\,q^3V_{DE}^2}{h^2\varepsilon_{Si}}C_{jE0} \tag{2.10.2-8}$$

and the coefficient

$$a_{BEt} = \frac{8\pi\sqrt{2m^*E_G}E_G}{3qh}\,\frac{w_{BE0}}{2V_{DE}} \tag{2.10.2-9}$$

are model parameters, that depend on physical and process data as well as on geometry. Note that i_{BEt} is a continuously differentiable expression since the depletion capacitance is continuously differentiable. The above equation is based on a description of band-to-band tunneling, which dominates at reverse bias and becomes less accurate for a forward biased junction, i.e. if trap-assisted tunneling dominates.

In most processes, the breakdown effect occurs first at the peripheral emitter junction, because the doping concentrations are highest there, and due to the curvature of that junction which leads

to a narrower space-charge region and, thus, to a higher electric field. In this case, C_{jE0}, V_{DE}, z_E, and V_e in the above equations have to be replaced by C_{jEp0}, V_{DEp}, z_{Ep} and $v_{B*E'}/V_{DEp}$. However, in most SiGe (and also III-V) processes, the tunnelling occurs at the internal (bottom) BE junction. In this case, C_{jEi0}, V_{DEi}, z_{Ei} and $v_{B'E'}/V_{DEi}$, respectively, need to be inserted instead. Also, the tunnelling current source in the HICUM equivalent circuit needs to be connected to either the perimeter or internal base node as shown in Fig. 2.10.2/1. Thus, in order to provide a flexible description and to also allow proper geometry scaling, the parameter *TUNODE* has been introduced that defines the (base) node at which the tunneling current source is supposed to be connected. Note, that the current source has to be connected either to the internal base node (*TUNODE* = 0) or to the perimeter base node (*TUNODE* = 1), but not to both.

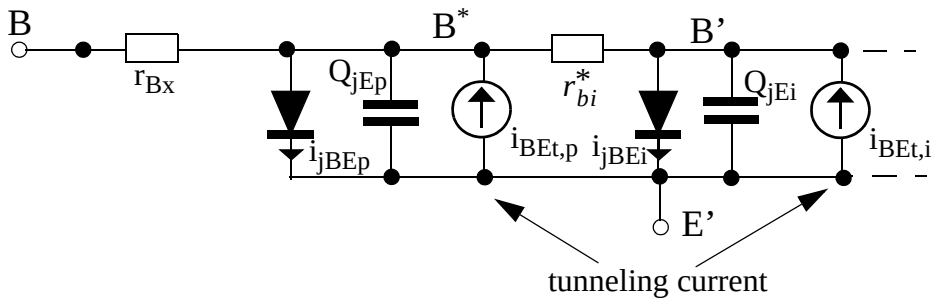

Fig. 2.10.2/1:Possible locations of the BE tunnelling current source: $i_{BEt,p}$ or $i_{BEt,i}$.

2.11 Substrate network

The substrate contact of a transistor may be at the bottom of the wafer only or, more preferably, at the surface. But even the surface contact is usually located relatively far away from the CS junction, so that a significant resistance r_{Su} may exist in series to the CS depletion capacitance, due to the usually quite high substrate resistivity ρ_{Su}. In addition, the high permittivity of silicon, ε_{Si}, leads to a capacitance C_{Su} in parallel to r_{Su} that becomes important at high operating speed. Physically, the connection between the substrate contact and the CS depletion capacitance can be partitioned into a bulk (or bottom) and a periphery *RC* network (cf. Fig. 2.11.0/2), each of which having the time constant $\tau_{Si}=\rho_{Su}\varepsilon_{Si}$. In HICUM, starting from v2.34 on, this applies only to the bottom capacitance C_{jS}, but not to the perimeter component C_{SCp} (cf. Fig. 2.1.0/1). An additional time-constant for the latter can be obtained though by adding a series resistor (and parallel capacitor) to the substrate terminal of the transistor in a subcircuit. Note that the values of r_{Su} and C_{Su} are strongly geometry dependent.

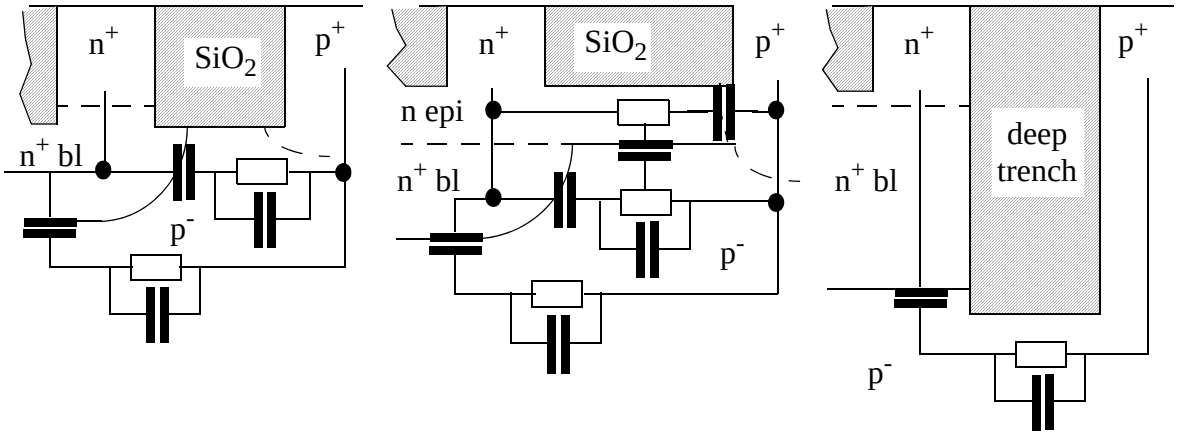

Fig. 2.11.0/2: Process variants of the CS junction, including components for modelling the depletion capacitance and intra-device substrate coupling [1].

Fig. 2.11.0/3 shows that the impact of substrate coupling on the frequency dependent output conductance is already visible in a 25GHz process.

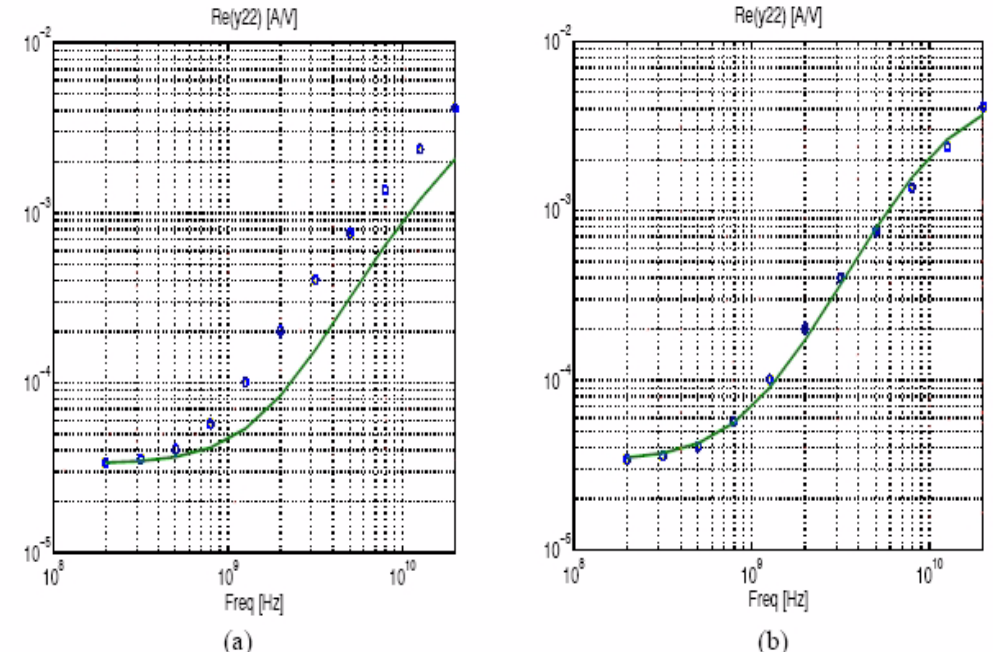

Fig. 2.11.0/3: Impact of intra-device substrate-coupling on transistor output conductance (real part of y_{22}) as function of frequency. Comparison of measurements (symbols) and HICUM (lines): (a) model without substrate network r_{su}, C_{su}; (b) model with substrate network. Emitter size: 0.4*14µm^2; bias point: I_C/A_E=0.22 mA/µm^2, V_{CE}=0.8V.

The substrate network displayed in Fig. 2.11.0/3 are most likely not sufficient for accurately modelling the frequency dependence of the output conductance in actual circuit applications. There, the highly doped substrate ring with its contact close to the collector is often discarded to save chip space. Hence, any parameters for the substrate networks obtained during parameter extraction are unusable and need to be re-extracted based on the actual circuit layout, i.e. the actual location of the substrate contact on the chip. Therefore, providing a complete substrate (coupling) network within a compact model does not make sense since it is the task of a parasitic extractor to determine such a network and attach it to the transistor substrate node!

2.12 Parasitic substrate transistor

Under certain electrical circumstances, the parasitic substrate transistor can be turned on, depending also upon the processes and layout of the transistor. First of all, one can distinguish between a bulk substrate transistor given by the buried layer area and - dependent on the process - a peripheral substrate transistor. The most likely electrical condition for turning on the substrate transistor is a forward-biased BC junction which occurs either at high current densities under the emitter (internal BC junction) or if the transistor is operated in hard saturation (external and internal BC junction). An example for this are power amplifiers, in which the transistor is operated in hard saturation with $V_{CE} \rightarrow V_{CEs}$ and strongly forward biased V_{BC}. Another condition for turning on the substrate transistor is a forward biased CS junction caused by voltage drops in the substrate (latch-up).

Since the bulk substrate transistor usually has a current gain of less than 1 due to the highly doped and wide buried layer, its influence is negligible and needs not to be considered at high collector current densities. Device simulations confirmed this for an advanced bipolar process. A peripheral substrate transistor action can be avoided by a surrounding collector sinker with high enough doping concentration at the buried layer depth. Also, this peripheral transistor does not exist at all in trench-isolated processes.

In (npn) transistors without surrounding collector sinker, however, the epitaxial collector acts as a lightly doped base between the external base (now the emitter) and the substrate (now the collector), resulting in a pnp transistor with considerable current gain that may be required to be modelled in addition to the vertical npn transistor. HICUM contains a simplified substrate transistor model in order to take the corresponding effects into account.

The parasitic substrate transistor consists of the elements i_{Ts}, i_{SC}, C_{jS}, i_{BCx} and C_{BCx} in the equivalent circuit of Fig. 2.1.0/1. While C_{jS}, i_{BCx} and C_{BCx} already belong to the standard HICUM equivalent circuit, a substrate *transistor* action requires the addition of a substrate transfer current source. Since substrate transistor action is considered as second order effect, a simplified model has been chosen for i_{Ts}:

$$\boxed{i_{TS} = I_{TSf} - I_{TSr} = I_{TSS}\left[\exp\left(\frac{v_{B*C'}}{m_{Sf}V_T}\right) - \exp\left(\frac{v_{S'C'}}{m_{Sr}V_T}\right)\right]} \qquad (2.12.0\text{-}10)$$

with the saturation current I_{TSS} and the emission coefficients m_{Sf} and m_{Sr} as model parameters. The second term is only relevant if the SC junction becomes forward biased which of little practical importance; therefore, to reduce the number of model parameters, $m_{Sr} = m_{Sf}$ is assumed.

In case of a forward biased SC junction, also a "base" current component exists, that is modelled by the diode equation:

$$\boxed{i_{jSC} = I_{SCS}\left[\exp\left(\frac{v_{S'C'}}{m_{SC}V_T}\right) - 1\right]} \qquad (2.12.0\text{-}11)$$

with the saturation current I_{SCS} and the emission coefficient m_{SC} as model parameters. Although this current (and its derivative) are usually of little practical relevance it is generally useful for simulator convergence.

The minority charge storage in the epitaxial region under the external base is taken into account by a diffusion charge

$$\boxed{Q_{dS} = \tau_{Sf}\, i_{TSf}} \qquad (2.12.0\text{-}12)$$

with the forward transit time τ_{Sf} as a model parameter of the substrate transistor. τ_{Sf} depends on the average current path (neutral base width) under the external base and at the buried layer periphery. So far, the classical base transit time expression turned out to be a good approximation for estimating the value of τ_{Sf}. Also, device simulations have shown that for high-speed processes the stored charge represented by Q_{dS} has only negligible effect on transistor switching out of hard saturation.

Note, that in advanced bipolar processes the emitter terminal of the substrate transistor (B*) moves towards the (npn) base contact (B), which makes the external realization of such a parasitic transistor by a subcircuit even easier.

2.13 Noise model

The noise behaviour is modelled by employing the small-signal equivalent circuit and adding to all series resistances, diodes, and to the transfer current source their corresponding equivalent noise current sources. Compared to the SGPM, the more sophisticated equivalent circuit and more accurate model equations of HICUM/L2 allow a more accurate overall description of the noise behaviour, especially at high frequencies. Fig 2.13.0/4(a) shows the different noise sources in HICUM. The red arrow indicates the correlation between base and collector shot noise sources, which is modeled by the adjunct network in Fig 2.13.0/4(b). The various noise sources and the correlation are described in more detail below.

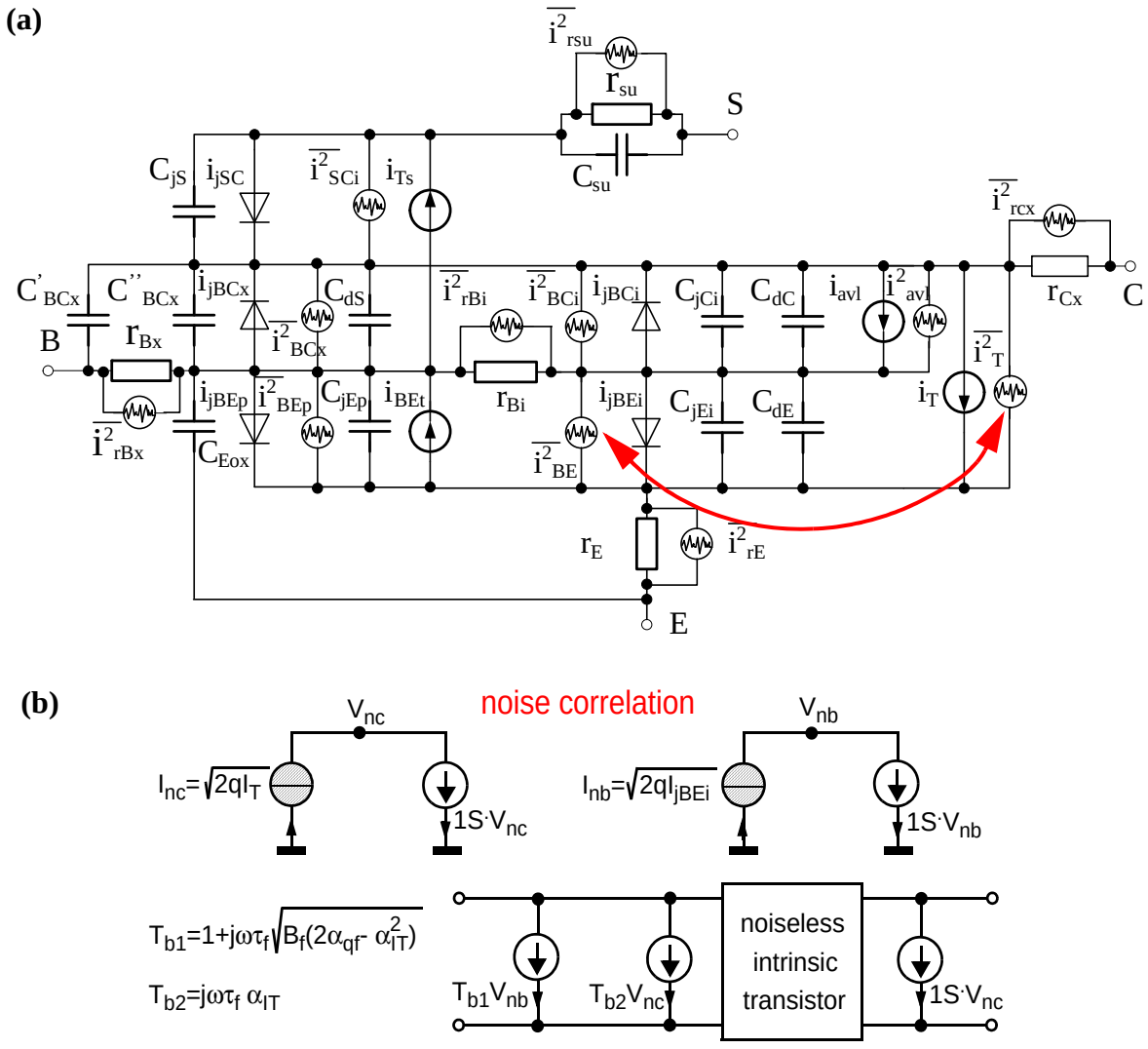

Fig. 2.13.0/4:Equivalent circuit of HICUM/L2 showing the noise sources.

2.13.1 Thermal and shot noise

In ohmic resistances thermal noise is taken into account by an equivalent noise current source with the noise spectral density

$$\boxed{\overline{I_r^2} = \frac{4k_B T \Delta f}{r}} \tag{2.13.1-1}$$

where $r = r_E$, r_{Cx}, r_{Bx}, or r_{Bi}, k_B is the Boltzmann constant, T is the device temperature, and Δf is the frequency interval. Investigations have shown that for certain processes a distributed model of the internal base yields an improved description of the high-frequency noise behaviour, which can only be achieved with a multi-transistor model.

Shot noise is assumed for transfer current with the noise spectral density

$$\boxed{\overline{I_T^2} = 2qI_T \, \Delta f}, \tag{2.13.1-2}$$

as well as for the avalanche current I_{AVL} and for currents across junctions (diode currents),

$$\boxed{\overline{I_{j\,diode}^2} = 2qI_{jdiode} \, \Delta f} \ , \tag{2.13.1-3}$$

with the index *diode* = {*BEi*, *BCi*, *BEp*, *BCx*, *SC*}. Note that eq. (2.13.1-3) is only a rough approximation.

2.13.2 Flicker noise

Investigations of flicker noise in polysilicon-emitter bipolar transistors seem to indicate that the flicker noise is generated by traps at the polysilicon to monosilicon interface. This corresponds to a strong correlation between the bottom and perimeter component, which is simply modelled as

$$\boxed{\overline{I_{BE}^2} = k_F \, (I_{jBEi} + I_{jBEp})^{a_F} \, \frac{\Delta f}{f}} \ . \tag{2.13.2-1}$$

For flexibility and backward compatibility, a flag has been introduced to allocate the correlated flicker noise to either the internal base node (*CFBE* = -1) or the perimeter base node (*CFBE* = -2). The default value is -1 for compatibility down to version 2.1. The value range [0,1] is reserved for a correlation factor in a possible future implementation.

From v2.31 on, the flicker noise of the emitter resistance has been included:

$$\boxed{\overline{I_{rE}^2} = k_{FrE}\left(\frac{v_{E'E}}{R_E}\right)^{a_{FrE}}\frac{\Delta f}{f} + \frac{4kT}{R_E}} \qquad (2.13.2\text{-}2)$$

2.13.3 Correlation between base and collector noise

For advanced HBTs, correlation between the shot noise of the back-injection current component of the base current and the transfer current becomes important at frequencies below peak f_T and can lead to, e.g., a significant reduction of the minimum noise figure. According to [1], the complex valued base current noise spectral density correlated with the transfer current noise given by

$$\underline{S}_{i_{nb}i_{nc}} = 2qj\omega\alpha_{iT}\tau_{Bf}I_T \qquad (2.13.3\text{-}1)$$

where τ_{Bf} is base transit time. The collector current shot noise spectral density is given by

$$S_{i_{nc}} = 2qI_T \ . \qquad (2.13.3\text{-}2)$$

Finally, the base current related noise spectral density reads

$$S_{i_{nb}} = 2qI_{jBEi}[1 + 2\alpha_{qf}B_f(\omega\tau_{Bf})^2] \qquad (2.13.3\text{-}3)$$

The above model and implementation was shown to be valid up to at least 500 GHz [31] as shown in Fig. 2.13.3/1.

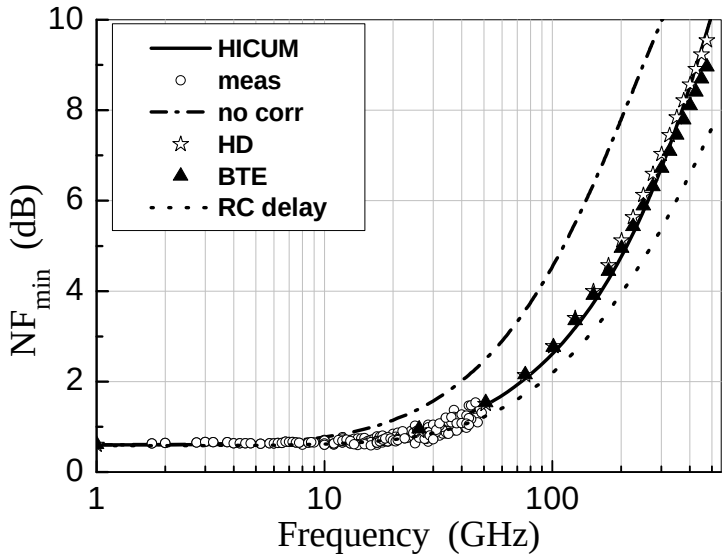

Fig. 2.13.3/1: Visualization of the effect of noise correlation on $NF_{\min}$ on measurements and device simulation results. The deviation between correlated and uncorrelated noise figure value increases with frequency [31].

The implementation of the noise correlation in typical simulator engines that can handle only uncorrelated noise sources is described in detail in [31]. The noise correlation model is enabled by the parameter *flcono*. The implementation of correlated noise (cf. Fig 2.13.0/4(b)) further requires

$$\alpha_{qf} > \alpha_{iT}^2 / 2$$

2.14 Temperature dependence

Temperature dependence is described in HICUM via those model parameters that are related to physical quantities like intrinsic carrier density or mobility. In the following formulas, T_0 is the reference temperature (e.g. 300K) for which the model parameters have been determined. The validity range of the equations depends somewhat on the technology considered.

In most circuit simulators a linear dependence of bandgap with temperature is assumed for the saturation currents, which are most sensitive to temperature changes, while for the built-in voltages often a more complicated function $V_g(T)$ is used (e.g. [13]), which is valid down to quite low temperatures. This was also the case for HICUM up to version 2.1. From version 2.2 on a nonlinear temperature dependence of the bandgap voltage has been employed for various reasons (see later). Note though, that specific low-temperature effects such as freeze-out are not taken into account, and it is presently not recommended to use the industry standard model version below about 250K unless its parameters have been extracted or at least verified specifically for that temperature range.

For numerical reasons (over- or underflow), some of the theoretical equations have to be modified, mostly towards extreme temperatures. The respective smoothing functions to be used for circuit simulator implementation are given below. It is assumed though that every circuit simulator prevents negative or zero temperature. Furthermore, relative temperature coefficients (TCs) are designated by the symbol α and temperature factors (without unit) are designated by ζ.

2.14.1 Temperature dependent bandgap voltage

In order to allow simulations of devices fabricated in different materials and to make the model simulator-independent, a temperature dependent bandgap voltage has been added to the model equations. The formulation suggested in [65] has been selected,

$$V_g(T) = V_g(0) + K_1 T \ln(T) + K_2 T \qquad (2.14.1\text{-}1)$$

due to the following advantages:

- a higher accuracy w.r.t. measured data in the relevant temperature range compared to the classical formulation, and
- compatibility with existing temperature dependent current formulations in compact models that are based on the assumption of a simple linear temperature dependence $V_g(T) = V_{g,\,cl}(0) - a_g T$, but higher accuracy at the same time.

Note, that in (2.14.1-1) the temperature T decreases faster towards zero than $ln(T)$ increases towards infinity, so that the equation assumes the finite value $V_g(0)$ at $T = 0$. The original coefficient values are given in Table 2.14.1/1; the second row contains an improved set of parameters which is more accurate both at low temperatures and with respect to the classical formulation:

$$V_g(T) = V_{g,cq}(0) - \frac{\alpha_g T^2}{T + T_g} \tag{2.14.1-2}$$

Tab. 2.14.1-1:

Parameter	K_1 [V/K]	K_2 [V/K]	$V_g(0)$ [V]
[65]	$-8.459\ 10^{-5}$	$3.042\ 10^{-4}$	1.1774
[66]	$-1.02377\ 10^{-4}$	$4.3215\ 10^{-4}$	1.170

Table 2.14.1/1Coefficients for calculating the bandgap voltage in *silicon* as a function of temperature from (2.14.1-1). In the range from 250 to 400K, a smaller error can be obtained by simply setting $V_g(0)$=1.1777V in the original parameter set.

For compact model and application purposes, it is sometimes more convenient to re-write above equation in terms of a reference temperature T_0 (e.g. for parameter extraction), which gives

$$V_g(T) = V_g(T_0) + k_1 \frac{T}{T_0} \ln\left(\frac{T}{T_0}\right) + k_2\left(\frac{T}{T_0} - 1\right) \tag{2.14.1-3}$$

with the definitions

$$k_1 = K_1 T_0 \qquad k_2 = K_2 T_0 + k_1 \ln(T_0) \tag{2.14.1-4}$$

and the bandgap voltage at the measurement reference temperature,

$$V_g(T_0) = k_2 + V_g(0) \tag{2.14.1-5}$$

Fig. 2.14.1/2 shows the temperature dependent bandgap voltage according to (2.14.1-1) compared to the most popular conventional formulations.

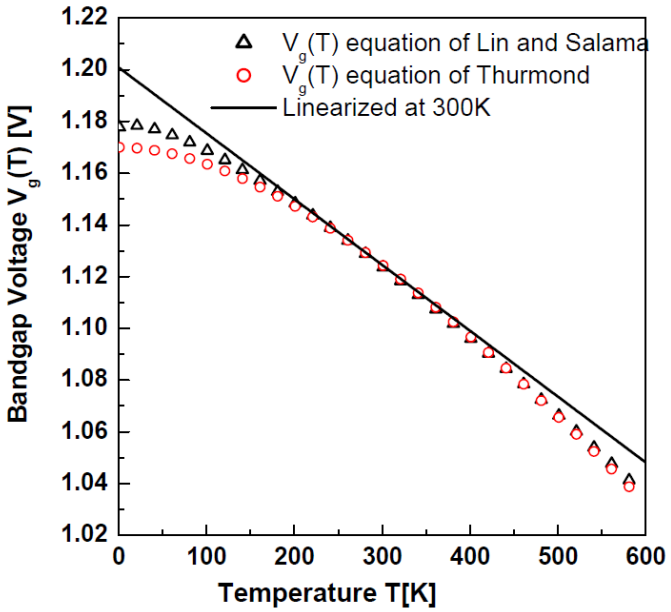

Fig. 2.14.1/2:Comparison of bandgap voltage approximations. The parameters used for (2.1.14-2) are $V_g(0)$ = 1.170 V, α_g = 4.73 10^{-4} V/K, T_g = 636 K. The parameters for the (at T_0) linearized equation are $V_g(0)$ = 1.2009 V, α_g = 2.5461 10^{-4} V/K.

The choice of the bandgap description also influences the formulation of the effective intrinsic carrier density, which now reads

$$n_{ie}^2(T) = n_{ie}^2(T_0)\left(\frac{T}{T_0}\right)^{m_g}\exp\left[\frac{V_{geff}(0)}{V_T}\left(\frac{T}{T_0}-1\right)\right] \tag{2.14.1-6}$$

with the effective bandgap voltage V_{geff} that includes the impact of material composition and bandgap narrowing, the constant

$$m_g = 3-\frac{k_1}{V_{T0}} = 3-\frac{qK_1}{k_B} \tag{2.14.1-7}$$

and the parameter K_1 from the bandgap voltage equation (2.14.1-1). Using the values in Table 2.14.1/1 for Si gives m_g = 4.188.

2.14.2 Transfer current

The transfer current is strongly temperature dependent via the intrinsic carrier density n_i. Up to v2.1, in the temperature dependent expression of the model parameter c_{10} (and the associated saturation current) so far a constant value 3 has been used in the n_i prefactor $(T/T_0)^3$. Since the value 3 is an approximation, assuming a cancellation of the temperature dependence of the diffusivity (in a sufficiently highly doped base region), a more flexible representation is to replace 3 by the parameter ζ_{CT},

$$c_{10}(T) = c_{10}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{CT}} \exp\left[\frac{V_{gBeff}(0)}{V_T(T)}\left(\frac{T}{T_0}-1\right)\right]. \qquad (2.14.2\text{-}1)$$

Here, $V_{gBeff}(0)$ is the towards $T = 0$ extrapolated effective bandgap voltage in the base region and

$$\zeta_{CT} = m_g + 1 - \zeta_{\mu mB}, \qquad (2.14.2\text{-}2)$$

given by its physics-based value, where ζ_{mmB} is the exponent factor of the mobility temperature dependence for the minority carriers in the base region. The default value is $\zeta_{CT} = 3$. The above model parameter c_{10} is shown in Fig. 2.14.2/1 as a function of temperature for various values of ζ_{CT}. Obviously, the impact of ζ_{CT} is quite small, although the selected values already cover more than the physically meaningful range. Note that V_{Gb} can assume values smaller than in Fig. 2.14.1/2 due to high doping effects in the base region.

The above description with ζ_{CT} as parameter provides a higher flexibility in modeling the temperature dependence of the transfer current characteristic for designing bandgap-reference circuits; a more detailed study [1] has shown though, that only very large and non-physical values of ζ_{CT} do have an impact on the temperature dependent output voltage of bandgap reference circuits (in circuit simulation only, of course), and that such non-physical values of ζ_{CT} were usually accompanied with non-physical values for the bandgap voltage itself as well.

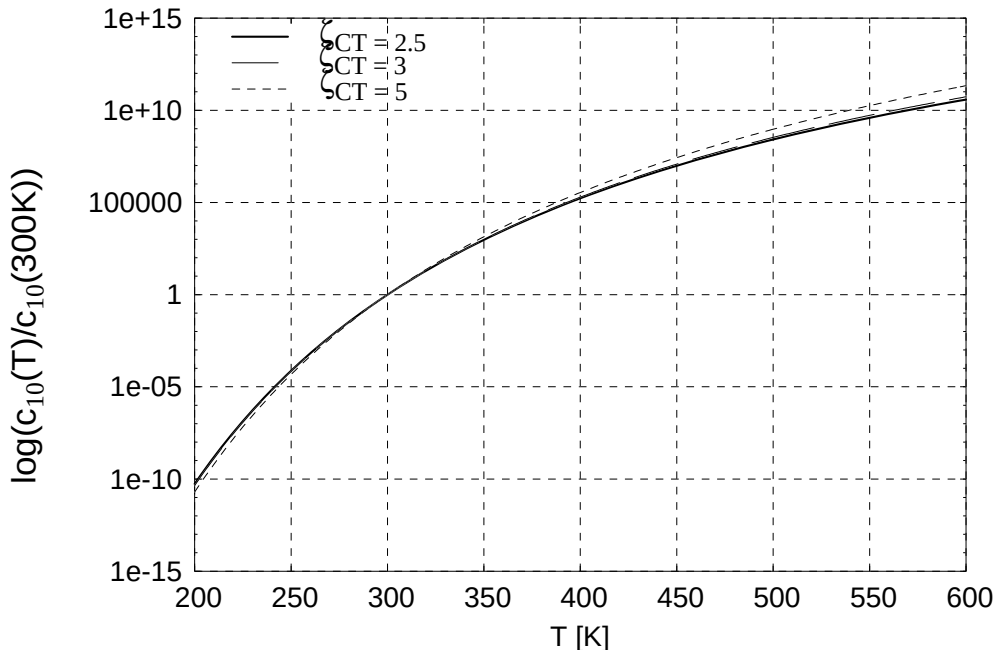

Fig. 2.14.2/1: Normalized ICCR constant vs normalized temperature with a_{CT} as parameter and fixed value of V_{gBeff} = 1.17V.

2.14.3 Zero-bias hole charge

Fig. 2.14.3/1 shows an example for the temperature dependence of Q_{p0}, obtained directly from 1D device simulation. The zero-bias hole charge Q_{p0} is only weakly temperature dependent via the influence of base width change with temperature that is mainly caused by the change in depletion width of the BE junction. The temperature dependence can be approximated by the simple expression

$$Q_{p0}(T) \;=\; Q_{p0}(T_0)\left[2-\left(\frac{V_{DEi}(T)}{V_{DEi}(T_0)}\right)^{z_{Ei}}\right] \qquad (2.14.3\text{-}1)$$

which requires no additional model parameters. As Fig. 2.14.3/1 shows, above equation (2.14.3-1) yields excellent agreement over a large temperature range. Also, for typical values of V_{DEi} in the order of V_{Gb} the value of Q_{p0} will remain positive up to extremely high temperatures. Therefore, a smoothing function is omitted here to keep the computational effort minimal, particularly during

self-heating calculations. The temperature derivative in the code is directly given by the already available derivative dV_{DEi}/dT.

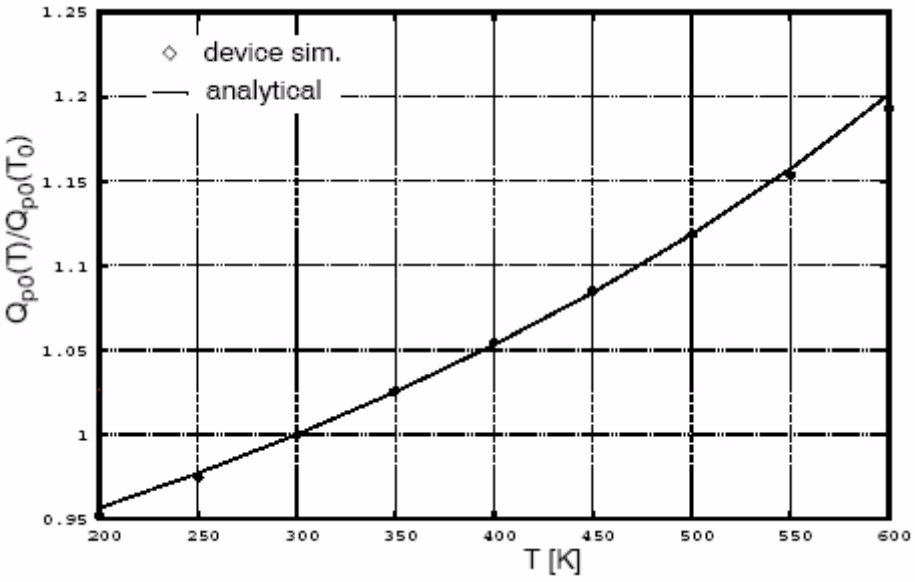

Fig. 2.14.3/1: Temperature dependence of Q_{p0} from 1D device simulation (symbols) compared to (2.14.3-1) (solid line) using existing model parameters to calculate the temperature dependence of the built-in voltage. The required internal BE depletion capacitance parameters V_{DEi} and z_{Ei} were obtained from a simple C-V fit.

2.14.4 Weight factors

Since in HICUM, the charge weight factors are normalized to that of the neutral base in equilibrium, the temperature dependence of all weight factors is mainly caused by the bandgap difference of the respective region and the neutral base. Therefore, the temperature dependence of h_{f0}, h_{fE} and h_{fC} is implemented with

$$h(T) = h(T_0)\exp\left[\frac{\Delta V_g}{V_T}\left(\frac{T}{T_0}-1\right)\right]. \qquad (2.14.4\text{-}1)$$

The parameters used to calculate the bandgap difference for each weight factor are summarized in Tab. 2.14.4/1. Here, v_{gB}, v_{gC}, v_{gE} and Δv_{gBE} are model parameters. Δv_{gBE} is used for h_{f0}, since the main portion of the minority charge at low injection is located within the BE SCR.

weight factor	Δv_g
h_{f0}	ΔV_{gBE}
h_{fE}	V_{gB}-V_{gE}
h_{fC}	V_{gB}-V_{gC}

Table 2.14.4/1 Bandgap voltages describing the temperature dependences of the minority charge weight factors.

Since the weight factors h_{jEi} and h_{f0} are associated with the BE SCR, Δv_{gBE} is also used in their description. Note that in contrast to [32] ΔV_{gBE} (<0 for SiGe HBTs) and not $-\Delta V_{gBE}$ is inserted to reflect the physical origin of the parameter. A dedicated parameter is used instead of V_{gB}-V_{gE} since this difference can significantly deviate from the actual ΔV_{gBE} due to bandgap narrowing in the emitter. However, in order to provide more flexibility during parameter extraction an additional parameter ζ_{vgBE} is included, leading to

$$h_{jEi0}(T) = h_{jEi0}(T_0)\exp\left[\frac{\Delta V_{gBE}}{V_T}\left(\left(\frac{T}{T_0}\right)^{\zeta_{V_{gBE}}} - 1\right)\right], \qquad (2.14.4\text{-}2)$$

Although a temperature dependence of a_{hjEi} can be derived from (2.2.0-12) and the known temperature dependences of C_{jEi} and V_T a more flexible equation is implemented with

$$a_{hjEi}(T) = a_{hjEi}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{h_{jEi}}} \qquad (2.14.4\text{-}3)$$

and the model parameter ζ_{hjEi}.

2.14.5 Base (junction) current components

Since in HICUM not the current gain but the physically independent base current is described, the respective saturation currents are modelled as a function of temperature. The saturation current of the internal base-emitter diode is given by

$$I_{BEiS}(T) = I_{BEiS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{BET}} \exp\left[\frac{V_{gEeff}(0)}{V_T}\left(\frac{T}{T_0}-1\right)\right] \tag{2.14.5-1}$$

with the new model parameters ζ_{BET} and the effective bandgap voltage $V_{gEeff}(0)$ in the emitter, which includes, e.g., high-doping effects. An estimate for $V_{gEeff}(0)$ can be calculated from the known effective bandgap voltage in the base and the measured relative TC α_{Bf} of the current gain:

$$V_{gEeff}(0) = V_{gBeff}(0) - \alpha_{Bf} T_0 \; V_{T0} \tag{2.14.5-2}$$

This estimate can be used as default or preliminary value, e.g., when converting the HICUM v2.1 parameter α_{Bf} to $V_{gEeff}(0)$. In HICUM v2.2, α_{Bf} will be phased out as a model parameter in favour of the separate model parameters ζ_{BET} and $V_{gEeff}(0)$ in an equation form that is the same for all junction components (see below). Although defining the temperature dependence of the current gain at given collector bias current is more useful for circuit design than defining a bandgap voltage from a $V_{B'E'} = 0$ extrapolated characteristic, the latter approach has been used in HICUM from version 2.2 on in order to

- provide a more flexible description of the current gain temperature dependence,
- be consistent with the independent modeling of the bias dependence of the base current components, and
- provide a clear definition of how to extract the corresponding model parameters.

As a consequence, HICUM employs for all junction related current components, except the transfer current, equations of the form

$$I_j = I_{jS} \exp\left(\frac{V}{m V_T}\right) \tag{2.14.5-3}$$

with the generic temperature dependent saturation current formulation

$$I_{jS}(T) = I_{jS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_T} \exp\left[\frac{V_{geff}(0)}{V_T}\left(\frac{T}{T_0}-1\right)\right] \tag{2.14.5-4}$$

The corresponding variables that are inserted into above equation for each junction component are listed in Table 2.14.5/1. For the BE recombination components, the average value

$$V_{gBEeff} = \frac{V_{gBeff} + V_{gEeff}}{2} \tag{2.14.5-5}$$

that is already being used for the BE depletion capacitance components, is inserted. The temperature dependence of base-emitter recombination current components is given by n_i (rather than n_i^2 as for the injection components), the SCR width and an effective lifetime τ_{eq}. The temperature dependence of τ_{eq} and of the SCR width are very small compared to the *T*-dependence of n_i and also partially compensate each other. Thus, the *T*-dependent recombination saturation currents read:

$$I_{jRS}(T) = I_{jRS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_T/m_{jR}} \exp\left[\frac{V_{geff}(0)}{m_{jR}V_T}\left(\frac{T}{T_0}-1\right)\right] \tag{2.14.5-6}$$

In model versions older than v2.3, m_{jR} is always set to 2, while from version 2.3 on it has become a variable (i.e. a model parameter).

component I	V	I_S	m	V_{geff}	ζ_T	m_{jR}
I_{jBEi}	$V_{B'E'}$	I_{BEiS}	m_{BEi}	V_{gEeff}	ζ_{BET}	n/a
I_{jBEp}	$V_{B*E'}$	I_{BEpS}	m_{BEp}	V_{gEeff}	ζ_{BET}	n/a
I_{jBCi}	$V_{B'C'}$	I_{BCiS}	m_{BCi}	V_{gCeff}	ζ_{BCiT}	n/a
I_{jBCx}	$V_{B*C'}$	I_{BCxS}	m_{BCx}	V_{gCeff}	ζ_{BCxT}	n/a
I_{jSC}	$V_{S'C'}$	I_{SCS}	m_{SC}	V_{gSeff}	ζ_{SCT}	n/a
I_{jREi}	$V_{B'E'}$	I_{REiS}	m_{REi}	V_{gBEeff}	$\mu\gamma$	m_{REi}
I_{jREp}	$V_{B*E'}$	I_{REpS}	m_{REp}	V_{gBEeff}	$\mu\gamma$	m_{REp}

Table 2.14.5/1 Junction current components and their corresponding parameters and controlling voltages

Commercially implemented SGP models contain the components I_{jBEi}, I_{jBCi} (or I_{jBCx}) and I_{jSC}. In some variants, each of these components is assigned a different set (V_{geff}, ζ_T) of parameters. Extending this to the additional components in HICUM would increase the number of parameters

without significantly increasing accuracy and flexibility, or in other words: it is questionable from a practical application point of view for a compact model whether introducing separate model parameters for those base current components, that are of *little importance* for *circuit design* makes sense. Therefore, to keep the model as simple as possible (in terms of parameter determination), currents associated with same regions have been assigned the same parameters in Table 2.14.5/1. Furthermore, since the mobility exponent factor ζ_{Ci} of the internal collector region, defined by

$$\mu_{Ci}(T) = \mu_{Ci}(T_0)\left(\frac{T}{T_0}\right)^{-\zeta_{Ci}} \tag{2.14.5-7}$$

is already available as a model parameter, the respective exponent factor for I_{jBCi} can be expressed as

$$\zeta_{BCiT} = m_g + 1 - \zeta_{Ci} \tag{2.14.5-8}$$

with m_g from (2.1.14-7). Hence, ζ_{BCiT} does not need to be added as model parameter and is calculated internally. Similarly, the factor for the external collector current I_{jBCx} reads

$$\zeta_{BCxT} = m_g + 1 - \zeta_{Cx} \tag{2.14.5-9}$$

with the mobility factor ζ_{Cx} of the external collector (epi-)region that is also being used for modeling the temperature dependence of the minority storage time of the parasitic substrate transistor.

Since the substrate doping is fairly low, the mobility exponent factor $\zeta\mu_{pS} = 2.5$ can be assumed as a good approximation, yielding

$$\zeta_{SCT} = m_g + 1 - \zeta_{\mu pS} \tag{2.14.5-10}$$

leaving the bandgap voltages as the only new model parameters for these regions. For silicon, the values of the above constants are: $m_g = 4.188$, $\zeta_{BCT} = 5.188\text{-}\zeta_{Ci}$, $\zeta_{SCT} = 2.69$.

2.14.6 Transit time and minority charge

The critical current density I_{CK}/A_E depends on temperature via physical parameters like mobility of the epitaxial collector and saturation velocity. The internal collector resistance contains the low-field electron mobility and reads

$$\boxed{r_{Ci}(T) = r_{Ci}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{Ci}}} \quad . \tag{2.14.6-1}$$

The model parameter ζ_{Ci} is a function of the collector doping concentration. The voltage V_{lim} contains both collector mobility and saturation velocity,

$$V_{lim}(T) = \frac{v_s(T)}{\mu_{nCi0}(T)} \tag{2.14.6-2}$$

According to [67], experimental results of the saturation velocity for T ≥ 250K can be approximated by

$$v_s(T) = v_{s0}(T_0)\left(\frac{T}{T_0}\right)^{-a_{vs}} \tag{2.14.6-3}$$

with T_0 =300K, $v_s(T_0)$ = 1.071*10^7 cm/s and a_{vs} = 0.87. The relation between a_{vs} and the existing HICUM model parameter a_{vs}, which is the relative TC, can be calculated from the derivative of (2.14.6-3) at T_0 and is given by

$$a_{vs} = \alpha_{vs} T_0 \tag{2.14.6-4}$$

Inserting the temperature dependence of the collector electron mobility and (2.14.6-3) into (2.14.6-2) gives the physics-based formulation

$$\boxed{V_{lim}(T) = V_{lim}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{Ci} - a_{vs}}} \tag{2.14.6-5}$$

which is simple and numerically stable, and does not require any additional model parameters. The equation is valid up to about 600K, which is the highest temperature of available experimental data for mobility and saturation velocity.

The CE saturation voltage can be modelled as a linear function of temperature,

$$\boxed{V_{C'E's}(T) = V_{C'E's}(T_0)[1 + \alpha_{CEs}\Delta T]} \ , \tag{2.14.6-6}$$

with α_{CEs} as a model parameter. Its value can be estimated from the difference between the respective relative temperature coefficients of the built-in voltages V_{DEi} and V_{DCi}. Similarly, the optional parameter $\mathrm{V_{DCk}}$ is modeled as a linear function of temperature according to

$$\boxed{V_{DCk}(T) = V_{DCk}(T_0)[1 - \alpha_{DCk}\Delta T]}, \tag{2.14.6-7}$$

with the temperature coefficient α_{DCk} as model parameter.

The temperature dependence of the transit time model requires no additional model parameters, except for the low-current transit time. The low-current portion of the transit time, τ_{f0}, as a function of temperature is mainly determined by the quadratic temperature dependence of the parameter τ_0:

$$\boxed{\tau_0(T) = \tau_0(T_0)[1 + \alpha_{\tau 0}\Delta T + k_{\tau 0}\Delta T^2]} \ . \tag{2.14.6-8}$$

The model parameters α_{t0} and k_{t0} can be expressed by physical quantities.

The time constants τ_{Bfvs} and τ_{pCs} depend on temperature via the same diffusivity (of the collector) and, therefore, the temperature dependence of the composite parameter τ_{hcs} can be expressed as

$$\boxed{\tau_{hcs}(T) = \tau_{hcs}(T_0)\left(\frac{T}{T_0}\right)^{(\zeta_{Ci}-1)}} \ . \tag{2.14.6-9}$$

The emitter time constant τ_{Ef0} depends on temperature via mainly the hole diffusivity in the neutral emitter and the current gain. Assuming a large emitter concentration with a negligible temperature dependence of the mobility (exponent coefficient ≈ 0.5), the temperature dependence of the emitter transit time can be neglected.

The temperature dependence of the mobile charge and of the additional delay times, that cause vertical NQS effects, follows automatically from that of the transit time using (2.3.1-1) and (2.9.1-1), respectively.

2.14.7 Temperature dependence of built-in voltages

In order to avoid the built-in voltages becoming negative at high temperatures, an empirical smoothing function was included in v2.1. This function has been replaced in v2.2 by a physics-based formulation, that can be derived from the behavior of the intrinsic carrier density at high temperatures [8].

At first, an auxiliary voltage is calculated at the reference temperature from the model parameter V_D given at the reference (or nominal) temperature T_0

$$\boxed{V_{Dj}(T_0) \;=\; 2V_{T0}\ln\left[\exp\left(\frac{V_D(T_0)}{2V_{T0}}\right) - \exp\left(-\frac{V_D(T_0)}{2V_{T0}}\right)\right]} \tag{2.14.7-1}$$

with the thermal voltage $V_{T0} = k_B T_0/q$. Then, the respective value at the actual temperature is calculated using the temperature dependent effective bandgap voltage of the respective junction, resulting in

$$V_{Dj}(T) \;=\; V_{Dj}(T_0)\frac{T}{T_0} - 3V_T\ln\left(\frac{T}{T_0}\right) + V_{geff}(T) - V_{geff}(T_0)\frac{T}{T_0} \tag{2.14.7-2}$$

For the bandgap voltage formulation (2.14.1-1), above equation reads

$$\boxed{V_{Dj}(T) \;=\; V_{Dj}(T_0)\left(\frac{T}{T_0}\right) - m_g V_T\ln\left(\frac{T}{T_0}\right) - V_{geff}(0)\left(\frac{T}{T_0} - 1\right)} \tag{2.14.7-3}$$

which reduces to the classical equation (that assumes a linear temperature dependence of V_{geff}) if $m_g = 3$. Finally, the built-in voltage is calculated as

$$\boxed{V_D(T) \;=\; V_{Dj}(T) + 2V_T\ln\left(\frac{1}{2}\left[1 + \sqrt{1 + 4\exp\left(-\frac{V_{Dj}(T)}{V_T}\right)}\right]\right)} \tag{2.14.7-4}$$

Since V_D is associated with the junction region, an average effective value is used for V_g, which is given by, e.g.,

$$V_{geff} \rightarrow V_{g(x,y)eff} = \frac{V_{gxeff} + V_{gyeff}}{2} \tag{2.14.7-5}$$

with $(x,y) = (B,E), (B,C), (C,S)$. The temperature dependence of the built-in voltages enters the zero-bias capacitance relations. Fig. 2.14.7/1 shows the impact of the choice of the V_g value on the temperature dependence of the zero-bias capacitance.

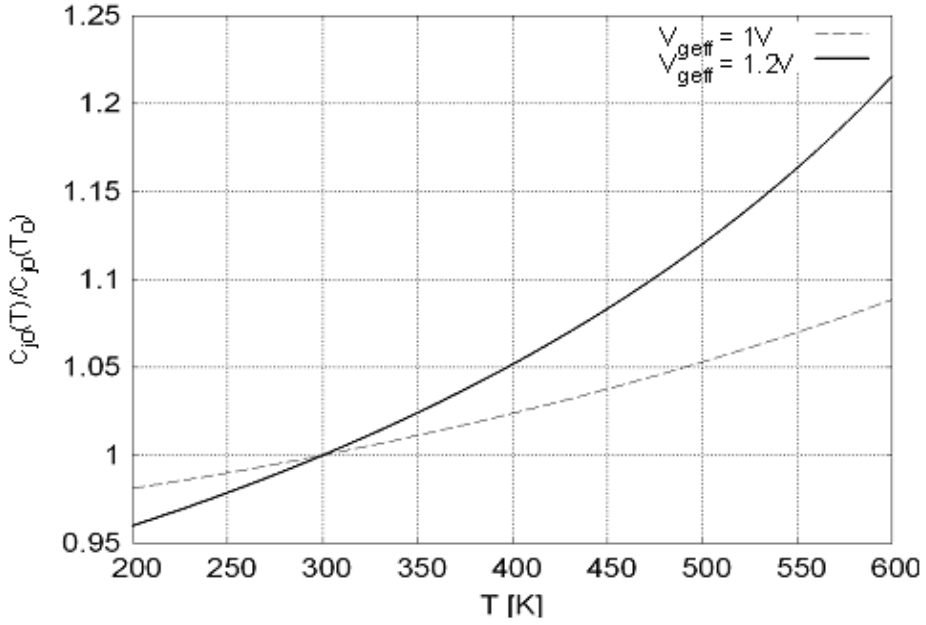

Fig. 2.14.7/1: Impact of bandgap values on the temperature dependence of the zero-bias depletion capacitance.

For electro-thermal simulations as well as for calculating the temperature coefficient of $Q_{p0}(T)$, the temperature derivative of the built-in voltage at the (parameter) reference temperature is required. In the code, the full expression for dV_D/dT as derived from (2.14.7-3) is used. However, since for $Q_{p0}(T)$ only its value at the reference (extraction) temperature T_0 is needed, the following expression can be used for parameter extraction:

$$\left.\frac{dV_D(T)}{dT}\right|_{T_0} \cong \left.\frac{dV_{Dj}(T)}{dT}\right|_{T_0} \tag{2.14.7-6}$$

Using the expression (2.14.1-1) for the bandgap voltage gives

$$\left.\frac{dV_{Dj}(T)}{dT}\right|_{T_0} = \frac{V_{Dj}(T_0) - V_{geff}(0) - m_g V_{T0}}{T_0} \tag{2.14.7-7}$$

As Fig. 2.14.7/2 shows, above equation is an excellent approximation for any reasonable extraction temperature.

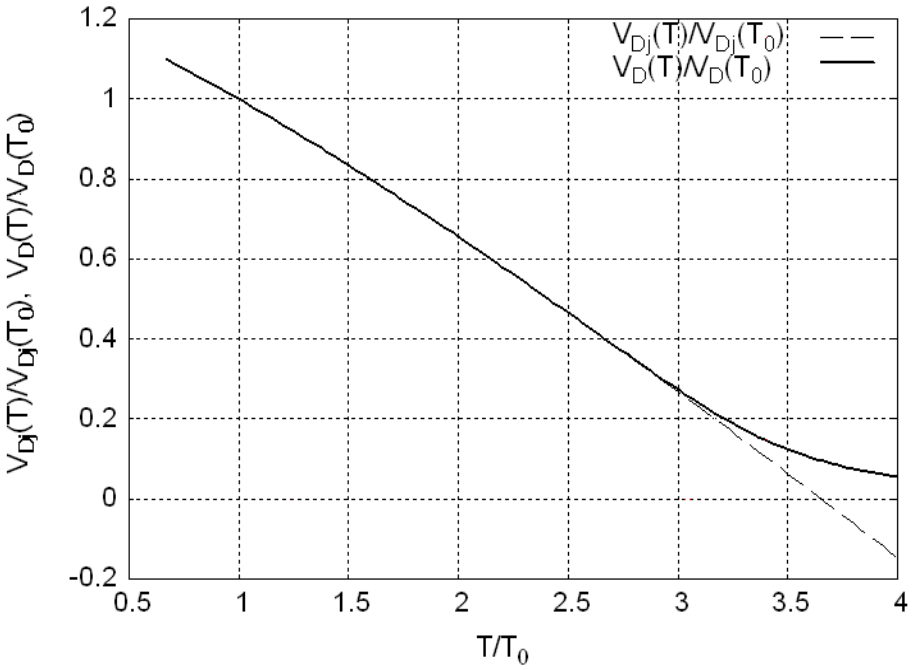

Fig. 2.14.7/2:Normalized built-in voltage vs normalized temperature (range $200 \le T/K \le 1200$); parameter $m_g = 3$.

2.14.8 Depletion charges and capacitances

The key parameter for the temperature dependence of the depletion charges and capacitances is the diffusion (or built-in) voltage, temperature dependence of which is formulated in the previous section.

The zero-bias junction capacitance can be expressed generally as $C_{j0} \sim V_D^{-z}$ so that its temperature dependence can be directly calculated from that of V_D:

$$\boxed{C_{j0}(T) = C_{j0}(T_0)\left(\frac{V_D(T_0)}{V_D(T)}\right)^z} \; . \tag{2.14.8-1}$$

The temperature dependence of the depletion charge follows automatically from (2.4.0-2) by applying the above formulas and assuming that the exponent-factor *z* does not depend on temperature.

The parameter α_j determining the maximum value of a depletion capacitance at forward bias decreases with increasing temperature and is (empirically) modified as follows:

$$a_j(T) = a_j(T_0)\frac{V_D(T)}{V_D(T_0)} \quad . \tag{2.14.8-2}$$

As can be seen in Fig. 2.14.8/1, the zero-bias capacitance increases, while the voltage at the maximum and the maximum itself decrease with increasing temperature.

The parameter C_{BEpar}, f_{BEpar} and f_{BCpar} do not depend on temperature.

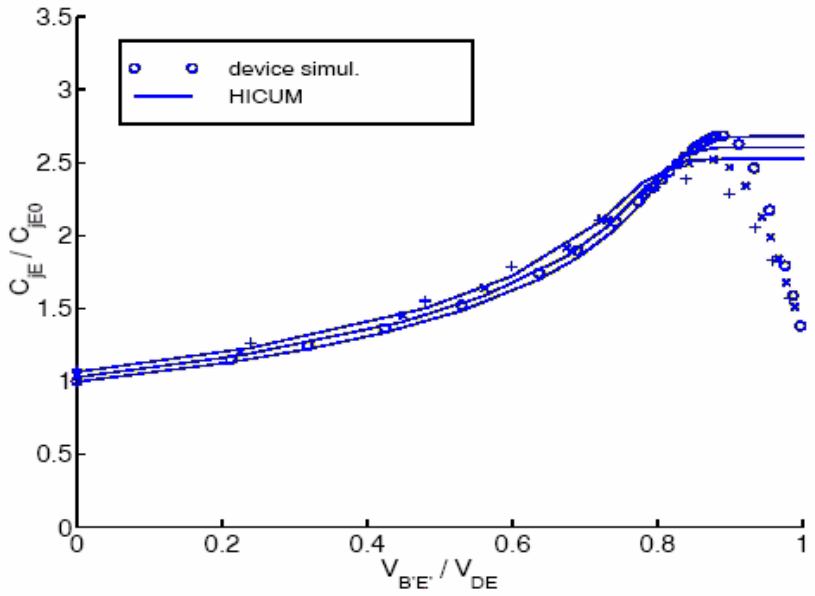

Fig. 2.14.8/1: Temperature dependence of the base-emitter depletion capacitance, normalized to its zero-bias value at 300K, vs. normalized applied voltage: comparison between 1D device simulation (symbols) and model equation (lines). The curves are for the temperatures *T*/K = 300 (o), 350 (*), 400 (+).

2.14.9 Series resistances

The internal base resistance depends on temperature mainly via the mobility in the neutral base region, which is contained in the internal base sheet resistance. Thus, the zero-bias resistance is described as

$$r_{Bi0}(T) = r_{Bi0}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{rBi}} \quad . \tag{2.14.9-1}$$

The model parameter ζ_{rBi} is a function of the (average) base doping concentration (cf. $r_{Ci0}(T)$). Conductivity modulation and emitter current crowding in r_{Bi} are automatically described as a function of T by the corresponding charges and currents. The shunt capacitance C_{rBi} is temperature dependent via the capacitances of the internal transistor.

External base resistance r_{Bx}, external collector resistance r_{Cx}, and emitter series resistance follow a similar relationship as r_{Bi0}. This requires the model parameters ζ_{rBx}, ζ_{rCx} and ζ_{rE} which are a function of the (average) doping concentrations within the corresponding regions.

Fig. 2.14.9/1 shows the various types of temperature dependence that can be modelled with the above equation.

The temperature dependence of the substrate coupling resistance r_{su} is presently not modeled but can easily be included employing the same formulation as (2.14.9-1) and the mobility factor $\zeta_{rsu} = 2.5$.

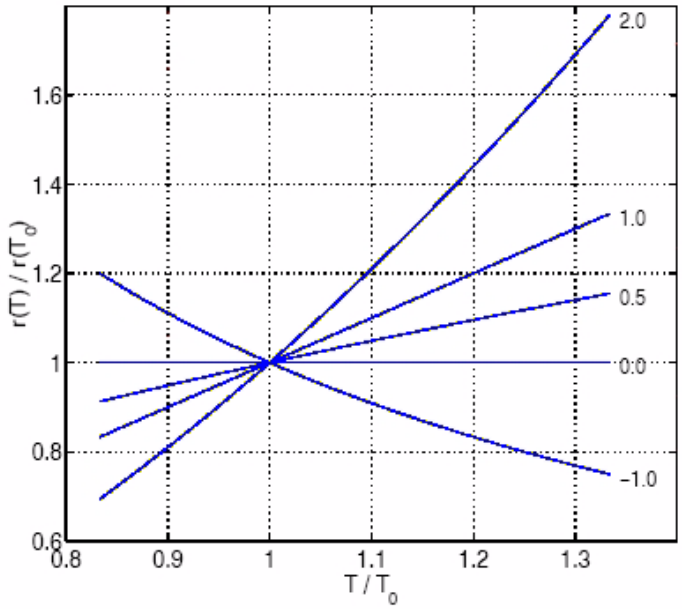

Fig. 2.14.9/1: Normalized resistance as a function of temperature according to eq. (2.14.9-1) for different values of ζ (= ζ_{Ci}, ζ_{rBi}, ζ_{rBx}, ζ_{rCx} or ζ_{rE}) as parameter.

2.14.10 Breakdown

2.14.11 Base-collector junction (avalanche effect)

The temperature dependence of the coefficients describing avalanche breakdown can be described as [17]

$$a_{\mathrm{n}}(T) = a_{\mathrm{n}}(T_0)\ exp(\alpha_{\mathrm{na}}\,\Delta T)\ , \tag{2.14.11-1}$$

$$b_{\mathrm{n}}(T) = b_{\mathrm{n}}(T_0)\ exp(\alpha_{\mathrm{nb}}\,\Delta T) \tag{2.14.11-2}$$

with $\Delta T = T - T_0$ and the temperature coefficients α_{na} and α_{nb}. Insertion of these equations into (2.10.1-4,5) gives for the model parameters

$$\boxed{f_{AVL}(T) = f_{AVL}(T_0)\exp(\alpha_{fav}\Delta T)} \quad \text{and} \quad \boxed{q_{AVL}(T) = q_{AVL}(T_0)\exp(\alpha_{qav}\Delta T)} \tag{2.14.11-3}$$

with the temperature coefficients $\alpha_{\mathrm{fav}} = \alpha_{\mathrm{na}} - \alpha_{\mathrm{nb}}$ and $\alpha_{\mathrm{qav}} = \alpha_{\mathrm{nb}}$ which are considered as model parameters. According to the study in [18], the temperature dependence of the parameter a_{n} is negligible while only b_{n} varies slightly with temperature. Therefore, the exp-function reduces to (or can be approximated by) its first series terms, i.e. $\exp(\alpha_{nb}\Delta T) \approx 1 + \alpha_{nb}\Delta T$.

The fitting parameter kAVL in (2.10.1-2) is modeled temperature dependent based on the same equation type by

$$\boxed{k_{AVL}(T) = k_{AVL}(T_0)\exp(\alpha_{kav}\Delta T)}. \tag{2.14.11-4}$$

2.14.12 Base-emitter junction (tunnelling effect)

The temperature dependence of the parameters describing BE tunnelling is mainly determined by the bandgap's temperature dependence. The saturation current is then given by

$$\boxed{I_{BEtS}(T) = I_{BEtS}(T_0)\sqrt{\frac{V_G(T_0)}{V_G(T)}}\left(\frac{V_{DE}(T)}{V_{DE}(T_0)}\right)^2\frac{C_{jE0}(T)}{C_{jE0}(T_0)}}\ . \tag{2.14.12-1}$$

The exponent-coefficient as a function of temperature reads:

$$a_{BEt}(T) = a_{BEt}(T_0)\left(\frac{V_g(T)}{V_g(T_0)}\right)^{3/2}\frac{V_{DE}(T_0)}{V_{DE}(T)}\frac{C_{jE0}(T_0)}{C_{jE0}(T)} \tag{2.14.12-2}$$

where either internal or perimeter related parameters have to be inserted for V_{DE} and C_{jE0}, according to the node assignment of the tunnelling current source.

In the above equations, no additional model parameters are required since the model's internal band-gap voltage (cf. eq. (2.14.1-3)) can be used. Employing the model internal band-gap voltage also enables the evaluation of the above parameters for different materials. Since the tunneling current is associated with the BE junction region, physically the bandgap voltage corresponds to the average value of the base and emitter bandgap voltage,

$$V_g(T) \;=\; V_{gBEeff}(T) \;=\; \frac{V_{gBeff}(T) + V_{gEeff}(T)}{2} \qquad (2.14.12\text{-}3)$$

which is already available from the calculation of the BE depletion capacitance and junction saturation current component. However, only the ratio of the bandgap voltages enters the equations (2.14.12-1) and (2.14.12-2).

Fig. 2.14.12/1 shows an example for the temperature dependence of the model parameters calculated from (2.14.12-1) and (2.14.12-2).

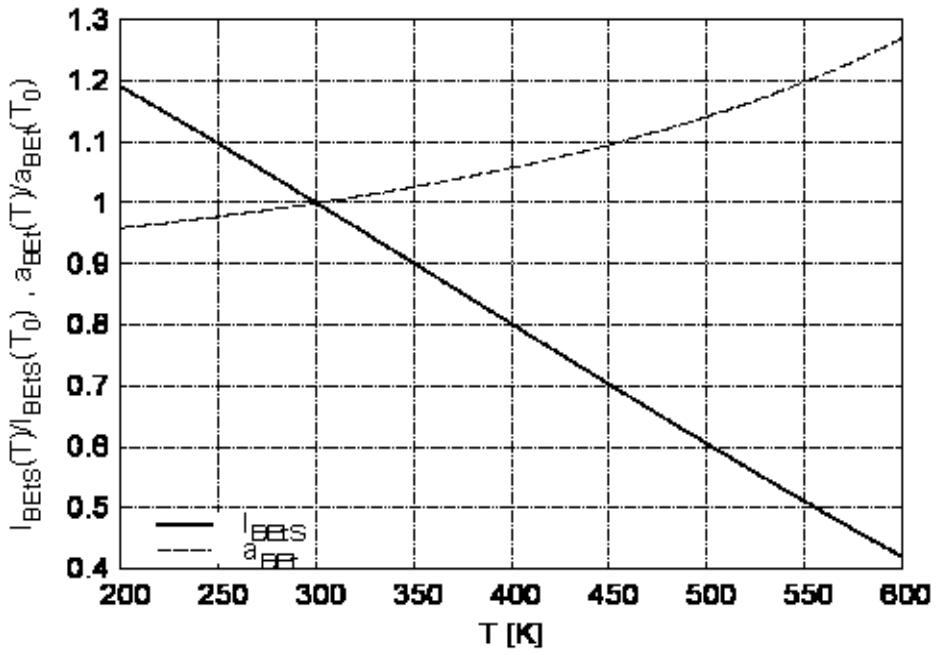

Fig. 2.14.12/1: Example for the temperature dependence of tunnelling current parameters, normalized to their values at 300K.

2.14.13 Parasitic substrate transistor

The temperature dependence of the transfer current of the parasitic substrate transistor is given by

$$I_{TS}(T) = I_{TSS}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{BCxT}} \exp\left[\frac{V_{gCeff}(0)}{V_T}\left(\frac{T}{T_0}-1\right)\right] \tag{2.14.13-1}$$

with the factor ζ_{BCxT} from (2.14.5-9).

The temperature dependence of the current across the CS junction has already been given in section 2.14.5

The transit time of the parasitic substrate transistor is described as a function of temperature similar to (2.14.6-9),

$$\boxed{\tau_{Sf}(T) = \tau_{Sf}(T_0)\left(\frac{T}{T_0}\right)^{(\zeta_{Cx}-1)}}, \tag{2.14.13-2}$$

with the temperature factor ζ_{Cx} as additional model parameter, that can be determined from the mobility in the external collector region.

Note, that substrate transistor action can generally be avoided by a surrounding collector sinker.

2.14.14 Thermal resistance

The temperature dependence of the thermal resistance is modeled by

$$\boxed{R_{th}(T) = R_{th}(T_0)[1+\alpha_{Rth}\Delta T]\left(\frac{T}{T_0}\right)^{\zeta_{Rth}}} \tag{2.14.14-1}$$

with the model parameters α_{Rth} and ζ_{Rth}. The linear dependence, which was introduced to avoid a possible numerical instability, has turned out to be sufficient for practical applications. Therefore, the last term is planned to be dropped in future.

2.15 Self-heating

The increase of the transistor's "junction" temperature T_j caused by self-heating is calculated using a thermal network as shown in Fig. 2.1.0/1b. The current source corresponds to the power dissipated in the device, and the node voltage corresponds to the junction temperature. The calculation requires the thermal resistance, R_{th}, and thermal capacitance, C_{th}, (of the particular transistor) as model parameters. The thermal network is solved together with each transistor model (provided $R_{th}>0$ and the flag for self-heating calculation, *FLSH*, are not equal to zero for d.c. and transient operation. The node voltage is passed on to the model routine in order to calculate the temperature dependent model parameters.

The power dissipation is generally caused by all dissipative elements in the equivalent circuit (i.e. excluding any energy storage elements). If *FLSH* = 2, the power in the model is calculated including all the relevant elements in the equivalent circuit as follows,

$$P = I_T V_{C'E'} + \sum I_{jd} V_{diode} + I_{AVL}(V_{DCi} - V_{B'C'}) + \sum \frac{\Delta V_n^2}{r_n} \quad , \tag{2.15.0-2}$$

with d={*BEi,BCi,BEp,BCx,SC*}, V_{diode} as respective diode voltage, r_n as (non-zero) series resistance (n={*Bi,Bx,E,Cx*}) and ΔV_n as the corresponding voltage drop across those resistances.

However, since not only the accuracy of the single-pole network and, in particular, of the determination (and geometry scaling) of R_{th} and C_{th} are fairly limited, but also the consideration of *all* dissipative elements generates elaborate expressions for the derivatives in the Jacobian, only the most relevant dissipative elements are included in the power calculation for *FLSH* = 1:

$$P = I_T V_{C'E'} + I_{AVL}(V_{DCi} - V_{B'C'}) \tag{2.15.0-3}$$

The purpose of this measure is to reduce the computational effort without sacrificing convergence.

Note that only *self*-heating is presently taken into account but not the thermal coupling between different devices on the chip, which is a much more complicated topic and does not belong directly into a transistor model formulation. However, the already existing temperature node of the model can be used for modelling thermal coupling in a circuit, like in HICUM/L4 [59].

2.16 Lateral scaling

Due to many different processes the geometry scaling of bipolar transistors is generally more complicated than for MOS transistors. An extensive set of scaling formulas for a variety of technologies has been implemented over many years in the program TRADICA [23] which is used to generate model parameters for a given transistor configuration. The description of the full set of lateral scaling equations is beyond the scope of this manual. A detailed overview on BJT and HBT scaling with emphasis on HICUM/L2 is given in [1]. Below, only those equations that have been implemented in the HICUM/L2 code are described.

2.16.1 Bias *dependent* collector current spreading

If the transistor enters the high-current region, minority charge is stored in the collector within the injection zone w_i which is strongly bias dependent. This width also depends on the collector current spreading angle and can be calculated in normalized from as

$$w = \frac{w_i}{w_C} = \begin{cases} \dfrac{\kappa - 1}{\zeta_l - \kappa\zeta_b} & , \quad l_{E0} > b_{E0} \\ \dfrac{1}{\zeta_b}\left[\dfrac{1+\zeta_b}{1+i_{ck}\zeta_b} - 1\right] & , \quad l_{E0} = b_{E0} \end{cases} \tag{2.16.1-1}$$

with the width and length related spreading factors

$$\zeta_b = \xi_b w_{Ci} \quad \text{and} \quad \zeta_l = \xi_l w_{Ci}\,, \tag{2.16.1-2}$$

the auxiliary variable

$$\kappa = \frac{1+\zeta_l}{1+\zeta_b}\exp\left[i_{ck}\ln\left(\frac{1+\zeta_b}{1+\zeta_l}\right)\right] = \left(\frac{1+\zeta_b}{1+\zeta_l}\right)^{i_{ck}-1}, \tag{2.16.1-3}$$

and the normalized current

$$i_{ck} = 1 - \frac{i + \sqrt{i^2 + a_{hc}}}{1 + \sqrt{1 + a_{hc}}} \quad \text{with} \quad i = 1 - \frac{I_{CK}}{I_{Tf}} \tag{2.16.1-4}$$

Fig. 2.16.1/1 shows the normalized injection width as a function of normalized (forward) collector current with the current spreading angle δ_C as a parameter. δ_C=0 corresponds to the 1D case; with increasing spreading angle, the current density in the collector is reduced and, therefore, the extension of the injection width decreases relative to the 1D case. Compared to long transistors (Fig. (a)), which correspond to the 2D case with $l_E >> b_E$, the impact of current spreading is smaller than for a square-emitter transistor (Fig. (b)), since in the latter current spreading in all four lateral directions becomes significant.

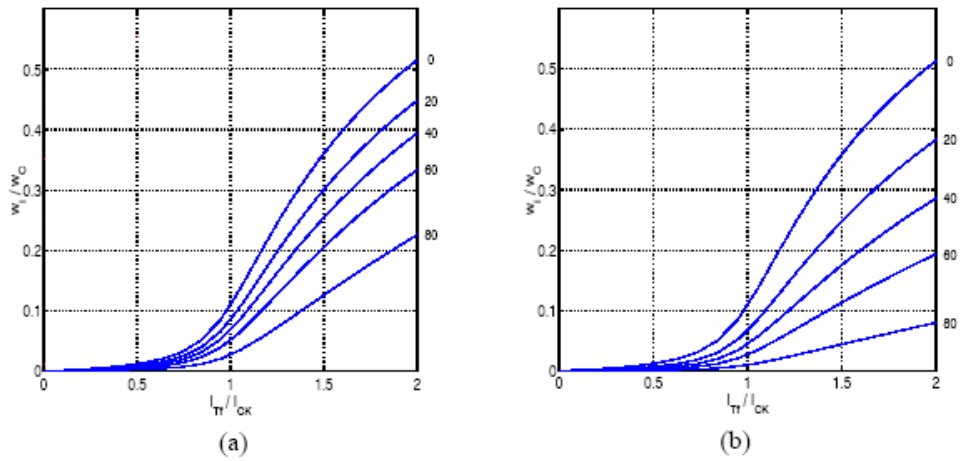

Fig. 2.16.1/1: Normalized injection width as a function of normalized (forward) collector current for various current spreading angles δ_C: (a) long emitter l_E>>b_E; (b) square-emitter l_E=b_E. Parameters: w_C/b_E = 1, a_{hc}=0.05, w_C/l_E = 0.01 for (a) and w_C/l_E = 1 for (b).

Also, the equations for τ_{fC} and Q_{fC} have to be extended in order to be able to describe the bias dependence of the occurring 2D and 3D current spreading effects:

$$Q_{Cf} = \tau_{pCS}\, I_{Tf} \exp\left(\frac{\Delta V_{cBar} - V_{cBar}}{V_T}\right) \begin{cases} 2\dfrac{f_{CSl} - f_{CSb}}{\zeta_b - \zeta_l} & , \; l_{E0} > b_{E0} \\ \dfrac{1 + \zeta_b w/3}{1 + \zeta_b w} w^2 & , \; l_{E0} = b_{E0} \end{cases} \tag{2.16.1-5}$$

with $\tau_{pCS} = f_{thc}\,\tau_{hcs}$, and the auxiliary (bias dependent) functions

$$f_{CSl} = \frac{\ln(1+\zeta_l w)}{\zeta_l}\left(\frac{1}{2} - \frac{\zeta_b}{6\zeta_l}\right) + w\left(\frac{\zeta_b}{6\zeta_l} + \frac{\zeta_b w}{6}\right) \tag{2.16.1-6}$$

$$f_{CSb} = \frac{\ln(1+\zeta_b w)}{\zeta_b}\left(\frac{1}{2} - \frac{\zeta_l}{6\zeta_b}\right) + w\left(\frac{\zeta_l}{6\zeta_b} + \frac{\zeta_l w}{6}\right), \tag{2.16.1-7}$$

which are invariant to swapping ζ_b and ζ_l and so is f_{CCS}. For the often encountered case of long emitter fingers (2D case), the function reduces to

$$f_{CCS}(\zeta_l = 0) = \frac{2}{\zeta_b}\left[w\left(\frac{1}{2} + \frac{\zeta_b}{4}w\right) - \frac{\ln(1+\zeta_b w)}{\zeta_b}\frac{1}{2}\right]. \tag{2.16.1-8}$$

In the implementation of these equations, potential divisions by zero, that could occur for $\zeta_b = 0$ or $\zeta_l = 0$ or $\zeta_b = \zeta_l = 0$ (1D case), have been taken into account by appropriate series expansions, which then also include the 1D theory described before. For the 2D/3D case discussed above, the transit time is calculated as:

$$\tau_{Cf} = \left.\frac{dQ_{Cf}}{dI_{Tf}}\right|_{V_{C'E'}}. \tag{2.16.1-9}$$

The base charge component at high current densities, ΔQ_{Bf}, is still calculated without current spreading, using the saturation storage time $\tau_{Bfvs} = \tau_{hcs}(1\text{-}f_{thc})$ and the analytical expression of the corresponding transit time $\Delta\tau_{Bf}$, while in (2.16.1-5) $\tau_{pCs} = f_{thc}\tau_{hcs}$.

Collector current spreading changes the cross section of the current flow or, equivalently, the internal collector resistance. At the critical current, the resistance of the internal ohmic collector is then given by (2.3.1-8), in which the 1D value has been modified by the collector current spreading function [1]

$$f_{cs} = \begin{cases} \dfrac{\zeta_b - \zeta_l}{\ln[(1+\zeta_b)/(1+\zeta_l)]} & , l_E > b_E \\ 1 + \zeta_b & , l_E = b_E \end{cases}. \tag{2.16.1-10}$$

2.16.2 Bias *independent* approximation of collector current spreading (not implemented)

The analytical formulation for 3D collector current spreading implemented in HICUM/L2 consists of a bias dependent portion and a bias independent portion that can be obtained from preprocessing the internal collector resistance in I_{CK} (e.g. using TRADICA). If the collector current spreading effect is turned on by setting either one of the parameters LATB and LATL to a value greater than zero, the corresponding bias dependent equations in some cases seem to add significant computational effort to the overall model execution time. An alternative approach that reduces the computational effort while maintaining sufficient accuracy in the bias region of interest is based on a shift of data processing from within the model (i.e. circuit simulator) to a preprocessing and corresponding model parameter modification.

During the preprocessing, the complete set of 3D collector current spreading equations (if LATB > 0 and/or LATL > 0) is exercised only at $I_{Tf} = I_{CK}$, resulting in the transit time $\tau_f(I_{CK})$. The latter is supposed to closely match the reference (i.e. measurements), since the transit time model parameters have been extracted from that same reference. In addition, evaluating the corresponding 1D equations with only the current spreading factor included in I_{CK} (i.e. same I_{CK} as in (2.3.1-7) for the 3D case), gives the (generally higher) transit time $\tau_{f,1D}(I_{CK})$. From these two time constants, a correction factor can be found,

$$f_{ccs} = \frac{\tau_f(I_{CK}) - \tau_{f0}}{\tau_{f,\,1D}(I_{CK}) - \tau_{f0}} \,, \tag{2.16.2-1}$$

which is then used to multiply the collector transit time of the 1D equations. Fig. 2.16.2/1 shows a comparison of the various curves for an extreme example with large current spreading angle (i.e. large current spreading) and a large relative contribution of the collector transit time. The corrected curves match the reference very well in the region of the increase below and up to the critical current I_{CK}, and still reasonably well beyond I_{CK}. As a consequence, the computationally more expensive 3D current spreading calculations can be replaced in most cases, and especially for SiGe HBTs, by exercising the simpler 1D equations, in which the 3D I_{CK} values are still being used and a model parameter τ_{hcs} has been modified. The corresponding correction factor can be easily included in the modified saturation transit time:

$$\tau_{hcs} = f_{ccs}\tau_{pCs} + \tau_{Bfvs} = f_{ccs}\frac{w_C^2}{4\mu_{nC0}V_T} + \frac{w_{Bm}w_C}{2G_{\zeta i}\mu_{nC0}V_T} \ . \qquad (2.16.2\text{-}2)$$

In practice, the original model parameter τ_{hcs} will be extracted from measurements together with the partitioning factor

$$f_{thc} = \frac{\tau_{pCs}}{\tau_{hcs,x}} \ . \qquad (2.16.2\text{-}3)$$

Thus, during preprocessing for model card generation the modified extracted time constant

$$\tau_{hcs} = (1 - f_{thc})\tau_{hcs,x} + f_{ccs}\tau_{pCs} = [(1 - f_{thc}) + f_{ccs}f_{thc}]\tau_{hcs,x} \qquad (2.16.2\text{-}4)$$

is calculated and used as model parameter.

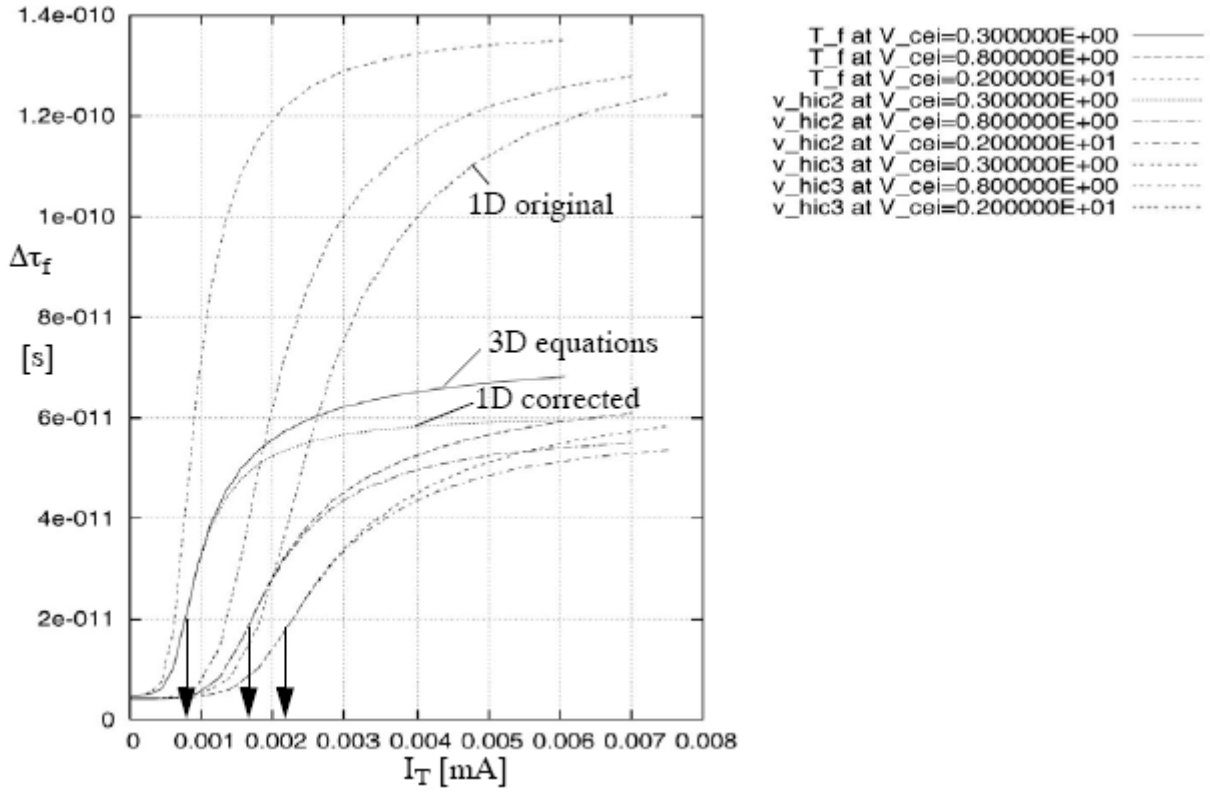

Fig. 2.16.2/1: Transit time vs. transfer current (1D test transistor) for different internal CE voltages: 3D collector current spreading equations with LATB=5.55 and LATL=0.55 ("T_f"); 1D equations with $I_{CK}(f_{cs})$ and correction factor ("v_hic2"); the emitter transit time was turned of in this example.

2.16.3 Emitter current crowding

The model parameter f_{geo} occurring in the current crowding factor (2.6.0-15) of the internal base resistance is given by

$$f_{geo} = \frac{1}{g_i\, g_\eta} \tag{2.16.3-1}$$

in which the geometry functions

$$g_\eta = 18.3 - \left[12.2\frac{b_E}{l_E} - 19.6\left(\frac{b_E}{l_E}\right)^2\right] \quad \text{and} \quad g_i = \frac{1}{12} - \left(\frac{1}{12} - \frac{1}{28.6}\right)\frac{b_E}{l_E} \tag{2.16.3-2}$$

depend on the emitter dimensions only and describe a smooth transition from long to short emitter windows. The variable f_{Qi} in (2.6.0-19) is given by

$$\tau_0 = \tau_{f0i}\frac{1 + (\tau_{f0p}/\tau_{f0i})\gamma_C P_{E0}/A_{E0}}{1 + \gamma_C P_{E0}/A_{E0}} = \frac{\tau_{f0i}}{f_{Qi}}. \tag{2.16.3-3}$$

The geometry functions above have not been implemented in the HICUM/L2 code but need to be calculated by a geometry scaling preprocessor.

3 Parameters

This chapter contains a reference list of model parameters with a brief description. The provided default values should be used for model implementation in a circuit simulator; with these values, all but the absolutely necessary functions that define a bipolar transistor, are turned off. This way, the user only needs to specify the parameters for those effects that are desired to be taken into account. Next to that column specifies the possible range of the parameter values, where according to the standard mathematical notation, brackets [ ] indicate that the range includes the endpoints, but parentheses ( ) signifies the exclusion of the endpoints. Few of the parameters (e.g. some flags) take only one of the two or three possible values and the corresponding values are given as *x/y* or *x/y/z*, where the parameter takes either of the values given. Empty ‘range’ column signifies that the particular parameter can take any value. In addition to these, a second set of parameter values is provided for exercising the model with most of the physical effects being turned on. This set can be used for, e.g. model testing.

Finally, in the most right column, a device layout multiplication factor is given, which represents the scaling of the respective parameter in case of M identical devices connected in parallel. Note though, that this scaling becomes inaccurate at high frequencies due to the missing interconnect elements that need to be accounted for separately for such device structures.

The following list of model parameters is supposed to be available in all (commercial) implementations of the model. The list is divided into groups of parameters according to the elements in the HICUM equivalent circuit shown in Fig. 2.1.0/1 as well as those for additional physical effects such as noise and temperature dependence. Although the total number of model parameters appears to be large, less time and effort needs to be spent for model parameter extraction - assuming the same physical effects are considered as in the SGPM - due to (a) the physical nature and modularity of the model formulation and (b) the reliable and clearly defined extraction procedure. Note, that not every parameter always needs to be specified for a particular process or application in order to achieve the required accuracy. For example, certain parameters are related to HBTs only and, therefore, can be left at their default values for homojunction transistors.

Many HICUM parameters have been chosen as simple factors that are related to physically meaningful basic parameters like a capacitance, charge or transit time. This choice significantly reduces changes (and the probability of errors) in the parameter list if the basic parameters are changed for,

e.g., statistical simulation, because the factors often assume very similar values even for different process technologies.

Input for the factor M in the last column is interpreted as follows: multiplication of the parameter value is indicated by M while division is indicated by 1/M and no action by leaving the entry blank. Caution is required if the factor is applied to r_{su}, C_{su}, R_{th} and C_{th}, in which no interaction between parallel devices is assumed.

For production-type parameter library releases, it is recommended to have self-heating, non-quasi-static effects, and HF noise correlation turned off by their respective flags, since the effects may not be required for many design tasks, especially not for first phase design and feasibility studies. Including these effects will unneccessarily increase the simulation time for *all* users during the entire design phase. These effects can become important in the last phase for tuning the performance of certain types of circuits or for design verification before tape-out. It is suggested to make these flags available in the design system as options for circuit designers.

As reference temperature, 27^{o}C has been chosen to remain compatible with other simulators and models. The value for "∞" may be dependent on the simulator system. **Therefore, the user is referred to the manual of the respective simulator.**

3.1 Transfer current

no	name	description	default	range	test	unit	factor
1	**c10**	GICCR constant (related to the saturation current by Is=c10/qp0)	2E-30 (1E-16)	[0:1] ([0:1])	3.76e-32 (1.35E-18)	AC (A)	M^2 (M)
2	**qp0**	Zero-bias hole charge	2E-14	(0:1]	2.78e-14	C	M
3	**hf0**	Weight factor for the low current minority charge	1	[0:inf)	1.0	-	
4	**hfe**	Emitter minority charge weighting factor in HBTs	1	[0:inf]	1.0	-	
5	**hfc**	Collector minority charge weighting factor in HBTs	1	[0:inf]	1.0	-	

no	name	description	default	range	test	unit	factor
6	**hjei0**	B-E depletion charge weighting factor in HBTs	1	[0:100]	1.0	-	
7	**ahjei**	Slope factor of $h_{jEi}(V_{BE})$	0	[0:100]	3.0	-	
8	**rhjei**	Smoothing factor for $h_{jEi}(V_{BE})$ at high forward bias	1	(0:10)	2.0		
9	**hjci**	B-C depletion charge weighting factor in HBTs	1	[0:100]	1.0	-	
10	**mcf**	non-ideality factor (for III-V HBTs)	1	(0:10]	1.0	-	

3.2 Base current: base-emitter components

no	name	description	default	range	test	unit	factor
1	**ibeis**	Internal B-E saturation current	1E-18	[0:1]	1.16e-20	A	M
2	**mbei**	Internal B-E current ideality factor	1	(0:10]	1.0150	-	
3	**ireis**	Internal B-E recombination saturation current	0	[0:1]	1.16e-16	A	M
4	**mrei**	Internal B-E recombination current ideality factor	2	(0:10]	2.0	-	
5	**ibeps**	Peripheral B-E saturation current	0	[0:1]	3.72e-21	A	M
6	**mbep**	Peripheral B-E current ideality factor	1	(0:10]	1.0150	-	
7	**ireps**	Peripheral B-E recombination saturation current	0	[0:1]	1.0e-30	A	M
8	**mrep**	Peripheral B-E recombination current ideality factor	2	(0:10]	2.0	-	
9	**tbhrec**	base current recombination time constant at the BC barrier for high forward injection (default is v2.1 compatible)	0 ($\equiv \infty$)	[0:inf)	250	s	

3.3 Base current: base-collector components

no	name	description	default	range	test	unit	factor
1	**ibcis**	Internal B-C saturation current	1E-16	[0:1]	1.16e-20	A	M
2	**mbci**	Internal B-C current ideality factor	1	(0:10]	1.0150	-	
3	**ibcxs**	External B-C saturation current	0	[0:1]	4.39e-20	A	M
4	**mbcx**	External B-C current ideality factor	1	(0:10]	1.03	-	

3.4 Base-emitter tunnelling current

no	name	description	default	range	test	unit	factor
1	**ibets**	B-E tunnelling saturation current	0	[0:50]	0.0	A	M
2	**abet**	Exponent factor for tunnelling current	40	[0:inf)	40	-	
3	**tunode**	specifies the base node connection of the tunneling current source (default is v2.1 compatible)	1	[0/1]	0	-	

3.5 Base-collector avalanche current

no	name	description	default	range	test	unit	factor
1	**favl**	Avalanche current factor	0	[0:inf)	1.186	1/V	
2	**qavl**	Exponent factor for avalanche current	0	[0:inf)	11.1e-15	C	M
3	**kavl**	Flag/factor for turning strong avalanche on or off	0	[0:3]	0.1	-	
4	**hcavl**	Flag/factor for current dependent avalanche model	0	[0:10]	1	-	
5	**hvdavl**	Factor for current dependent avalanche (spatially dep. C doping)	0	[0:10]	0.5	-	

3.6 Series resistances

no	name	description	default	range	test	unit	factor
1	**rbi0**	Zero-bias internal base resistance	0	[0:inf)	71.76	Ω	1/M
2	**rbx**	External base series resistance	0	[0:inf)	8.83	Ω	1/M
3	**fgeo**	Factor for geometry dependence of emitter current crowding (r_{Bi})	0.6557	[0:inf]	0.73	-	
4	**fdqr0**	Correction factor for modulation by B-E and B-C Space charge layer	0	[-0.5:100]	0.2	-	
5	**fcrbi**	Ratio of HF shunt to total internal capacitance (lateral NQS effect)	0	[0:1]	0.0	-	
6	**fqi**	Ratio of internal to total minority charge	1.0	[0:1]	0.9055	-	
7	**re**	Emitter series resistance	0	[0:inf)	12.534	Ω	1/M
8	**rcx**	External collector series resistance	0	[0:inf)	9.165	Ω	1/M

3.7 Substrate transistor

no	name	description	default	range	test	unit	factor
1	**itss**	Saturation current of substrate transistor transfer current	0	[0:1]	1.0e-16	A	M
2	**msf**	Forward ideality factor of substrate transfer current (note: set $m_{sr} = m_{sf}$ in (2.12.0-10))	1	(0:10]	1.05	-	
3	**iscs**	Saturation current of C-S diode	0	[0:1]	1e-17	A	M
4	**msc**	Ideality factor of C-S diode	1	(0:10]	1.0	-	
5	**tsf**	Transit time (forward operation)	0	[0:inf)	1.05	s	

3.8 Intra-device substrate coupling

Note: using the M factor is dangerous in this case, unless the transistor cell is exactly replicated and no coupling exists between cells.

no	name	description	default	range	test	unit	factor
1	**rsu**	Substrate series resistance	0	[0:inf)	0	Ω	1/M
2	**csu**	Shunt capacitance (caused by substrate permittivity)	0	[0:inf)	0	F	M

3.9 Depletion charge and capacitance components

Version 2.1 parameters *ALJEI* and *ALJEP* (instead of the correct parameter names *AJEI* and *AJEP) are not supported anymore*.

no	name	description	default	range	test	unit	factor
1	**cjei0**	Internal B-E zero-bias depletion capacitance	1E-20	[0:inf)	8.11e-15	F	M
2	**vdei**	Internal B-E built-in potential	0.9	(0:10]	0.95	V	
3	**zei**	Internal B-E grading coefficient	0.5	(0:1)	0.5	-	
4	**ajei**	Ratio of maximum to zero-bias value of internal B-E capacitance	2.5	[0:inf)	1.8	-	
5	**cjep0**	Peripheral B-E zero-bias depletion capacitance	1E-20	[0:inf)	2.07e-15	F	M
6	**vdep**	Peripheral B-E built-in potential	0.9	(0:10]	1.05	V	
7	**zep**	Peripheral B-E grading coefficient	0.5	(0:1)	0.4	-	
8	**ajep**	Ratio of maximum to zero-bias value of peripheral B-E capacitance	2.5	[0:inf)	2.4	-	
9	**cjci0**	Internal B-C zero-bias depletion capacitance	1E-20	[0:inf)	1.16e-15	F	M
10	**vdci**	Internal B-C built-in potential	0.7	(0:10]	0.8	V	
11	**zci**	Internal B-C grading coefficient	0.4	(0:1)	0.333	-	

no	name	description	default	range	test	unit	factor
12	**vptci**	Internal B-C punch-through voltage	100	(0:100]	100	V	
13	**cjcx0**	External B-C zero-bias depletion capacitance	1E-20	[0:inf)	5.4e-15	F	M
14	**vdcx**	External B-C built-in potential	0.7	(0:10]	0.700	V	
15	**zcx**	External B-C grading coefficient	0.4	(0:1)	0.333	-	
16	**vptcx**	External B-C punch-through voltage	100	(0:100]	100	V	
17	**cjs0**	C-S zero-bias depletion capacitance	0	[0:inf)	3.64e-14	F	M
18	**vds**	C-S built-in potential	0.6	(0:10]	0.6	V	
19	**zs**	C-S grading coefficient	0.5	(0:1)	0.447	-	
20	**vpts**	C-S punch-through voltage	100	(0:100]	100	V	
21	**cscp0**	Peripheral C-S zero-bias depletion capacitance	0	[0:inf)	3.64e-14	F	M
22	**vdsp**	Peripheral C-S built-in potential	0.6	(0:10]	0.6	V	
23	**zsp**	Peripheral C-S grading coefficient	0.5	(0:1)	0.447	-	
24	**vptsp**	Peripheral C-S punch-through voltage	100	(0:100]	100	V	

Note: The punch-through voltages should be limited to values > 0.

3.10 Minority charge storage effects

no	name	description	default	range	test	unit	factor
1	**t0**	Low-current forward transit time at VBC=0V	0	[0:inf)	4.75e-12	s	
2	**dt0h**	Time constant for base and B-C space charge layer width modulation	0	(-inf:inf)	2.1e-12	s	
3	**tbvl**	Time constant for modelling carrier jam at low VCE	0	(-inf:inf)	4.0e-12	s	
4	**tef0**	neutral emitter storage time	0	[0:inf)	1.8e-12	s	

no	name	description	default	range	test	unit	factor
5	**gtfe**	Exponent factor for current dependence of neutral emitter storage time	1	(0:10]	1.4	-	
6	**thcs**	Saturation time constant at high current densities	0	[0:inf)	30e-12	s	
7	**ahc**	Smoothing factor for current dependent of base and collector transit time	0.1	(0:50]	0.75	-	
8	**fthc**	Partitioning factor for base and collector portion	0	[0:1]	0.6	-	
9	**rci0**	Internal collector resistance at low electric field	150	(0:inf)	127.8	Ω	1/M
10	**vlim**	Voltage separating ohmic and saturation velocity regime	0.5	(0:10]	0.70	V	
11a 11b	**vces** **vdck**	Internal C-E saturation voltage Internal BC built-in voltage	0.1 0	[0:1] [0:1]	0.1 0.8	V V	
12	**vpt**	Collector punch-through voltage	0 (≡ ∞)	(0:inf]	5	V	
13	**delck**	Field dependence factor for ICK	2.0	(0:10]	2.0		
14	**aick**	Smoothing term for ICK	1e-3	(0:10]	1e-3		
15	**tr**	Storage time for inverse operation	0	[0:inf)	0	s	
16	**vcbar**	BC barrier voltage	0	[0:1]	0	V	
17	**icbar**	Current normalization parameter	0	[0:1]	0	A	M
18	**acbar**	Smoothing parameter for bias dependence of barrier voltage	0.01	(0:10]	0.1		

3.11 Parasitic isolation capacitances

The version 2.1 names *CEOX* and *CCOX* has been phased out and replaced by the names below.

no	name	description	default	range	test	unit	factor
1	**cbepar**	total parasitic BE capacitance (spacer and metal component)	0.0	[0:inf)	0.6E-15	F	M

no	name	description	default	range	test	unit	factor
2	**fbepar**	partitioining factor of parasitic BE cap (default is v2.1 compatible)	1.0	[0:1]	0.5	-	
3	**cbcpar**	total parasitic BC capacitance (trench and metal component)	0.0	[0:inf)	2.97e-15	F	M
4	**fbcpar**	partitioining factor of parasitic BC cap (default is v2.1 compatible)	0.0	[0:1]	0.5	-	

3.12 Vertical non-quasi-static effects

no	name	description	default	range	test	unit	factor
1	**alqf**	Factor for additional delay time of minority charge	0.167	[0:1]	0.225	-	
2	**alit**	Factor for additional delay time of transfer current	0.333	[0:1]	0.45	-	
3	**flnqs**	flag for turning on (1) or off (0) vertical NQS effects	0	[0/1]	1	-	

3.13 Noise

no	name	description	default	range	test	unit	factor
1	**kf**	Flicker noise coefficient (no unit only for AF=2)	0	[0:inf)	1.43e-8	-	M^{1-AF}
2	**af**	Flicker noise exponent factor	2	(0:10]	2	-	
3	**cfbe**	flag for determining where to tag the flicker noise source	-1	[-2/-1]	-2		
4	**kfre**	Emitter resistance flicker noise coefficient (no unit only for AFRE=2)	0	[0:inf)	0	-	M^{1-AF}
5	**afre**	Emitter resistance flicker noise exponent factor	2	(0:10]	2	-	

no	name	description	default	range	test	unit	factor
6	**flcono**	Flag for turning correlated noise on/off	0	[0:1]	1		

3.14 Lateral geometry scaling (at high current densities)

no	name	description	default	range	test	unit	factor
1	**latb**	Scaling factor for collector minority charge in direction of emitter width b_E	0	[0:inf)	3.765	-	
2	**latl**	Scaling factor for collector minority charge in direction of emitter length l_E	0	[0:inf)	0.342	-	

3.15 Temperature dependence

The parameter *ALB* (version 2.1) has been deleted; cf. release notes for version 2.2. Note that *f1vg* and *f2vg* are not HICUM specific, but can be made general parameters in a simulator.

no	name	description	default	range	test	unit	factor
1	**vgb**	Bandgap voltage V_{gBeff} extrapolated to 0K	1.17	(0:10]	1.17	V	
2	**f1vg**	coefficient K_1 in T dependent bandgap equation	-1.023 77E-4		-1.023 77E-4	V/K	
3	**f2vg**	coefficient K_2 in T dependent bandgap equation	4.32 15E-4		4.32 15E-4	V/K	
4	**zetact**	exponent coefficient in transfer current temperature dependence	3.0	[-10:10]	3.5	-	
5	**vge**	effective emitter bandgap voltage V_{gEeff}	VGB	(0:10]	1.07	V	
6	**zetabet**	exponent coefficient in BE junction current temperature dependence	3.5	[-10:10]	4	-	
7	**vgc**	eff. collector bandgap voltage V_{gCeff}	VGB	(0:10]	1.14	V	

no	name	description	default	range	test	unit	factor
8	**vgs**	eff. substrate bandgap voltage V_{gSeff}	VGB	(0:10]	1.17	V	
9	**dvgbe**	bandgap difference between neutral base and BE SCR (for hjEi0 and hf0)	0	[-10:10]	0	V	
10	**zetahjei**	temperature coefficient for a_{hjEi}	1	[-10:10]	1		
11	**zetavgbe**	temperature coefficient for h_{jEi0}	1	[-10:10]	1		
12	**alt0**	First-order relative temperature coefficient of parameter t0	0		0	1/K	
13	**kt0**	Second-order relative temperature coefficient of parameter t0	0		0	$1/K^2$	
14	**zetaci**	Temperature exponent for rci0	0	[-10:10]	1.6	-	
15	**alvs**	Relative temperature coefficient of saturation drift velocity	0		1e-3	1/K	
16a 16b	**alces** **aldck**	Relative TC of vces Relative TC of vdck	0 0		0.4e-3 0	1/K 1/K	
17	**zetarbi**	Temperature exponent of internal base resistance	0	[-10:10]	0.588	-	
18	**zetarbx**	Temperature exponent of external base resistance	0	[-10:10]	0.206	-	
19	**zetarcx**	Temperature exponent of external collector resistance	0	[-10:10]	0.223	-	
20	**zetare**	Temperature exponent of emitter resistance	0	[-10:10]	0	-	
21	**zetarth**	Temperature exponent of the thermal resistance	0	[-10:10]	0	-	
22	**alrth**	First-order relative temperature coefficient of parameter Rth	0	[0:1]	0	1/K	
23	**zetacx**	Temperature exponent of the mobility in substrate transistor transit time	1.0	[-10:10]	2.2	-	
24	**alfav**	Relative temperature coefficient for favl	0		8.25e-5	1/K	

no	name	description	default	range	test	unit	factor
25	**alqav**	Relative temperature coefficient for qavl	0		1.96e-4	1/K	
26	**alkav**	Relative temperature coefficient for kavl	0		0.004	1/K	
27	**alb**	Relative temperature coefficient of forward current gain	0		6e-3		

3.16 Self-Heating

no	name	description	default	range	test	unit	factor
1	**rth**	Thermal resistance	0	[0:inf)	0.0	K/W	1/M
2	**cth**	Thermal capacitance	0	[0:inf)	0.0	Ws/K	M
3	**flsh**	flag for turning on (1 = main currents, 2 = all currents) or off (0) self-heating effects	0	[0/1/2]	1	-	M

3.17 Circuit simulator specific parameters

The parameters *TNOM* and *DT* are available in most simulators and are also mostly named the same. The “model version identifier” enables version control in simulators with different HICUM generations.

The parameter *flcomp* enables backward compatibility of the model. The flag is supposed to be used for production model cards to maintain model results independent of new features in the model (for simulators without a dedicated version management system). By assigning a specific version number to *flcomp* (in the form “2.xx”) the equations of the corresponding version are used and its terminal behavior is recovered. Note that in the case of *flcomp* < “*latest version”* those features that have been added since version *flcomp* are turned off. During parameter extraction, setting *flcomp* = “*actual version”* is suggested to avoid unexpected results.

no	name	description	default	unit
1	**tnom**	temperature at which parameters are specified	27	°C
2	**dt**	temperature change w.r.t. chip temperature for particular transistor	0	°C
3	**flcomp**	compatibility flag and model version identifier	0	-
4	**type**	For transistor type NPN(+1) or PNP (-1)	1	

The Table below contains the syntax for calling HICUM in various circuit simulators (listed in alphabetical order).

Table 4.0.0/1:

simulator name	call
ADS	HICUM
ELDO	Level = 9
HSPICE	Level = 8

Table 4.0.0/1:

SPECTRE	bht
APLAC	HICUM
AnalogOffice	HICUM_L2 (npn) , HICUM_L2_P (pnp)
Silvaco SPICE	Level = 6
NEXXIM	HICUM
Smart-SPICE	libHICUM
GoldenGate	HICUM

4 Operating Point Information from Circuit Simulators

Below is a list of those variables that circuit simulators are supposed to provide to the model user as “operating point information”. The voltages in the expressions are defined as follows:

$$V_{BEi} = V_{B'} - V_{E'}$$
$$V_{BEx} = V_{B*} - V_{E'}$$
$$V_{BCi} = V_{B'} - V_{C'}$$
$$V_{BCx} = V_{B*} - V_{C'}$$
$$V_{SCi} = V_{S'} - V_{C'}$$

Table 5:

Variable	Unit	Description	Definition
IB	A	Base terminal current	as calculated in the model
IC	A	Collector terminal current	as calculated in the model
IS	A	Substrate terminal current	as calculated in the model
IAVL	A	Avalanche current	as calculated in the model
VBE	V	External *BE* voltage	as calculated in the model
VBC	V	External *BC* voltage	as calculated in the model
VCE	V	External *CE* voltage	as calculated in the model
VSC	V	External *SC* voltage	as calculated in the model
BETADC		Common emitter forward current gain	$\beta_{dc} = \frac{I_C}{I_B}$
GMi	A/V	Internal transconductance (same definition as for SGPM)	$g_{mi} = \left.\frac{\partial I_T}{\partial V_{BEi}}\right\|_{V_{CEi}} = \left.\frac{\partial I_T}{\partial V_{BEi}}\right\|_{V_{BCi}} + \left.\frac{\partial I_T}{\partial V_{BCi}}\right\|_{V_{BEi}}$
GMS	A/V	Transconductance of the parasitic substrate PNP	$g_{ms} = \left.\frac{\partial I_{TS}}{\partial V_{BCx}}\right\|_{V_{SCi}} - \left.\frac{\partial I_{TS}}{\partial V_{SCi}}\right\|_{V_{BCx}}$
RPIi	Ω	Internal base-emitter (input) resistance	$\frac{1}{r_{\pi i}} = \left.\frac{\partial I_{BEi}}{\partial V_{BEi}}\right\|_{V_{BCi}}$

Table 5:

Variable	Unit	Description	Definition
RPIx	Ω	External base-emitter (input) resistance	$\frac{1}{r_{\pi x}} = \left.\frac{\partial I_{BEp}}{\partial V_{BEx}}\right\|_{V_{BCx}} - \left.\frac{\partial I_{BEt}}{\partial V_{BEx}}\right\|_{V_{BCx}}$ (second term is due to tunnelling current)
RMUi	Ω	Internal feedback resistance	$\frac{1}{r_{\mu i}} = \left.\frac{\partial I_{BCi}}{\partial V_{BCi}}\right\|_{V_{BEx}} - \left.\frac{\partial I_{AVL}}{\partial V_{BCi}}\right\|_{V_{BEi}}$ (second term is due to avalanche current)
RMUx	Ω	External feedback resistance	$\frac{1}{r_{\mu x}} = \left.\frac{\partial I_{BCx}}{\partial V_{BCx}}\right\|_{V_{BEx}}$
ROi	Ω	Internal output resistance	$\frac{1}{r_o} = -\left.\frac{\partial I_T}{\partial V_{BCi}}\right\|_{V_{BEi}} + \left.\frac{\partial I_{AVL}}{\partial V_{BCi}}\right\|_{V_{BEi}}$
CPIi	F	Total internal *BE* capacitance	$C_{\pi i} = C_{jEi} + C_{dE}$
CPIx	F	Total external *BE* capacitance	$C_{\pi x} = C_{jEp} + C_{BEpar}$
CMUi	F	Total internal *BC* capacitance	$C_{\mu i} = C_{jCi} + C_{dC}$
CMUx	F	Total external *BC* capacitance	$C_{\mu x} = C_{jCx} + C_{BCpar} + C_{dS}$
CCS	F	*CS* junction capacitance	C_{jS}
RBI	Ω	Internal base resistance	as calculated in the model
RB	Ω	Total base resistance	as calculated in the model (R_{BI} + $R_{BX}(T)$)
RCX_T	Ω	External (saturated) collector series resistance	Temperature dependent operating point $R_{CX}(T)$
RE_T	Ω	Emitter series resistance	Temperature dependent operating point $R_E(T)$
BETAAC		Small signal current gain	$\beta_{ac} = g_{mi} \cdot (r_{\pi i} r_{\pi x})/(r_{\pi i} + r_{\pi x})$
CRBI	F	Shunt capacitance across R_{BI}	as calculated in the model

Table 5:

Variable	Unit	Description	Definition
TF	s	Forward transit time	as calculated in the model
FT	Hz	Transit frequency (Note this is an approximation)	$f_T = \frac{g_{mi}}{2\pi \cdot (C_{BE} + C_{BC} + r \cdot C_{BC} \cdot g_{mi})}$, $C_{BE} = C_{\pi i} + C_{\pi x}$, $C_{BC} = C_{\mu i} + C_{\mu x}$, $r = R_{Cx} + R_E + \frac{R_B + R_E}{\beta_{ac}}$
TK	K	Absolute device temperature including self-heating	
DTSH	K	Increase of device temperature with respect to ambient temperature due to self-heating	

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