7 Experimental Results

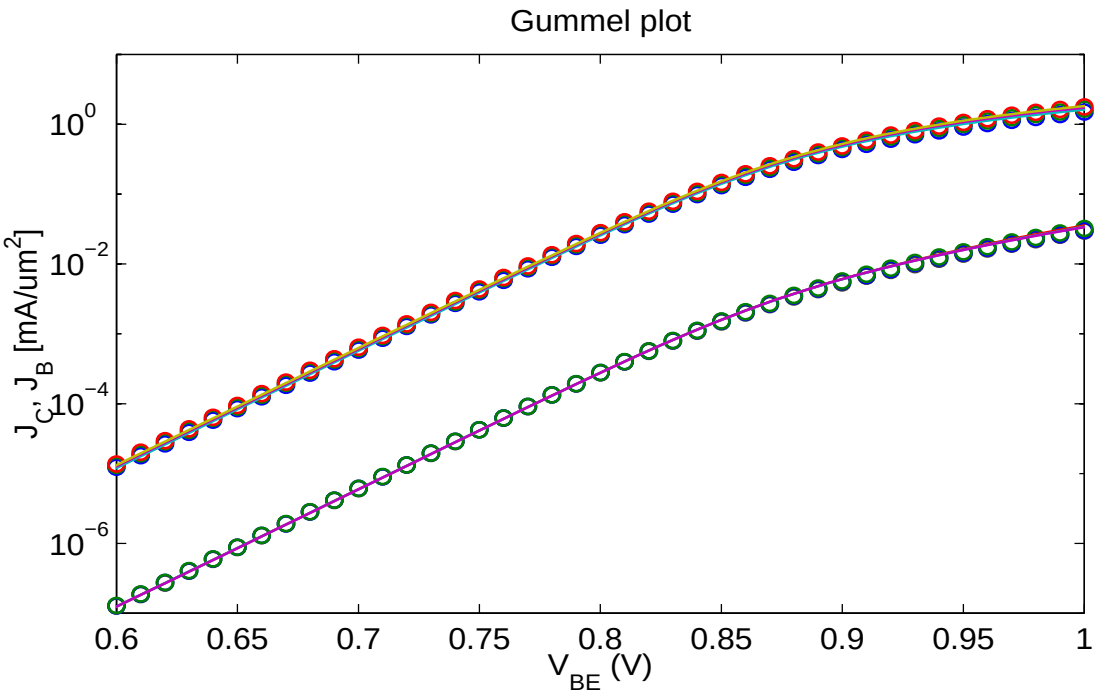
This chapter contains selected examples that demonstrate HICUM's capabilities of modeling bias, frequency, geometry and temperature dependent transistor behaviour. If not specified otherwise, all results were obtained using a *scaleable single basic parameter set* (cf. chapter 4 and 5). The results cover not only a large variety of processes, ranging from low-speed (6 GHz) to high-speed (50 GHz SiGe) processes and even an example for a vertical pnp, but also various modes of operation (d.c. small-signal, large-signal). The major emphasis is on high-frequency (h.f.) characteristics and figures of merit that are related to h.f. (circuit) applications. Considering the above mentioned variables (bias, geometry, temperature, frequency), model verification is becoming a quite difficult task, the effort of which is often severely underestimated.

Wherever possible, the following comparisons are performed in normalized form and in variables that are related to circuit design; for instance, often the current density I_C/A_E is employed (to allow process comparisons), and the bias points are defined by (I_C/A_E,V_{CE}) . The results do not contain examples for junction capacitance modeling, which has already been shown to be accurate. The experimental results given below cover the following areas:

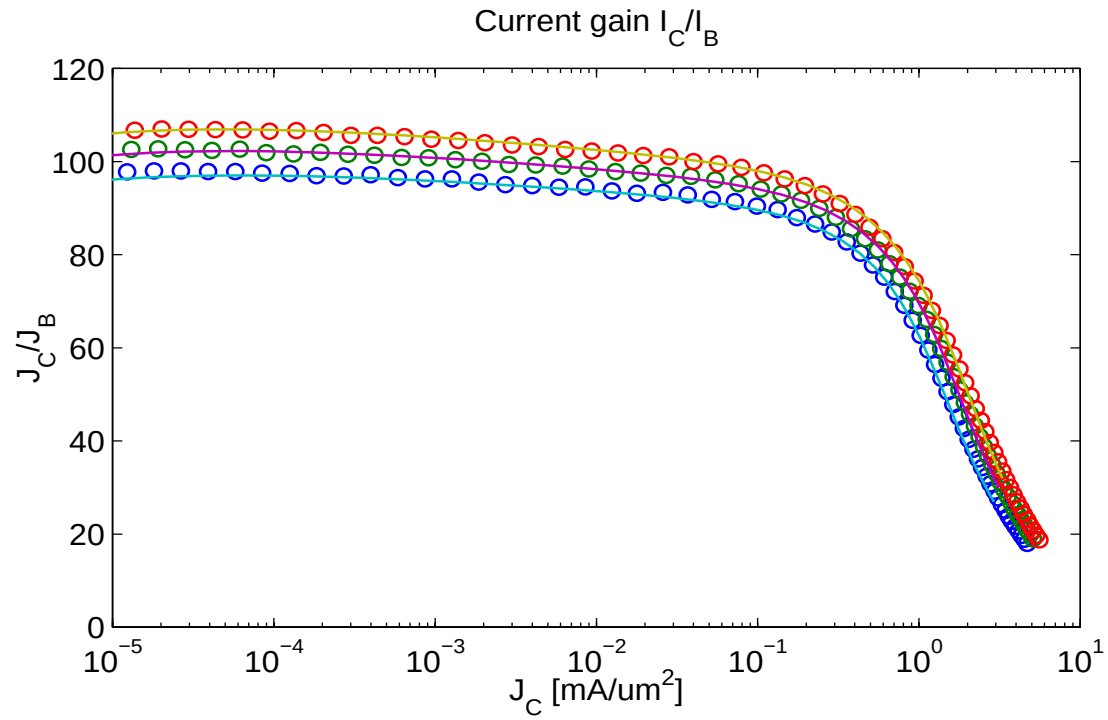
- d.c. characteristics including I-V and current gain curves as well as conductances vs. bias.
- Bias dependence of transit time τ_f and transit frequency f_T. An accurate approximation of the transit time and the junction capacitances, which are a fundamental (linearly independent) variables in HICUM, guarantee an accurate modeling of composite parameters, such as f_T and y-parameters.
- For small-signal characteristics, y-parameters are preferred, since they can be easier linked directly to elements in the transistor equivalent circuit (e.g. [15,29,41]). The examples contain comparsions of all four y-parameters vs. frequency, bias, and geometry.
- High-speed switching is difficult to measure directly and accurately for today's fast transsitors; therefore, HICUM was verified by 2D and 3D mixed-mode device/circuit simulation [42]. For older (slower) processes, however, HICUM could be verified experimentally [26,34].
- Temperature dependent modeling has been pursued and compared to experimental data for several process generations (e.g. [34,35,46]), leading to reliable model formulations.
- Noise: both 1/f and high-frequency noise have been investigated as a function of bias, frequency and geometry (cf. [3,4,5,53]) and have been compared to measurements.
- Non-linear h.f. distortion can be considered as another way to verify a model's large-signal behavior. In the presented examples, the output power P_{out} as response to a single-tone input power P_{in} is compared to measurements over frequency, bias and geometry for different types of transistors.
- Predictive and statistical modeling capability is important for reducing design cycle time, but have not been included for bipolar applications in commercial simulators and design tools in a physics-based and generic way. The given examples show f_T as one of several useful figures of merit (FoM) for high frequency applicatios; compared to other h.f. FoMs, f_T is clearly defined and can most easily be measured, although its measurement time is still not suitable for statistical data acquisition.
- Circuit results have been included for a CML ring-oscillator as standard benchmark circuit for for digital applications. Sufficiently simple benchmark circuits for wireless applications are more difficult to obtain.

7.1 d.c. characteristics

(a)



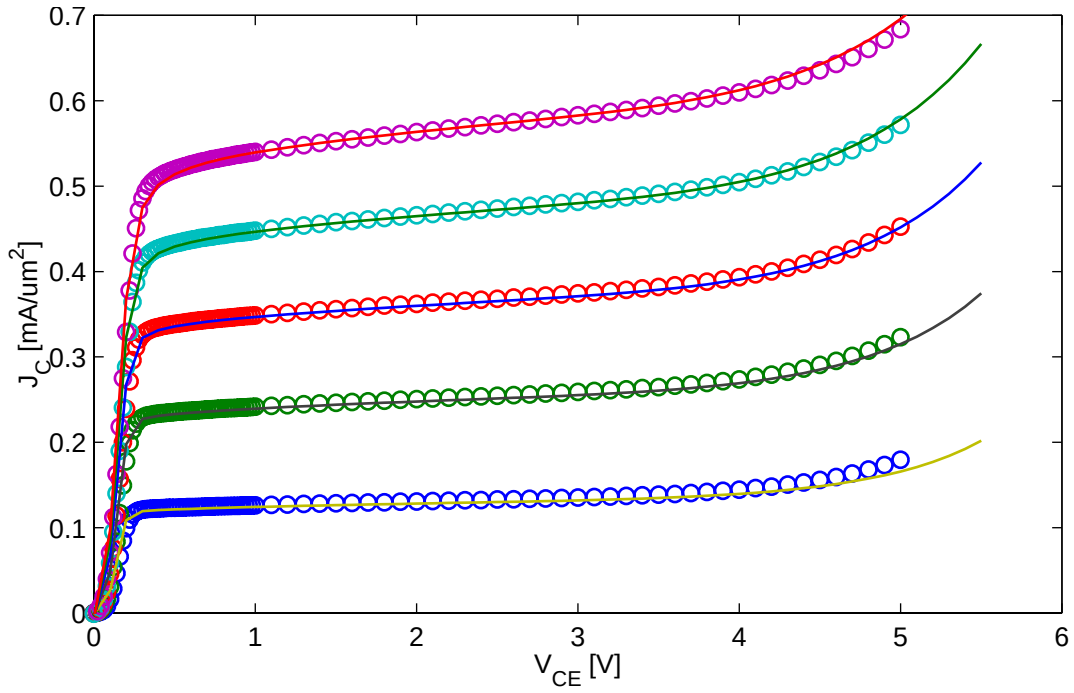
(b)



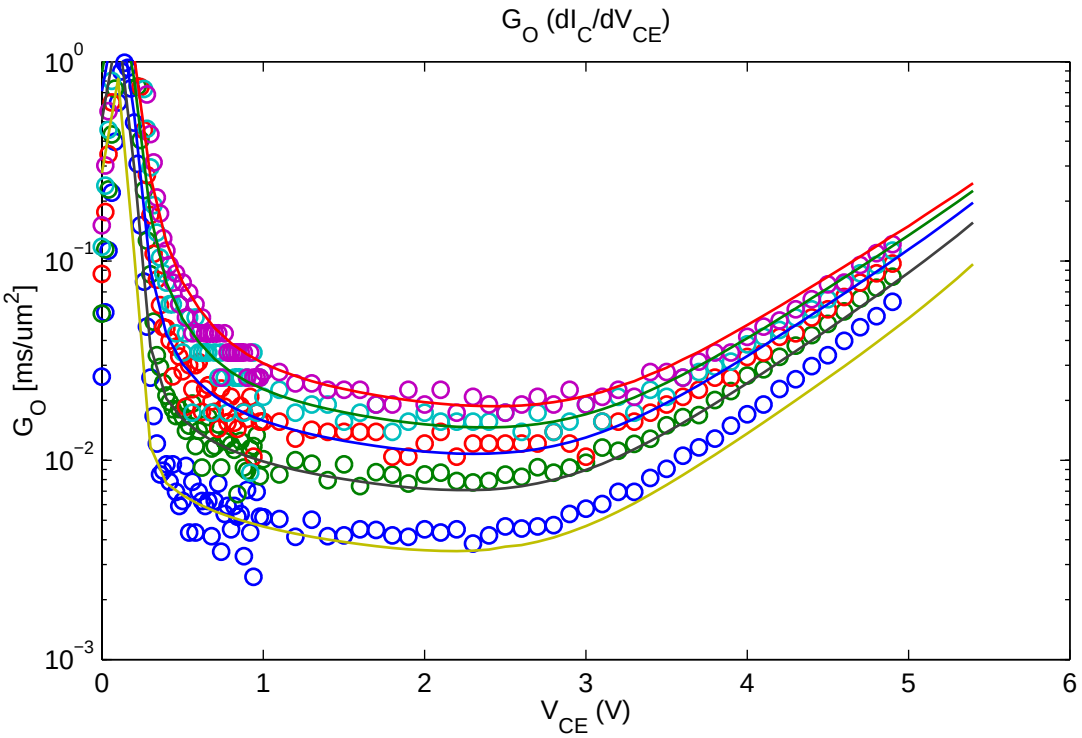
Comparison between measurement (symbols) and HICUM (solid lines) from a single transistor extraction for a 12 GHz bipolar transistor [2]: (a) Gummel plot; (b) current gain.
V_{BC}/V = 0,-2,-4; emitter size: 0.6*4.8µm^2

contd.: d.c. characteristics

(a)



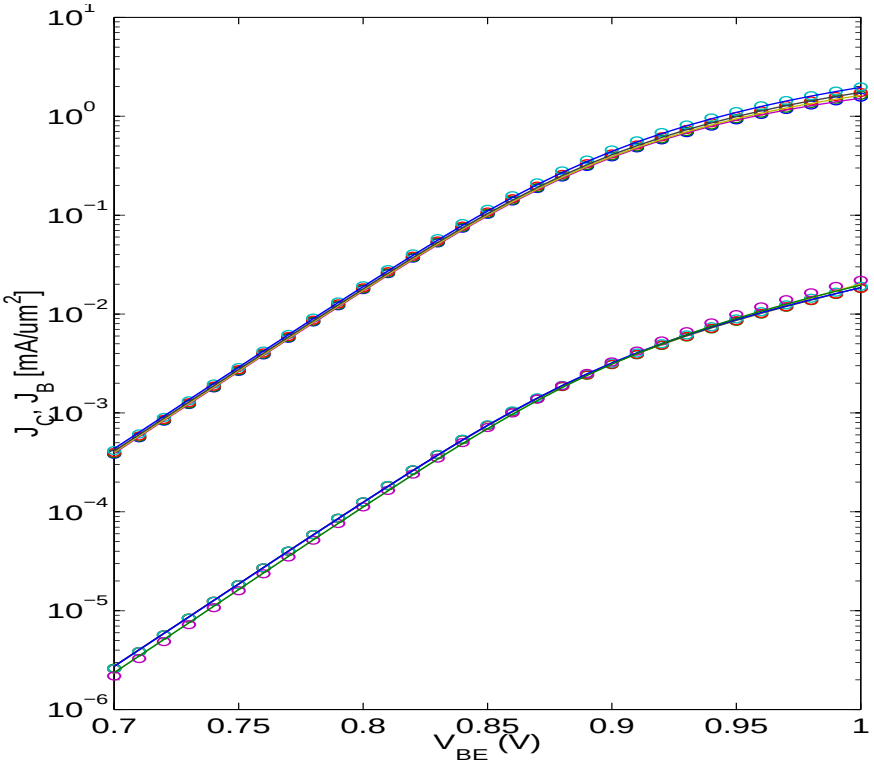
(b)



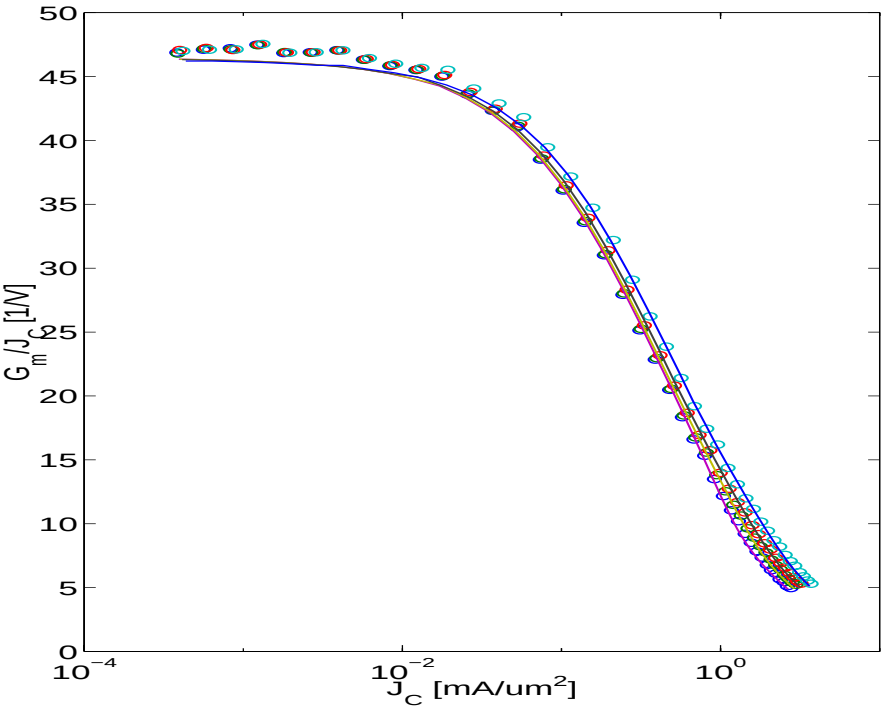
Comparison between measurement (symbols) and HICUM (solid lines) from a single transistor extraction for a 12 GHz bipolar transistor [2]: (a) output characteristics for I_B=const;
(b) output conductance dI_C/dV_{CE}; emitter size: 0.6*4.8µm^2

contd.: d.c. characteristics

(a)



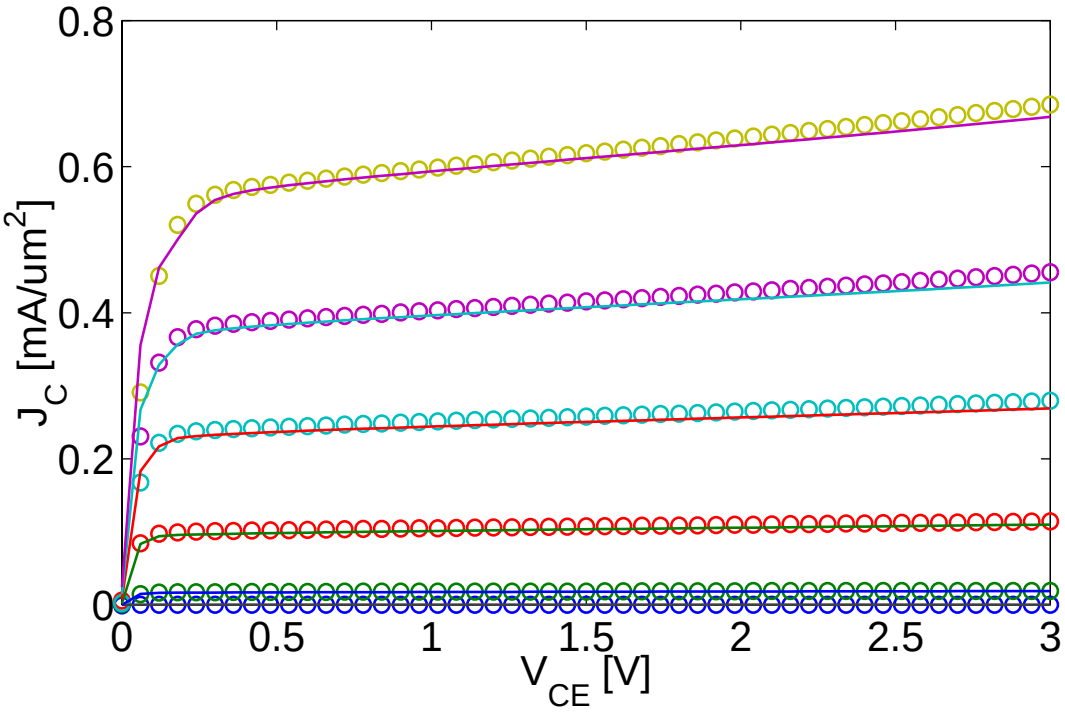
(b)



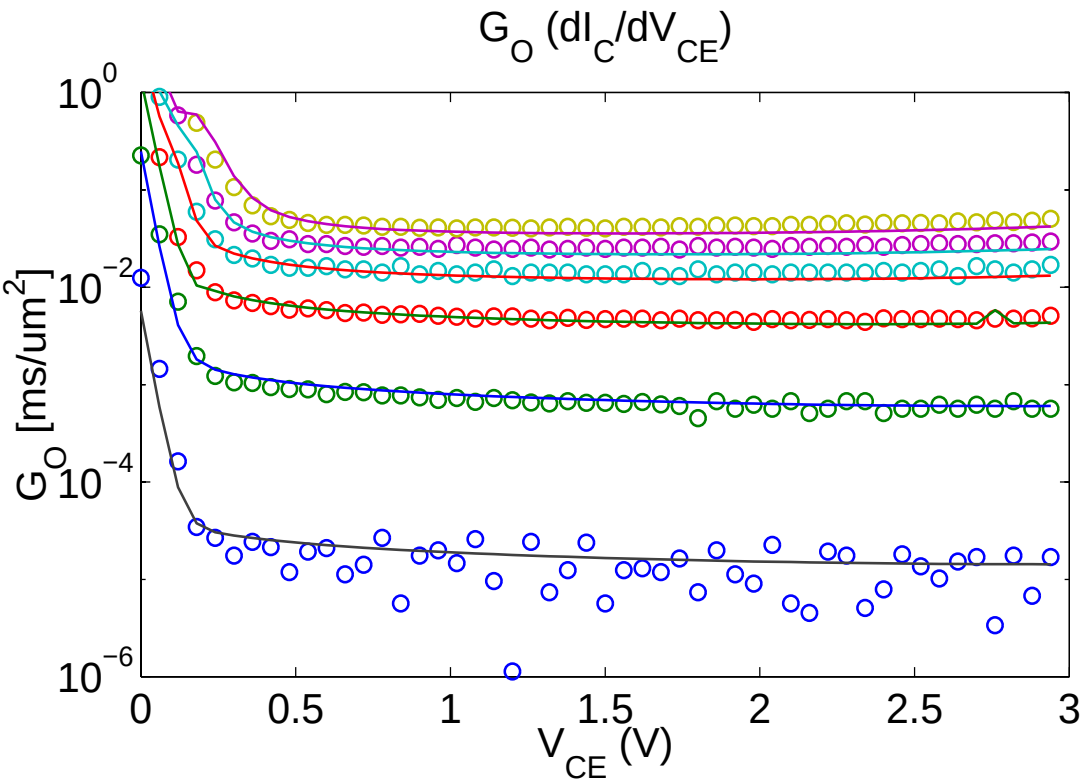
Comparison between measurement (symbols) and HICUM (solid lines) for a 25 GHz bipolar transistor: (a) Gummel plot; (b) normalized transconductance. V_{CE}/V=0.5,0.8,1.5,3; emitter size: 0.4*14µm^2

contd.: d.c. characteristics

(a)



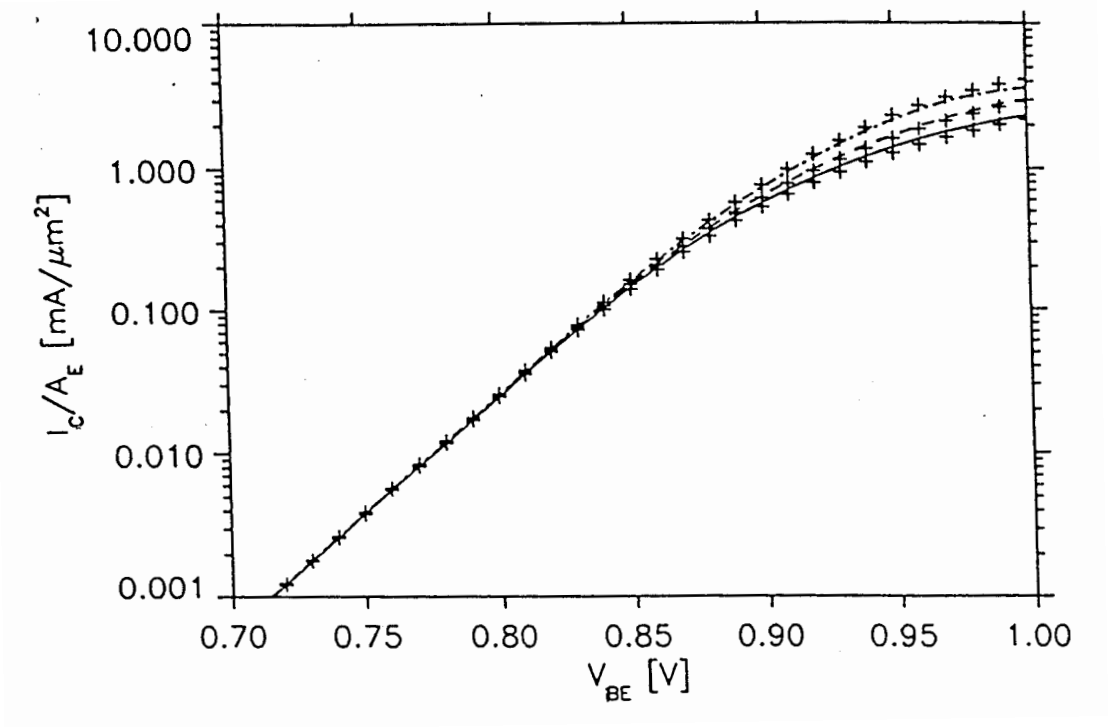
(b)



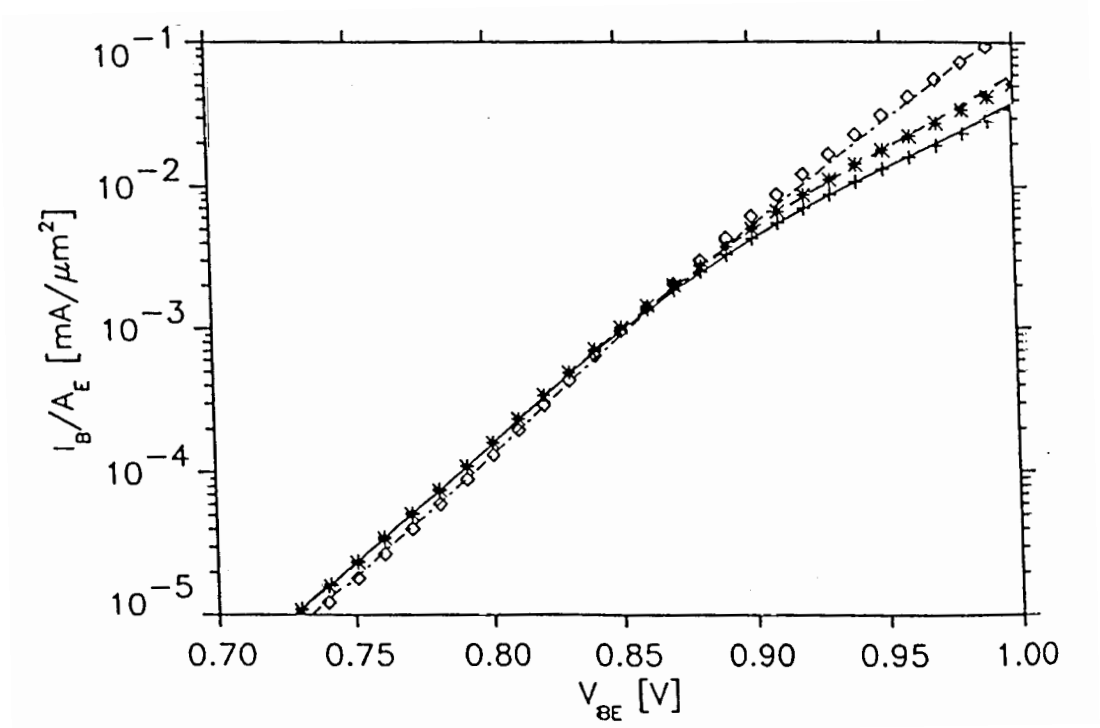
Comparison between measurement (symbols) and HICUM (solid lines) for a 25 GHz bipolar transistor: (a) output characteristics for V_{BE}=const; (b) output conductance dI_C/dV_{CE}; emitter size: 0.4*14µm^2.

contd.: d.c. characteristics

(a)



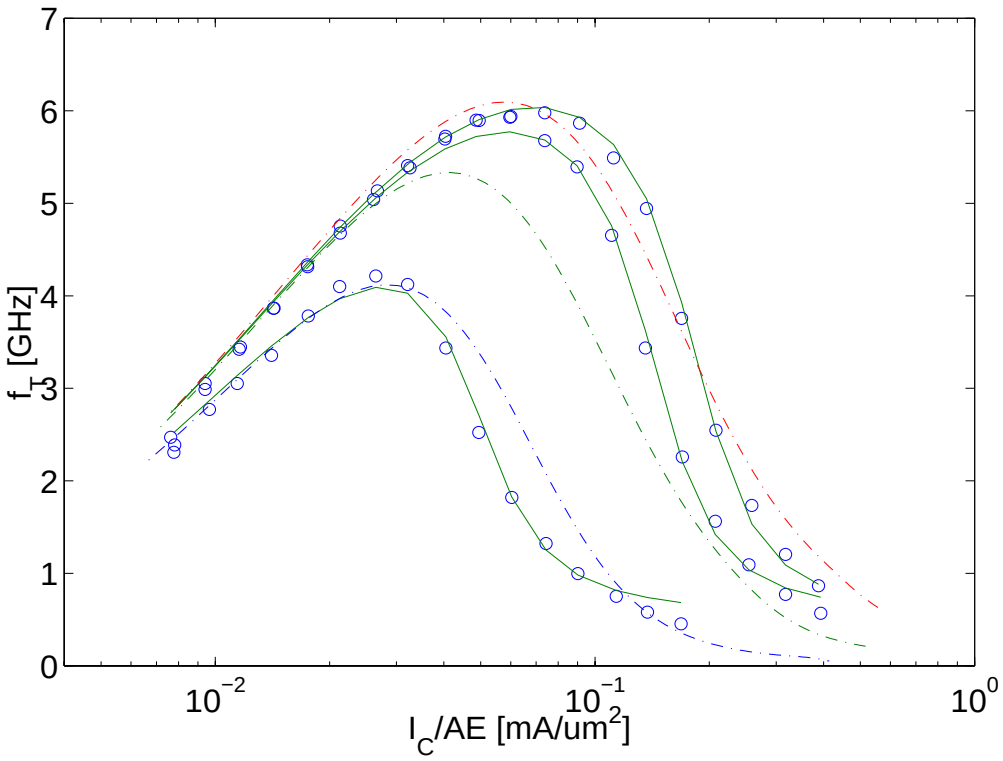
(b)



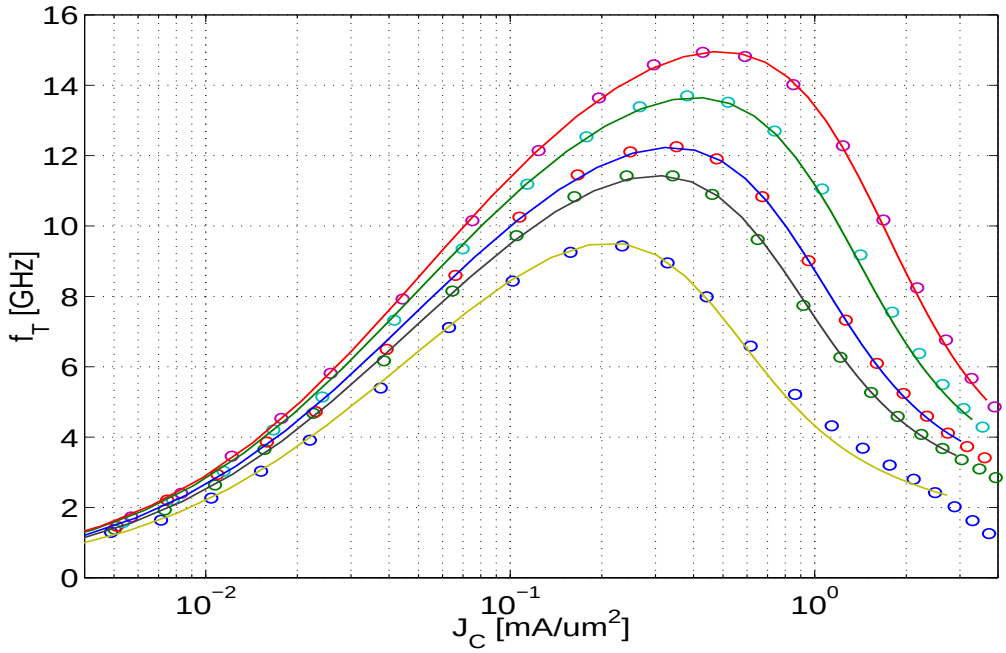
Comparison between measurement (symbols) and HICUM (solid lines) for a 45 GHz IBM SiGe bipolar transistor [51,52]: (a) collector current density; (b) base current density. V_{CE}/V=0.8,1.6,2.4; emitter size: 0.5*10μm^2. Self-heating and avalanche breakdown are quite pronounced for this transistor.

7.2 Transit frequency and transit time

(a)



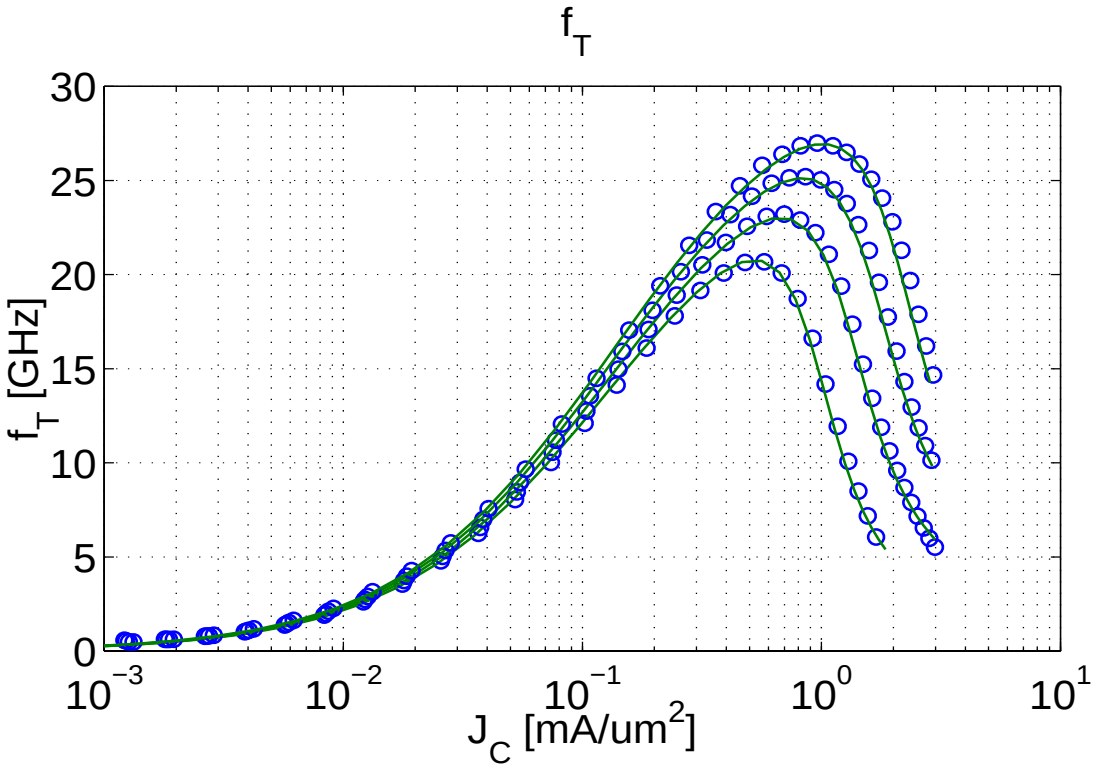
(b)



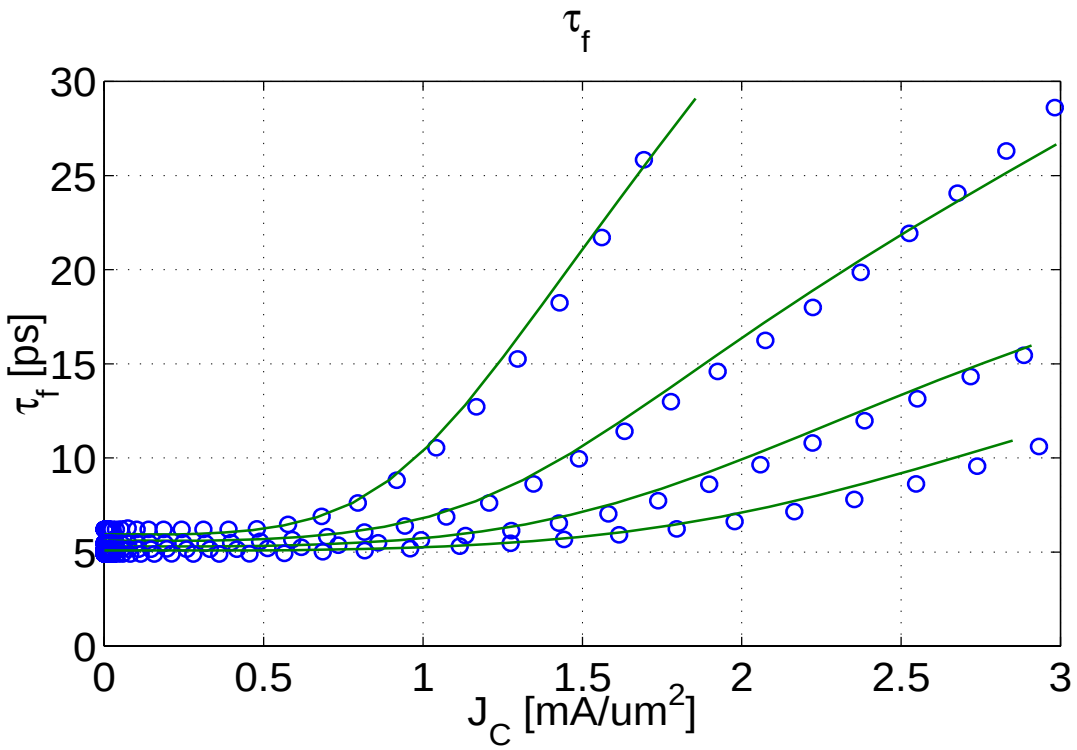
Transit frequency vs. collector current density (V_{BC}=const) for different bipolar processes. Comparison between measurement (symbols) and HICUM (solid lines) from single parameter extraction: (a) emitter size 0.5*10µm^2, V_{BC}/V=0,-5,-10 (the dashed lines are the results of the SPGM) [18,46]; (b) emitter size 0.6*4.8µm^2; V_{BC}/V = 0.5, 0, -0.5, -2,-4 [2,18].

contd.: Transit frequency and transit time

(a)



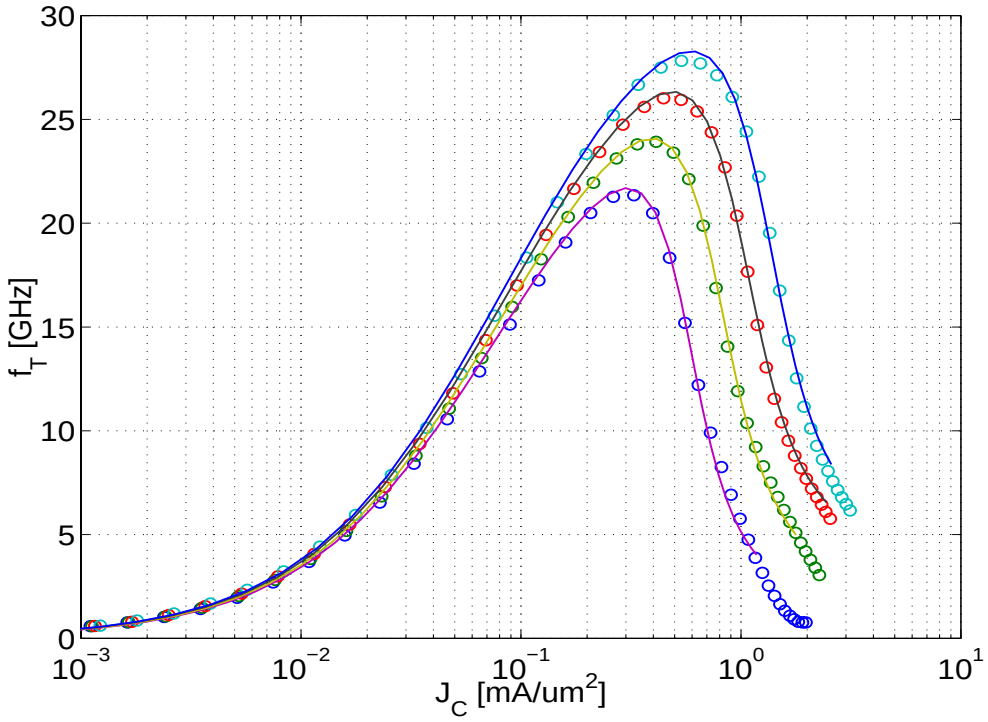
(b)



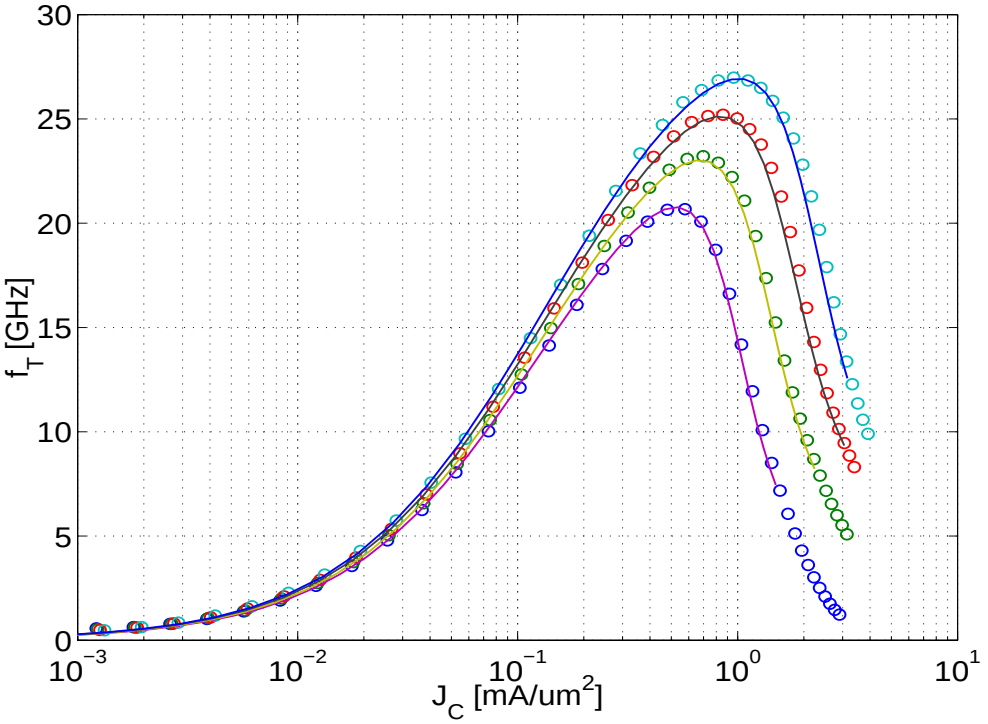
Comparison between measurement (symbols) and HICUM (solid lines) for a 25GHz bipolar process [46]: (a) transit frequency; (b) transit time. Emitter size 0.4*14µm^2, V_{CE}/V=0.5,0.8,1.5,3.

contd.: Transit frequency and transit time

(a)

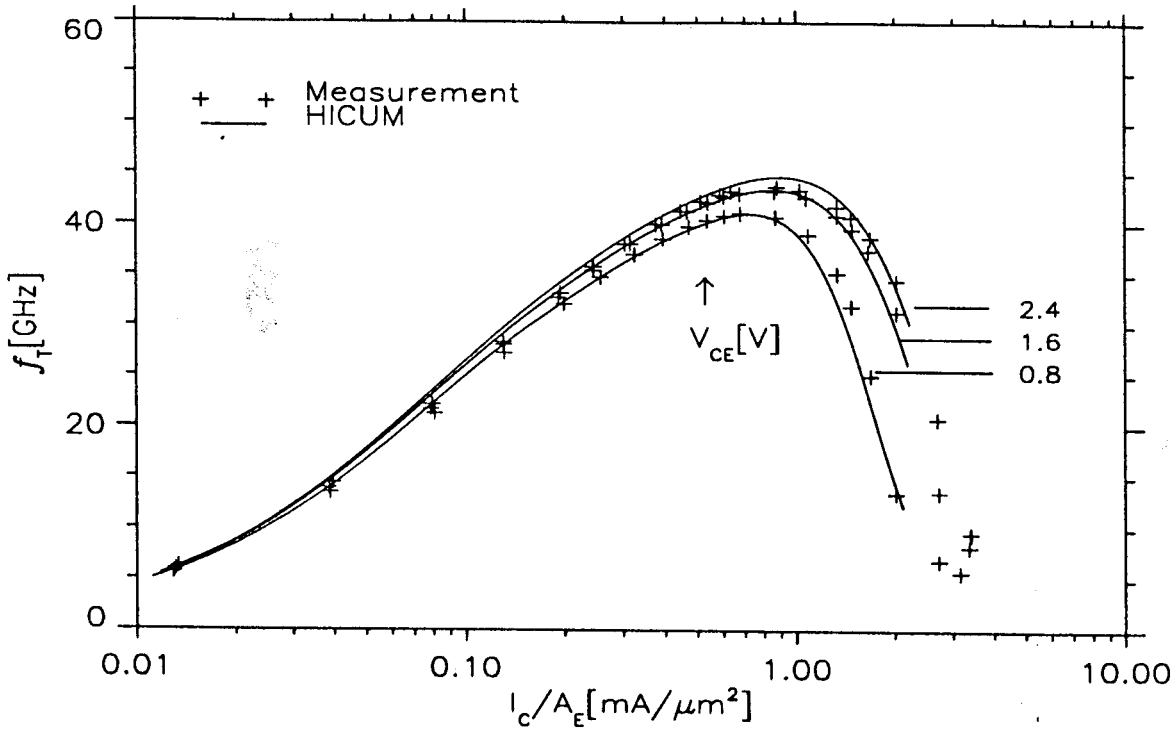


(b)

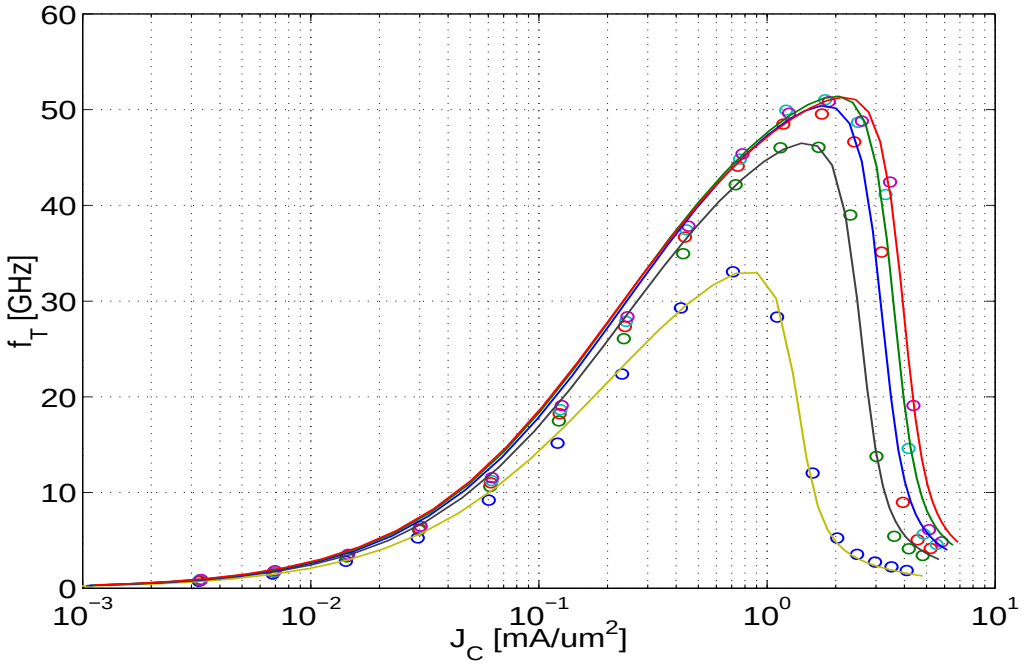


Comparison for the bias dependent transit frequency between measurement (symbols) and HICUM (solid lines) for a 25GHz bipolar process. Transistor size: (a) 1.2*14µm^2; (b) 0.4*1.4µm^2. V_{CE}/V=0.5, 0.8, 1.5, 3.

contd.: Transit frequency and transit time



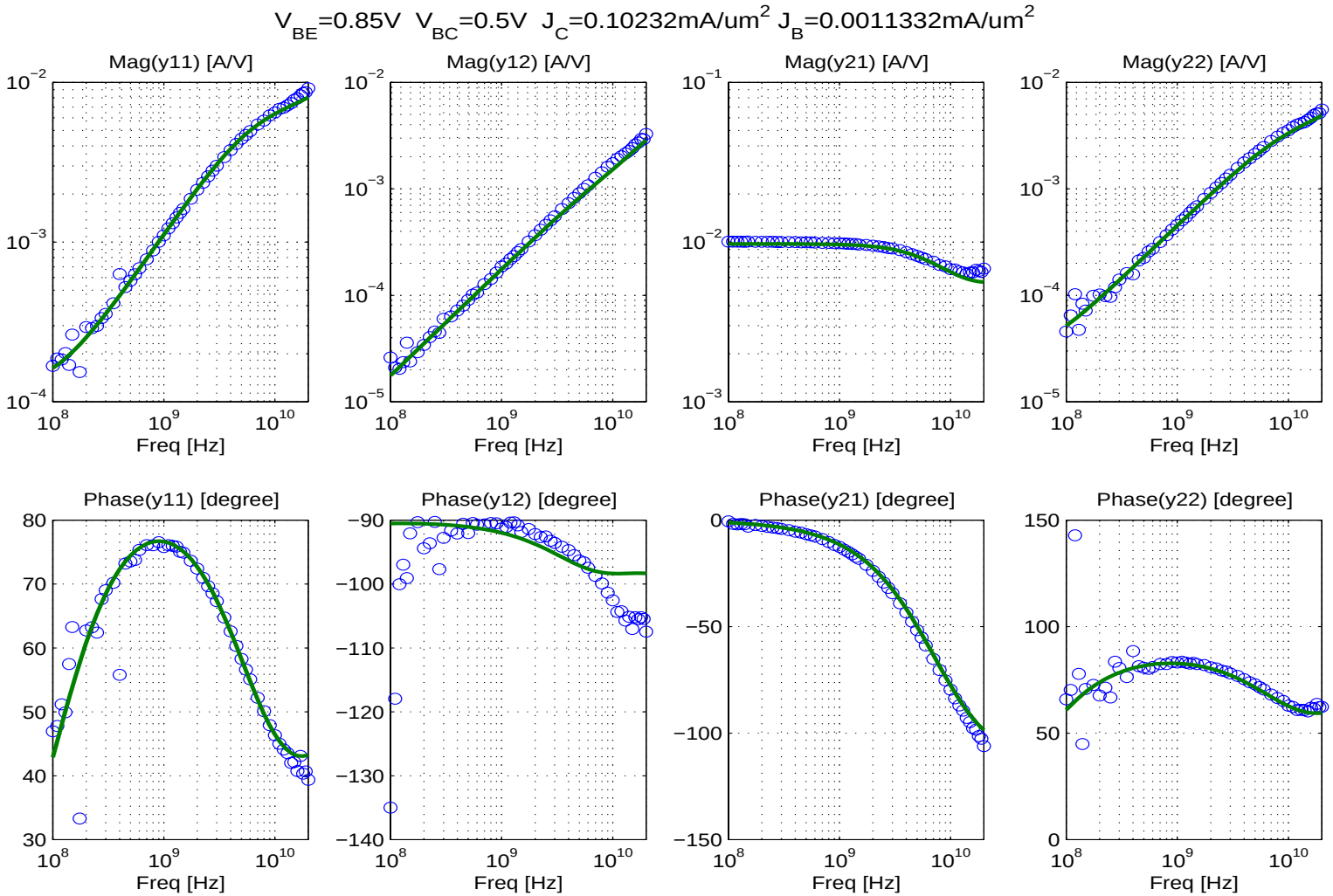
Bias dependent transit frequency of an IBM SiGe bipolar transistor. Comparison between measurement (symbols) and HICUM (solid lines) [52]; emitter size 0.5*10μm^2; V_{CE}/V=0.8,1.6,2.4.



Bias dependent transit frequency of a SiGe bipolar process [2]. Comparison between measurement (symbols) and HICUM (solid lines); emitter size 0.4*2μm^2; V_{BC}/V = 0.5, 0, -0.5, -1, -1.5.

7.3 High-frequency small-signal characteristics

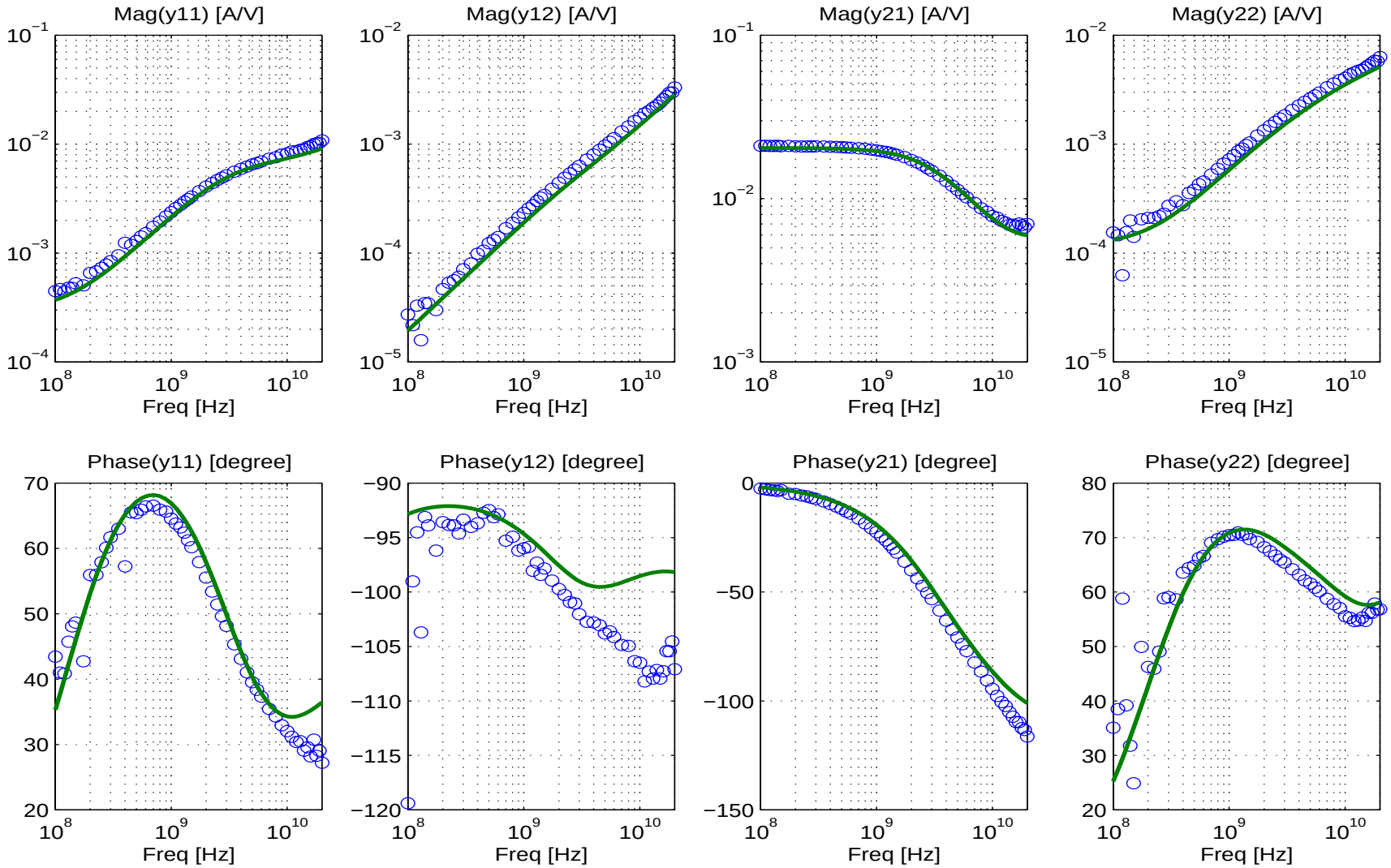
Note: real{y_{12}} is very small and usually of little practical interest, but can cause the modeled phase of y_{12} to deviate from measurements.



Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.1mA/µm^2, V_{BC} = 0.5 V (cf. f_T curves): comparison between measurement (symbols) [2] and HICUM (lines). Single transistor parameter extraction.

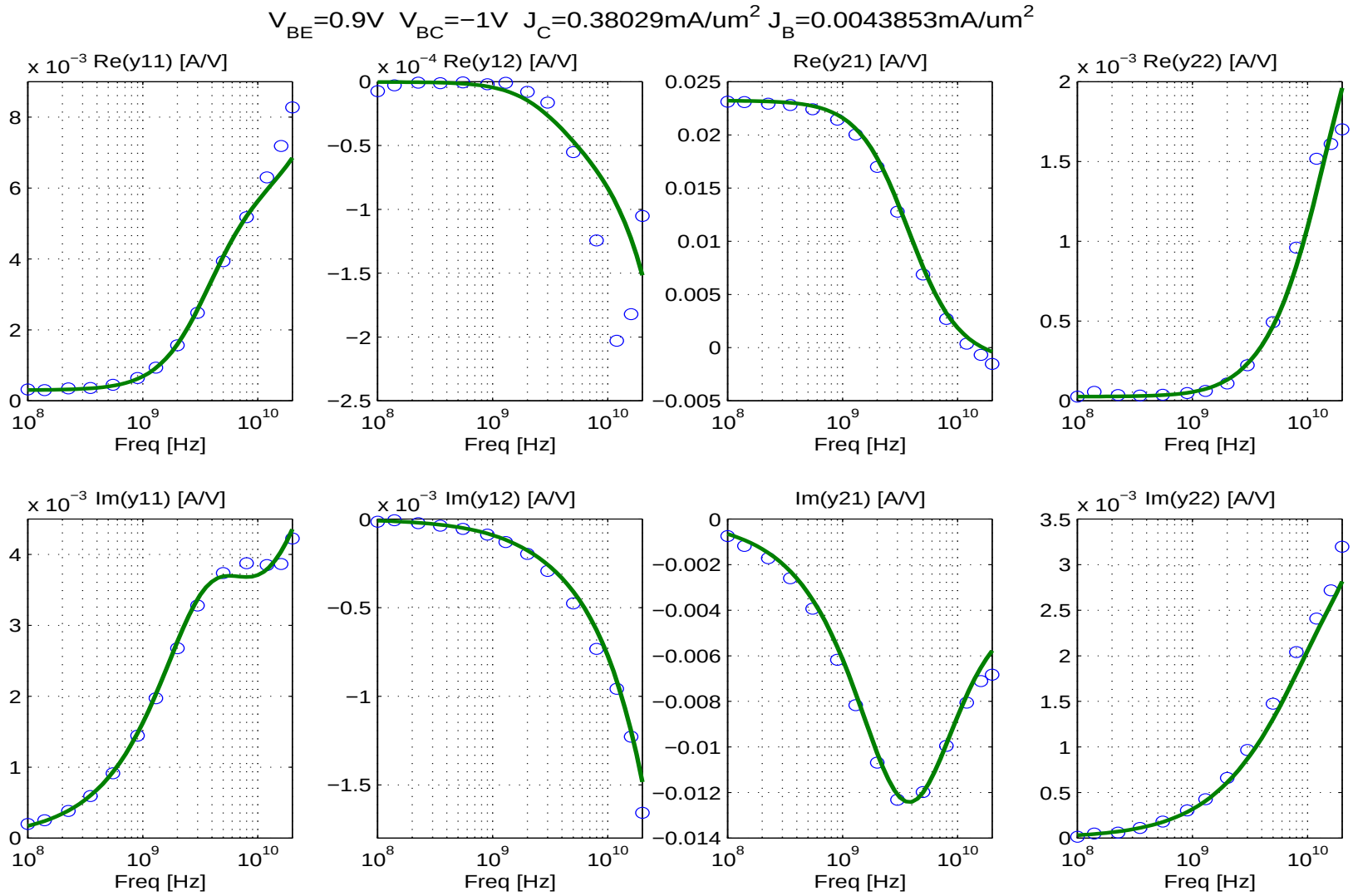
contd.: High-frequency small-signal characteristics

V_{BE}=0.9V V_{BC}=0.5V J_C=0.34382mA/um^2 J_B=0.0042794mA/um^2



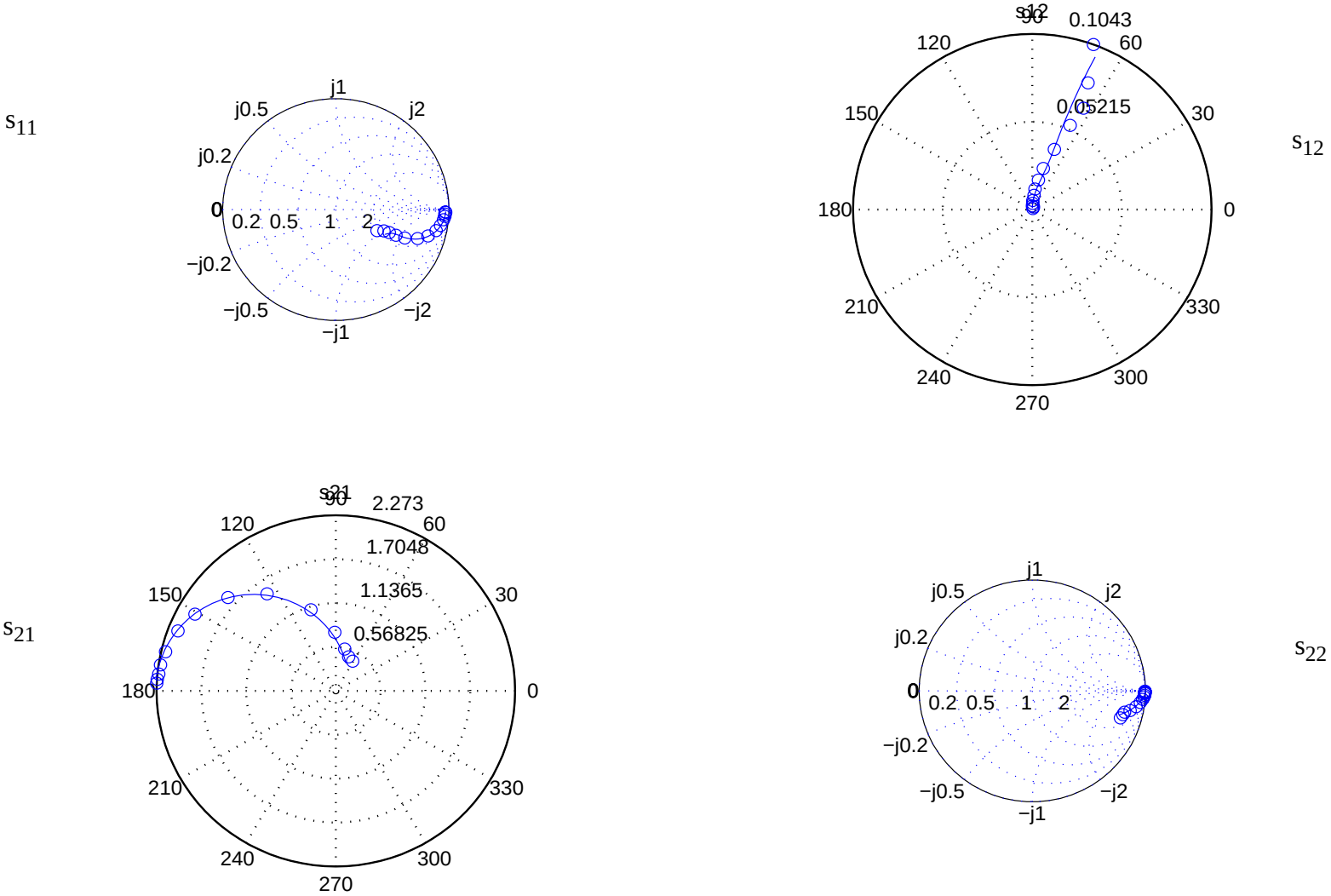
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.34 mA/µm^2, V_{BC} = 0.5 V (cf. f_T curves): comparison between measurement (symbols) [2] and HICUM (lines). Single transistor parameter extraction.

contd.: High-frequency small-signal characteristics



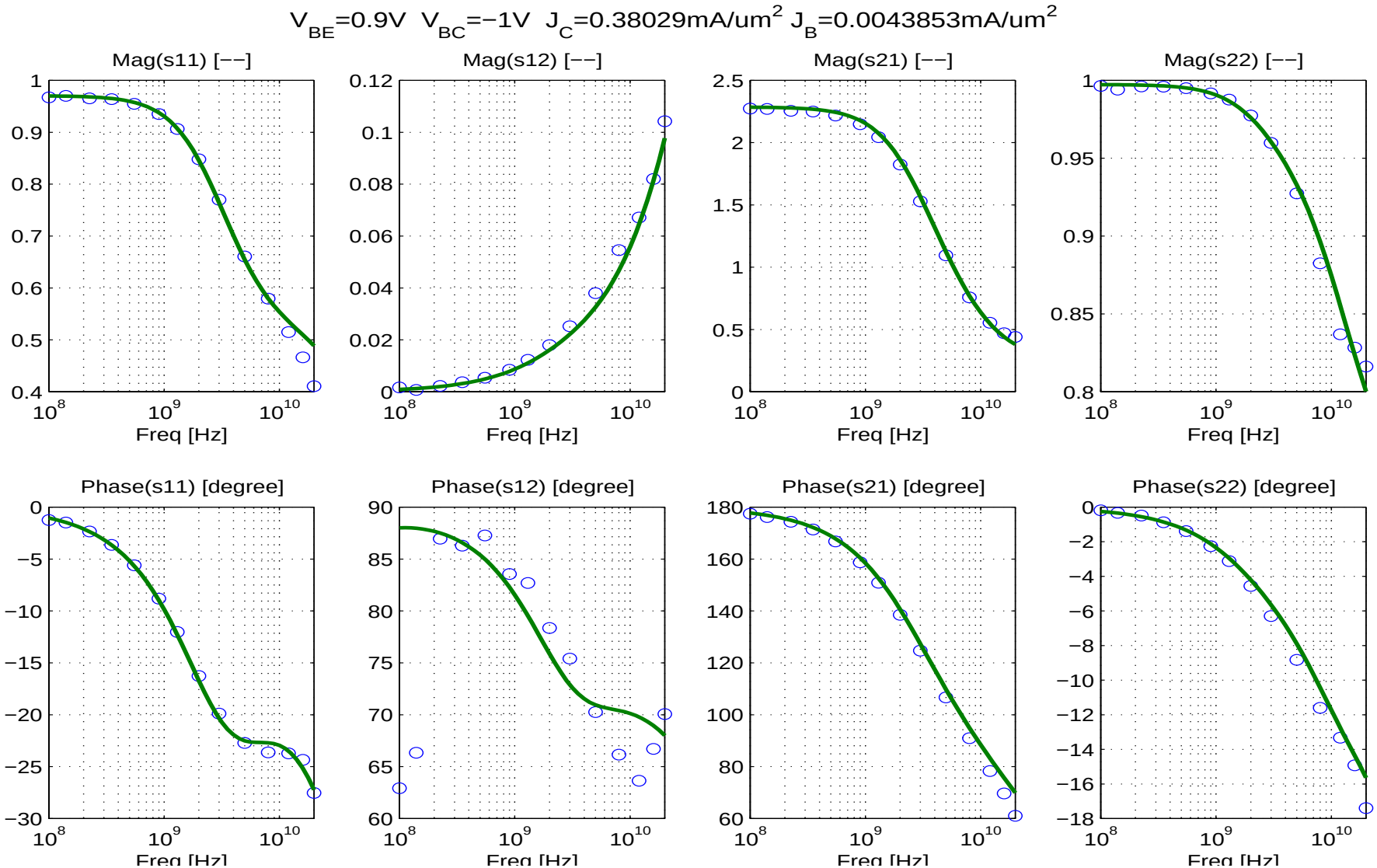
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.38 mA/µm^2, V_{BC} = -1 V (cf. f_T curves): comparison between measurement (symbols) [2] and HICUM (lines). Single transistor parameter extraction.

contd.: High-frequency small-signal characteristics



Frequency dependence of S-parameters (in Smith and polar chart) for a 12 GHz transistor ($0.6*4.8\mu m^2$) at I_C/A_E = 0.38 mA/µm^2, V_{BC} = -1 V (cf. f_T curves): comparison between measurement (symbols) [2] and HICUM (lines). Single transistor parameter extraction.

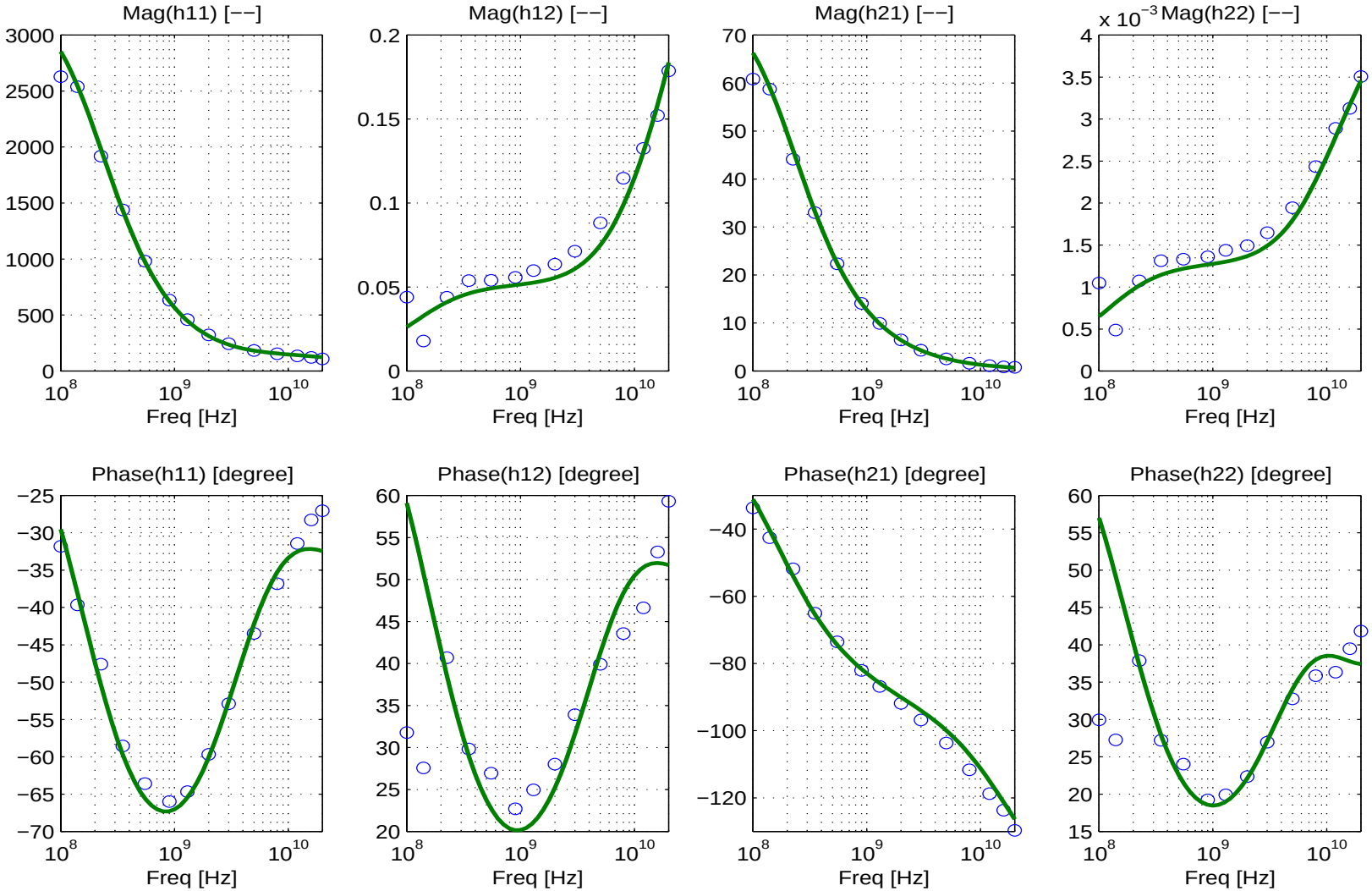
contd.: High-frequency small-signal characteristics



Frequency dependence of S-parameters (in magnitude and phase) for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.38 mA/µm^2, V_{BC} = -1 V (cf. f_T curves): comparison between measurement (symbols) [2] and HICUM (lines). Single transistor parameter extraction.

contd.: High-frequency small-signal characteristics

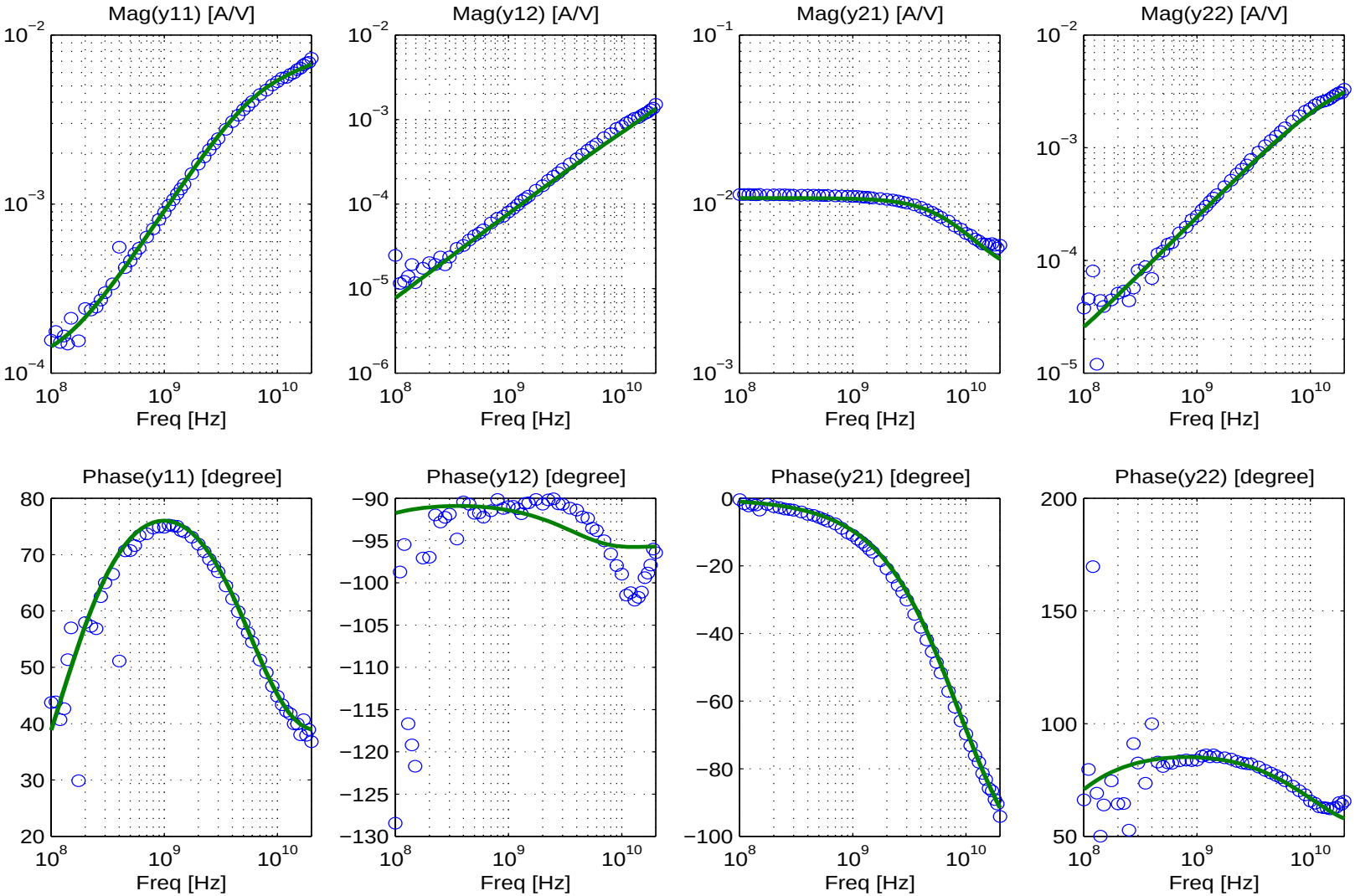
V_{BE}=0.9V V_{BC}=−1V J_C=0.38029mA/um^2 J_B=0.0043853mA/um^2



Frequency dependence of H-parameters for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.38 mA/µm^2, V_{BC} = -1 V (cf. f_T curves): comparison between measurement (symbols) [2] and HICUM (lines). Single transistor parameter extraction.

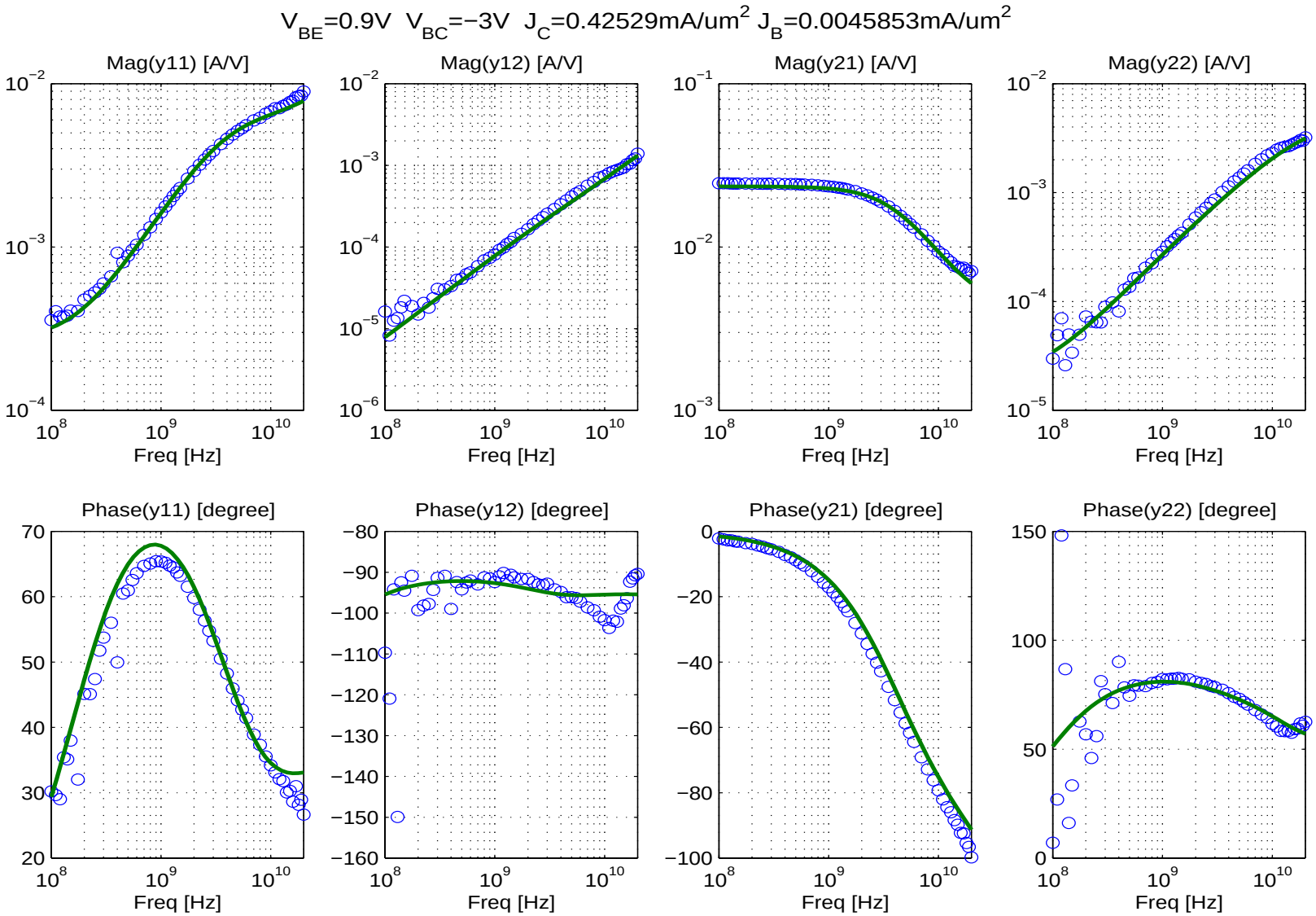
contd.: High-frequency small-signal characteristics

V_{BE}=0.85V V_{BC}=−3V J_C=0.11924mA/um^2 J_B=0.0011321mA/um^2



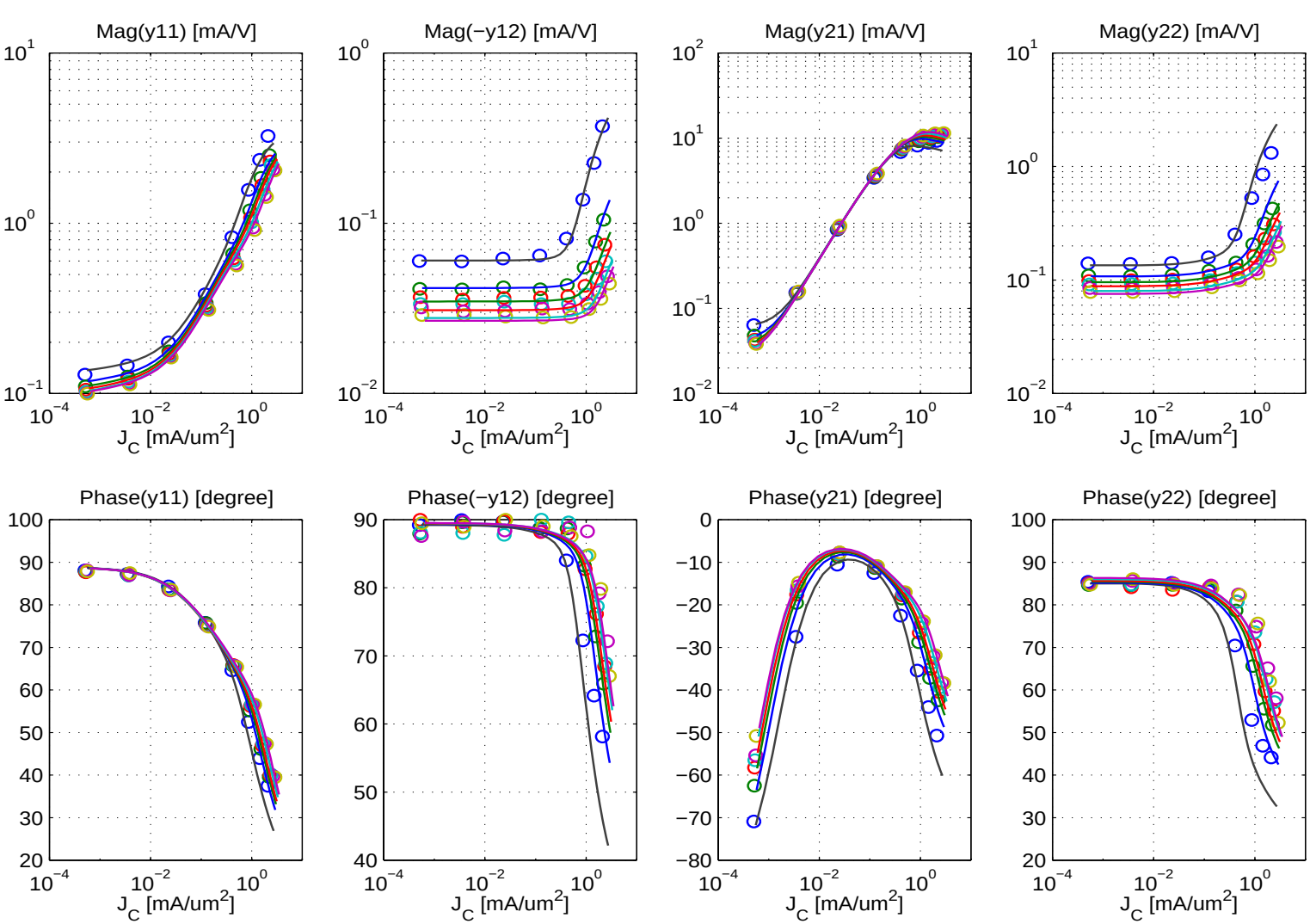
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.12 mA/µm^2, V_{BC} = -3 V (cf. f_T curves): comparison between measurement (symbols) [2] and HICUM (lines). Single transistor parameter extraction.

contd.: High-frequency small-signal characteristics



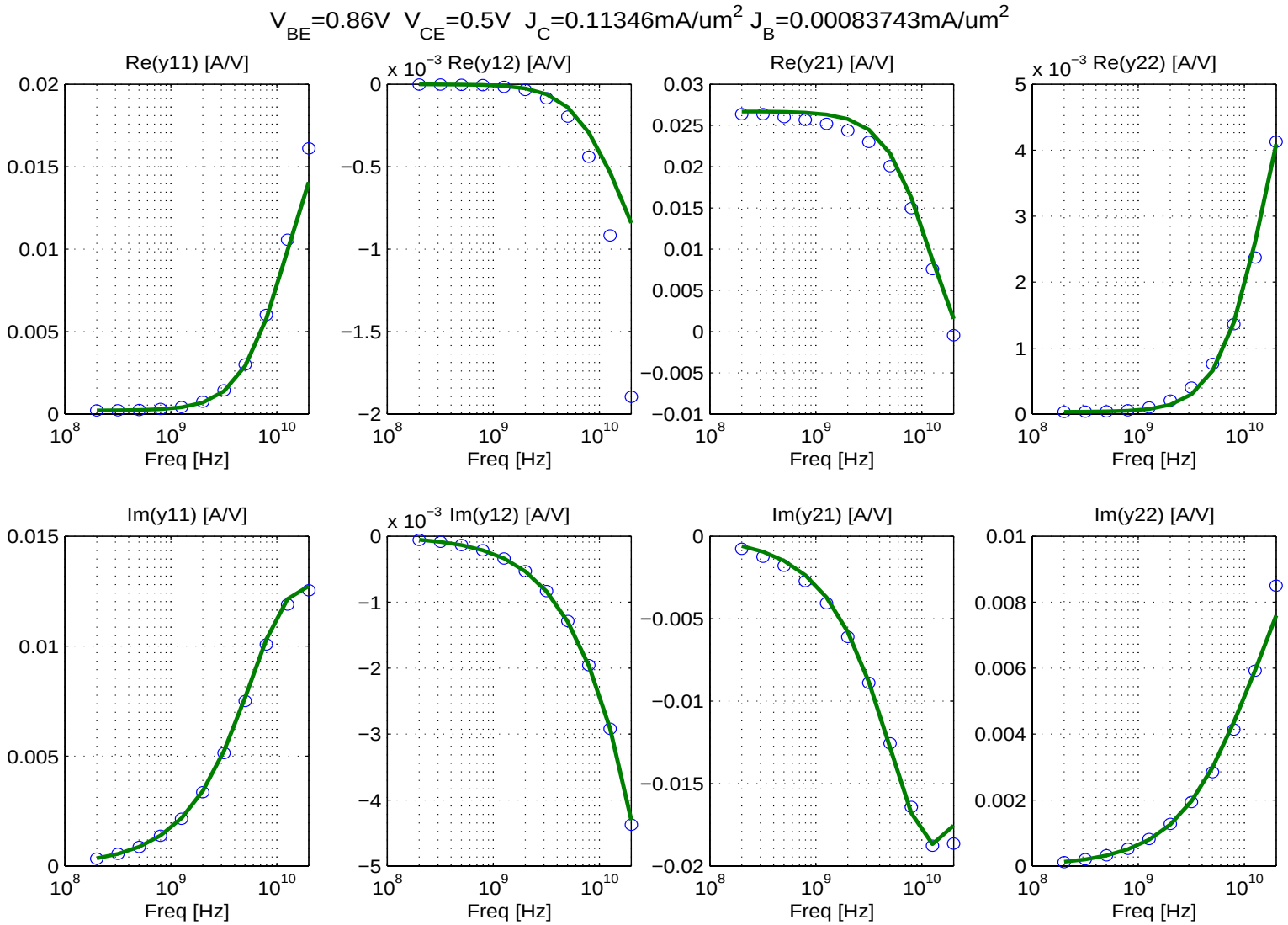
Frequency dependence of Y-parameters for a 12 GHz transistor (0.6*4.8µm^2) at I_C/A_E = 0.425 mA/µm^2, V_{BC} = -3 V (cf. f_T curves): comparison between measurement (symbols) [2] and HICUM (lines). Single transistor parameter extraction.

contd.: High-frequency small-signal characteristics



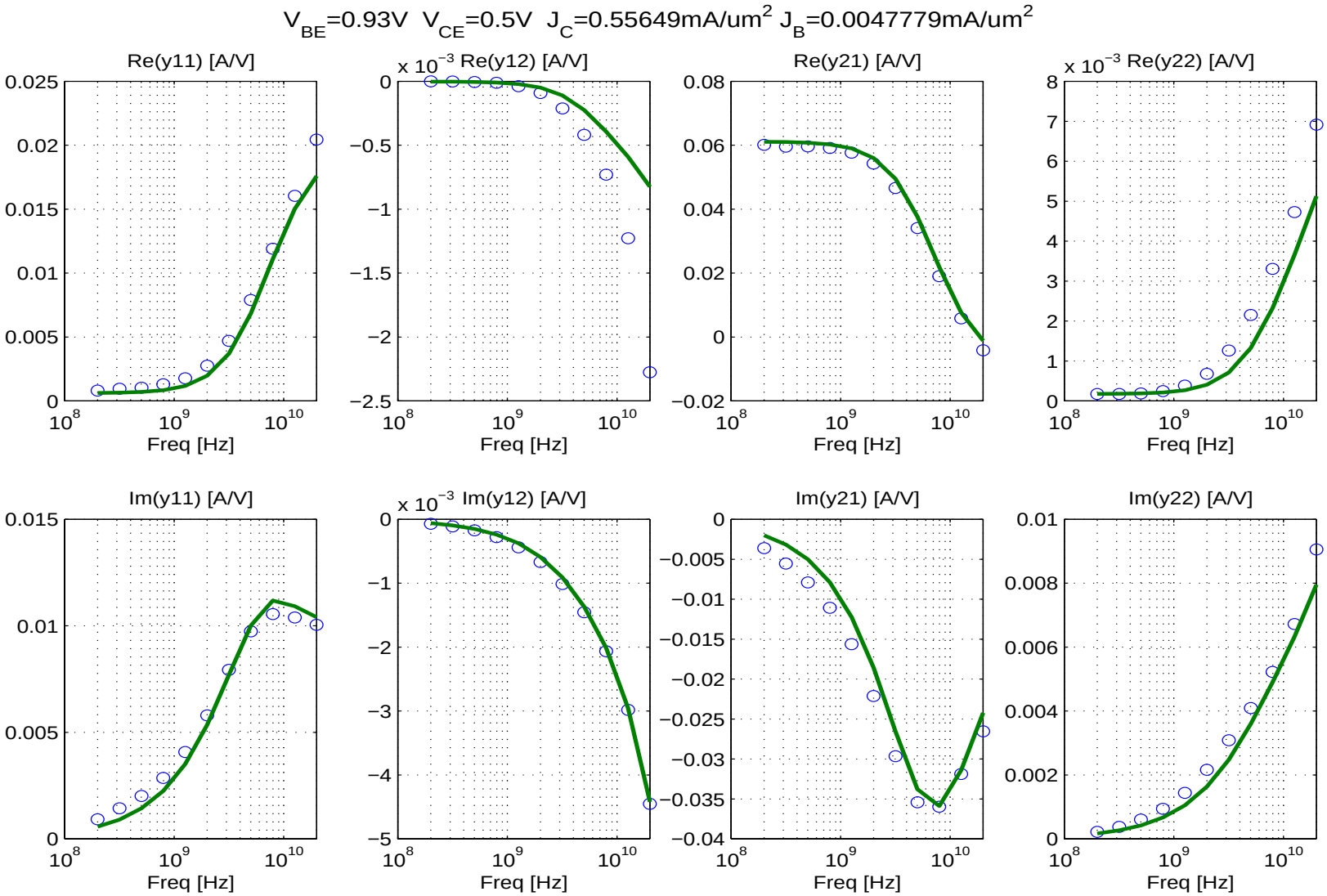
Y-parameters as a function of collector current density for a 12 GHz transistor ($0.6*4.8\mu m^2$) at f = 1GHz: comparison between measurement (symbols) and HICUM (lines). V_{CB}/V= -0.5, 0, 0.5, 2, 4.

contd.: High-frequency small-signal characteristics



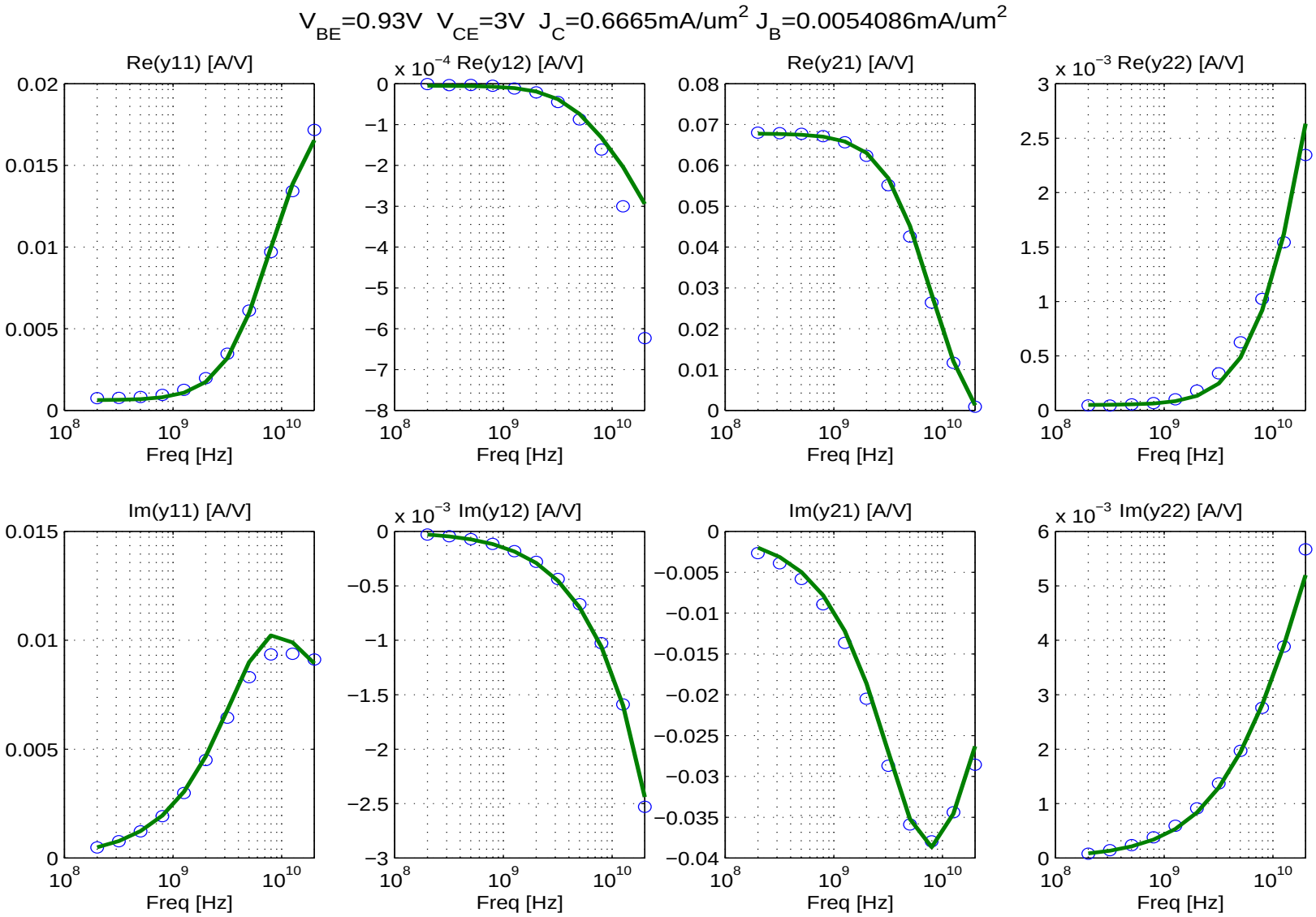
Frequency dependence of Y-parameters for a 25 GHz transistor (0.4*14µm^2) at I_C/A_E = 0.1 mA/µm^2, V_{CE} = 0.5 V (cf. f_T curves): comparison between measurement (symbols) and HICUM (lines).

contd.: High-frequency small-signal characteristics



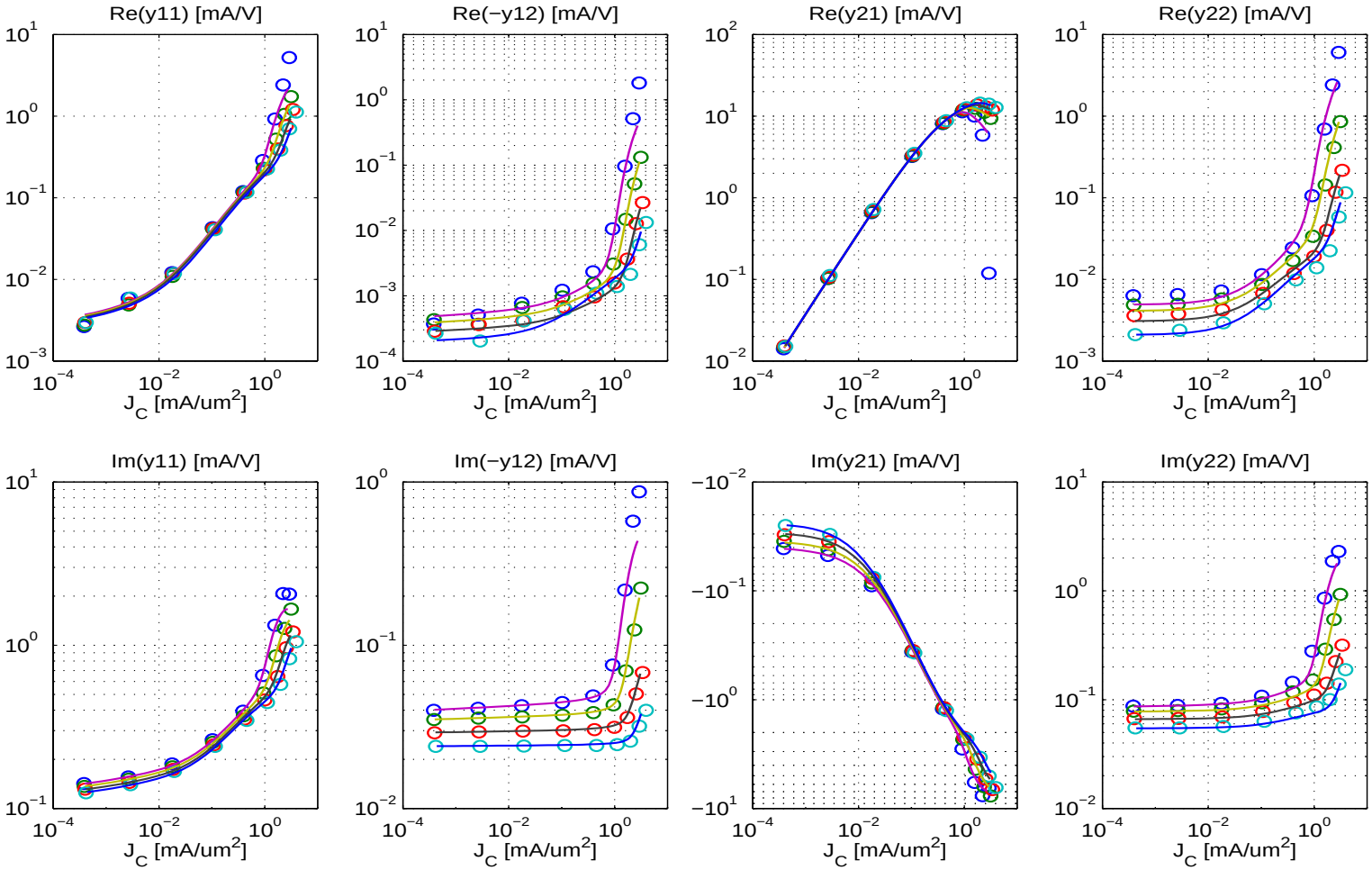
Frequency dependence of Y-parameters for a 25 GHz transistor (0.4*14µm^2) at I_C/A_E = 0.56 mA/µm^2, V_{CE} = 0.5 V (cf. f_T curves): comparison between measurement (symbols) and HICUM (lines).

contd.: High-frequency small-signal characteristics



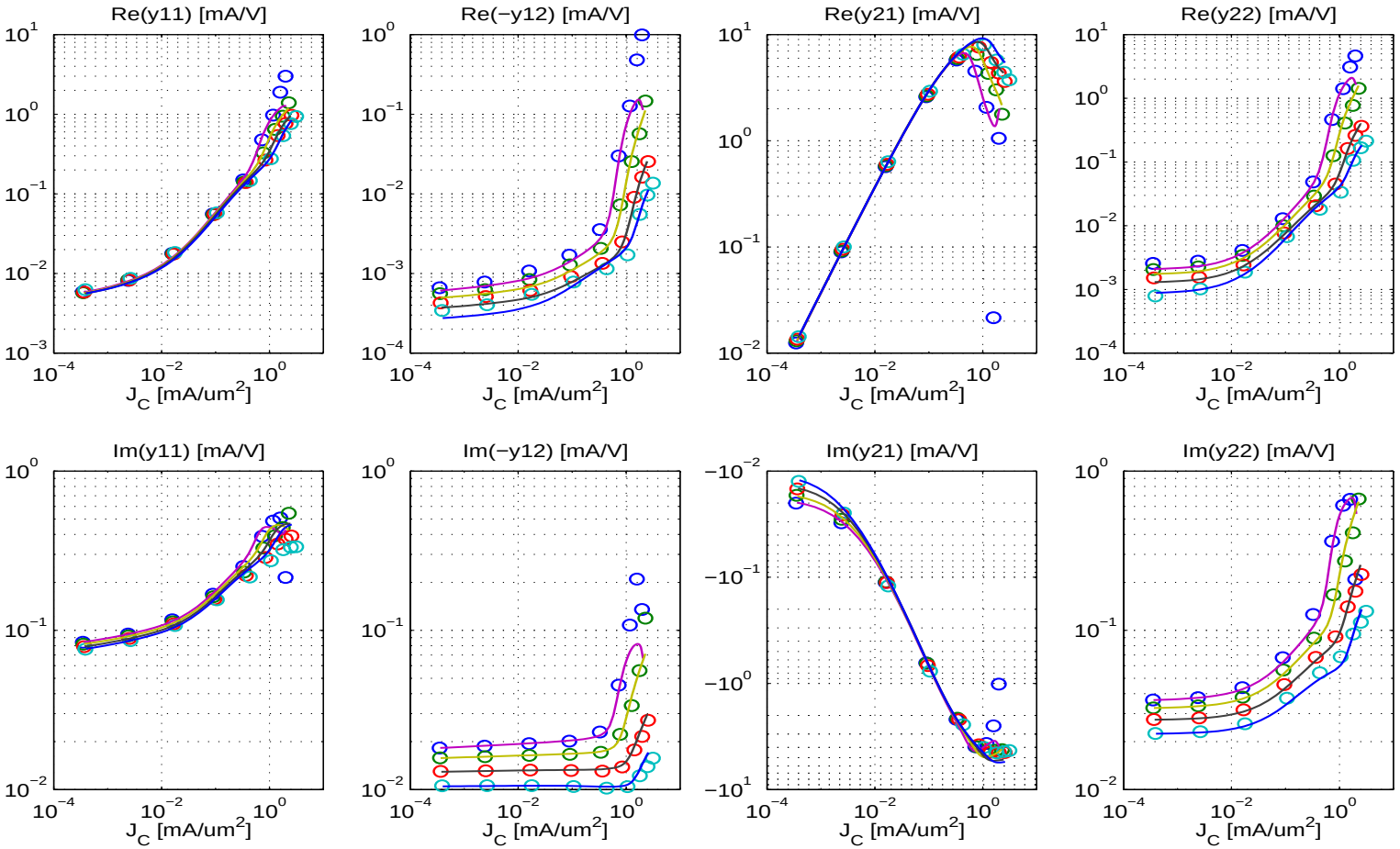
Frequency dependence of Y-parameters for a 25 GHz transistor (0.4*14µm^2) at I_C/A_E = 0.67 mA/µm^2, V_{CE} = 3 V (cf. f_T curves): comparison between measurement (symbols) and HICUM (lines).

contd.: High-frequency small-signal characteristics



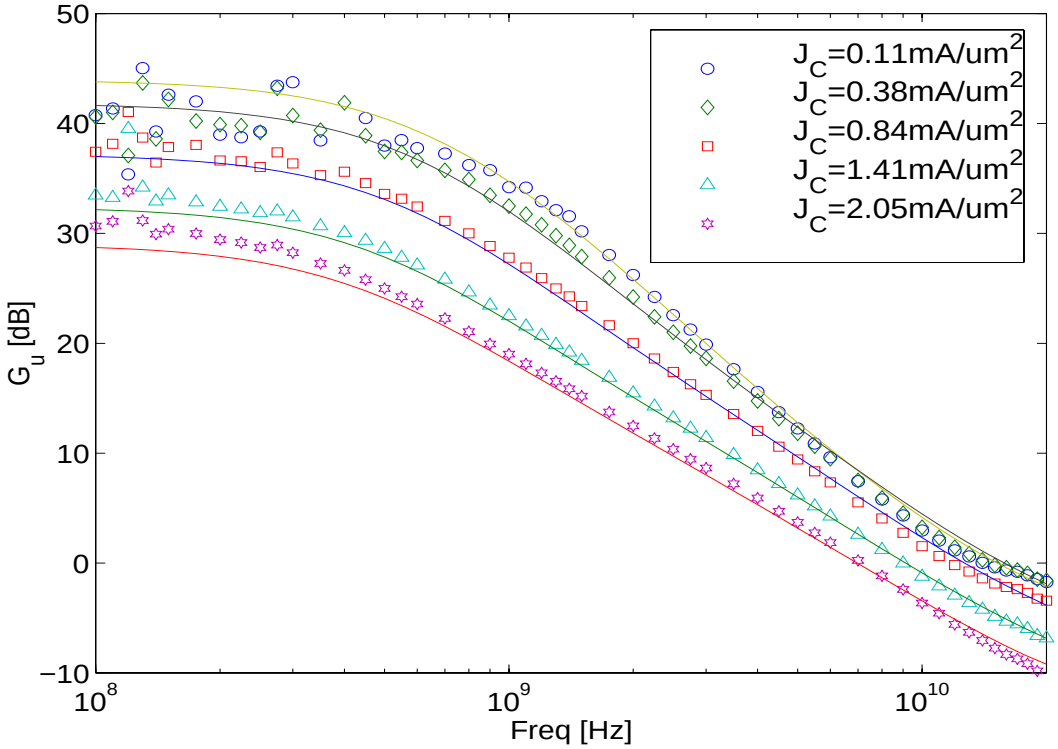
Y-parameters as a function of collector current density (V_{CE} = const.) for a 25 GHz transistor (0.4*14µm^2) at f = 1 GHz: comparison between measurement (symbols) and HICUM (lines). V_{CE}/V= 0.5, 0.8, 1.5, 3.

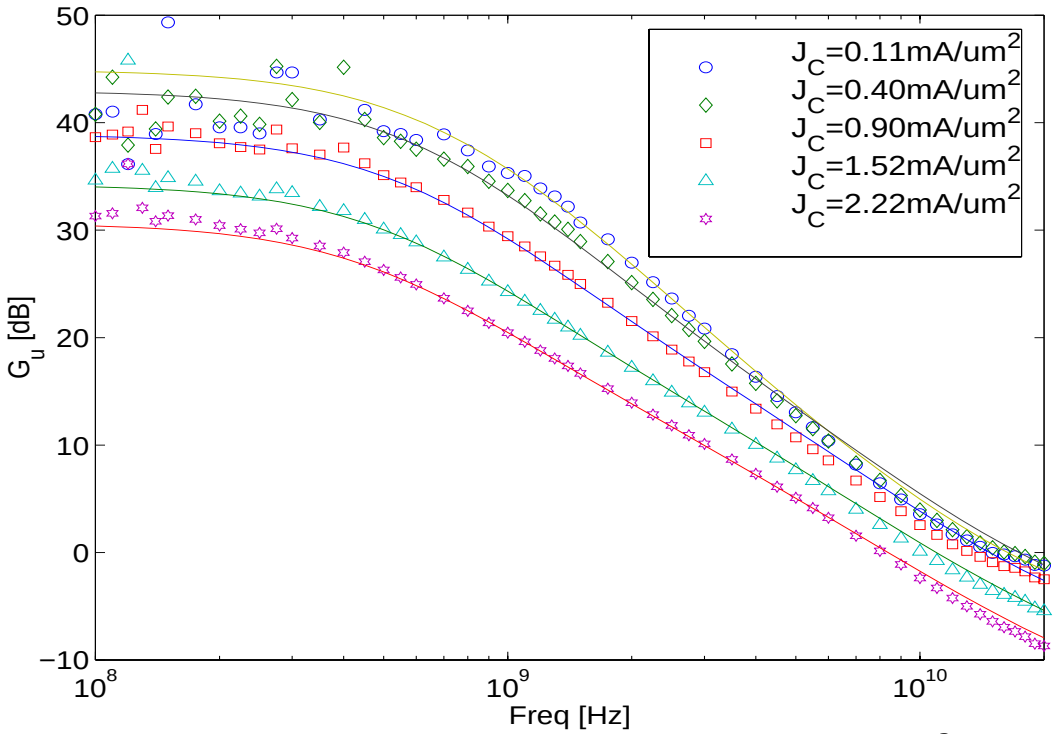
contd.: High-frequency small-signal characteristics



Y-parameters as a function of collector current density (V_{CE} = const.) for a 25 GHz transistor (1.2*14µm^2) at f = 1 GHz: comparison between measurement (symbols) and HICUM (lines). V_{CE}/V= 0.5, 0.8, 1.5, 3.

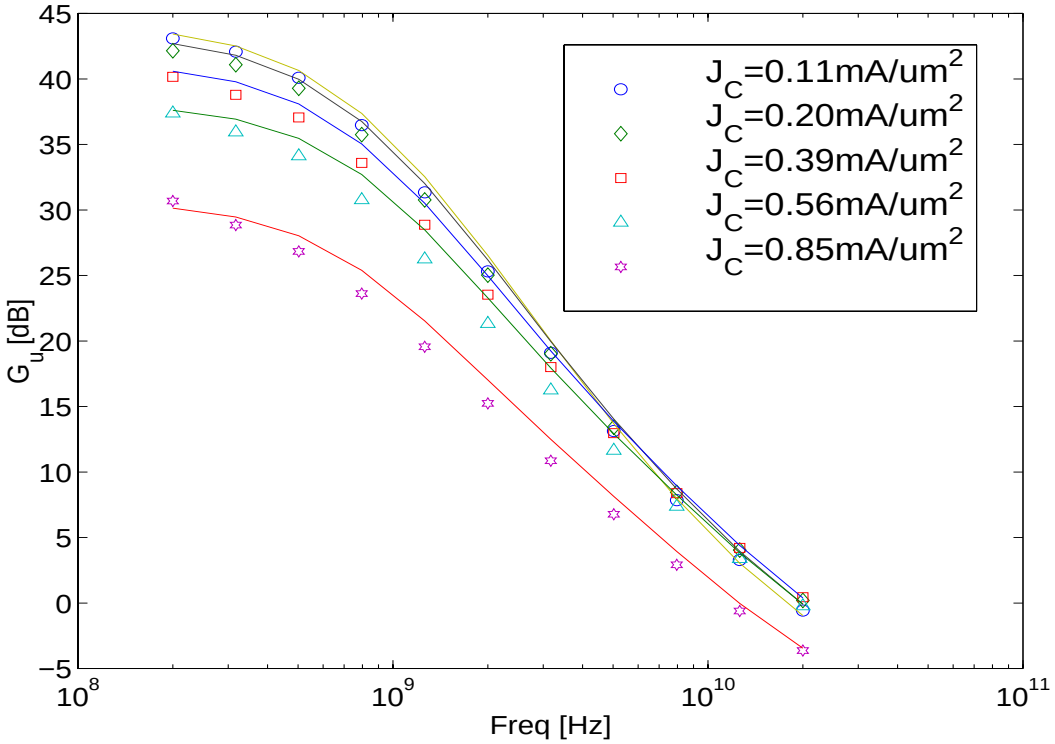
contd.: High-frequency small-signal characteristics - power gain

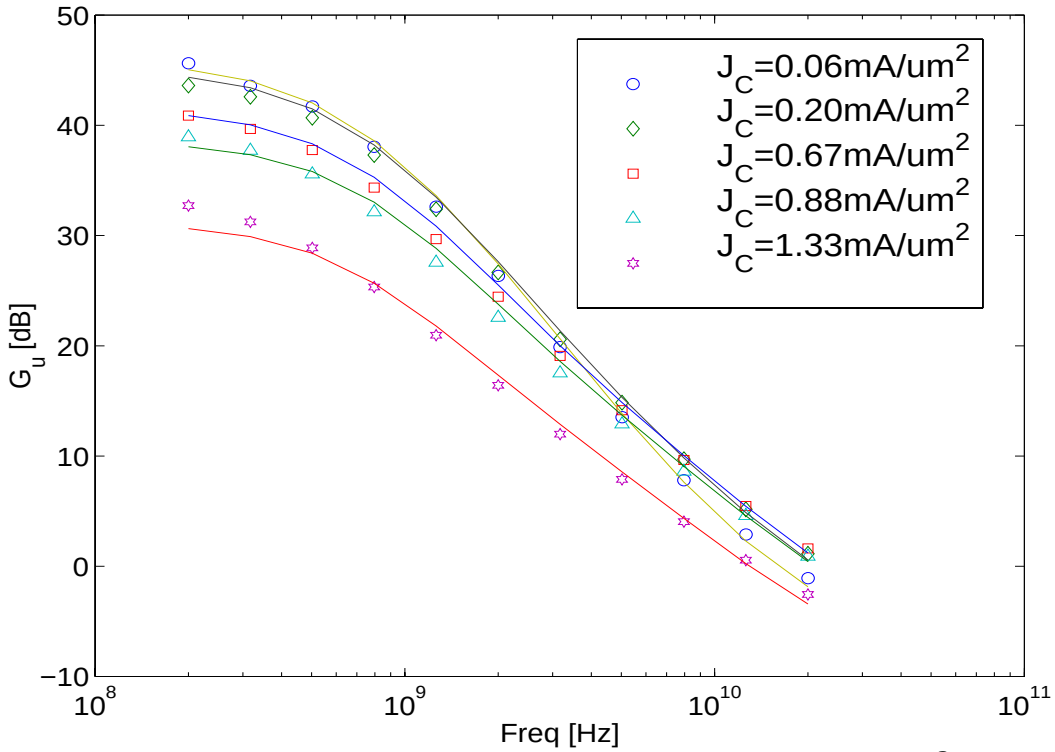




Unilateral gain G_U as a function of frequency for a 12 GHz transistor (0.6*4.8µm^2) at various bias points. Comparison between measurement (symbols) and HICUM (lines): (a) V_{BC} = -1 V; (b) V_{BC} = -2 V. Note the high accuracy even at current densities far beyond I_C/A_E(@peak f_T).

contd.: high-frequency small-signal characteristics - power gain

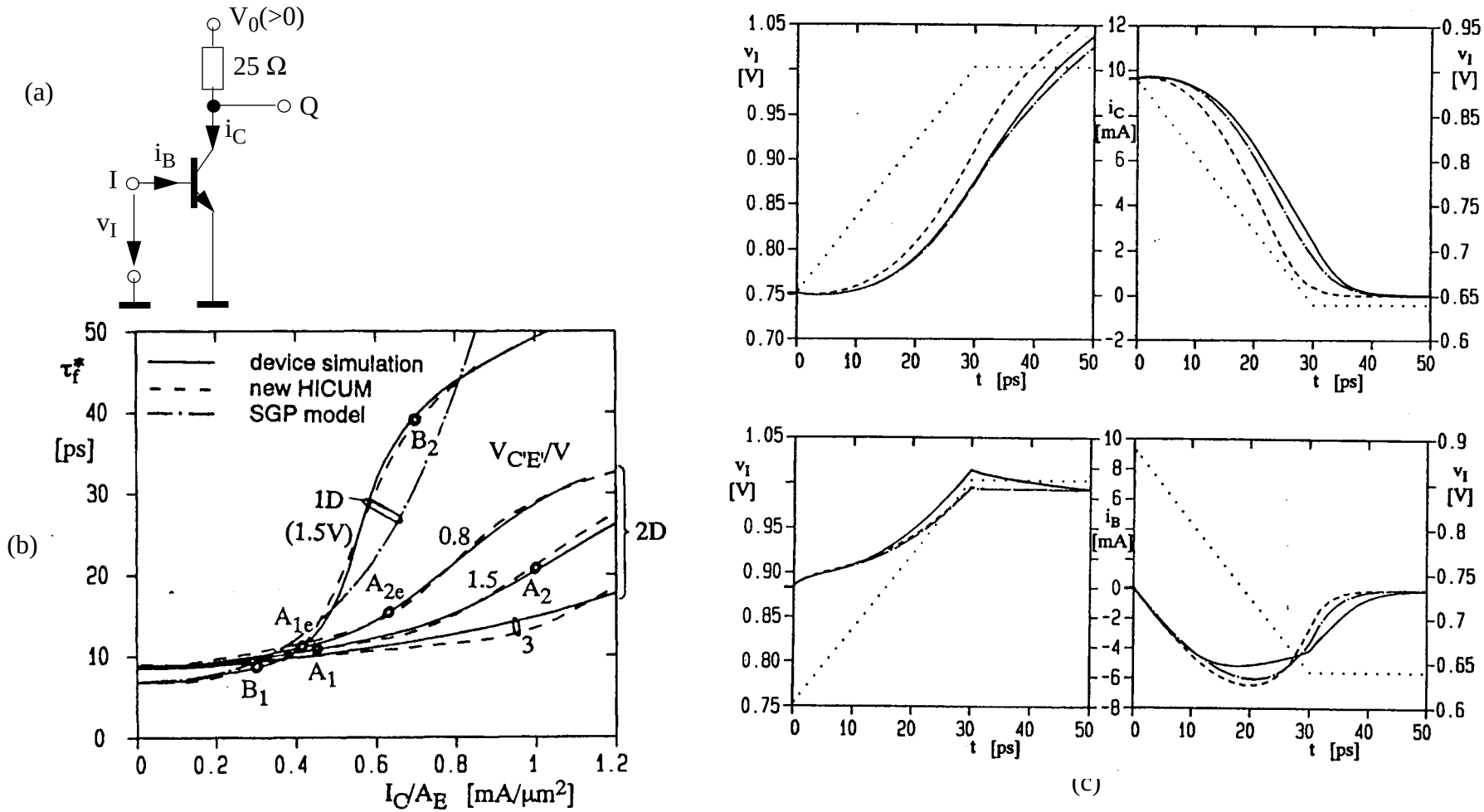




Unilateral gain G_U as a function of frequency for a 25 GHz transistor (0.4*14µm^2) at various bias points. Comparison between measurement (symbols) and HICUM (lines): (a) V_{CE} = 0.5 V; (b) V_{CE} = 0.8 V. Note the high accuracy even at current densities far beyond I_C/A_E(@peak f_T).

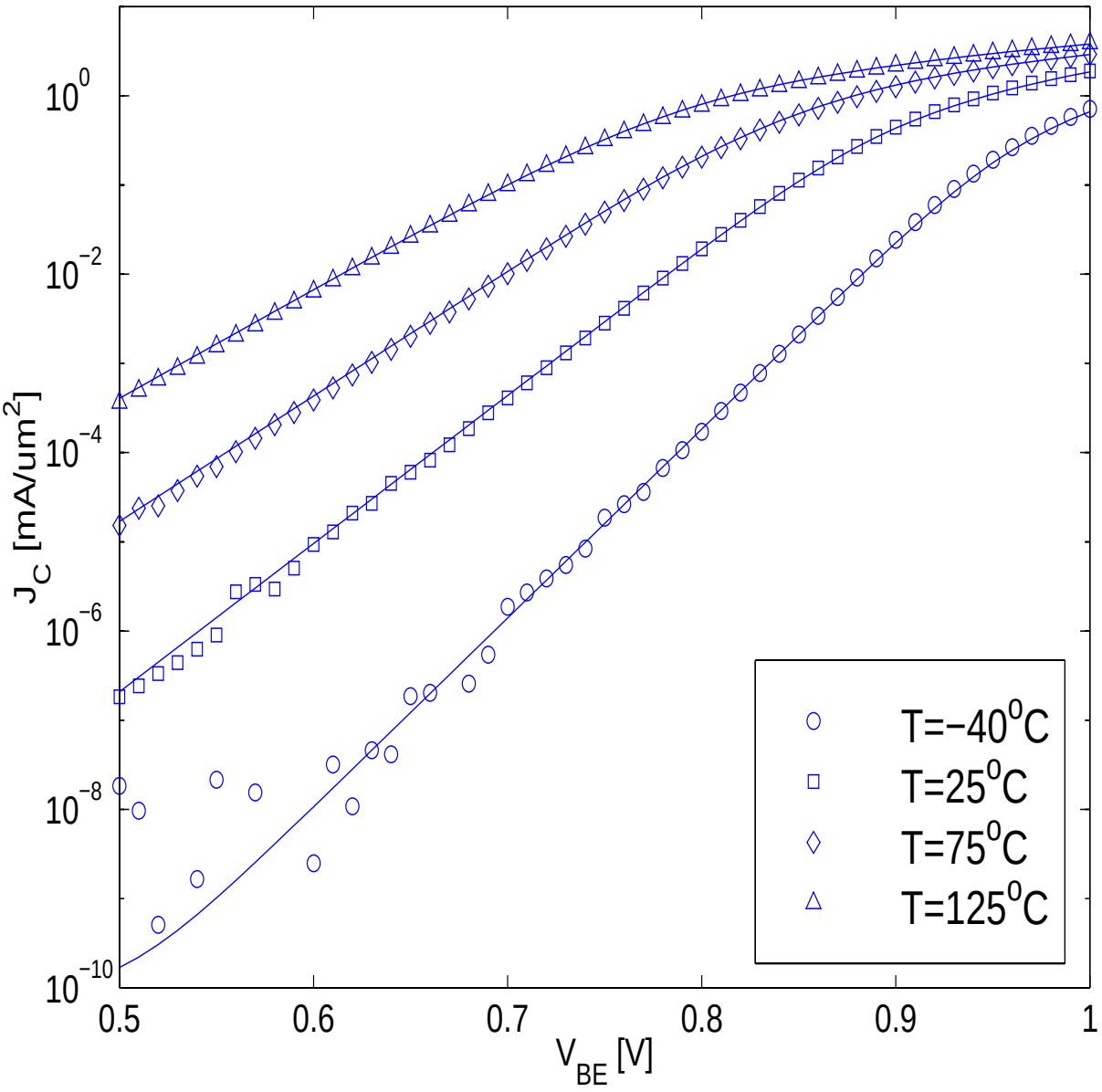
7.4 high-speed switching

(2D mixed-mode device/circuit simulation [42]; for experimental results of an older process see [26])



(a) Transistor inverter (worst-case for switching behavior comparison). (b) Transit time vs. collector current density of a 14 GHz bipolar transistor. (c) Switching-on and -off behavior for i_C (top) and i_B (bottom) into and out of, respectively, the bias point A_2 in Fig. (b). Comparison between device simulation (solid lines), HICUM with NQS effects (dash-dotted lines), and HICUM without NQS effects (dashed lines) [42].

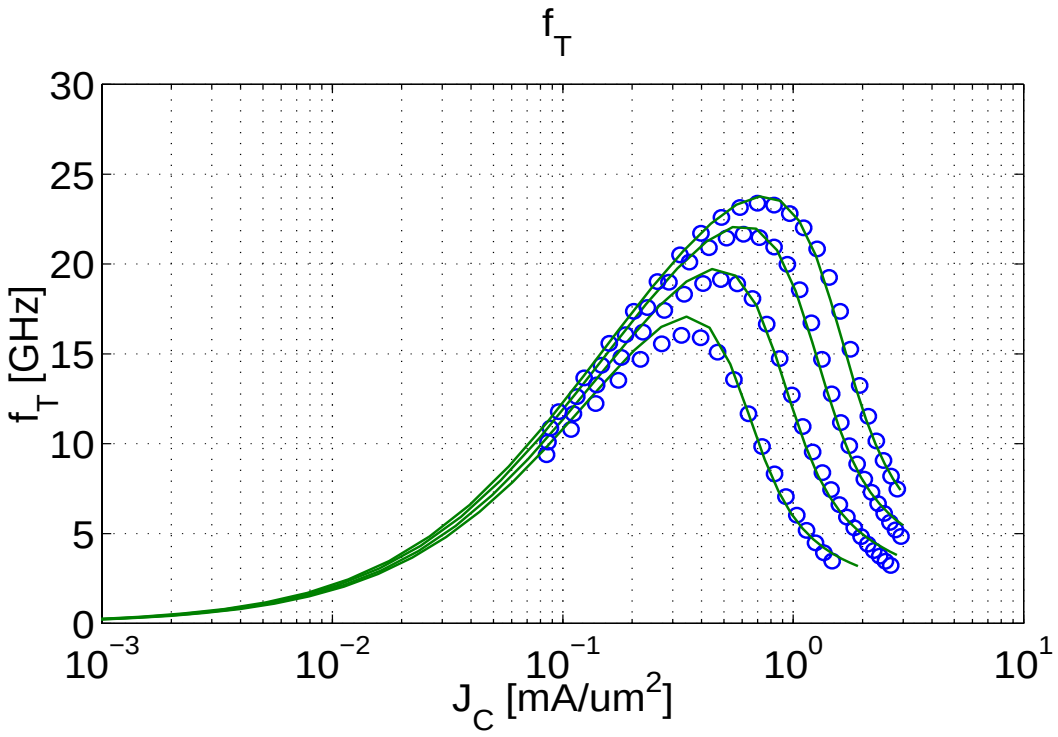
7.5 Temperature dependence: d.c. characteristics



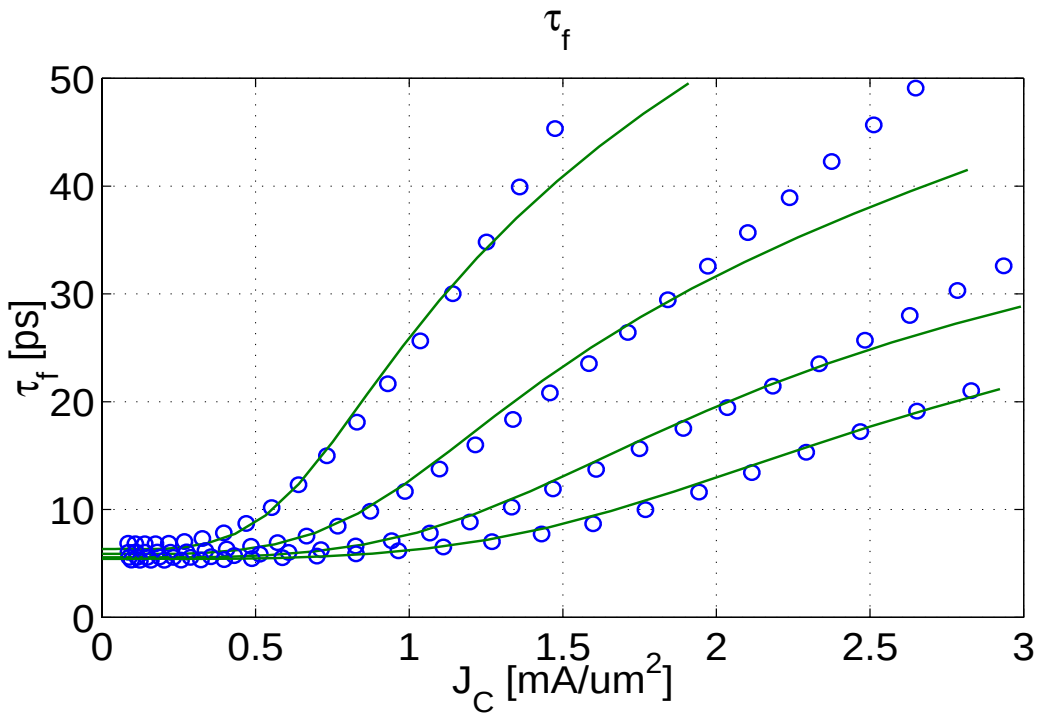
Comparison between measurement (symbols) and HICUM (solid lines) for a 25 GHz bipolar transistor: collector current density I_C/A_E vs. V_{BE} for different temperatures. Emitter size: 0.4*14 μm^2; V_{BC} = 0 V.

contd.: Temperature dependence of transit time and frequency

(a)



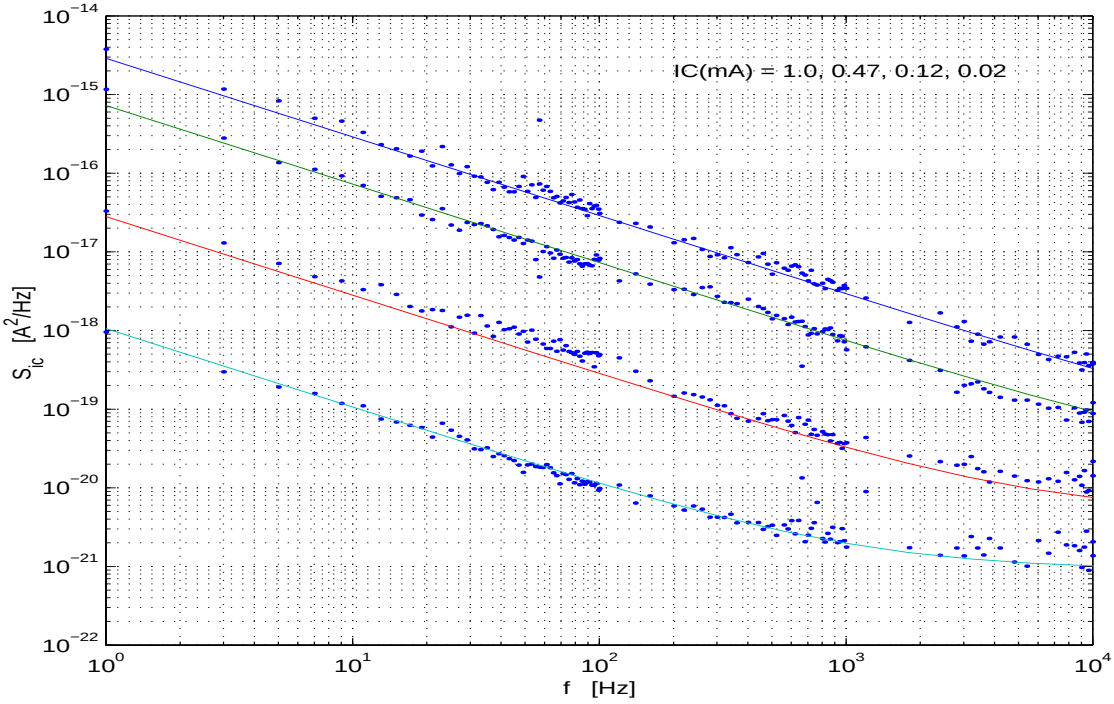
(b)



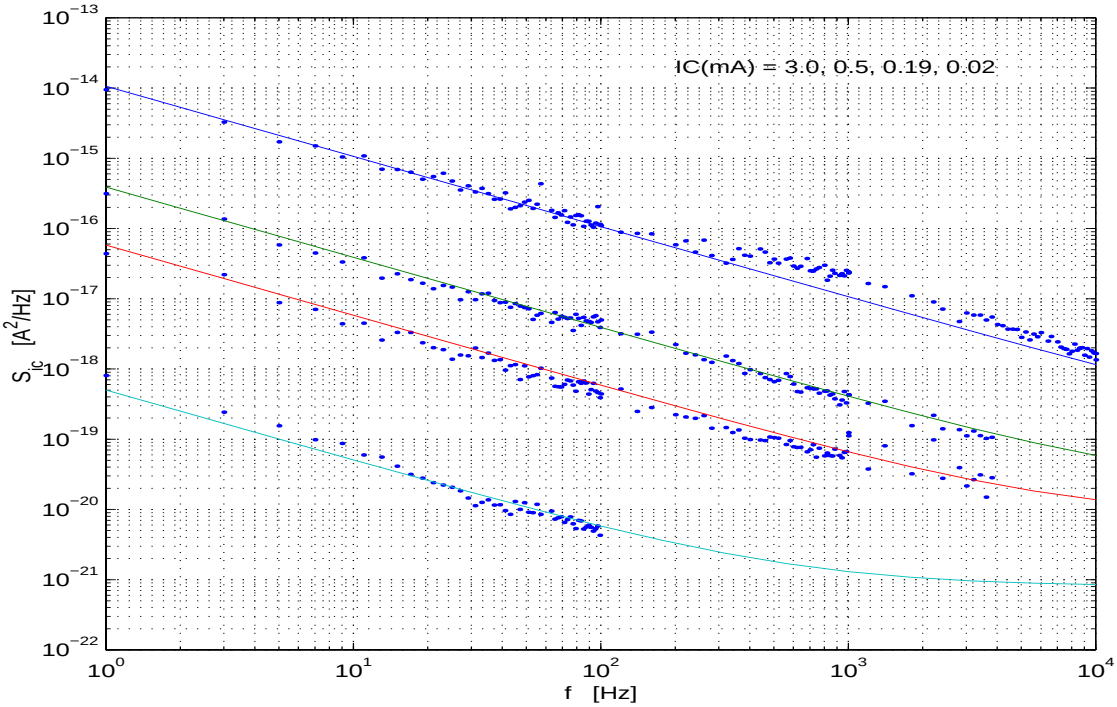
(a) Transit time and (b) transit frequency vs. I_C/A_E for T = 125 C: comparison between measurement (symbols) and HICUM (solid lines) [46]. Emitter size: 0.4*14 μm^2; V_{CE}/V = 0.5,0.8,1.5,3. Note, that the results were generated with a single model parameter set, except for the temperature coefficients of τ_0.

7.6 Low-frequency noise

(a)



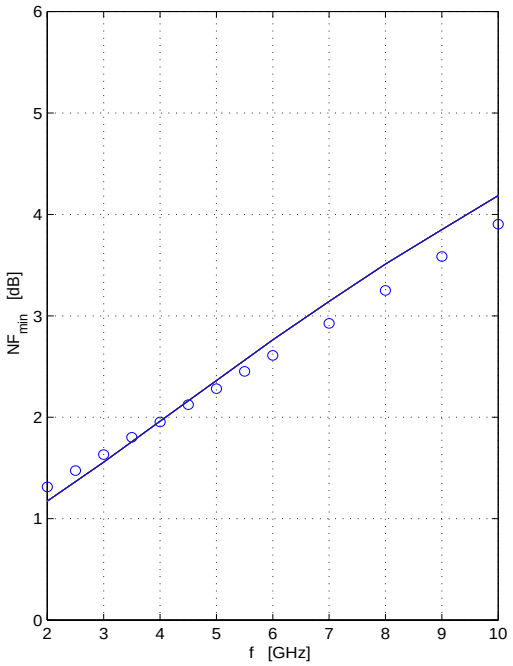
(b)

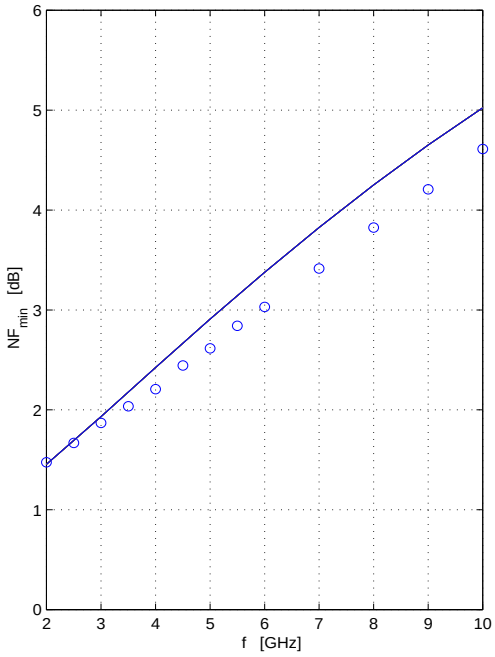


Collector current noise spectral density S_{iC} vs. frequency f for 25 GHz transistors at T = 25 C and various bias points I_C (cf. insert) and V_{CE} = 1 V. Comparison between measurement (symbols) and HICUM (lines): (a) A_{E0} = 0.4*14µm^2, (b) A_{E0} = 0.8*14µm^2.

7.7 High-frequency noise

(a)

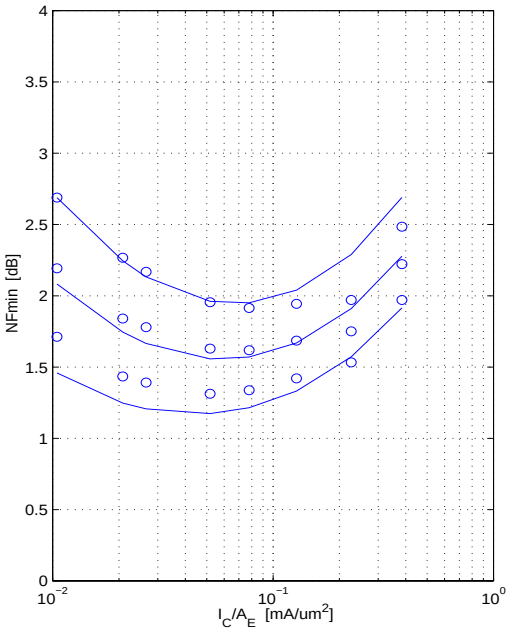


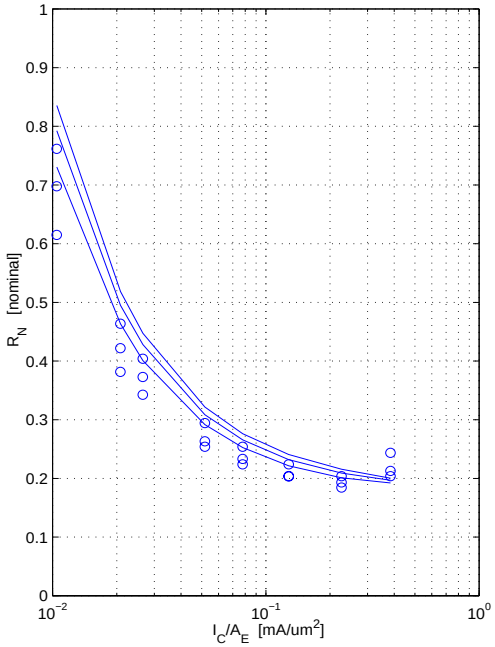


(b)

Minimum noise figure F_{min} vs. frequency f for a 25 GHz transistor. Comparison between measurement (symbols) and HICUM (lines): (a) emitter size is 4*0.4*21µm^2, I_C/A_E = 0.405mA/µm^2, V_{CE} = 1V; (b) emitter size is 0.8*14µm^2, I_C/A_E = 0.03mA/µm^2, V_{CE} = 1V.

(a)





(b)

Comparison between measurement (symbols) and HICUM (lines) for a 25 GHz transistor (4*0.4*21µm^2): (a) Minimum noise figure F_{min} vs. collector current density I_C/A_E; (b) equivalent noise resistance R_n vs. collector current density. f/GHz = 1, 2, 3; V_{CE} = 1V.

7.8 High-frequency distortion

Some general remarks are required for explaining and understanding the distortion results.

The transistors were measured on-wafer in a 50Ω system using the same h.f. pad configuration that is employed for small-signal S-parameter measurements. An automated measurement system was set-up which facilitates bias point sweeps [20]. The system was carefully calibrated in order to take into account all losses up to the device and to accurately obtain both output power P_{in} and input power P_{out} at the transistor terminals for all relevant frequencies. Single-tone measurements were performed at four different fundamental frequencies f_1/GHz = (0.05, 0.1, 0.9, 1.8). The two low frequencies at 50 and 100 MHz were chosen to be able to separate later the cause of non-linearities during model comparison. The following table shows the relation between P_{in} specified in dBm by the power sweeper (defined for a 50Ω load) and the respective voltage amplitude.

P [dBm]	-40	-30	-20	-10
$\hat{v}$ [V]	6.4	20	64	200

As response at the output, the signals at the respective fundamental frequency as well as the second and third harmonic frequency (f_2 and f_3) were measured with a spectrum analyzer for different transistor types. The table below lists the frequencies that belong together. The resulting P_{out} at the various frequencies can then be compared to model characteristics as a function of d.c. bias and geometry. Figures of merit, such as the 1dB compression point and harmonic distortion, can also be calculated.

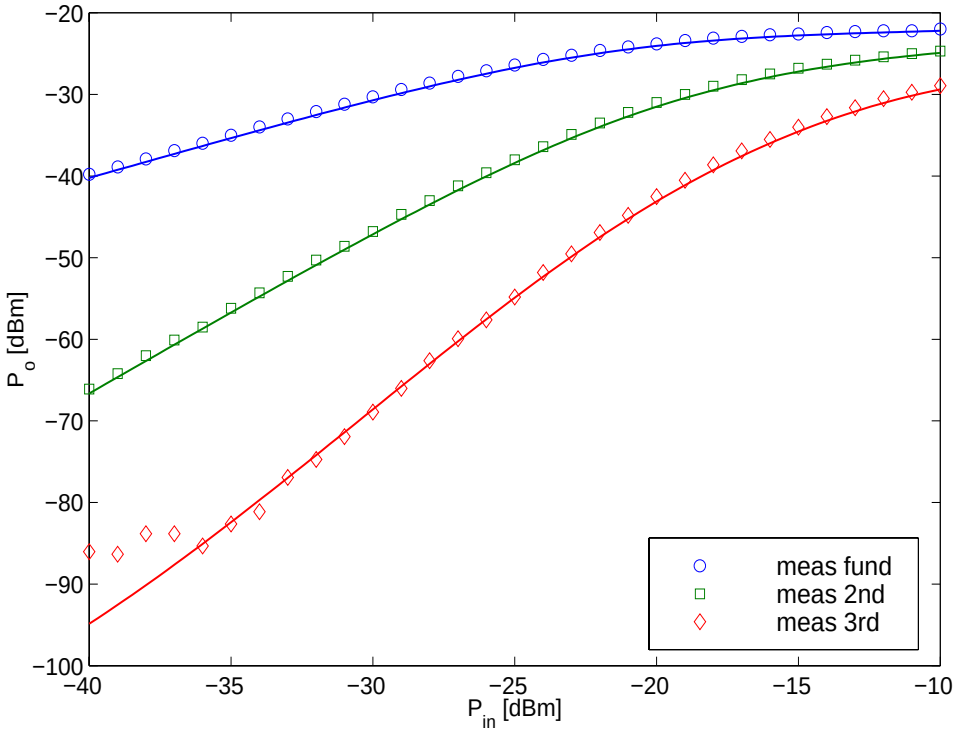
f_1/GHz	0.05	0.1	0.9	1.8
f_2/GHz	0.1	0.2	1.9	3.6
f_3/GHz	0.15	0.3	2.7	5.4

For circuit simulation, the periodic steady-state method available in SPECTRE-RF was used. However, time-domain based simulators seem to generate an incorrect d.c. component (probably converted from the second harmonic) at the transistor input, which causes the d.c. bias point to run away at high input power. This (probably) numerical effect, which should not occur according to the measurement set-up, was not observed during harmonic balance simulations (using HP-MDS) with the same circuit and parameters. A corresponding correction algorithm was developed and implemented in MATLAB, the results of which were verified by HP-MDS.

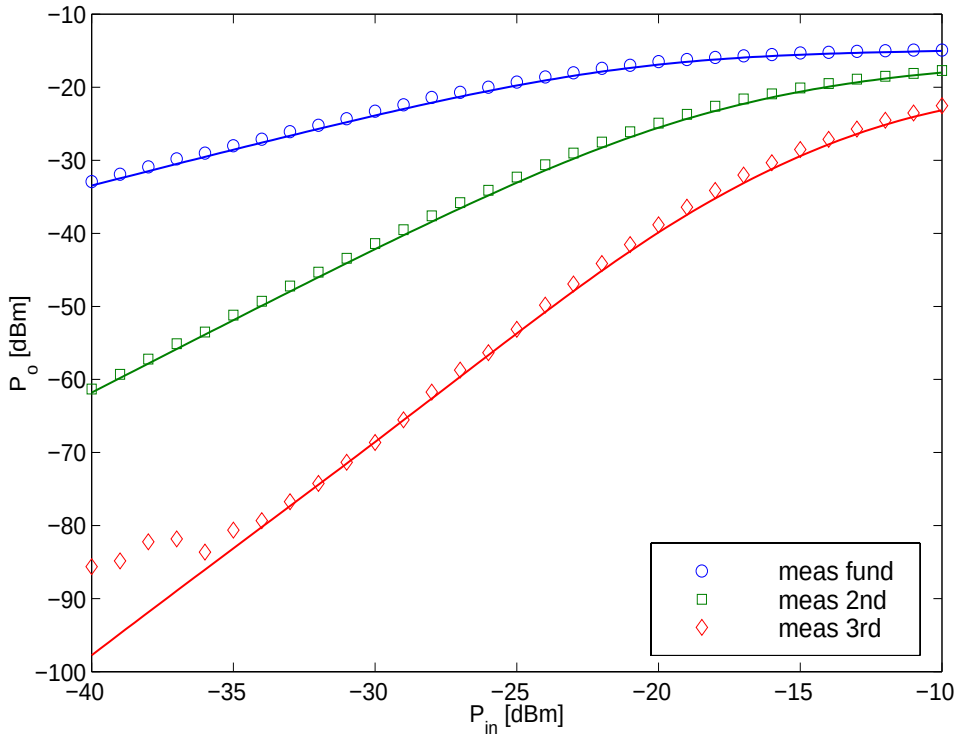
For logistical reasons the measurements were carried out on a different die of the same wafer the parameter extraction was performed on. Process variations across the wafer might cause slightly increased deviations between model and measurements. Nevertheless, the model still turned out to be quite accurate.

contd.: High-frequency distortion

(a)



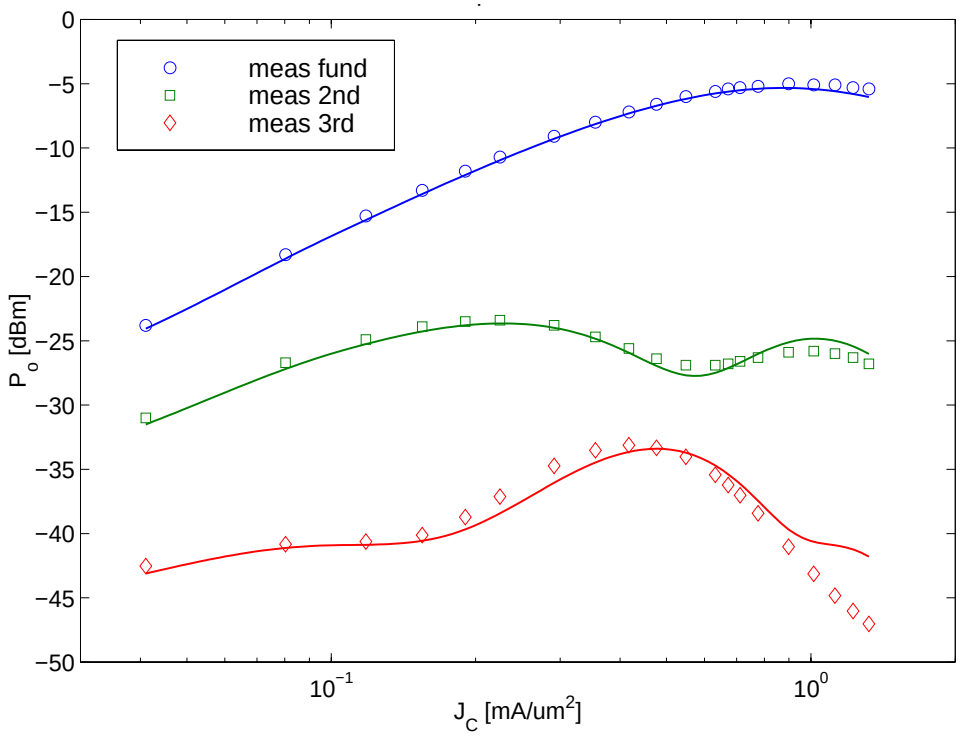
(b)



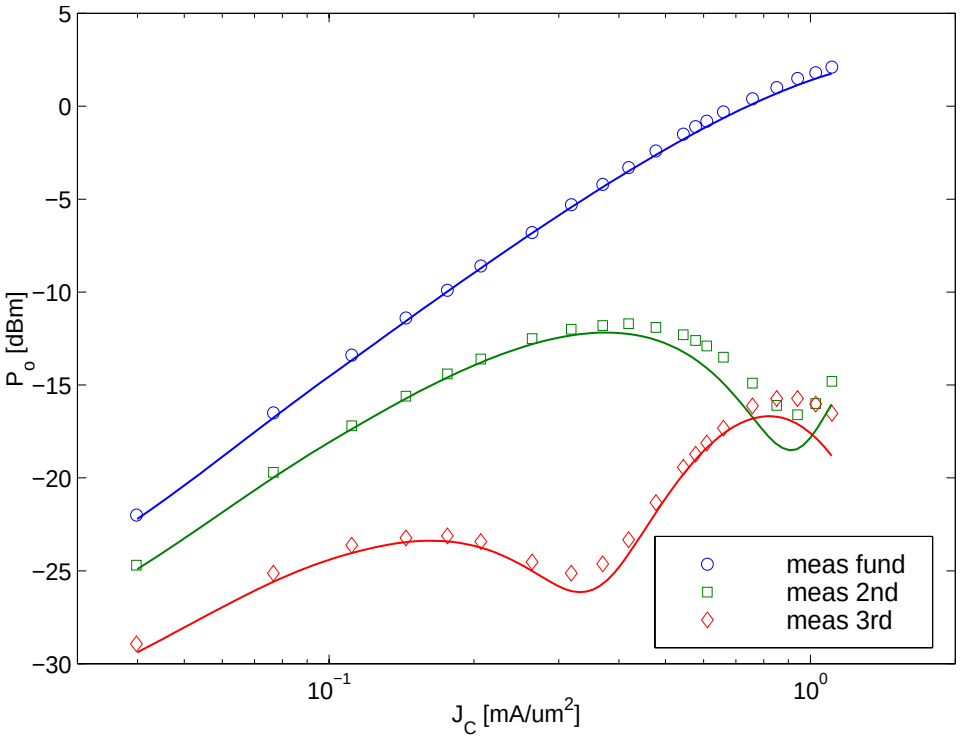
P_{out} vs. P_{in} for f_0 = 0.9 GHz; comparison between measurement (symbols) and HICUM (lines):
(a) 10 GHz (power) transistor (0.4*14µm^2) at I_C/A_E = 0.05 mA/µm^2, V_{CE} = 0.8 V;
(b) 25 GHz transistor (0.4*14µm^2) at I_C/A_E = 0.13 mA/µm^2, V_{CE} = 3 V.

contd.: High-frequency distortion

(a)



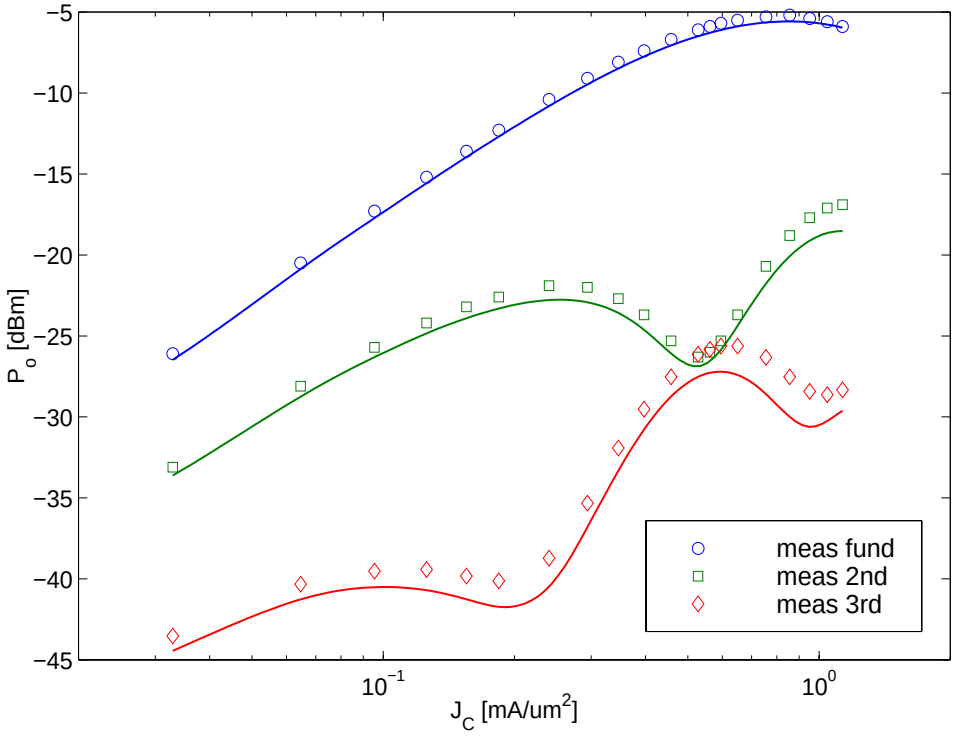
(b)



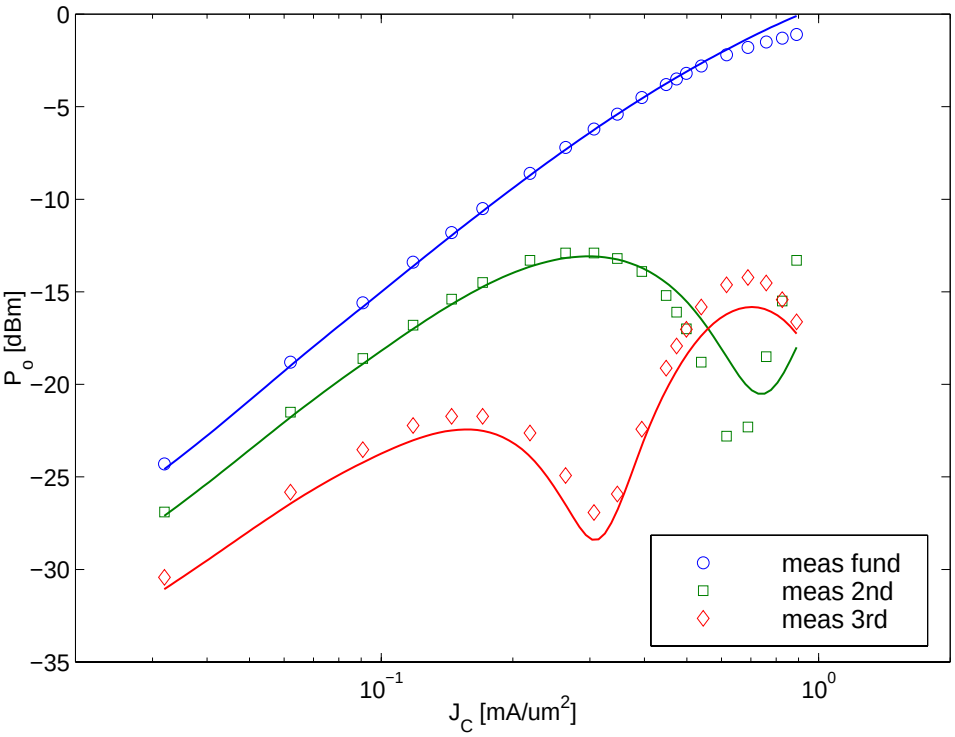
P_{out} vs. collector current density I_C/A_E at f_0 = 0.9 GHz for a 10 GHz (power) transistor (0.4*14µm^2); comparison between measurement (symbols) and HICUM (lines):
(a) P_{in} = -20 dBm; (b) P_{in} = -10 dBm. V_{CE} = 0.8 V.

contd.: High-frequency distortion

(a)



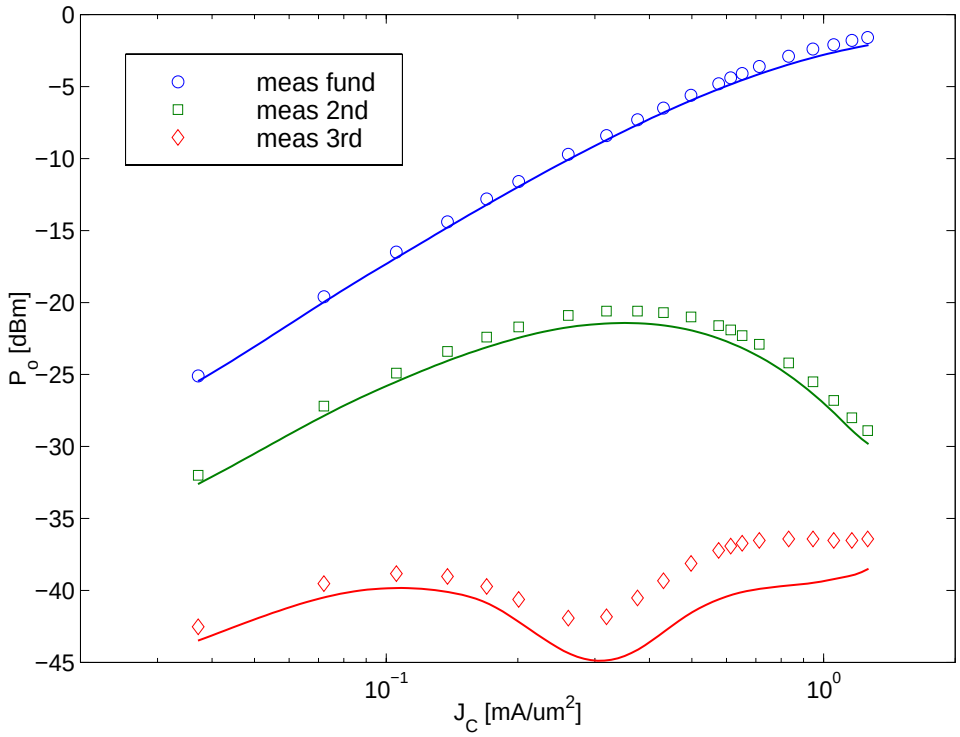
(b)



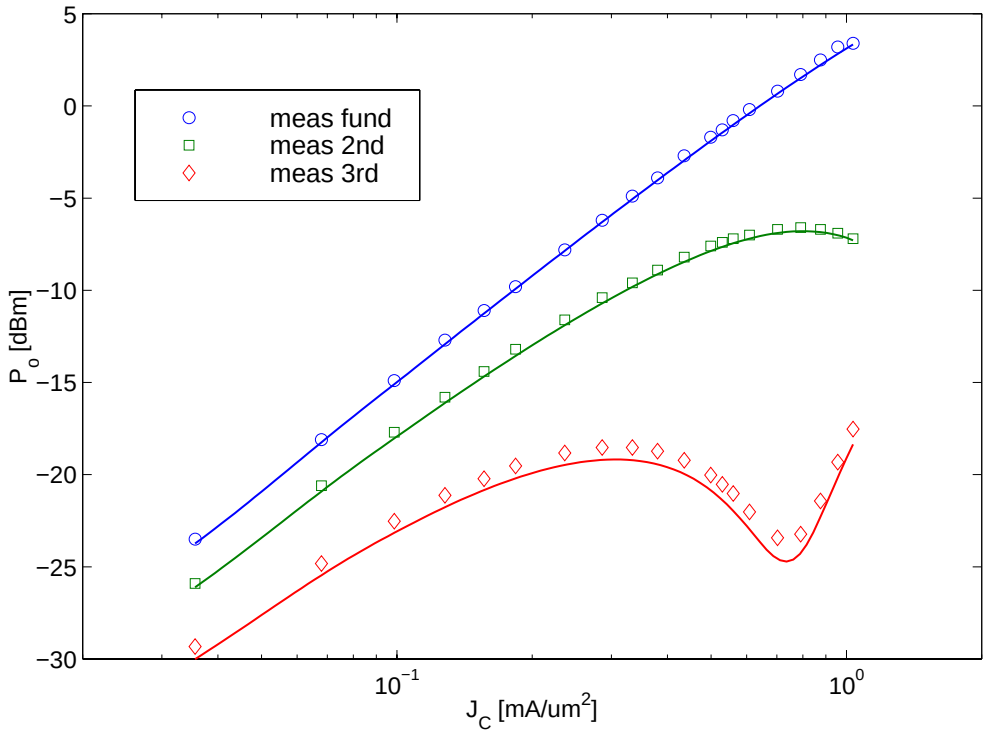
P_{out} vs. collector current density I_C/A_E at f_0 = 0.9 GHz for a 25 GHz transistor (0.4*14µm^2); comparison between measurement (symbols) and HICUM (lines):
(a) P_{in} = -20 dBm; (b) P_{in} = -10 dBm. V_{CE} = 0.5 V.

contd.: High-frequency distortion

(a)



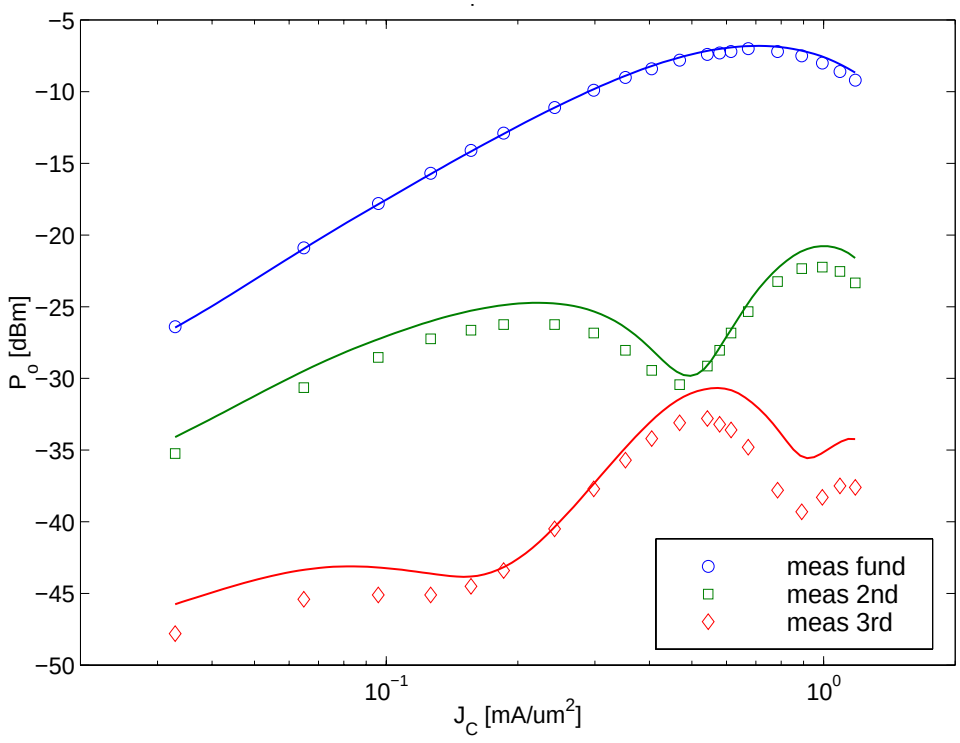
(b)



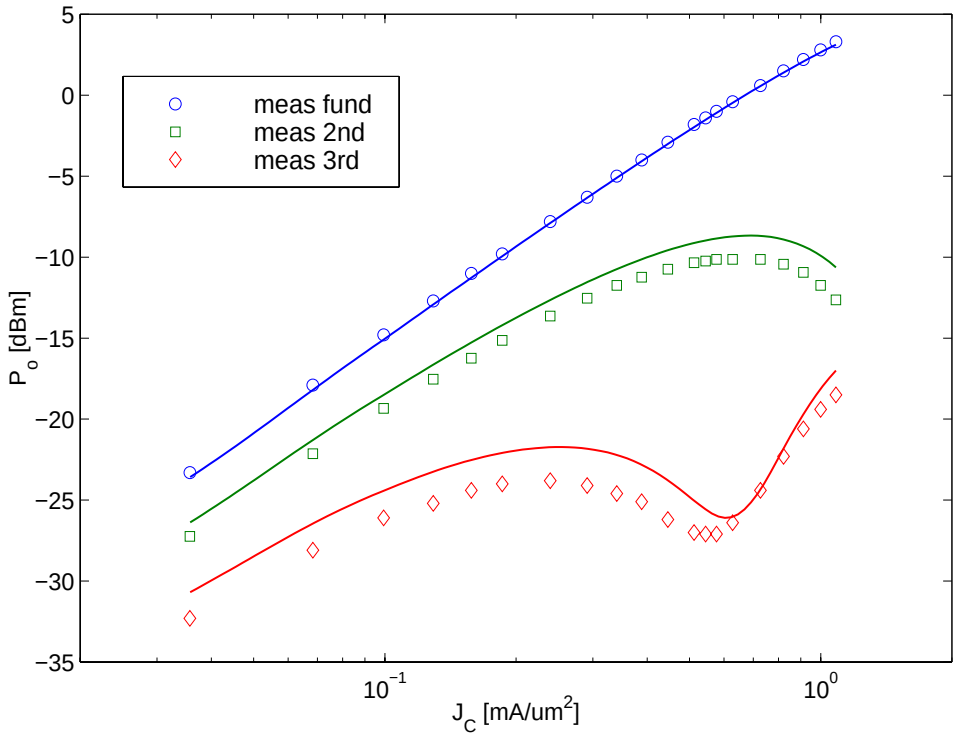
P_{out} vs. collector current density I_C/A_E at f_0 = 0.9 GHz for a 25 GHz transistor (0.4*14µm^2); comparison between measurement (symbols) and HICUM (lines):
(a) P_{in} = -20 dBm; (b) P_{in} = -10 dBm. V_{CE} = 3 V.

contd.: High-frequency distortion

(a)

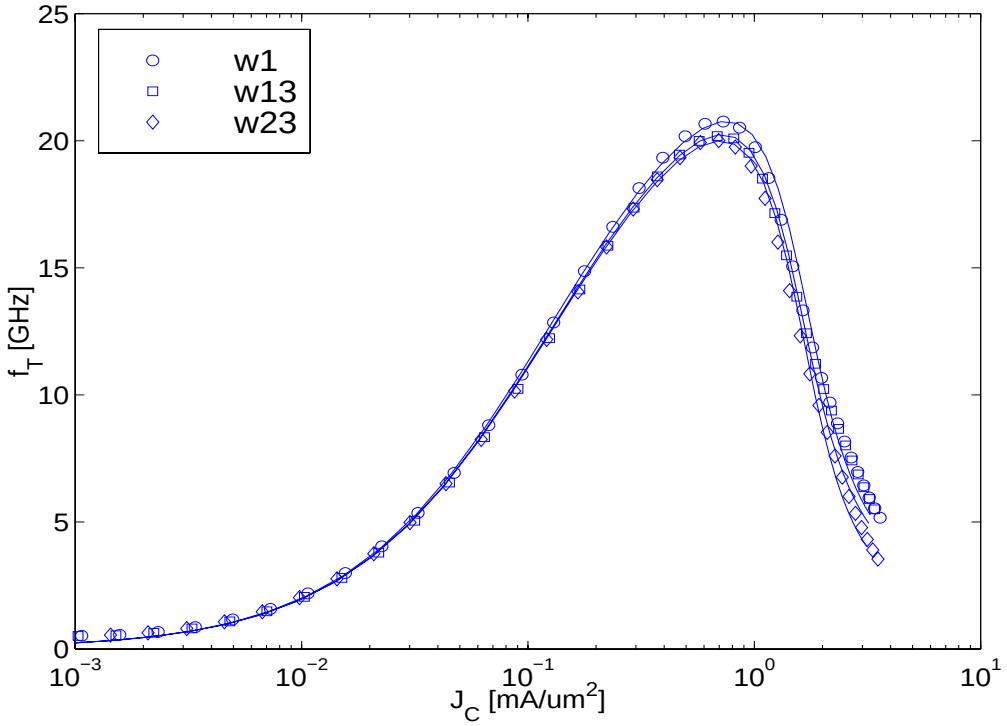


(b)

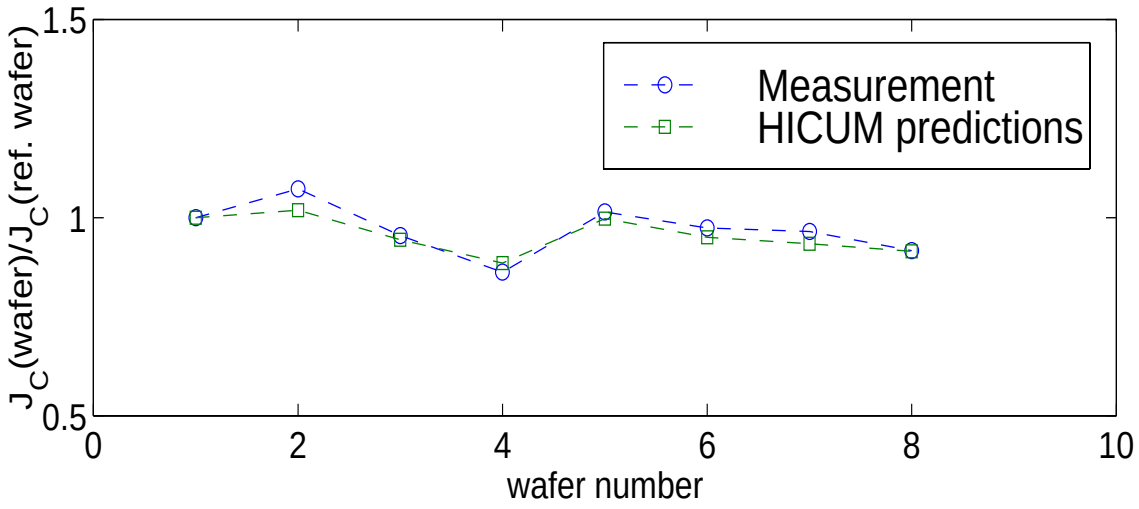


P_{out} vs. collector current density I_C/A_E at f_0 = 1.8 GHz for a 25 GHz transistor (0.4*14µm^2); comparison between measurement (symbols) and HICUM (lines):
(a) P_{in} = -20 dBm, V_{CE} = 0.5 V; (b) P_{in} = -10 dBm, V_{CE} = 3 V.

7.9 Predictive modeling

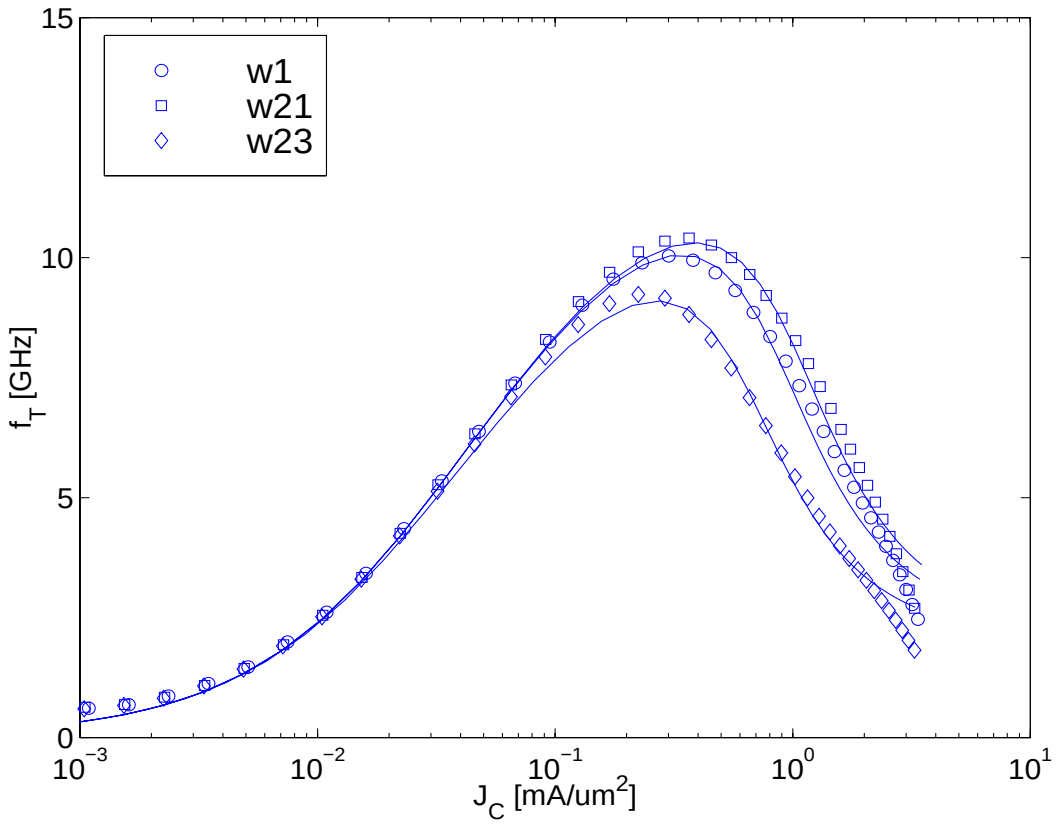


Transit frequency vs. collector current density for several process variations: base line (circles), 10% decrease of selectively implanted collector dose (squares), 25% increase of epi width w_C (diamonds). Comparison between measurement (symbols) and HICUM predictions (solid lines). V_{CE} = 0.8 V; emitter size: 0.4*14 µm^2.



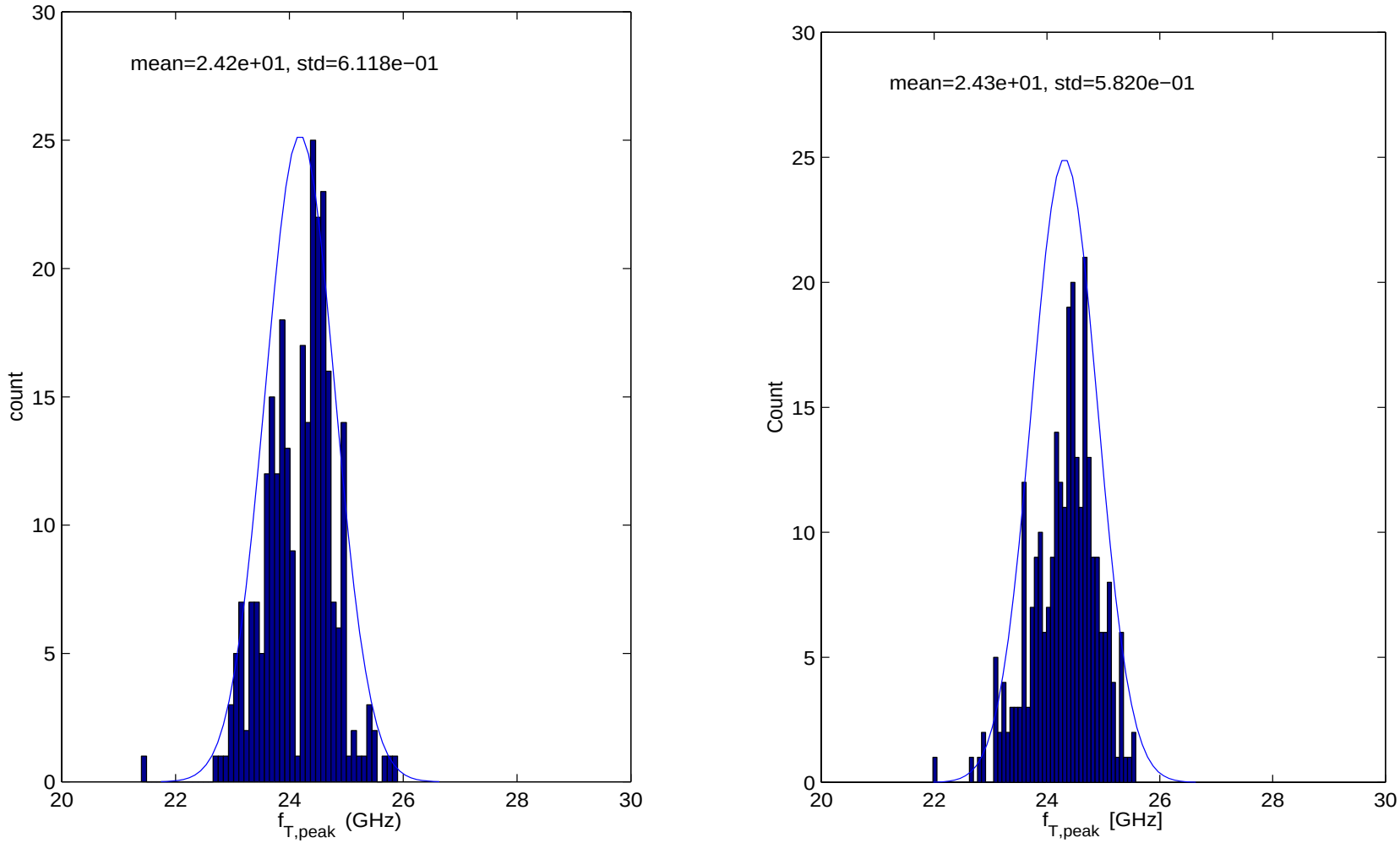
Collector current density at fixed V_{BE} = 0.8V for the same process variants as above; comparison between measurement (o) and HICUM predictions (-). V_{CE} = 0.8V; Emitter size: 0.4*14µm^2

contd.: Predictive modeling



Transit frequency vs. collector current density for several variations of a "high-voltage" process: base line (circles), ≈5% increase of epi collector doping (squares), 25% increase of epi width w_C (diamonds). Comparison between measurement (symbols) and HICUM predictions (solid lines). V_{CE} = 0.8 V; emitter size: 0.4*14 µm^2.

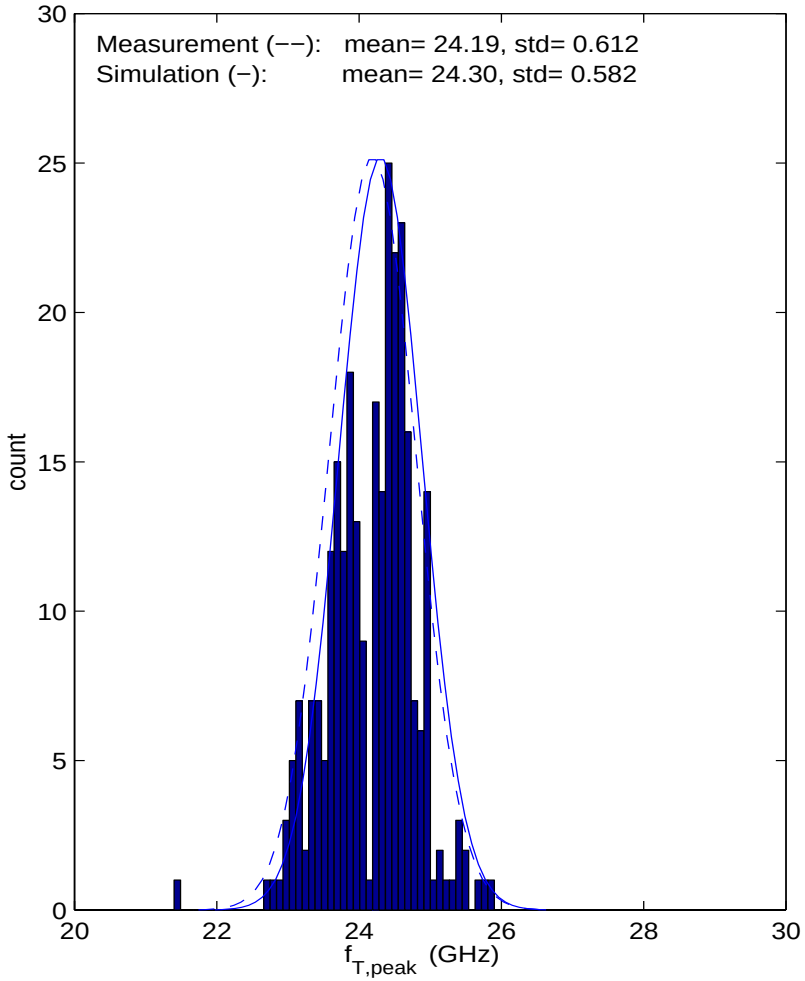
7.10 Statistical modeling



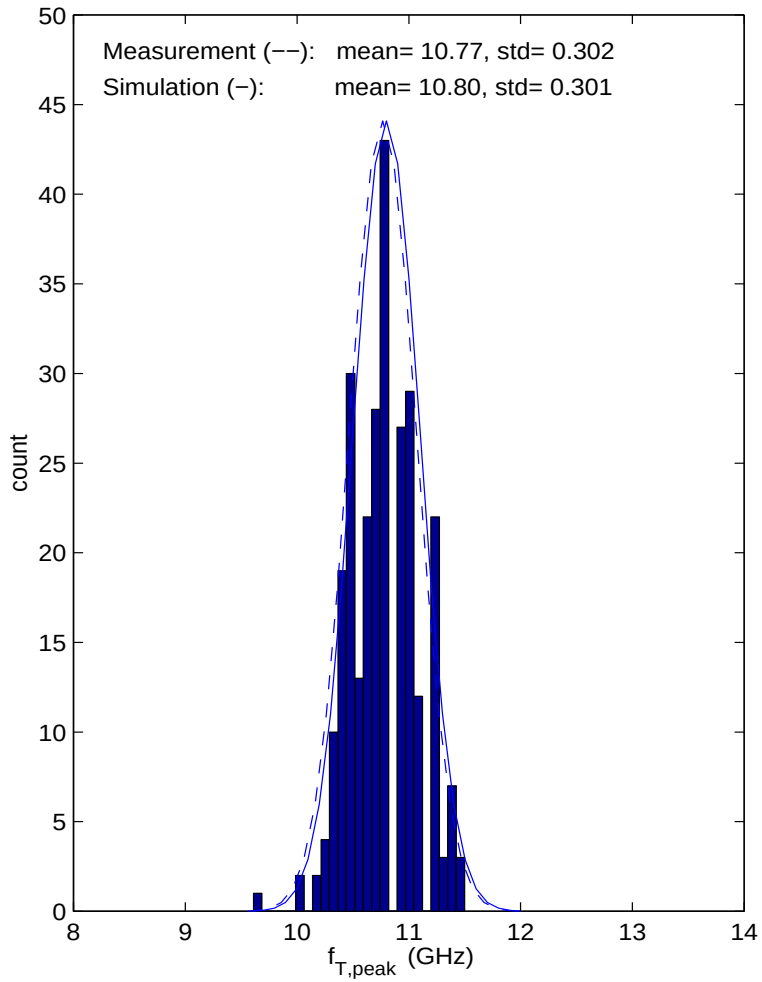
(a) (b)

Statistical distribution curves of peak f_T for a "high-speed" process. Comparison between (a) measurements and (b) HICUM predictions from process monitors. V_{CE} = 2 V; emitter size: 0.4*14 µm^2. The results were obtained from 5 different lots.

contd.: Statistical modeling



(a)

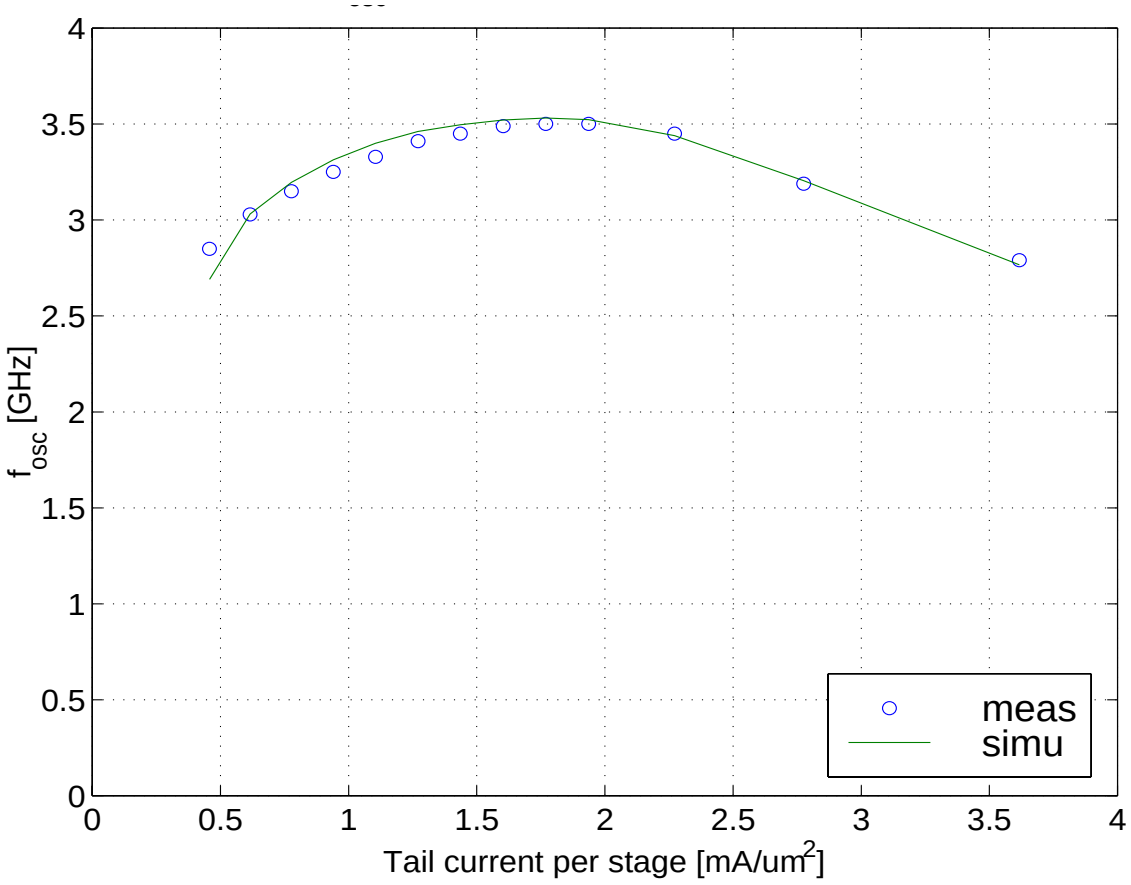


(b)

Statistical distribution curves of peak f_T for transistors with 0.4*14μm^2 emitter size. Comparison between measurements (histogram and solid lines) and HICUM predictions from process monitors (dashed lines): (a) “high-speed” process; (b) “high-voltage” process. The results were obtained from 5 different lots.

7.11 Circuit results

A few remarks are required here. In principle, there is agreement between design and modeling engineers that model validation on benchmark circuits is beneficial for both sides (cf chapter 4). However, this validation loop is rarely closed in an industrial environment for various reasons, such as simply the large schedule and product pressure on one hand and the very limited resources on the other hand. In addition, it is difficult to obtain agreement on which benchmark circuits satisfy at least the majority of design applications. For digital applications, often frequency dividers and ringoscillators consisting of CML or ECL gates are employed; experimental results for the latter will be shown below. For h.f. analog (e.g.. wireless) applications, not only the selection but also the design and testing itself is much more difficult. A larger variety of designs that are suited for on-wafer testing are required. As of now, results of only few production circuits are available that agree well with model “predictions”, but which have not been included here due to proprietary reasons.



Oscillation frequency f_{osc} vs. current density (I_{tail}/A_E) per stage for a CML ring-oscillator fabricated in a 25 GHz process; comparison between measurement (symbols) and HICUM (lines).
Due to power considerations, the smallest manufacturable emitter size ($0.4*0.7\mu m^2$) has been used; no specific or other model parameters were adjusted for this example.

9 References

[1] [Ant88] P. Antognetti and G. Massobrio, "Semiconductor device modelling with SPICE", McGraw-Hill, 1988.

[2] [STM] D. Celi, private communication.

[3] X.Y. Chen, M.J. Deen, Z.X. Yan, and M. Schroter, “Effects of emitter dimensions on low-frequency noise in double-polysilicon BJTs ”, Electronics Letters, Vol. 34, No. 2, pp. 219-220, 1998.

[4] X.Y. Chen, M.J. Deen, A.D. van Rheenen, Z.X. Yan, and M. Schroter, “Low-frequency noise in npn and pnp double-polysilicon BJTs, effects of temperature and emitter dimensions”, Proc. IEDMS, pp. - , 1998.

[5] M.J. Deen, S.L. Rumyantsev, and M. Schroter, “On the origin of 1/f noise in polysilicon emitter bipolar transistors”, J. Appl. Phys., Vol. 85, No. 2, pp. 1192-1195, 1999.

[6] [Get78] I.E. Getreu, "Modeling the bipolar transistor", Amsterdam: Elsevier Scient. Publ. Comp., 1978.

[7] [Fon95] N. Fong and M. Schröter, "Evaluation of emitter resistance measurement methods", Report, Bell Northern Research, 1995.

[8] [Gum69] H.K. Gummel, "On the definition of the cutoff frequency fT", Proc. IEEE, Vol. 57, pp. 2159, 1969.

[9] [Gum70] H.K. Gummel, "A charge-control relation for bipolar transistors", BSTJ, Vol. 49, pp. 115-120, 1970.

[10] [Gum70b] H.K. Gummel and Poon, "A integral charge-control model for bipolar transistors", BSTJ, Vol. 49, pp. 827-852, 1970.

[11] [Jac95] M. Jackson et al., "Picosecond large-signal switching characteristics of a pseudomorphic AlGaAs/InGaAs modulation-doped field effect transistor", Appl. Phys. Lett. 61, pp. 1187-1189, Sept. 1992.

[12] R. Dennison and K. Walter, “Local thermal effects in high performance bipolar devices/circuits”, Proc. IEEE Bipolar and BiCMOS Circuits and Technology Meeting, Minneapolis, pp. 164-167, 1989.

[13] [ICCAP] ICCAP, User's Manual, Hewlett-Packard, Semiconductor Systems Center, CA.

[14] C.T. Kirk, “A theory of transistor cutoff frequency falloff at high current densities”, IEEE Trans. Electron Dev., Vol. 9, pp. 914-920, 1962.

[15] [Kol93] A. Koldehoff, M. Schröter, and H.-M. Rein, "A compact bipolar transistor model for very high-frequency applications with special regard to narrow stripes and high current densities", Solid-State Electron., Vol. 36, pp. 1035-1048, 1993.

[16] T.-Y. Lee and M. Schröter, “Methodology for bipolar transistor model parameter extraction”, documentation for the CMC, (http://www.eigroup.org/cmc), Feb. 1999.

[17] [Mae] W. Maes, K. DeMeyer, and R. Van Overstraaten, “Impact ionization in silicon: a review and update”, Solid-State Electron., Vol. 33, pp. 705-718, 1990.

[18] [Mal90] C. Mallardeau et al., “A 12V BiCMOS technology for mixed analog-digital applications with high performance vertical pnp”, Proc. ESSDERC ‘90, pp. 397-400, 1990.

[19] [Mar71] P. Mars, "Temperature dependence of avalanche breakdown voltage in pn junctions", Int. J. Electronics, Vol. 32, No. 1, pp. 23-37, 1971.

[20] [Peh98] D.R. Pehlke, private communication, 1998.

[21] [Pfo95] M. Pfost, H.-M. Rein, and T. Holzwarth, "Modeling substrate effects in the design of high-speed Si bipolar ICs",. IEEE J. Solid-State Circuits, Vol. 31, pp. 1493-1502, 1996.
[22] R.L. Pritchard, “Transistor Characterictics”, McGraw Hill, 1967.
[23] [Rei83] H.-M. Rein, "Proper choice of the measuring frequency for determining fT of bipolar transistors", Solid-State Electronics, Vol. 26, pp. 75-82 and p. 929, 1983.
[24] [Rei84] H.-M. Rein, "A simple method for separation of the internal and external (peripheral) currents of bipolar transistors", Solid-State Electronics, Vol. 27, pp. 625-632, 1984.
[25] [Rei85] H.-M. Rein, H. Stübing, and M. Schröter, "Verification of the Integral Charge-Control Relation for high-speed bipolar transistors at high current densities", IEEE Trans. Electron Dev., Vol. 32, pp. 1070-1076, 1985.
[26] [Rei87] H.-M. Rein and M. Schröter, "A compact physical large-signal model for high-speed bipolar transistors at high current densities - Part II: Two-dimensional model and experimental results", IEEE Trans. Electron Dev., Vol . 34, pp. 1752-1761, 1987.
[27] [Rei89] H.-M. Rein and M. Schröter, "Base spreading resistance of square emitter transistors and its dependence on current crowding", IEEE Trans. Electron Dev., Vol. 36, pp. 770-773, 1989.
[28] [Rei91] H.-M. Rein and M. Schröter, "Experimental determination of the internal base sheet resistance of bipolar transistors under forward-bias conditions", Solid-State Electron., Vol. 34, pp. 301-308, 1991.
[29] [Rei92] H.-M. Rein, M. Schröter, A. Koldehoff, and K. Wörner, "A semi-physical bipolar transistor model for the design of very high-frequency analog ICs", Proc. IEEE Bipolar and BiCMOS Circuits and Technology Meeting, Minneapolis, pp. 217-220, 1992.
[30] [Rei94] H.-M. Rein and M. Friedrich, "Anomalies in the output conductance of SiGe HBTs", Proc. IEDM, pp. 94-97, 1994.
[31] [Rsc92] M. Reisch, "Self-heating in BJT circuit parameter extraction", Solid-State Electronics, Vol. 35, pp. 677-679, 1992.
[32] [Sch84] M. Schröter and H.-M. Rein, "Two-dimensional modelling of high-speed bipolar transistors at high current densities using the Integral Charge-Control Relation relation", Proc. ESSDERC '84; see also: Physica B, North Holland Phys. Publ. Div., pp. 332-336, 1985.
[33] [Sch86] M. Schröter and H.-M. Rein, "A compact physical large-signal model for high-speed bipolar transistors including the high-current region" (in German), NTG meeting, Würzburg, Mai 1986.
[34] [Sch87] M. Schröter, "A compact physical large-signal model for high-speed bipolar transistors with special regard to high current densities and two-dimensional effects", (in German), Dissertation, Ruhr-University Bochum, Bochum, Germany, Jan. 1988.
[35] [Sch89] M. Schröter and H.-M. Rein, "Transit time of high-speed bipolar transistors in dependence on operating point, technological parameters, and temperature", Proc. IEEE Bipolar Circuits and Technology Meeting, Minneapolis, pp. 85-88, 1991.
[36] [Sch91a] M. Schröter, "Simulation and modelling of the low-frequency base resistance of bipolar transistors in dependence on current and geometry", IEEE Trans. Electron Dev., Vol. 38, pp. 538-544, 1991.
[37] [Sch91c] M. Schröter, "Transient and small-signal high-frequency simulation of numerical device models embedded in an external circuit", COMPEL, Vol. 10, No. 4, pp. 377-378, 1991.
[38] [Sch92] M. Schröter, "Modeling of the low-frequency base resistance of single base contact bipolar transistors", IEEE Trans. Electron Dev., Vol. 39, pp. 1966-1968, 1992.

[39] [Sch93a] M. Schröter, "A survey of present compact models for high-speed bipolar transistors", FREQUENZ, Vol. 47, pp. 178-190, 1993.
[40] [Sch93b] M. Schröter, M. Friedrich, and H.-M. Rein, " A generalized Integral Charge-Control Relation and its application to compact models for silicon based HBT's", IEEE Trans. Electron Dev., Vol. 40, pp. 2036-2046,1993.
[41] [Sch94] (a) M. Schröter, "Physical models for high-speed silicon bipolar transistors - A comparisonandoverview",(inGerman),Habilitationthesis,1994;(excerptsareavailableonrequest). (b) M. Schröter, "Bipolar transistor modelling for integrated circuit design", Graduate Course, Carleton Univesity, Ottawa, 1995.
[42] [Sch95] M. Schröter and H.-M. Rein, "Investigation of very fast and high-current transients in digital bipolar circuits by using a new compact model and a device simulator", IEEE J. Solid-State Circuits, Vol. 30, pp. 551-562, 1995.
[43] [Sch96] M. Schröter and D.J. Walkey, "Physical modeling of lateral scaling in bipolar transistors", IEEE J. Solid-State Circuits, Vol. 31, pp. 1484-1491, 1996.
[44] [Sch98a] M. Schröter, Z. Yan, T.-Y Lee, and W. Shi, "A compact tunneling current and collector breakdown model", Proc. IEEE Bipolar Circuits and Technology Meeting, Minneapolis, pp. 203-206, 1998.
[45] [Sch98] M. Schröter and T.-Y. Lee, “HICUM - a physics-based scaleable compact bipolar transistor model“, presentation to the Compact Model Council, Dec. 1998.
[46] [Sch99a] M. Schröter and T.-Y. Lee., "A physics-based minority charge and transit time model for bipolar transistors", IEEE Trans. Electron Dev., vol. 46, pp. 288-300, 1999.
[47] [Sch99b] M. Schröter et al., “Physics- and process-based bipolar transistor modeling for integrated circuit design", accepted for publication in IEEE Journal of Solid-State Circuits, vol. 34 , pp. , 1999.
[48] [Stü87] H. Stübing and H.-M. Rein, " A compact physical large-signal model for high-speed bipolar transistors at high current densities - Part I: One-dimensional model", IEEE Trans. Electron Dev., vol. 34, pp. 1741-1751, 1987.
[49] [Sze81] S. Sze, "Physics of semiconductor devices", Wiley & Sons, New York, 1981.
[50] [TRADI] M. Schröter, "TRADICA - A program for dimensioning and calculation of integrated bipolar transistors", Manual Version 4.1, June 1996.
[51] H.Q. Tran, “Investigation of SiGe heterojunction bipolar transistors with respect to compact modeling for integrated circuit design”, M.EE. thesis, Carleton University, Ottawa, Canada, 1997.
[52] [Tra97] H.Q. Tran et al., “Simultaneous extraction of thermal and emitter series resistances in bipolar transistors”, Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Minneapolis, pp., 1997.
[53] S. Voinigescu et al., “A scaleable high-frequency noise model for bipolar transistors and its application to optimal transistor sizing for low-noise amplifier design“, IEEE J. Sol.-St. Circ., Vol. 32, pp. 1430-1439, 1997.
[54] [Wal95] D. Walkey, M. Schröter, and S. Voinigescu, "Predictive Modeling of lateral scaling of bipolar transistors", Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting, Minneapolis, pp. 74-77, 1995.
[55] [Wei78] P.B. Weil and L.P. McNamee "Simulation of excess phase in bipolar transistors", IEEE Trans. Circ. Syst., Vol. 25, pp. 114-116, 1978.
[56] [Win73] J. TeWinkel, "Extended charge-control model for bipolar transistors", IEEE Trans. Electron Dev., Vol. 20, pp. 389-394, 1973.