HICUM status update

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Outline

• Introduction
• HICUM status and development
• Parameter extraction
• Model generation
• Summary
Introduction

- bipolar technology development accelerated after integration into CMOS
  - low-cost Si-BiCMOS
  - high-performance SiGe-BiCMOS
- high-frequency process features
  => process complexity ↑
  => process (mask) cost ↑
  => need to reduce design iterations
- good modeling is part of the solution
- large variety of transistor designs
  - self-aligned BJTs
  - SiGe (non-selective epi, selective epi, LEC)
  - III-V HBTs (mesa)
  - VPNPs (low-cost, high-performance)
  - ... + flavors (high-speed, high-voltage)
- ... and a large variety of configurations

goal of this presentation: provide overview on status of HICUM and related activities
Status of HICUM

Overview

• Version 2.1: simulator availability

• HICUM/Level2: migration to version 2.2

• model development

• simulator implementation and support (issues)
Equivalent circuit (large-signal)
HICUM/Level2 v2.1 for Si and Si/SiGe bipolar transistors
Availability of HICUM/Level2 V2.1 in Circuit Simulators

(Please contact simulator vendor for details and the latest status of availability)

<table>
<thead>
<tr>
<th>simulator</th>
<th>first release</th>
<th>latest release</th>
<th>comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>ELDO-RF</td>
<td>10/99</td>
<td>7/03</td>
<td>ELDO v6.1 with externally accessible thermal node</td>
</tr>
<tr>
<td>SPECTRE-RF</td>
<td>10/99</td>
<td>11/01...</td>
<td>version &gt; 446.100.70 with HICUM2.1</td>
</tr>
<tr>
<td>ADS</td>
<td>7/00</td>
<td>5/03</td>
<td>(combined with ICCAP); also, first version ADS2003</td>
</tr>
<tr>
<td>Smart-SPICE</td>
<td>11/00</td>
<td>11/00</td>
<td>can be combined with UTMOST</td>
</tr>
<tr>
<td>APLAC</td>
<td>10/01</td>
<td>6/03</td>
<td>APLAC 7.62a; new release upcoming in 03</td>
</tr>
<tr>
<td>HSPICE</td>
<td>2/01</td>
<td>2/02</td>
<td>version 2001.2 with HICUM2.0; AURORA compatible</td>
</tr>
<tr>
<td>TEKSPICE</td>
<td>8/02</td>
<td>8/02</td>
<td>various numerical improvements</td>
</tr>
<tr>
<td>Xpedion</td>
<td>?/03</td>
<td>?/03</td>
<td>(available according to customers)</td>
</tr>
<tr>
<td>SPICE3F5</td>
<td>4/02</td>
<td>4/02</td>
<td>reference circuit simulator</td>
</tr>
</tbody>
</table>

Apache NSpice, HSIM, MicrowaveOffice (HICUM/L0): code sent as per request, implementation in progress

- Various (other) proprietary simulators (ASX (IBM), ...)
- Verilog-A version of model code; also, stand-alone kit enabling coupling with other tools
HICUM/Level2 version 2.2 - List of major improvements

numerical formulation, implementation, documentation

- robust formulation of current spreading function at (very) small LATL, LATB (large transistors)
- improved formulations: substrate transistor equations, limiting numbers, hyperbolic smoothing, ...
- simplify QJC and CJC formulation at forward bias
  (e.g. linearize CJCI @ high forward bias => possible “kink” in g₀ disappears)
- replace numerical derivatives by analytical derivatives
- improved s.h. derivatives
  (problem: this is handled differently in simulators)

  model compilers will take care of derivatives in future

- manual
  - extensions for V2.2 features
  - corrections
  - derivation of model equations ?
HICUM/Level2 version 2.2 (cont’d)
physics-based extensions
(delayed as per user request)

- temperature dependence of transfer current
  add parameter ACT: \((T/T0)^3 \to (T/T0)^\text{ACT}\) in IS and C10

- replace \(V_D(T)\) smoothing towards high \(T\) by physics-based smoothing (incl. BGN)

- base current
  - add parameter ABE, \(\text{VGEFF}: (T/T0)^3 \to (T/T0)^\text{ABE} \) in IBSi => nonlinear \(T\) dependence of current gain
  => improved formulation of emitter time constant (\(T\) dependence and smoothing)

- extension for modeling increase at high forward bias (due to collector barrier effect)

- parameter for splitting CEOX, IBETS between external and perimeter base node

- split CJS into bottom and perimeter portion: better done in subcircuit?

- recommendations for EDA companies:
  - include noise correlation between IB and IC (mainly for III/V HBTs)
  - flags for turning on/off: self-heating, vertical NQS effects, lateral NQS effects \((C_{rBl})\)
  - separate thermal node for thermal coupling
  - use nonlinear \(T\) dependent bandgap voltage \(VG(T)\) to guarantee same results across simulators
Major model development activities

• main effects in (advanced) SiGe HBTs (LEC-HBT, $f_T > 200$ GHz)
  • improved physics-based collector model => efficient calculation of high-current effects (incl. barrier effects), BC avalanche effect, current dependent BC capacitance
• 3D GiCCCR theory and application to compact model element definition
• high-frequency noise analysis and component decomposition
• Low-Emitter Concentration (LEC) SiGe HBTs

• III-V HBTs (AlGaAs, InGaAs, InP, ...)
  • non-stationary transport => impact on transit time and transit frequency (in certain III-V HBT processes)
  • geometry scaling (in conjunction with TRADICA)

• predictive and statistical modeling (in conjunction with TRADICA)
  • improved predictive equations
  • application to advanced SiGe processes (verification of critical 1D equations based on DEVICE)

• model verification for actual process data (with various industry partners)
  • benchmark circuit design: BGR, LNA (both on Infineon test chip)
  • PA device modeling (Atmel, Jazz, ST) => includes distortion (harmonic and intermodulation)
  • statistical modeling (Atmel, Jazz) => includes dynamic characteristics
Model support issues

demand for model support exceeds resources => requires funding for full-time engineer

• simulator implementation: commercial (EDA support)
  • model testing, verification of correct implementation => need “entity” to certify quality of implementation
• company specific interfaces
  => cannot support any of those anymore (but rather wait for model compilers)
  => these are main issues (license donation is only partially suitable as compensation for support effort)

Experience: effort and cost for commercial implementation is as large as for development

• simulator implementation: internal (for model development)
  • DEVICE (to avoid licensing and platform compatibility issues)
  • Verilog-A for distribution and model compilers
  • development tool, e.g. MATLAB, but probably migration to TRADICA (needed anyway) or stand-alone kit
  • MNA stand-alone kit (for linking model to extraction tools) => requested by some customers
  • symbolic tool for derivatives (e.g., MAPLE) => will be dropped once model compilers are available)

  => need to focus on Verilog-A, DEVICE, TRADICA [, stand-alone kit]

• parameter extraction
  • should a tool developed at CEDIC be made (publicly) available ?
    If yes, it needs to be commercialized in order to be able to pay for its support and updates !!
    => XMOD approach is one suitable option

• if CMC recommends a model and wants to control its releases => provide funding for support
Modeling the intrinsic collector current: homojunction transistors

- 1D (electron) transport equation: \( J_{nx} = -q\mu_n n \frac{d\varphi_n}{dx} \) with \( n = n_i \exp\left(\frac{\psi - \varphi_n}{V_T}\right) \)

- integration over total 1D transistor (\( \varphi_n(E_{contact}) = 0, \ varphi_n(C_{contact}) = V_{C,E'} \)) gives:

\[
J_T = (qV_T)^2 \mu_{nB} n_i^2 \frac{x(C)}{q} \int_{x(E')}^{x(C')} \frac{\mu_{nB} n_i^2}{J_T} \left[ \exp\left(\frac{V_{B'E'}}{V_T}\right) \left[ 1 - \exp\left(\frac{V_{CE'}}{V_T}\right) \right] \right] J_{nx}(x) \exp\left(\frac{V_{B'E'} - \varphi_p(x)}{V_T}\right) p(x) dx
\]

ideal voltage dependence

constant

weighting function \( h(x) \)

(note: \( J_T = J_C = I_C/A_E \))

- assumptions (for further evaluation):
  - negligible recombination (in \( J_{nx}(x) \) only)
  - sufficiently low frequency (\( \partial/\partial t = 0 \) in continuity equation)
  - spatially independent \( \mu_n n_i^2 \approx \mu_{nB} n_i^2 \) (referred to neutral base) \( \Rightarrow q \int_{x(E')}^{x(C')} h p dx = \tilde{h} Q_p \)
  - \( \varphi_p(x) = V_{B'E'} \) for all \( x \) where \( p(x) \) is significant
Modeling the intrinsic collector current
(Generalized) Integral Charge-Control Relation (GICCR)

- HICUM transfer current for BJTs

\[
i_T = \frac{(q A_E)^2 V_T \mu n_B^2}{c_{10}} \frac{\exp(v_{B'E}/V_T) - \exp(v_{B'C}/V_T)}{Q_p}
\]

split into components: \(i_T = i_{Tf} - i_{Tr}\)

- hole charge (in emitter, base, and collector region)

\[
Q_p = Q_{p0} + Q_{jEi}(v_{B'E}) + Q_{jCi}(v_{B'C}) + Q_m(i_T, v_{CE})
\]

- depletion charges:

\[
Q_{jEi} = q \int_0^{v_{BE}} C_{jEi}(v)dv \quad \text{and} \quad Q_{jCi} = q \int_0^{v_{BC}} C_{jCi}(v)dv
\]

- minority charge:

\[
Q_m(i_T, v_{CE}) = Q_f(i_{Tf}, v_{CE}) + Q_r(i_{Tr}, v_{CE})
\]

with forward and reverse component:

\[
Q_f = \int_0^{I_{Tf}} \tau_f di = Q_{fE} + Q_{fB} + Q_{fC} \quad \text{and} \quad Q_r = \tau_r i_{Tr}
\]
Model for the intrinsic transistor: heterojunction transistors

Extension of the transfer current using the GICCR

- weighting function
  \[ h(x) = \frac{\mu_{nB} n_{iB}^2}{\mu_{ni}^2} \frac{J_n}{J_T} \exp \left( \frac{V_{B'E'} - \phi_p}{V_T} \right) \]

- still valid: \( \phi_p(x) = V_{B'E'} \) and \( J_{nx} = J_T \)

- but now \( \mu_{ni}^2 \neq \mu_{nB} n_{iB}^2 \) outside of neutral base

- weighted hole charge (index “T” for transfer current)
  \[ Q_{p,T} = Q_{0} + h_{jEi} Q_{jEi}(v_{B'E'}) + h_{jCi} Q_{jCi}(v_{B'C'}) + Q_{f,T} + Q_{r,T} \]
  with the weighted forward minority charge
  \[ Q_{f,T}(v_{CE}) = h_{fE} Q_{fE} + h_{fB} Q_{fB} + h_{fC} Q_{fC} \]
  and \( Q_{f0} = \int_{i}^{i'} \tau_{f0}(i) \, di \) (\( v = E, B, C \)) in neutral regions

- weighting factors \( h_{jEi}, h_{jCi}, h_{fE}, h_{fC} \) represent mobility and bandgap variation in various regions (\( v = jEi, jCi, fE, fC \)): \( h_v = \frac{\mu_{nB} n_{iB}^2}{\mu_{n} n_{i}^2} \)

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Extension of the transfer current to HBTs (cont’d)  
... using the GICCR

- HICUM transfer current for (SiGe) HBTs

\[ i_T = c_{10} \frac{\exp(v_{B'E}/V_T) - \exp(v_{B'C}/V_T)}{Q_{p,T}} \]

⇒ functional form still the same
- charges in \( Q_{p,T} \) still the same as in transient analysis
- description of the material composition effects is fully physics-based

- relation to existing model formulations

\[ i_T = I_S \frac{\exp(v_{B'E}/V_T) - \exp(v_{B'C}/V_T)}{Q_{p,T}/Q_{p0}} \]

- normalized hole charges often contain lumped parameters (such as Early voltage, knee current)

- not included (according to transport equation)
  - thermionic emission
  - tunnelling
  ⇒ taken into account in HICUM by parameter \( m_{Cf} \)
Extension of the transfer current (cont’d): example
... for calculating the weighting factors

- box doping profile
- linear composition grading

• weighting factor for the BC depletion charge

\[ h_{jC_i} = \begin{cases} 
1 & \text{, box} \\
\frac{\Delta V_{G,B}/V_T}{\exp(\Delta V_{G,B}/V_T) - 1} & \text{, triangular grading} 
\end{cases} \]

• resulting Early voltage

\[ V_{Ef} = \frac{Q_{p0}}{h_{jC_i} C_{jC_i0}} = \frac{Q_{p0}}{C_{jC_i0}} \begin{cases} 
1 & \text{, box} \\
\frac{\exp(\Delta V_{G,B}/V_T) - 1}{\Delta V_{G,B}/V_T} & \text{, triang.} 
\end{cases} \]

is a function of bias and material composition
⇒ fully physics-based expression !!

• similar expressions can be derived for
  • other weighting factors
  • a variety of doping and composition profiles
  • weighting factors are close to 1 in conventional homojunction BJTs
Model for the intrinsic HBT: base current
additional current at high forward bias

- at high forward bias, the electric field at the BC junction decreases
  ⇒ high-current effects, onset described by \( I_{CK} \)
  ⇒ formation of dipole layer
    (i.e. pile-up of holes “before” the Ge drop)
  ⇒ conduction band barrier
  ⇒ pile-up of electrons
  ⇒ increased recombination
  ⇒ increase of base current

- observable in 1D case (no series resistances)
- add’l current component can be modelled as

\[
\Delta J_B = \frac{\Delta Q_{fB}}{\tau_{jcr}}
\]

- in 2D case: effect in possibly masked by series resistances
  ⇒ difficulty for extracting parameter \( \tau_{jcr} \)
FAQs

• how is the Early-effect being modelled in HICUM? $V_{Af} = I_T f \left( \frac{dI_T f}{dV_{CB}} \right)_{V_{BE}}^{-1} \approx \frac{Q_p}{\eta_{jet} C_{jCj}}$ @ low $J_C$

• where is the bias dependent internal collector resistance? $r_{Ci}$ is included in the minority charge formulation = impact on
  - DC characteristics via GICCR
  - dynamic behavior via the transit time (as time constant)

• self-heating:
  - cause for divergence for (strong) s.h.? s.h. is a positive feedback mechanism => inherently unstable => stability depends on implementation and circuit measures (e.g., ballast resistance)
  - there should be no impact on $f_T$ due to the large thermal time constant (make sure to have $R_{TH} C_{TH} >> \tau_{elec}$)

• a kink in IC-VCE (or output conductance) under hard saturation ... is associated with
  - the formulation of the transit time as function of $V_{BC}$ (via $C_{jCj}$) (developing a truly physics-based formulation, its implementation and test cost effort and CPU time)
FAQs (cont’d)

how to use the additional thermal node?

• interaction between 2 heat sources

\[ \Delta T_1 = R_{TH,1}P_1 + c_{12}\Delta T_{22} \]
\[ \Delta T_2 = c_{21}\Delta T_{11} + R_{TH,2}P_2 \]

with the thermal coupling coefficients

\[ c_{12} = \frac{R_{TH,12}}{R_{TH,2}} , \quad c_{21} = \frac{R_{TH,21}}{R_{TH,1}} \]

• realization in a compact model using the externally accessible thermal node:

VCVS approach

\[ P_k \uparrow R_{TH} \rightarrow \infty R_{TH,k} \downarrow \Delta T_{kk} \]
\[ \sum_{j=1, j \neq k}^{K} c_{kj} \Delta T_{jj} \]
Emitter periphery effects and effective emitter area

- transfer current $\Rightarrow$ carrier injection into base (2D-case)

$$I_T = \frac{I_{Ti}}{A_{E0}} + I_{Tp}P_{E0} = \frac{I_{Ti}}{A_{E0}} \left(1 + \frac{I_{Tp}}{I_{Ti}} \frac{P_{E0}}{A_{E0}} \right) = I_{Ti} A_E$$ (1)

$\Rightarrow$ merging internal and peripheral transistor into single transistor with effective electrical emitter width $b_E$ and area $A_E$

(Note: $I_{Ti} = J_{Ti} = 1D$ transfer current from GICCR)

- minority charge $Q_{fp}$ is associated with perimeter carrier injection

$\Rightarrow$ merge minority charge into single charge storage element with $Q_f(I_T) = Q_{fi} + Q_{fp}$ and single $\tau_f(I_T)$

- apply $A_E$ as defined from $I_T$ to base current and depletion charges

$\Rightarrow$ effective internal quantities $I_{jBEi}, I_{jBCi}, Q_{jEi}, Q_{jCi}$ and $\Rightarrow$ remaining perimeter quantities $I_{jBEP}, C_{jEp}$ (if $\gamma_B > \gamma_C, \gamma_{jE} > \gamma_C$)

- define effective internal base resistance $r^*_B, C_i = r_{Bi} (C_i - C_{dEp})$ that maintains same input time constant

$\Rightarrow$ equivalent circuit for “effective” internal transistor

emitter window dimensions:

$A_{E0} = b_{E0} l_{E0}$

$P_{E0} = 2(b_{E0} + l_{E0})$
**Parameter extraction**

- biggest obstacle for deploying a (new) model in industry
  - most companies still like to have their own infrastructure, only slowly changing situation
  - often still a fitting exercise rather than a well-defined physics-based approach

- model accuracy depends on extraction = the best model is useless with wrong parameters

- requires continuous adaption to process (and model) development

- do you know all possible error sources?

- single device vs geometry scalable extraction method

- what’s available for HICUM right now
  - single device extraction: HICUM-Aperitif from XMOD Technologies, based on ICCAP
  - geometry scalable: (i) extension of HICUM-Aperitif (under construction)
    (ii) being integrated into TRADICA
    (iii) documented procedure for building in-house infrastructure
Thoughts on geometry scalable extraction

size variations (compared to layout dimensions) are unavoidable

• extracted parameters only correspond to measured die (at best) => never see these devices again

• single geometry extraction may assign model parameter set to incorrect size

• problem should be treated statistically (which is the nature of the variations)
  => the more devices are being used for extraction the better the "average" model accuracy

=> alternatives

use more data of the "same" geometry
  => single geometry extraction

=> ideally: average values of parameters
actually: unavoidable errors due to fitting
  are also included, often yields
  non-physical values

=> no predictive capability (electrical, process variations)

uses multiple geometry devices
  => geometry scalable extraction

=> average out geometry uncertainty,
  (more) physical parameters ...

=> fundamentally more accurate than single device geometry extraction

=> enables predictive and statistical design,
  model hierarchy
Geometry scalable extraction - revisited

• consider \( \frac{C}{A_0} = \bar{C} + C' \frac{P_0}{A_0} \) with \( \bar{C}, C' \) as area and perimeter specific parameters to be extracted from measured \( C \), window area \( A_0 = b_0 l_0 \) and window perimeter \( P_0 = 2(b_0 + l_0) \)

• measurement error sources:
  • electrical and intra-die (variation of \( C \)): \( \Delta C \)
  • geometry (assuming width and length vary uncorrelated, but with the same absolute value): \( \Delta b \)

• propagation of errors (cf. P. Bevington, "Data reduction and error analysis for the physical sciences") \( \Rightarrow \) error range for

  • the y-axis \( \frac{\Delta C}{C} = \sqrt{\frac{\Delta C}{C} + \Delta b_0 \left( \frac{1}{2} + \frac{1}{2} \right)} \)

  • the x-axis \( \Delta \left( \frac{P_0}{A_0} \right) = 2 \Delta b_0 \sqrt{\frac{1}{4 \ b_0} + \frac{1}{4 \ l_0}} \)

• experimental example see W. Kraus, ICCAP-Workshop 2002, Berlin, Germany
Impact of width uncertainty on capacitance determination

- assumptions
  - test structures with layout dimensions \( b_0 \ll l_0 \) => elimination of \( l_0 \) variation
  - actual emitter width \( b = b_0 + \Delta b \) with \( \Delta b \) as uncertainty or width variation

- use standard equation => area specific component \( \bar{C}_A = \text{value extrapolated to } b \to \infty \)
  - subtract standard equation for two different \( b \) (e.g. large and small \( b \))
    => perimeter specific component \( \bar{C}_{P0} \) from layout \((b_0, l_0)\) as function of actual (measured) \( \bar{C}_P \):

\[
\bar{C}_{P0} = \frac{\bar{C}_P + \frac{C}{l_0b_0} \frac{\Delta b}{2b_0}}{1 + \Delta b / b_0} \quad \Rightarrow \quad \text{for } \Delta b < 0 : \quad \bar{C}_{P0} = \frac{\bar{C}_P - \frac{C}{l_0b_0} \frac{|\Delta b|}{2b_0}}{1 - |\Delta b| / b_0}
\]

![Graph showing \( \bar{C}_P \), \( \bar{C}_{P0} \), and \( \bar{C}_A \) as functions of \( \Delta b \)]
BE capacitance in advanced SiGe processes

- trends:
  - \( x_{JE} \downarrow \Rightarrow N_{Bi} \uparrow \Rightarrow C_A \uparrow, C_P \downarrow \)
  - SiGe epi \( \Rightarrow N_{Bp} \downarrow \Rightarrow C_P \downarrow \)
  \[ \frac{C_P}{C_A} \downarrow \]

**BE spacer structure at emitter perimeter**

- Si cap layer grown during SiGe deposition is only lightly doped
  => punch-through of SCR at the perimeter (e.g. \( N = 10^{17} \text{cm}^{-3} \Rightarrow w_{SCR} = 0.1 \mu\text{m} \))
  => bias independent (specific) perimeter capacitance
  => indistinguishable from oxide capacitance \( C_{Eox} \) during parameter extraction
... self-heating

- unavoidable in modern processes during measurements (at higher current densities)

- need to be either included or avoided during extraction
  - include by using corrections (mostly model-based with measured TCs)
  - avoid by using pulsed measurements
  - avoid by using proper test structures and extraction methodology; example:
    determine series resistances from test structures rather than from I-V characteristics at high $J_C$

- trends for self-heating:
  - power dissipation is proportional to $A_{E0}$ (and thus $n_E$)
  - $R_{th}$ is less than proportional to emitter dimensions

  \[ \left\{ \begin{array}{c}
  \text{use } n_E = 1 \text{ for extraction, limit } l_{E0}
  \end{array} \right. \]
Review of error sources that can lead to model inaccuracy

- equipment:
  - chuck, wafer and device temperature
  - calibration substrate, cables, power and flatness, ...

- measurement:
  - bias point (e.g. need $I_C$, not $V_{BE}$ $=>$ $I_C$), S-parameters (magnitude, phase)
  - signal-amplitude (must be small enough to avoid distortion, but large enough for accurate detection)
  - de-embedding:
    - complexity (multi-step) depends on frequency
    - less structures available than DUTs $=>$ equivalent circuit or scalable de-embedding models

- device geometry
  - lateral dimensions (e.g. emitter size) $=>$ can be a function of topography (lithography)
  - vertical dimensions (can be a function of lateral dimensions)
  - process tolerances $=>$ variation from die to die ...

- model
  - validity limits (equations, equivalent circuit)
  - fit/optimization of characteristics (limited accuracy, selection of unsuitable characteristics,...)
Model generation

Trends in Communication Systems ... and impact on modeling requirements ...
higher frequencies (Broadband) ... effects have impact on circuit performance (noise, linearity/ACPR, ...) and modeling
⇒ need flexible modeling approach for reducing design iterations and cost
Geometry scaling

SiGe HBT example: dealing with different device designs . . .

. . . and configurations

. . . is accomplished by parameter generation and sizing tool TRADICA
TRADICA Overview

Process control monitor (PCM) data

Process specific parameters
sheet resistances, capacitances per area, sat. currents per area, ...

Design rules

Transistor configurations
E width and length, number of E, B, C stripes, location ...

TRADICA

model parameters
• device libraries
• for specified bias points

critical bias points ⇒ transistor sizing

model characteristics
(fT, fmax, NFmin ... as function of geometry and bias)
Model library

* fast generation of model parameter output for circuit simulators

... model library

* T1 AE0= 1* .20* 2.67( 1); NB= 2( ) ; NC=1(SIDE); T=300; Example

* HICUM/ Level 2 / ELDO

.SUBCKT N020261S02_01 3 2 1 9

Q 3 2 1 9 MOD

.MODEL MOD NPN level=9 TNOM= 26.85

+ c10=2.20E-32 qp0=4.66E-15 ich=5.82E+01 hjci=0.38 hfc=1.0 hjei=1.00

+ cjei0=2.91E-15 vdei=1.000 zei=.400 aljei= 2.20

+ cjlci0=6.99E-16 vdc= .850 zci=.286 vptci=3.50E+01

+ t0 =6.81E-13 d0h= 7.500E-13 tbulk=8.000E-13

+ tef0=1.00E-13 gtfe= 1.00 thcs=3.00E-11 alhc=0.200 fthc=0.426

+ rci0=1.03E+02 vlim= 1.000 vpt= 15.00 vces=.130

+ latb=5.417E+00 latl= .443

+ ibeis=1.75E-20 mbei=1.0100 ireis=1.75E-14 mrei=2.0000

+ alit=.450 FAVL=.20

+ favl= 1.000

+ rbi0= 77.97

+ ibeps=1.51E+01 bias point: JC [mA/um^2] = 1.691  VCE [V] = .800  VSC [V] = 3.000  T [K] = 30

+ rcx= 29.68 circuit: SG150 (SGPM ) f [GHz] = .0 (for NF)

+ ibcx=1.92E+01 rhoCi [Ohm cm] = .064 (NCi [1/cm^3] =1.63E+17) rhoSu [Ohm cm] = 6.13

+ cjcx=2.25E+01 configur. Tf CBE CjCi rBi CCBx rBx rE rCx CCS gm fT fm

(b 1 nE nB nC)[ps] [fF] [fF] [fF] [fF] [fF] [fF] [fF] [fF] [fF] [fF] [fF]

+ cjs=3.81E+01 [mS] [GHz] [C]

+ vgb= 1.170

+ alces=4.001

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Model complexity and hierarchy

HICUM/Level0 ➞ conceptual phase

HICUM/Level2 ➞ optimization and validation

HICUM/Level4 ➞ special applications (e.g., distributed effects)

(Note: model generation is based on HICUM/Level2 parameter extraction only!)
Example for electrically distributed model
Simulated load circles at 0.9, 2.4, 5.2 GHz

comparison of Level2 (lumped, o) and Level4 (distributed, *) at 2.4GHz
Integration of TRADICA into Cadence Design Framework

transistor specification in schematic capture:

```
<p>| | |</p>
<table>
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<tr>
<td>Q15</td>
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</table>
emitter width [µm]: 1.0
emitter length [µm]: 20.0
number of emitters: 2
number of bases: 1
number of collectors: 2
collector location: side
parallel devices: 1
contact sequence: CEBEC
```

Benefits:

- statistical and matching simulation
- circuit **optimization** via consistently scalable transistor models
- parameter transfer via single "technology" file (xxxx.DTA)

⇒ significant functionality enhancement for design at reduced maintenance effort for foundry
Summary

• HICUM/Level2 version 2.1 is available in many simulators

• HICUM/Level2 version 2.2 addresses mainly
  • simulation speed
  • temperature dependence
  • parasitic physical effects in advanced SiGe HBTs

• production libraries for HICUM/Level2 v2.1 have been delivered by
  • Atmel: SiGe1 (45 GHz HBT)
  • Conexant: B25 (25GHz BJT), BC35 (35GHz BJT)
  • Jazz: SBC35 (60GHz HBT), SBC18 (120 GHz HBT)

=> model is already being used by many design houses

• parameter extraction
  • different options are available
  • continuous development towards improving methodology and techniques

• model generation
  • can achieve generic and very efficient generation if geometry scalable approach is used
  • hierarchy of models
  • automated generation of other models