

HICUM - Update

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www.iee.et.tu-dresden.de/iee/eb/eb_homee.html

Outline

- Availability in simulators
- Model support
- Roadmap (migration and future development)

Availability in Simulators

simulator	code made available	implement. ongoing	test phase	release	comments
ELDO-RF				10/99	available to customers
SPECTRE-RF				10/99	<ul style="list-style-type: none"> • documentation being cleaned up • CNXT version = ref. for release
ADS				7/00	<ul style="list-style-type: none"> • combination with ICCAP • excess phases: ADS related issue
Smart-SPICE				11/00	<ul style="list-style-type: none"> • combination with UTMOST
APLAC		x (?)			target release date: 11/00
HSPICE			x		<ul style="list-style-type: none"> • combination with AURORA
Xpedion	x				code sent as per request
SABER	x				code sent as per request
TEKSPICE					in cooperation with MAXIM
DEVICE	-	-	-	-	reference simulator (except HB)

Model support

Software and general maintenance (CMC)

- support of implementation in circuit simulators
 - timely bug fixing
 - provide and maintain “original” model code; version control of “original” model code
 - testing and qualification of implementation - options:
 - provide test parameters and data to EDA companies
 - test at CEDIC (depending upon simulator license)
 - model documentation
 - parameter list and default values (zeroed and test); OP output in simulators
 - physical background of the model and its equations
 - support of parameter extraction
(provide generic, i.e. not tool specific, support for implementing parameter extraction sequence in commercial software packages)
 - maintain web-site
- ⇒ full-time service that has to be paid for to ensure certain quality
- ⇒ hire a person for this job (post-doc, ...)
- contingent on commitment for funding (from CMC or other sources)
- Cost estimate:
 - loaded labor cost: US \$50k (at the present exchange ratio)
(need to pay reasonable salary, otherwise loose person to industry)
 - travel expenses: US \$6k (to attend 4 CMC meetings/year)

Note: effort and cost are basically the same as for MOS models ...

Model development support

Semiconductor industry

- present cooperation partners (and contacts)
 - Alcatel (E. Gerhardt)
 - Atmel (W. Kraus)
 - Conexant (M. Matloubian, P. Zampardi)
 - IBM (D. Hame, J. Johnson, K. Newton, ...)
 - Infineon (P. Brenner, J. Berkner, ...)
 - Maxim (S. Simpkins, D. Harper, ...)
 - Motorola (C. McAndrew)
 - Silicon Wave
 - STM (A. Juge, D. Celi, ...)
- Activities include projects in the areas of
 - modeling
 - establishing geometry scalable parameter extraction and model parameter generation; transfer and implementation of appropriate test structures.
 - predictive and statistical modeling
 - extraction of “pilot” parameter sets
 - *extensions: suggestions of improvements and participation in development are encouraged and welcome* - will continue to do coordination
 - circuit design
 - courses on modeling and response to application relevant questions
 - benchmark circuit design
 - process development
 - feedback and debugging via special test structures and physics-based parameter extraction
 - model parameter prediction for next generation processes

⇒ most of the time is presently being spent on the above tasks

Documentation

[www: eigroup.org/cmc](http://www.eigroup.org/cmc) and iee.et.tu-dresden.de/iee/eb/eb_homee.html

- Model description
 - www: updated equations and default values for parameters; new OP data suggestion
 - complete CMC presentation of Dec. 98 can be obtained from: mschroter@iee.org
- Model parameter extraction
 - www: generic extraction procedure (incl. basic idea of some test structures)
 - www: overview on recommended measurements
 - detailed description of test structures (for cooperation partners)
 - detailed description of geometry scalable parameter extraction (for cooperation partners)
- Experimental results on many different processes
 - see www: geometry scalable models for production processes
 - see www: fitted on single transistors (mostly CMC data sets)

Roadmap

Migration path: options, suggestions, and overview on “investment”

- ... from single transistor fitting to geometry scalable modeling capability
 - implement appropriate test structures (also useful for process monitoring and debugging)
 - implement multiple geometry parameter extraction sequence (similar to CMOS)
 - ... from SGPM to HICUM - assuming geometry scalable modeling capability
 - understand (physical) background of HICUM to maximize its usefulness
 - incremental additional effort for extracting model-specific parameters of HICUM
 - library generation: parameters of both models can be generated at the same time (e.g., by TRADICA)
 - ... from SGPM to HICUM - assuming single transistor fitting
 - understand how to simplify HICUM
 - implement simplified, fitting based, parameter extraction sequence
- ⇒ documentation and courses are available to facilitate the migration and to support associated activities
(limited information on single-transistor-fitting though)

Model development

(mostly industrially funded activities)

- **SiGe HBTs (both types)**
 - issues in >50GHz processes
 - incorporation of features from SiGeM (s. Prof. Rein's group at RUB) where possible
- **III-V HBTs**
 - measurement based verification for industrial processes
 - electrothermal modeling
- **VPNP modeling**
 - verification of suitability; parameter extraction and TRADICA capability
(initial results for minority charge and transit time model (s. D. Celi/STM, 1998) are encouraging)
- **Parameter extraction**
 - develop improved/new methods and improve reliability of extraction
- **Simple version (Level0)**
 - finalize and implementation
 - parameter extraction: either from Level2 data or directly on single devices; i.e. no extra effort for user

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