Physics- and process-based bipolar transistor modeling for integrated circuit design
Motivation

• Increasing demand on circuit performance → often requires transistor operation close to the process performance limit ⇒ careful circuit optimization through proper transistor sizing

• Large variety of circuit applications → overall required number of transistor configurations\(^1\) can become very large (\(>100\)) ⇒ need geometry scalable compact models and parameters

• Reduce time-to-market: start circuit design during process development (concurrent engineering) ⇒ predicted but consistent model parameters and flexible parameter generation

• Align process development with product (design) needs ⇒ quick evaluation of process change impact on electrical device and circuit performance

• Include process tolerances in design (⇒ statistical modeling, matching simulation)

• Large variety of bipolar processes requires sophisticated geometry scaling equations that are difficult to integrate and maintain in large variety of (commercial) circuit simulators

⇒ TRADICA

\(^1\) defined by emitter dimensions \(b_{E0}\) and \(l_{E0}\) (\(\geq b_{E0}\)), number of emitter, base, and collector fingers/contacts and their spatial arrangement
TRADICA overview

**Process specific parameters**
- general: sheet resistances, capacitance per area ....
- compact model related: saturation current density, transit time ...

**Process control monitor (PCM) data**

**Transistor configurations**
- emitter width and length
- number of E, B, C stripes

**Design rules**

**Model parameters**
- device libraries
- for specified bias points

**Model characteristics**
(fT, fmax, NFmin ... as function of geometry and bias)

⇒ transistor sizing
Example
model parameters (base resistance, transconductance etc.) and model characteristics (transit frequency, noise figure etc.)
can be quickly calculated and displayed as a function of bias and geometry

internal base resistance @ VCE = 0.8V
noise figure (50 Ω) @ VCE = 0.8V, f = 2 GHz
Example (cont’d)

data output ...

... model library

* x      AE0= 1*  .20*  2.67( 1); NB= 2(   );
NC=1(SIDE),SIC;T=300;Example
* HICUM/ Level 2 / ELD0
V5.0
.SUBCKT N020261S02_01 3 2 1 9
  Q    3 2 1 9 MOD
.MODEL MOD NPN level=9 TNOM= 26.85
  + c10=2.20E-32 qp0=4.66E-15 ich=5.82E+01 hjci= .38 hfc=
hjei= 1.00
  + cjei0=2.91E-15 vdei=1.000 zei= .400 aljei= 2.20
  + cjc10=6.99E-16 vdc1= .850 zci= .286 vptc1=3.50E+01
  + t0 =6.81E-13 dt0h= 7.500E-13 tblv=8.000E-13
  + tef0=1.00E-13 gtfe= 1.00 thcs=3.00E-11 alhc= .200 ft:
  + rci0=1.03E+02 vlim= 1.000 vpt= 15.00 vces= .130
  + latb=5.417E+00 latl= .443
  + ibeis=1.75E-20 mbei=1.0100
  + ireis=1.75E-14 mrei=2.0000
  + alit= .450 alqf= .220
  + favl= 1.000 qavl=8.74E-15
  + rbi0= 77.97 fgeo= .7227 fdqr0= .200 fcrbi= .00 fqi= .
  + ibeps=1.51E-20 mbep=1.0100
  + ireps=1.51E-14 mrep=2.0000
  + ibets=5.58E-16 abet= 40.00

... bias point information

TRADICA VERSION 5.0

bias dependent vnpn transistor parameters process:

bias point:  JC [mA/um^2] = 1.691  VCE [V] = .800  VSC
circuit: SG150  (SGPM ) f [ rhoCi [Ohm cm] = .064 (NCi [1/cm^3] =1.63E+17) rho

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<td>02*026 1 02S1</td>
<td>.7</td>
<td>13.0</td>
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Integration into a geometry scalable parameter extraction infrastructure

consistent geometry scalable model parameter sets
Integration into RF design system

- Benefits:
  - circuit optimization via consistently scalable transistor models
  - statistical and matching simulation
  - parameter transfer via single "technology" file (xxxx.DTA)

⇒ significant enhancement of functionality for design at reduced maintenance effort for foundry

Integration scheme:
Program features

- Generation of consistent sets of geometry scalable compact model parameters for
  - HICUM
  - SGPM
    for each: hierarchy of equivalent circuits with different complexity
- Statistical modeling capability
  - generation of skewed model parameter sets
  - determination of corner-case parameter sets
- Transistor sizing
- Automatic extraction of specific SGPM parameters from specific HICUM parameters
- General features:
  - user friendly interactive operation
  - batch operation (for integration in extraction and design systems)
  - Manual and installation guide available
  - platforms: UNIX, Windows
Distribution list

Agere
Alcatel
Atmel
Cadence
Conexant
Cypress
IBM
Infineon
JazzSemi
Maxim
SiliconWave
STMicroelectronics
Universities ...