HICUM model overview

M. Schröter\textsuperscript{1,2}, A. Mukherjee\textsuperscript{1}, A. Pawlak\textsuperscript{1}, Y. Zimmermann\textsuperscript{1}
\textsuperscript{1}Chair for Electron Devices and Integr. Circuits, TU Dresden, Germany
\textsuperscript{2}ECE Dept. UC San Diego, La Jolla, CA, USA

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OUTLINE

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3 HICUM basics Parameter extraction
4 Geometry scaling
5 Parameter extraction
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Introduction

• Silicon-based bipolar transistor technology (incl. SiGe HBTs, BiCMOS) enjoys widespread use throughout industry

• Latest SiGe HBT development shows clear advantages of HBT over MOSFET for HF applications, especially for coming mm- and submm-wave markets

• Cost efficient circuit design requires accurate and numerically stable compact models in production PDKs

• existing Si-based BJT/HBT technologies’ performance spans from $f_T = 10...300 \text{ GHz}$, $BV_{CEO}$ from $1.5 ...30\text{V}$, $f_{T\text{max}} = 10...500 \text{ GHz}$,

=> Goals of this presentation:

• overview on SiGe HBT compact modeling approaches  =>  why HICUM
• HICUM basics in a nutshell
• application examples in production and prototyping technologies
SiGe HBT modeling overview

Goal: Unified compact HBT model (incl. model hierarchy)

- Include all physical effects
- Model parameters without wafers
- Rapid eval. of process variations
- "Debugging" of process issues

- EC topology, equations to fit in different interfaces
- I, Q contin. differentiable
- Modular, easily extendable

- Well-defined, fast, reliable
- Using standard equipment
- Min. parameter interaction

- Accurate, valid over wide range
- Smooth geom. scaling (for optim.)
- Computationally fast and reliable
- Easy to understand

- Standard extraction flow & test structures
  => Reduced development effort

- Available in all relevant circuit simulators
  => Numerically stable production version

⇒ Physics-based, geometry scalable, computationally fast model with simple equivalent circuit and fast parameter extraction covering all processes
## Modeling approaches

<table>
<thead>
<tr>
<th>Criteria</th>
<th>Behavioral, X-par.</th>
<th>Physics-based</th>
</tr>
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<tbody>
<tr>
<td>accuracy</td>
<td>high (within narrow ranges)</td>
<td>moderate to high over wide range</td>
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<tr>
<td>numerical stability</td>
<td>compromised outside fitting ranges</td>
<td>high (for standard models)</td>
</tr>
<tr>
<td>fabricated devices</td>
<td>need every possible layout used in circuits</td>
<td>only few devices (6 HF trs, 6 test structures)</td>
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<tr>
<td>measurement effort</td>
<td>moderate to high</td>
<td>moderate to low</td>
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<tr>
<td>par. extraction effort</td>
<td>moderate to low (per device)</td>
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<td>very high for library</td>
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<td>geometry scaling</td>
<td>inconsistent (typically)</td>
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<td>predictive capability</td>
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<td>moderate to high</td>
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<tr>
<td>statistical modeling</td>
<td>none (very high effort)</td>
<td>good to excellent</td>
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</table>

**Goal:** large variety of applications & circuit optimization (bias, T, f)

=> *Physics-based* model (cuts design cycle, supports process dev.)
Existing standard BJT and HBT models

- SPICE Gummel-Poon model
  - addresses effects present in "70ies" BJT technologies, no HBT effects
    => subset of HICUM/L0  =>  to be replaced by HICUM/L0 v1.31

- HICUM/L2, MEXTRAM, VBIC
  - include some or all SiGe HBT related effects
  - HICUM [3] includes mm-wave technology related effects in SiGeC HBTs (s. DOTFIVE)
**Existing standard BJT and HBT models**

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  => **HICUM/L2 v2.3**

  - physics-based
  - large-signal model (charge conservative)
  - geometry scalable
  - NQS & HF noise correl. adjunct networks not shown here

  => **available in 15+ circuit simulators**
HICUM basics

Building a compact model

• Step 1: intrinsic transistor operation
  • along 1D direction under emitter: mostly nonlinear physical and electrical effects
  • quasi-static currents and charges
  • vertical NQS effects, noise correlation

• Step 2: internal transistor
  • region under emitter => 2D effects
  • internal base resistance
  • emitter perimeter effects

• Step 3: external regions
  • access regions, structural parasitics => 3D effects

• Step 4: other effects
  • temperature dependence
  • noise in the internal and external region
  • electro-thermal effects

2D and 3D effects => geometry dependence
Transfer current: Generalized ICCR

- exact solution of q.s. transport equation over entire 1D transistor region:

\[
I_T = c_0 \frac{\exp\left(\frac{V_{BE}'}{V_T}\right) - \exp\left(\frac{V_{BC}'}{V_T}\right)}{\int_{x_E}^{x_C} h_g h_J h_v p dx}
\]

\[
c_0 = A_E q V_T \mu_{nr} n_{ir}^2
\]

- weight factors:

\[
h_g = \frac{\mu_{nr} n_{ir}^2}{\mu_n(x) n_i^2(x)}, \quad h_J = \frac{|J_{nx}(x)|}{I_T/A_E}
\]

\[
h_v = \exp\left(\frac{V_{BE}' - \phi_p(x)}{V_T}\right)
\]

- 1D case: \(h_J = h_v = 1\)

⇒ links charge and current very accurately over wide bias region
Visualization of the GICCR

• split transfer current into components:
  \[ i_T = i_{Tf} - i_{Tr} \]

• hole charge (in emitter, base, collector region)
  \[ Q_{pT} = Q_{p0} + h_{jEi} Q_{jEi}(v_{B'E'}) + \ldots + h_f Q_f(i_T, v_{B'E'}) \]

• depletion charges:
  \[ Q_{jEi} = q \int_{0}^{v_{B'E'}} C_{jEi}(v) dv \]
  \[ Q_{jCi} = q \int_{0}^{v_{B'C'}} C_{jCi}(v) dv \]

• minority charges:
  \[ Q_f = \int_{0}^{i_{Tf}} \tau_f(i) di \]
  \[ Q_r = \tau_r i_{Tr} \]

\[ i_T = c_{10} \frac{\exp(v_{B'E'}/V_T) - \exp(v_{B'C'}/V_T)}{Q_{pT}} \]

impact of charges on transfer current (at \( V_{B'C'} = 0 \))

\[ I_T(Q_{p0} + h_{jEi} Q_{jEi}) \]

\[ I_T(Q_{pT}) \]

\[ Q \]

\[ Q_{p0} \]

\[ V_{B'E'} \]

\[ \exp(-\exp(Q_{pT})) \]

\[ C, \tau \] are measurable

\[ \Rightarrow \] approach can be extended to 2D/3D case [WCM05]
Depletion charges and capacitances [3]

BE depletion capacitance

\[ C_j = \frac{C_{j0}}{(1 - V/V_D)^z} \]

model: modification at high bias to avoid pole at \( V_{DEi} \)

BC depletion capacitance

\[ C_{jC}/C_{jC0} \]

modified includes punch-through effect at \( V_{PT} \)

\( \bullet \) current dependent equ. existing

\[ \Rightarrow \text{accurate over wide bias range} \]
Mobile charge and transit time

- transit time is determined from
  \[ \tau_f = \frac{dQ_f}{dI_T} = (2\pi f_T)^{-1} - \left( \Sigma C_{Bv} \right) / g_m - \tau_{RC} \]

- analytical description
  \[ \tau_f(I_{ Tf}, V_{ B'C'}) = \tau_{f0}(V_{ B'C'}) + \Delta \tau_f(I_{ Tf}, V_{ B'C'}) \]

consists of models for regional components
  - \(\tau_B, \tau_{BC}\) usually dominate at low to medium current densities (ratio varies dep. on coll. profile)

- low current densities: \(\tau_{f0}(V_{ B'C'})\)
  - Early effect (base region)
  - BC SCR bias dependence

- high current densities: \(\Delta \tau_f(I_{ Tf}, V_{ B'C'})\)
  - BC barrier effect
  - collector injection zone
  - emitter component increase
Forward mobile charge and transit time

low-current component $\tau_{f0}$ (IEEE TED, pp. 288-300, 1999)

Early-effect

transit time through BC-SCR

$\Rightarrow$ both effects are modeled in HICUM
Mobile charge modeling: critical current

$I_{CK}$ indicates “onset” of high-current effects in the collector (Si and Si/SiGe transistors)

- calculated in HICUM from the conditions
  - $E_x = V_{ceff}/w_{Ci}$ at low voltages (cf. curve 3 above)
  - $E_x(x_{jc}) = E_{lim}$ at high voltages
  - connection by suitable smoothing function

$$f_{CK}(x) = 1 + \frac{x + \sqrt{x^2 + 10^{-3}}}{2}, \quad x = \frac{V_{ceff} - V_{lim}}{V_{PT}}$$

- effective CE voltage
  $$V_{ceff} = V_{CE} - V_{CES} \approx V_{DCi} - V_{B'C'}$$

- model parameters
  $$V_{lim} = E_{lim} w_{Ci}, \quad V_{PT} = \frac{qN_{Ci}}{2\varepsilon} w_{Ci}, \quad r_{Ci0} = \frac{w_{Ci}}{q\mu_nC_0^N C_i A_E}$$

⇒ physics-based relation and model parameters
⇒ enabling geometry, process, T dependent modeling and transistor sizing
Intrinsic transistor: base current components

The (internal) base current consists of various components

\[ i_{Bi} = \underbrace{i_{pEi} + i_{jREi}}_{i_{jBEi}} + i_{jBCi} + i_{AVL} \]

- back injection into the emitter (major contribution):
  \[ i_{pEi} = I_{BEiS} \left[ \exp\left( \frac{v_{BE}}{m_{BEi}V_T} \right) - 1 \right] \]
  - Model parameters: \( I_{BEiS} \) and \( m_{BEi} \)

- recombination in BE space charge region:
  \[ i_{jREi} = I_{REiS} \left[ \exp\left( \frac{v_{BE}}{m_{REi}V_T} \right) - 1 \right] \]
  - Model parameters: \( I_{REiS} \) and \( m_{REi} \)

- weak avalanche current (breakdown in BC junction):
  \[ i_{AVL} = I_T f_{AVL} \frac{V_{DCi}}{C_{c}^{1/z_{Ci}}} \exp\left( - \frac{q_{AVL}}{C_{jCi0}V_{DCi}} C_{c}^{(1/z_{Ci}-1)} \right) \]
  - Model parameters: \( f_{AVL} \) and \( q_{AVL} \)

- back injection into the collector:
  \[ i_{BCi} = I_{BCiS} \left[ \exp\left( \frac{v_{BC}}{m_{BCi}V_T} \right) - 1 \right] \]
  - Model parameters: \( I_{BCiS} \) and \( m_{BCi} \)
Internal base resistance

... strongly depends on operating mode

- **DC operation:** bias dependence [16]-[19]
  
  \[
  R_{Bi} = r_{SBi} \frac{b_E}{l_E} g_i(b_E, l_E) \psi_{dc}(I_{Bi}, r_{SBi}, b_E, l_E)
  \]

  conductivity modul. geometry func. current crowding (negl. in adv. HBTs)

- **large-signal** transient operation
  - **slow** switching \( \Rightarrow \) use DC \( R_{Bi} \)
  - **fast** switching \( \Rightarrow \) dynamic current crowding
    \( \Rightarrow \) no compact solution \( \Rightarrow \) distributed model [20]

- **small-signal** HF operation
  - analytical solution for negligible DC current crowding
    \( \Rightarrow \) input impedance [17][18]
  - equivalent circuit [21]
    \[
    Z_{Bi, lf} \approx \frac{R_{Bi}}{1 + j \omega g_\omega C_B R_{Bi}} \Rightarrow Z_{B^*E'}
    \]

  **Warning:** this solution does **not** apply to large-signal transient operation
Summary of model for *internal* transistor

- internal transistor
  - equivalent circuit
  - compact equations for each element as function of
    - bias
    - temperature
    - emitter dimensions

- summary of important effects explicitly covered in standard version
  - BE and BC depletion capacitance *forward bias limiting*
  - BC depletion capacitance *punch-through*
  - bias and *bandgap dependent Early-effect* (forward and reverse)
  - accurate mobile charge model incl. current blocking due to *BC conduction band barrier*
  - collector voltage dependent *impact ionization* ($i_{AVL}$)
  - vertical *non-quasi-static effects* for both *charge* and *transfer current*
  - non-ideal and recombination base current components in
  - BE perimeter injection transfer current
  - geometry dependence through *effective electrical* emitter area
    (includes (partial) perimeter components => avoid 2-transistor model, simplify extraction)
Emitter perimeter effects and effective emitter area

- carrier injection into base (transfer current):

\[ I_T = \bar{I}_{Ti} A_{E0} + I_{Tp} P_{E0} = \bar{I}_{Ti} A_{E0} \left( 1 + \frac{I_{Tp}}{I_{Ti}} \frac{P_{E0}}{\gamma_C A_{E0}} \right) \]

\[ = \bar{I}_{Ti} A_E \]

- \( A_E, b_E \): effective electrical emitter area and width
  \( \Rightarrow \) internal and perimeter transistor merged into a **single** transistor

  \( \Rightarrow \) **single** expression for transfer current (rather than 2-transistor model)

- Note: there are still leftover perimeter components for the base currents and depletion charges

Emitter window dimensions:

\[ A_{E0} = b_{E0} l_{E0} \]

\[ P_{E0} = 2(b_{E0} + l_{E0}) \]
External transistor

Each spatial region is represented by a corresponding equivalent circuit element.

- Additional effects included and implemented in simulator code:
  - Temperature dependent equations
  - Self-heating (via adjunct network)
  - Noise (including correlation between transfer and dynamic base current)

(for a complete list of relevant physical effects in HBTs and covered by HICUM/L2 but not available in SGPM => see [3][27])
Modeling the (total) base resistance

large variety of geometries and contact configurations to be covered ...

• geometries: wide range of $l_E/b_E$

• contact configurations
  • double/single base $B||E$, multi/single $B \perp E$

• 2D simulation of a plane through base under emitter [22]-[25],[19]

• analytical equations $r_B$(geometry, bias)
HICUM/L2 complete equivalent circuit

intrinsinc transistor

thermal network

vertical NQS effects

noise correlation

- $I_{nc} = \sqrt{2qI_{T}}$
- $I_{nb} = \sqrt{2qI_{BEI}}$
- $T_{b1} = 1 + j\omega\tau_f B_f (2\alpha_{Qf} - \alpha_{IT})^2$
- $T_{b2} = j\omega\tau_f \alpha_{IT}$
- $\frac{Q_{f,qs}}{\tau_f}$
- $\frac{i_{T,qs}}{\tau_f}$
- $V_{C1}$
- $V_{C2}$
- $R_{th}$
- $C_{th}$
- $\Delta T_j$
- $T$
- $R = \tau_f$
Geometry scaling

bipolar transistor structures: dealing with large variety of structures . . .

. . . and layout configurations

. . . is accomplished by parameter generation and sizing tool TRADICA [30]-[32]
Geometry scalable model (parameter) generation
dimensions / design rules
## Model related input: general specific electrical parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
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<td>rSBl0</td>
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<td>rSpo</td>
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<td>Ohm</td>
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### Electrical Parameters

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<tr>
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### Parameter temperature

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### Additional Information

- Directory: \de/arbeit\tradmenun/sigedb.dta
- Technology identifier: xpoly

© MS 24
## HICUM specific electrical parameters

*(grouped by function)*

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<td>qAVL</td>
<td>0.0</td>
<td>fC/µm²</td>
</tr>
<tr>
<td>fAVL</td>
<td>1.186</td>
<td>1/V</td>
</tr>
<tr>
<td>alqav</td>
<td>empty</td>
<td>1/K</td>
</tr>
<tr>
<td>aTfAV</td>
<td>empty</td>
<td>1/K</td>
</tr>
<tr>
<td>r'C10</td>
<td>200.0</td>
<td>Ohm.µm²</td>
</tr>
<tr>
<td>Vlim</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>VPT</td>
<td>10.0</td>
<td>V</td>
</tr>
<tr>
<td>VCES</td>
<td>0.1</td>
<td>V</td>
</tr>
<tr>
<td>delta_C</td>
<td>60.0</td>
<td>degree</td>
</tr>
<tr>
<td>a(VCES)</td>
<td>0.0004</td>
<td>1/K</td>
</tr>
<tr>
<td>KrBi</td>
<td>1.0</td>
<td></td>
</tr>
<tr>
<td>AF</td>
<td>2.0</td>
<td></td>
</tr>
<tr>
<td>KF</td>
<td>0.0</td>
<td>(µm²/mA)^AF</td>
</tr>
</tbody>
</table>

### Base current

- **JBEiS**: 1.62e-017 mA/µm²
- **mBEi**: 1.0144
- **JREiS**: 1e-030 mA/µm²
- **mREi**: 2.0
- **mBEp**: empty
- **mREP**: empty
- **JBCxS**: 1.68e-016 mA/µm²
- **mBCx**: 1.0245

### Thermal effects (self-heating)

- **Rth**: 1500.0 kΩ/µm
- **Cth**: 0.0 Ws/µm/K

### Noise

- **KrBi**: 1.0
## Model parameter generation

### Geometry scaling

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>bE0</td>
<td>1.3+0.1 μm</td>
</tr>
<tr>
<td>IE0</td>
<td>6.10+1 μm</td>
</tr>
</tbody>
</table>

### Transistor configuration

- Number of contacts/stripes:
  - base: 1
  - emitter: 2
  - collector: 1

- Collector location: side, fore, middle, surrounding

- BE contact configuration (single base only): CEB, CBE

### Transistor figures of merit

- $f_T$, $f_{max}$, $F_{min}$

### Other parameters

- Number of parallel structures: 1
- Factor for process tolerances: empty

### Optional input for bias point information

- $J_C$: 0.5 mA/μm²
- $V_{CE}$: empty V
- $V_{CS}$: empty V
- $f$: 2 GHz
- $R_O$: 50 Ohm

### Simulator selection

- Simulator name: ELDO, SPECTRA
- Temperature: 300 K

**Generate hundreds of consistent model cards in a second**
**Model parameter generation example (netlist)**

* dptest  AE0= 1* 0.30*  2.00( 1); NB= 2( ); NC=1(SIDE),lv ;T=300.00;
* HICUM/Level2 v2.2 / SPECTR  TRADICA A5.3
.SUBCKT N030201S02_01  3  2  1  9

simulator lang=spectre
cbemet  2  1  capacitor c=0.1848E-13
ccsmet  3  9  capacitor c=0.3300E-14

simulator lang=spice
Q  3  2  1  MOD
.model MOD  bht type=NPN  tnom= 26.85  version=2.2
+  c10=6.544E-33  qp0=8.449E-15  hjej=1.000E+00  hjci=1.000E+00  hfe=1.000E+00
+  hfc=1.000E+00  mcf=1.000E+00  ich=7.041E-03  cjei0=2.464E-15  vdei=9.500E-01
+  zcai=5.000E-01  ajei=2.500E+00  cjci0=4.034E-16  vdc=8.000E-01  zci=3.333E-01
+  vptci=3.780E+00  t0=6.523E-12  dt0h=-1.400E-12  tbv=1.000E-13  tef0=5.000E-13
+  qtf=2.000E+00  thc=3.000E-11  ahc=5.000E-01  fthc=6.000E-01  rci0=3.754E+02
+  vlim=7.000E-01  vpt=1.000E+01  vces=1.000E-01  latb=3.959E+00  latl=6.759E-01
+  tr=1.000E-09  alit=4.500E-01  alqt=2.250E-01  flinq=1.000E+00  ibes=1.141E-20
+  mbei=1.014E+00  ireis=7.041E-34  mpre=2.000E+00  favl=1.186E-04  qavl=4.225E-15
+  ibcis=7.041E-34  mbcx=1.000E+00  rbhrec=0.000E+00  rbi=1.282E+02  fgeo=7.934E-01
+  fdqr0=2.000E-01  fcrbi=0.000E+00  fqi=6.132E-01  ibeps=4.839E-20  mbep=1.040E+00
+  ireps=2.987E-33  mrep=2.000E+00  ibes=1.141E-20  fgeo=7.934E-01
+  ftc=2.000E+00  chci0=2.240E-15  vdcx=7.000E-01  zcx=3.333E-01
+  vptcx=1.250E+00  fbcpar=2.221E-02  cbcpf=7.126E-16  cjs=6.098E-15
+  vds=6.000E-01  zv=3.479E-01  vpts=1.000E+02  rsu=0.000E+00  csu=0.000E+00
+  itss=0.000E+00  msf=1.100E+00  iscs=0.000E+00  msc=1.050E+00  tfs=0.000E+00
+  kf=3.711E-09  af=2.100E+00  vgb=1.110E+00  zetact=4.100E+00  alt0=1.110E-03
+  kt0=2.220E-05  zetaci=1.453E+00  alvs=1.000E-03  alces=5.714E-04  alfav=3.300E-05
+  alqav=4.400E-06  zetarb=9.000E-01  zetarcx=2.237E-01
+  zetare=0.000E+00  zetabet=4.900E-01  vgel=1.061E+00  vge=1.175E+00  vgs=1.177E+00
+  zetar=2.500E+00  flv=1.024E-04  f2v=4.322E-04  rth=1.539E+03  cth=1.950E-09
+  fish=1.000E+00

.ENDS N030201S02_01

=> generation of complete libraries in seconds
### Parameter extraction

- **strongly impacted by self-heating**  =>  carefully been taken into account

| Specific depletion capacitance parameters extraction (bias and geometry) |
| Internal base sheet resistance and external base resistance extraction  Determination of Qp0 |
| Low current density collector and base current parameters (bias and geometry) |
| External collector and emitter parasitic resistances |
| Extraction of transit time parameters (bias and geometry) |
| Extraction of temperature parameters |
| Optimization of self-heating parameters on the base current (including geometry) |
| Optimization of transit time parameters (bias and geometry) |

#### Simultaneous optimization of RE and high current parameters from Gummel plots @ VBC=0 (bias and geometry)

| Fine Tuning of RTH and RE on both DC and S21 characteristics (bias and geometry) |
| NQS parameter extraction |
| Parasitic resistances and capacitance splitting fine tuning wrt S parameters and Unilateral Gain |
| Loop and repeat necessary extraction steps |

well-defined flow &
test structures

XMOD toolkit

↓

**model verification**

**issue:** existing *on-wafer* small- and large-signal capability insufficient for most advanced HBT technologies

⇒ selected results
Modeling results for production technologies

Example for model accuracy: ST SiGe BiCMOS process [37]

bias and geometry dependence of

collector current ...

... and transit frequency

⇒ similar results for, e.g., 200GHz\(f_T\) IBM & 300GHz\(f_T\) IHP process,

(for more results see [1] and HICUM website [3])
... more modeling results

Example for HBT model in production PDK:
TowerJazz SiGe BiCMOS process with \((f_T, f_{\text{max}}) = (240, 270)\) GHz

unilateral power gain vs. frequency

... and minimum noise figure vs. frequency

\[ V_{\text{BE}} = (0.8, 0.83, 0.86, 0.89)V \]

\[ f = (8, 20, 32, 40)\text{GHz} \]

⇒ complete results available in PDK documentation
Applications

- HICUM/L2 has been employed for production designs such as
  - SiGe PAs (WCDMS, OFDMA)
  - consumer products: laser drivers for CD/DVD/BD, OC192
  - GSM and GPS receiver front ends
  - transceivers for wireless key entry systems
  - UWB, DBS(SAT), radar, OC768

- During production circuit design, the model enables
  - selecting optimum ballast resistance (trade-off ruggedness vs. power density)
  - predicting device and metallization temperatures (identify reliability issues)
  - predicting optimum TSV placement (for optimizing RF gain)
  - predicting collector voltage waveforms (long-term reliability)

  => widely used => significant implementation effort (e.g. CMC)
  => well-proven & extensively tested numerically stable production code

- Examples for industrial applications: mostly proprietary ...
  - usually only feedback once problems are encountered
850MHz GSM output cell (RFMD)

- measurement
- model

850 MHz GSM output cell
- array of IBM 5PAe HV SiGe HBTs
- 3 E fingers with 0.8*20\(\mu\)m\(^2\) each
- total E area = 10000\(\mu\)m\(^2\)

Simulation with HICUM/L2
- thermal effects
- ballasting
- ADS
- IBM PDK v.1.2.0.2W50
- load-pull simulations for finding optimum PAE

=> good agreement even for very large power levels
Model availability and usage

- HICUM/L2 has been applied to every Si BJT and SiGe HBT process node since early eighties => continuous model development

- Examples for process technologies and design kit availability

<table>
<thead>
<tr>
<th>foundry → process ↓</th>
<th>IBM</th>
<th>TowerJazz</th>
<th>ST</th>
<th>TFK (Atmel)</th>
<th>IHP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si-BJT 10...30GHz</td>
<td></td>
<td>B25 BC35</td>
<td>avail.</td>
<td>UHF6S TSHSB-SOI</td>
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<tr>
<td>HS SiGe 40...80GHz</td>
<td>5HP?</td>
<td>SBC35</td>
<td>BiCMOS6 BiCMOS7</td>
<td>SiGe1RF SiGe2RF</td>
<td>SGB25V</td>
</tr>
<tr>
<td>HV SiGe 40...80GHz</td>
<td>5PAe</td>
<td>B25 to SBC18</td>
<td>BiCMOS6 to 9</td>
<td>SiGe2PW</td>
<td>SGB25V</td>
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<td>HS SiGe 90...240GHz</td>
<td>7HP 8HP</td>
<td>SBC18 variants</td>
<td>BiCMOS9 variants</td>
<td>process N/A</td>
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<td>HS SiGe ≥300 GHz</td>
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<td>process N/A</td>
<td>process N/A</td>
<td>process N/A</td>
<td>SG13G2</td>
</tr>
</tbody>
</table>

=> spans 0.1 to 0.8μm lithography, 10 to 300 GHz transit frequency

- >15 commercial circuit simulators (incl. RF simulators ADS, SPECTRE ...)

© MS
Conclusions

• Compact modeling approaches
  => physics-based approach has far more benefits than behavioral modeling

• Overview on state-of-the-art compact HBT model HICUM
  • most important physical effects in SiGe HBTs
  • parameter extraction flow
  • examples for results from production designs

• HICUM/L2 is available in all major commercial circuit simulators and many PDKs

• HICUM/L2 has turned out to be suitable for production circuit design of a large variety of applications, aiding trade-off optimization between performance and reliability
  => accurate modeling aids optimizing process capability (& RoI)

• Issues
  • large-signal model verification requires significant improvement in on-wafer characterization
  • insufficient funding for transfer into production, implementation, and (legacy) user support
  • need to have early enough access to advanced technologies to provide model in time
  • need to better educate circuit designers when using advanced (mm-wave) technologies
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• Cadence, Mentor Graphics (software)
• Agilent, AIST, Analog Devices, Ansoft, Atmel, IBM, ProPlus Solutions, Qualcomm, Renesas Electronics, RFMD, Samsung, STARC, Synopsys, Texas Instruments (National), TelefunkenSemi, Toshiba, TSMC, UMC
References (examples only)


References (2)

References (3)


[40] "EU project targets 0.5-THz SiGe bipolar transistor", EE Times Europe print edition covering March 17 – April 6, 2008. see also DOT-FIVE website: http://www.dotfive.eu/


HICUM model overview

References (examples only)


