Automated Transit Time and Transfer Current Extraction for Single Transistor Geometries

T. Rosenbaum, M. Schröter, A. Pawlak

Chair for Electron Devices and Integrated Circuits (CEDIC)  
University of Technology Dresden  
Germany

department of Electrical and Computer Engin.  
University of California at San Diego  
USA

tommy.rosenbaum@tu-dresden.de, mschroter@ieee.org

13th HICUM Workshop  
Delft (Netherlands), 2013
Outline

1 Motivation
2 Method overview
3 Intrinsic transistor
4 Fit procedure
5 Results
6 Conclusions
Motivation

- Observation in more advanced technologies: "classical" determination method of transit time from $f_T$ measurement appears to be inaccurate or inconsistent

- Simplify extraction progress
  - HICUM transit time and transfer current system involve 20 and 13 parameters, respectively
  - Transfer current at high current densities involves self-heating, base current and transit times

=> if a single system fails, $I_T$ extraction will be inconsistent

classical determination of $\tau_{f0}$ from $f_T$  \hspace{1cm} $\tau_{f0}$ parameter extraction \hspace{1cm} $f_T$ model playback

$\frac{1}{2\pi f_T}$  
\[ V_{BC} \left| V_{CE} = \text{const} \right. \]
\[ \Delta \tau_f \]
\[ \tau_{f0} + \tau_{cor} \]

High current region \hspace{0.5cm} Low current region

$1/I_C$

$\tau_{f0}$ vs. $f_T$

$V_{BC}$ vs. $V_{CE}$

$V_{BC} = 0.5\ V$  
$V_{BC} = -0.5\ V$

$\Delta$ slope max

$1/IC = \frac{1}{2\pi f_T}$

$\tau_{f0}$ parameter extraction

$\tau_{f0}$ vs. $f_T$

$V_{BC}$ vs. $I_C$

Reference Parameters

Extracted Parameters

$10^{-1}$  
$10^0$  
$10^1$

$10^{-1}$  
$10^0$  
$10^1$

$V_{BC}$ vs. $I_C$

$V_{BC}$ vs. $f_T$

$\tau_{f0}$ vs. $V_{BC}$

$\frac{1}{I_C}$ vs. $f_T$

=> inaccurate $\tau_f$ determination or extraction?
Method overview

• Transit time is associated with the intrinsic transistor Y-parameters

• External elements alter Y-parameters of intrinsic transistor
  • in addition: self-heating needs to be included for high current region

=> "De-embedding" of external elements necessary

• HICUM/L2 in common-emitter configuration (small-signal EC)
  • most relevant EC elements included (substrate transistor, -diode and -network deactivated)
Embedding procedure

• Express each element or physically associated set of elements by sub-two-port

⇒ various possibilities to arrange two-ports

Goal: intrinsic transistor

• For sake of simplicity: two-port of $C_{BCx'}$ and $C_{BCx''}$ are not shown in figure (more complex parallel connection)
Embedding procedure

• Calculate two-port parameters of each sub-two-port (example below)
  • choose suitable description for easy calculation (e.g. Y, Z or A parameters)

\[
Z_E = \begin{bmatrix}
  r_E & r_E \\
  r_E & r_E 
\end{bmatrix}
\]

• Determine behaviour of total equivalent circuit by means of two-port analysis
  • only simple matrix operations and two-port parameter conversion (e.g. Y → A) are needed

\[
A_{tot} = A_{bi} \cdot y2a(Y_i)
\]

=> perform step by step operations until two-port is fully reproduced
External base-collector capacitances

- Parallel-parallel connection of $C_{BCx'}$ and $C_{BCx''}$ (relative to rest of circuit)

$$Y_{x''} = Y_{tot} A_1$$

$$Y_{tot} = a 2 y(A_1) + Y_{x''}$$

$\Rightarrow Y_{x'}$ (outside $C_{BCx'}$) can be embedded similarly
Method overview

Embedding flowchart
... steps depend on two-port arrangement of equivalent circuit

\[
\begin{align*}
A_1 &= A_p A_{Bi} y_2 a(Y_i) \\
Z_2 &= Z_E + a_2 z(A_1) \\
Y_3 &= Y_{x''} + z_2 y(Z_2) \\
A_4 &= A_{Bx} z_2 a(Y_3) \\
Y_5 &= Y_{x'} + a_2 y(A_4) \\
Y_{tot} &= a_2 y (y_2 a(Y_5) A_{Cx})
\end{align*}
\]

- Rearrange equations to calculate \( Y_i \) => de-embedding!
- \( Y_{tot} \) is known from measurements, parasitics are known from previous extraction steps

=> intrinsic Y-parameters can be obtained!
Internal base resistance

• Internal base resistance depends on minority charge
  
  => cannot be evaluated before transit time extraction for whole bias

• Final equation for intrinsic Y-parameters

\[ A_r = A_p^{-1} \cdot z^2 a(y2z[A_{Bx}^{-1} \cdot y2a\{a2y[y2a(Y_{tot}) \cdot A_{Cx}^{-1}] - Y_x\} - Y_x^\prime] - Z_E) \]

  \[ \Rightarrow Y_i = a2y(A_{Bi}^{-1} \cdot A_r) \]

• Determination of \( r_{Bi} \) is possible by using additional information about \( Y_i \)

\begin{align*}
\text{option 1: } & \Im\{y_{i12}\} = \Im\left\{ \frac{-1}{a_{r12} - r_{Bi}a_{r22}} \right\} \approx -\omega C_{jCi} \\
\text{option 2: } & \Im\{y_{i22}\} = \Im\left\{ \frac{a_{r11} - r_{Bi}a_{r21}}{a_{r12} - r_{Bi}a_{r22}} \right\} \approx \omega C_{jCi} \\
\text{option 3: } & \Re\{y_{i12}\} = \Re\left\{ \frac{a_{r21}a_{r12} - a_{r11}a_{r22}}{a_{r12} - r_{Bi}a_{r22}} \right\} \approx 0
\end{align*}
Intrinsic transistor

- Analysis of the HICUM code shows: many derivatives (small-signal elements) are created due to the implementation in Verilog-A (e.g. \( \frac{d(\tau_f)}{d(V_{BC})} \cdot I_Tf \))

\[ \text{code} \quad \frac{\partial}{\partial \tau_f} C_{jEi} + \tau_f \cdot g_m + I_Tf \cdot \frac{\partial \tau_f}{\partial V_{B'C}} + C_{jEi} \]

- Transit time is included within the capacitance \( C_{dEb} \) => combining

\[ y_{i11} + y_{i21} \]

\( \sum \) \( y_{i11} \) and \( y_{i21} \) includes \( \tau_f \) as well as other elements
Fit procedure

• re-arrange equation for fit

\[
\tau_{fit} = \frac{\mathbb{I} \{y_{i11} + y_{i21}\}}{g_m \omega} = \tau_f + \frac{C_{\tau f0} + C_{jEi}}{g_m}
\]

with \( C_{\tau f0} = I_{Tf} \cdot \frac{\partial \tau_{f0}}{\partial V_{BC}} \) and \( g_m \approx Re\{y_{i21}\} \)

• equation contains 21 parameters in total

=> least square fit is likely to fail

• Split transit time by separating the low- and high-current transit time portion
  • depletion capacitance dominates at low bias
  • high-current transit time portion \( \Delta \tau_f \) dominates at high bias

=> apply fit to smaller parameter-subsets

=> coupling of subsets (loop) is required for final solution
Results

• Transit frequency (SiGe HBT from 130nm IHP process technology of [1])

\[ V_{BC} = [-0.5, 0, 0.5] \text{ V} \]

• New extraction method can provide accuracy similar to a manual procedure
  • high current characteristics are usually even more accurate than manual fit, as SH is included

Transfer current of high-speed HBT

- SiGe HBT from 130nm IHP process technology of [1]

Results are similar to those obtained from time consuming manual fine tuning
ST 9MW results

=> Good agreement for whole temperature range
High-voltage SiGe HBT (IHP) of [2]

transit frequency

\[
\begin{align*}
V_{BC} &= [0, -1, -5] \text{ V} \\
300 \text{ K} & \quad I_C (\text{mA}) \\
0 & \quad 10^{-1} \quad 10^1 
\end{align*}
\]

transfer current

\[
\begin{align*}
V_{BC} &= [0, -1, -2.5, -5] \text{ V} \\
300 \text{ K} & \quad V_{BE} (\text{V}) \\
0.7 & \quad 0.8 \quad 0.9 
\end{align*}
\]

\[\Rightarrow\] Extraction also suitable for HV-transistors

Conclusions

• observed discrepancy in standard method between measured and modeled transit frequency is due to inconsistent transit time determination from measurements => \( \tau_f \) cannot be accessed directly using \( f_T \)

• problem can be fixed by careful "de-embedding" of intrinsic transistor Y parameters

• method was shown to be consistent and accurate
  • with extraction fully adapted to HICUM/L2 v2.32 (ahlth recently included)

• method was implemented in automated extraction tool
  • adaption to model changes is easy (exchange of equations or transfer function only)
  • still: lot of settings are required to conduct the extraction

• Possible Issues
  • accuracy depends on accuracy of previously extracted parasitic elements
    => inaccurate information might render final results useless
  • implementation needs to be changed with each model (eq. or equivalent circuit) change

• method is generally useful for extractions from device simulation and for model development
Appendix

\[
C_{dEb} = \frac{dQ_f}{dV_{B'E}} \bigg|_{V_{CE} = \text{const}} = \frac{\partial Q_f}{\partial I_{Tf}} \cdot \frac{\partial I_{Tf}}{\partial V_{B'E}} + \frac{\partial Q_f}{\partial \tau_f} \cdot \frac{\partial \tau_f}{\partial V_{B'C}} + \frac{\partial Q_f}{\partial I_{CK}} \cdot \frac{\partial I_{CK}}{\partial V_{B'E}}
\]

\[
= \tau_f \cdot S_{fb} + I_{Tf} \cdot \frac{\partial \tau_f}{\partial V_{B'C}} + 0
\]

- Special term is visible in all frequency ranges (see DA TR p. 49+50), about 1% of \( \tau_f \) at low currents
- Term is caused by implementation in Verilog-A and physically correct
Internal base resistance (measurement data)

- Method applied on measurement data of [1]

\[ r_{Bi} \approx \frac{1}{a_{r12} - r_{Bi} a_{r22}} \]

\[ \Im \left\{ y_{i21} \right\} = \Im \left\{ \frac{-1}{a_{r12} - r_{Bi} a_{r22}} \right\} \approx -\omega C_{jC} \]

\[ \Im \left\{ y_{i22} \right\} = \Im \left\{ \frac{a_{r11} - r_{Bi} a_{r21}}{a_{r12} - r_{Bi} a_{r22}} \right\} \approx \omega C_{jC} \]

\[ \Re \left\{ y_{i12} \right\} = \Re \left\{ \frac{a_{r21} a_{r12} - a_{r11} a_{r22}}{a_{r12} - r_{Bi} a_{r22}} \right\} \approx ( \]

ST B5T results (difficult measurement conditions)

- **290 K**
  - $f_t$ vs $I_C$ for VBE = 0.75, 0.8, 0.85, 0.9, 0.95, 1 V
  - $I_C$ vs VBE for $f_t$ = 10, 100, 150, 200, 250, 300 GHz

- **350 K**
  - $f_t$ vs $I_C$ for VBE = 0.75, 0.8, 0.85, 0.9, 0.95, 1 V
  - $I_C$ vs VBE for $f_t$ = 10, 100, 150, 200, 250, 300 GHz

+ **meas**
  - Green dashed line
  - HICUM L2

The plots show the measured $f_t$ values and $I_C$ vs VBE characteristics at different temperatures, illustrating the impact of temperature on the device performance.
GUI interface