HF characterization of SiGe HBTs up to 325 GHz

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OUTLINE

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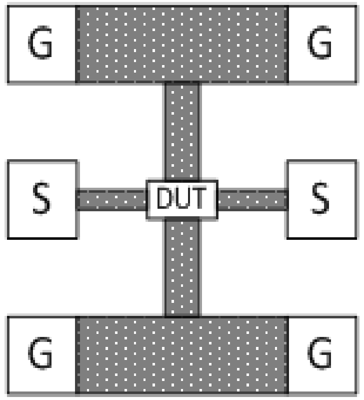
Introduction

- Recent developments in HBT technology (SiGe, InP) are attractive for mm- and sub-mm-wave applications
- Evaluation and verification of compact models at mm- and sub-mm-wave frequencies is very important for circuit design, but lacking due to
  - costly equipment
  - difficulty of calibration/deembedding
- Beyond 220 GHz, accuracy of conventional procedure for calibration/deembedding becomes questionable:
  - calibration and wafer substrate material are different
  - probe pad arrangements differ between ISS and wafer
  - ISS cal structures loose their characteristics at very high frequencies and behave differently than on wafer



=> need direct on-wafer calibration, preferably up to DUT reference plane

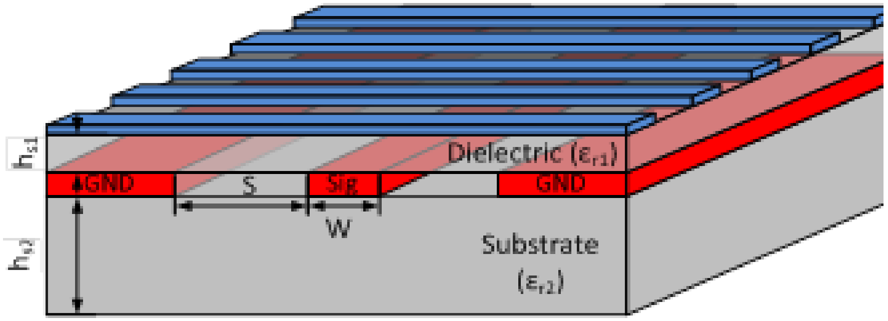
=> explore feasibility for direct on-wafer calibration and perform first SiGe HBT compact model evaluation at 220...325 GHz

(see: IEEE Trans. Microw. Theory & Techniq., Vol. 65, No. 12, pp. 4914-4924, 2017)

Concept of the CL-ICPW

CPW options

- CPWs on Si suffer high losses due to conductive substrate
  => shielding of Si substrate via (patterned) metal ground plane (M1)
- On-chip calibration/deembedding requires TLs in the same metal level as DUT => shield not possible for CPW in M1
- Possible solution: place ground plane above M1 as close as possible
  => leads to very narrow line width and large resistance (loss)
- Viable alternative: replace ground plane by *floating metal stripes* with minimum possible distance (typically given by M1 to M2 separation)
  => larger part of EM energy above M1 CPW, reduced losses in Si



Oxide (plus STI) between CPW and substrate omitted to simplify drawing

- Patterned shield with orthogonal floating bars avoids Eddy currents
  => slow-wave CPW line with capacitive load

  => structure of capacitively loaded (CL) inverted CPW (CL-ICPW)

Analytical model for cal kit design

- strongly diverse dimensions in vertical and horizontal direction lead to large computation times
  => simplified analytical model for saving time, but also for cal kit design
- analytical model was derived using conformal mapping (assuming $S >> h_s$ and metals as ideal conductors)
- effective permittivity ($k_0 = S/(S+2W)$)

$$\varepsilon_{eff} = \frac{\varepsilon_{r,Si} + 1}{2} + \frac{\varepsilon_{r,ox} W}{4 h_s} \frac{K(k'_0)}{K(k_0)}$$

contribution from CPW above Si substrate (no shield on top)

contribution from capacitive load of patterned shield on top

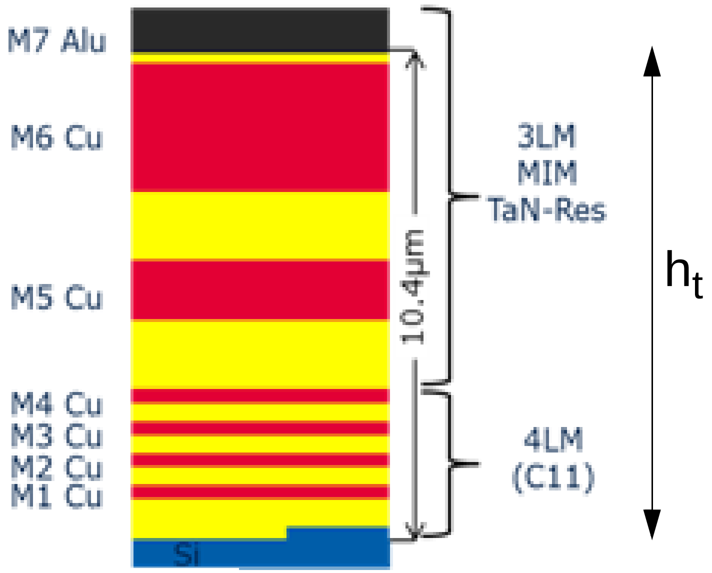
- phase velocity: $v_{ph} = c / \sqrt{\varepsilon_{eff}}$
- characteristic impedance: $Z_0 = \frac{1}{C_{tot} v_{ph}}$ with $C_{tot} = \varepsilon_{eff} C_{air}$

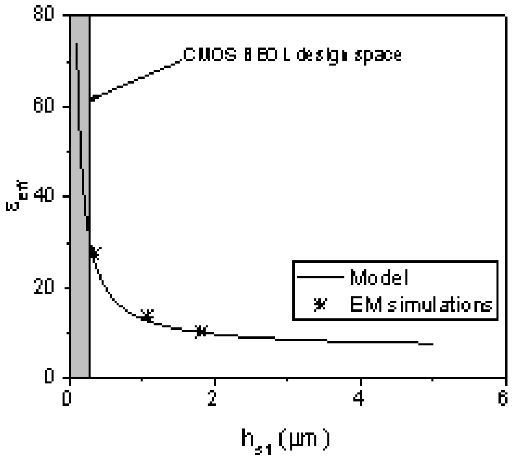
=> design variables: width *W* and spacing *S* of CPW, distance h_s to shield

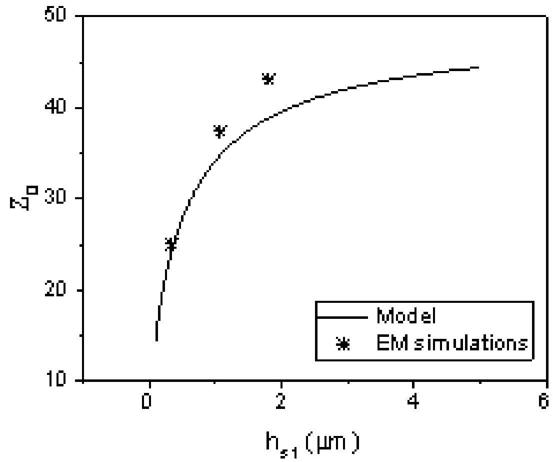
CL-ICPW and cal kit fabrication

130 nm BiCMOS process technology (B11HFC of Infineon)

- SiGe HBTs: f_T, f_{max} = (250, 380) GHz
- BEOL:
  - Cu (M1 to M6), Al (M7)
  - h_s = (0.34, 1.07, 1.8) µm
  - h_t = 10.4 µm
- CPW for calibration of analytical model vs EM simulation:
  - W = 5 µm, S = 10 µm
  - different h_s values
  - $\varepsilon_{r,Si}$ = 11.9, $\varepsilon_{r,ox}$ = 4.1
  - f = 220...325 GHz
  - Z_0 = 30 ... 70 Ω
- Good agreement between model and EM simulation (f = 300 GHz)







Loss in the CL-ICPW

... for a wide range of substrate conductivities

f = 300 GHz

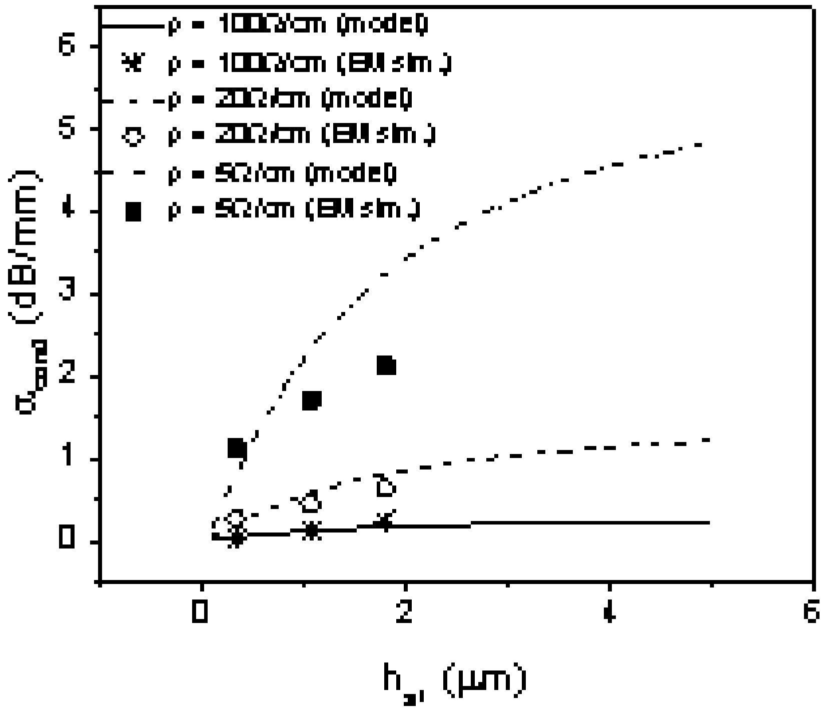
- dielectric losses due to the Si sub-strate:

$$\alpha_G = 8.66 A_{Si} \frac{Z}{10\rho_{Si}} \frac{K(k)}{K(k')}, \quad k = \frac{W}{2S + W}$$

- portion of EM field in the substrate represented by

$$A_{Si} = \frac{\varepsilon_{r,Si} + 1}{2\varepsilon_{eff}}$$

- losses decrease
  - for higher substrate conductivity
  - with smaller distance of shield

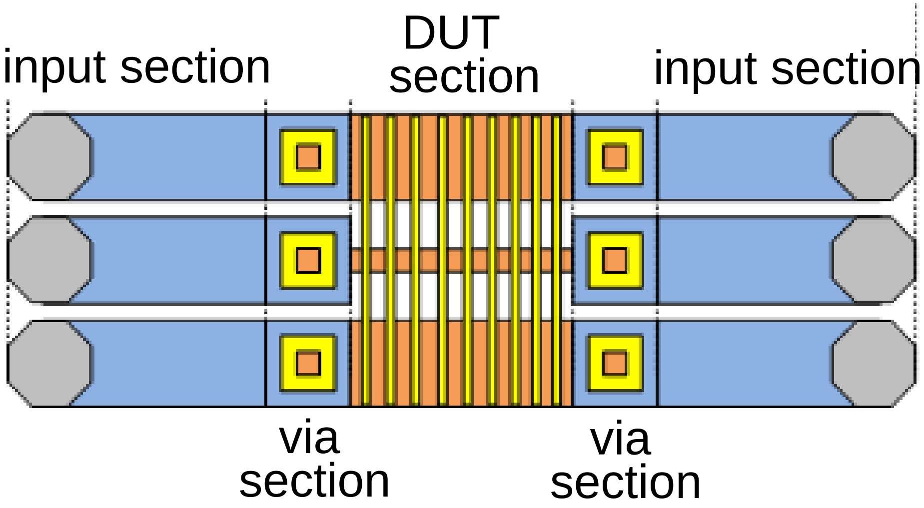


=> **good agreement of analytical model with EM simulation for M2 shielding layer and up to 20 Ωcm Si conductivity**

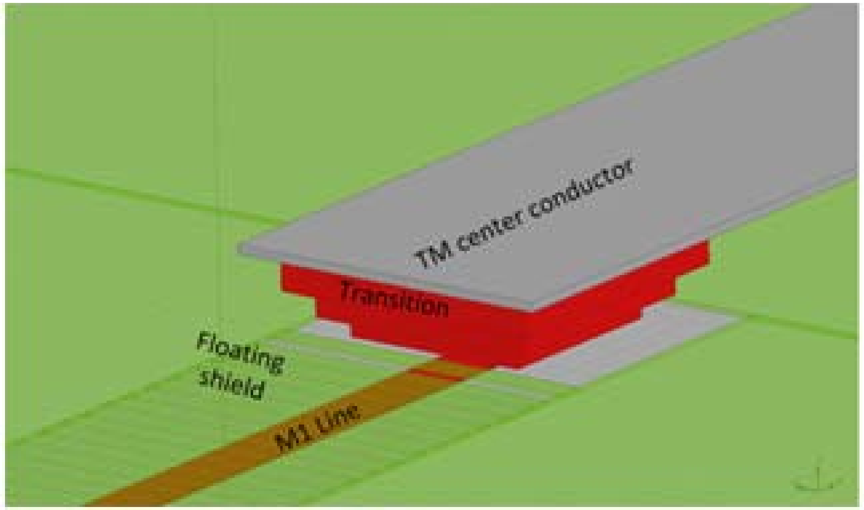
Cal kit design

Basic calibration/deembedding structure

schematic top view



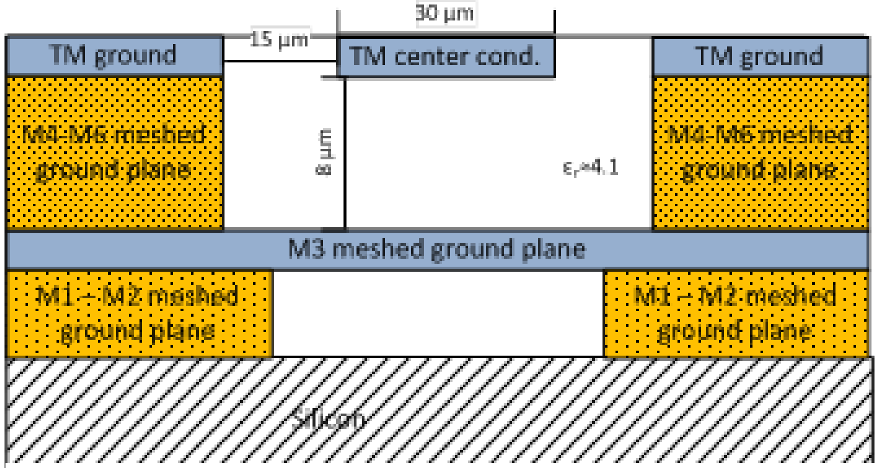
3D view



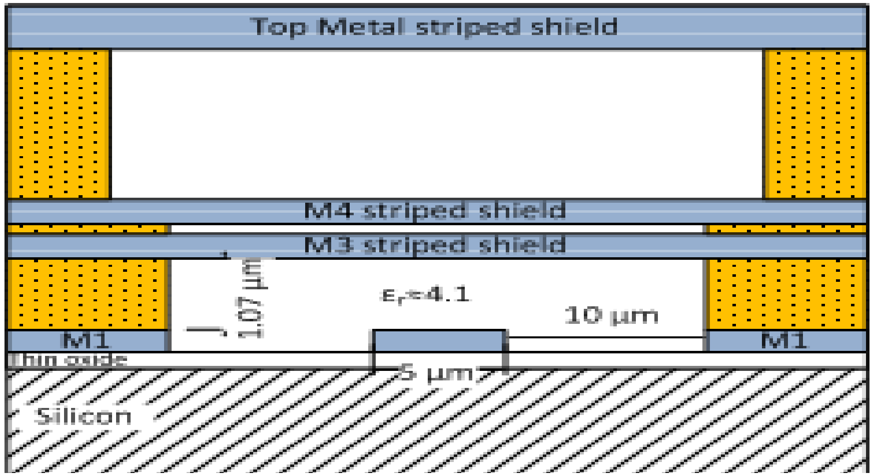
- signal line width equals pad width (30 μm)
  gap S = 15 μm => Z_0 = 35 Ω => close to Z_0(CL-ICPW) = 34 Ω
- obelisk-type transition from top layer (30 μm) to M1 (5 μm) CPW
- M3 chosen as meshed ground plane in input section and as floating shield in DUT region (for TLs only, not when transistor is present)
- shield: 2 μm wide metal stripes and fill factor of 50%
  M4 added to reduce losses due to field dispersion through M3

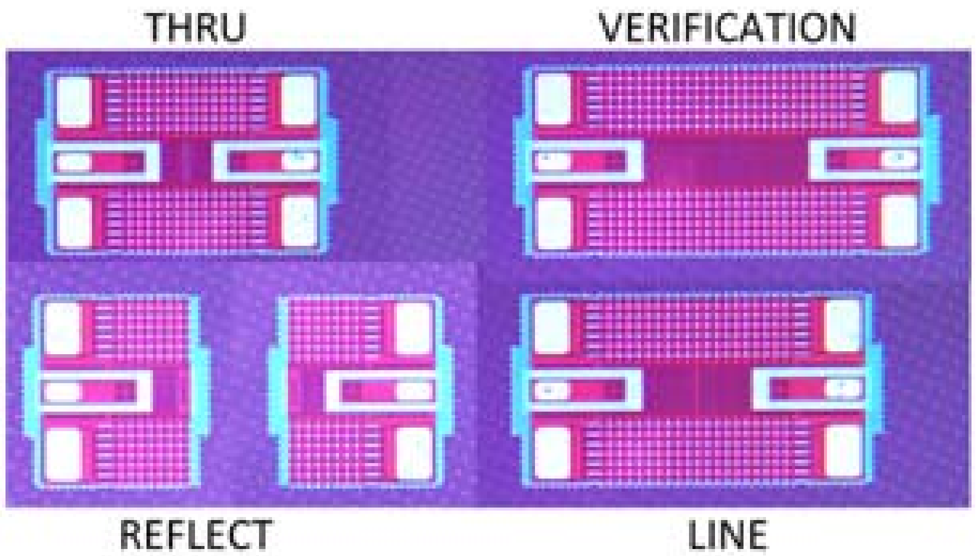
Cal kit structures

input region



DUT region



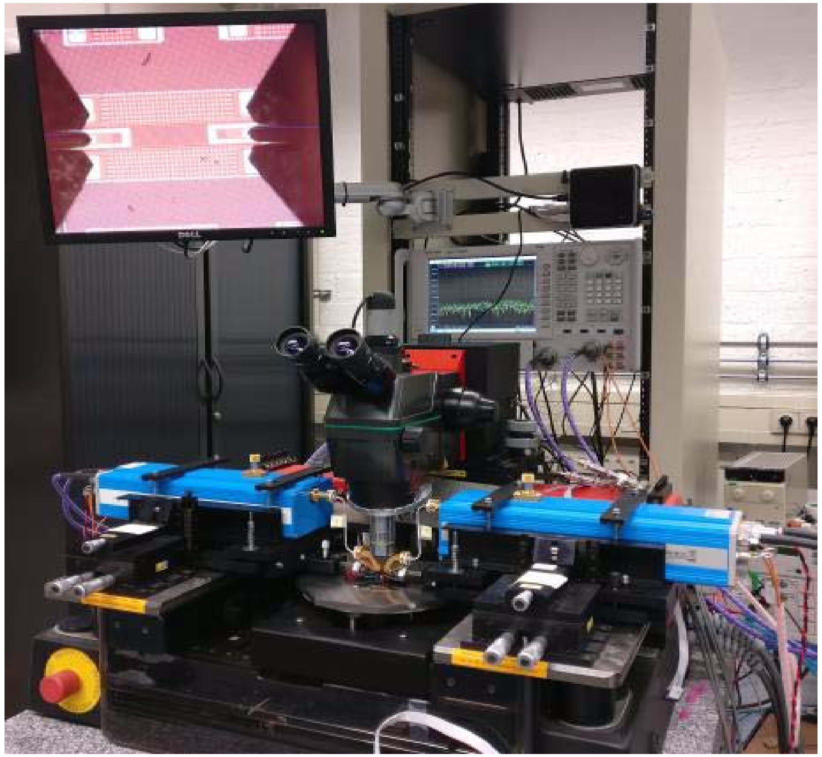


- designed for operation in 220...325 GHz
- 130 µm launch lines
- Thru: 150 µm CL-ICPW
- Shorts at 75 µm
- add'l 230 & 310 µm lines

TRL calibration

Measurement set-up and approaches

- semi-automatic probe station
  - repeatable probe pressure and placement



Approach

1. probe tip calibration using TRL cal-kit on fused silica
   => reference for cal comparison method
2. TRL measurement of new on-chip cal-kit
   => calculation of charact. impedance Z_0

$$Z_0 = Z_{sys}\sqrt{\frac{(1+S_{11}^2)-S_{21}^2}{(1-S_{11}^2)-S_{21}^2}}$$

S: renorm. to system impedance (50 Ω)

=> allows to determine unknown Z_0 from known Z_0 of system

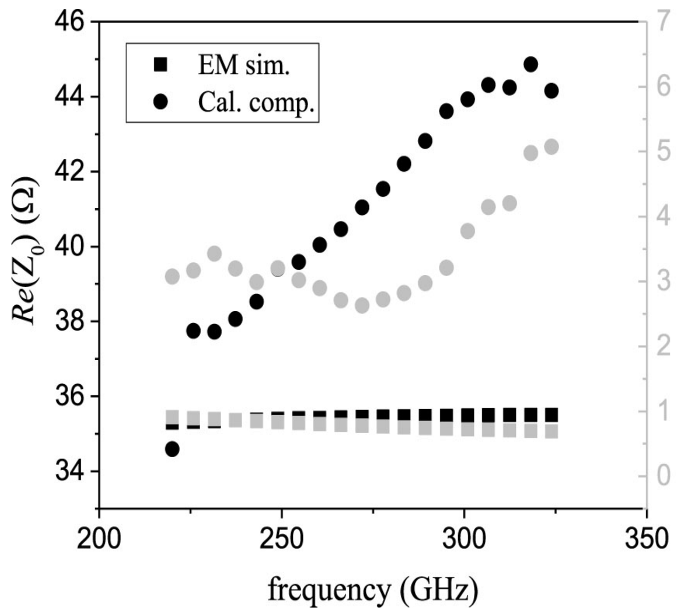
Approaches compared:

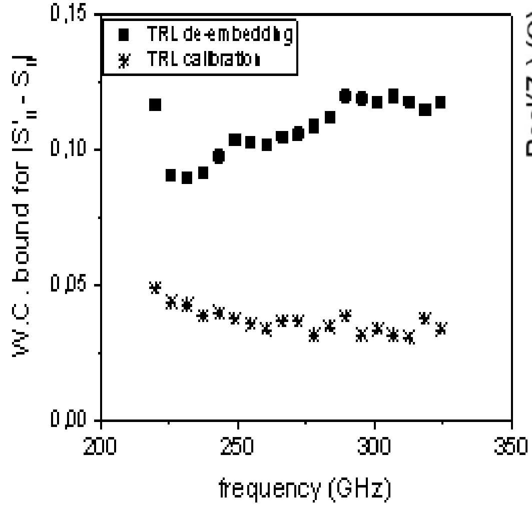
- calibration comparison method
- simulation-based Z_0 extraction

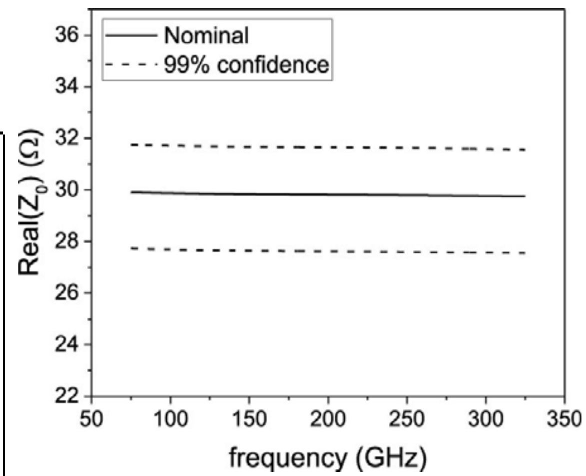
Extraction of characteristic impedance

TRL "deembedding" versus TRL "calibration"

- TRL deembedding = two-step method:
  1. calibration on fused silica substrate
  2. deembedding using on-wafer TRL structures
- TRL calibration: one-step method, using just on-wafer TRL structures







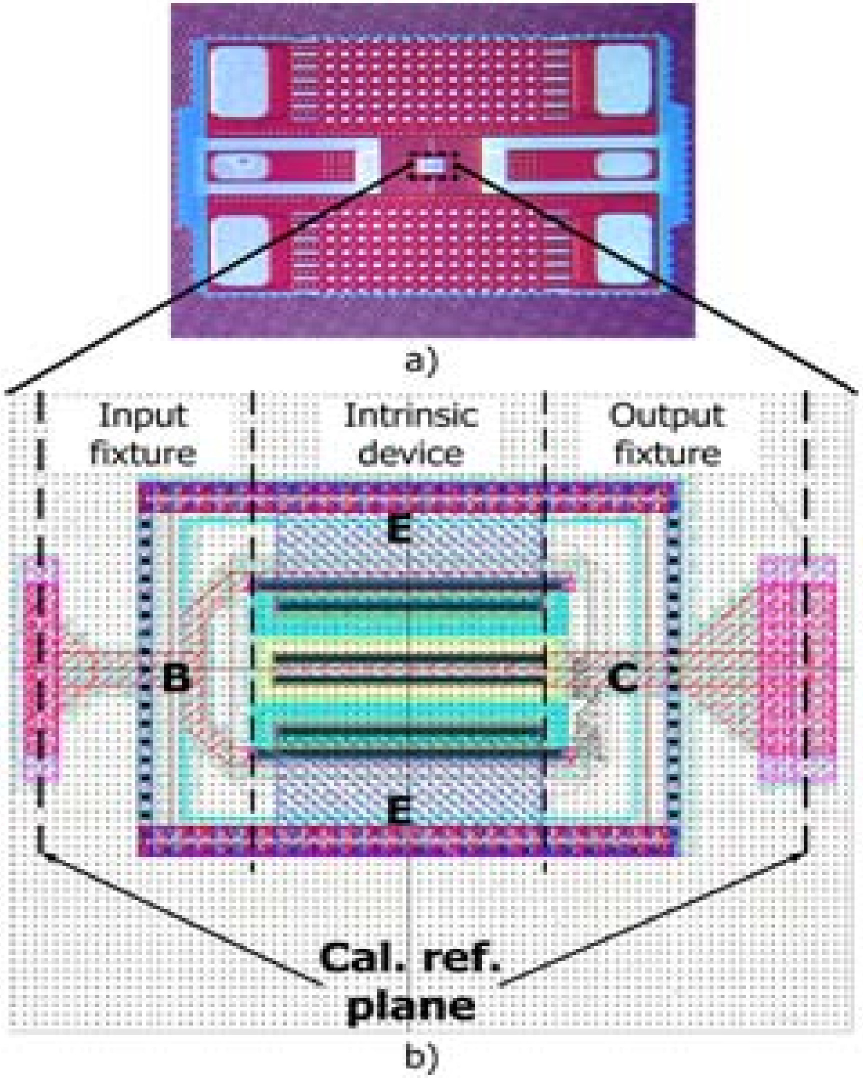
Z0 from EM simul. with metal stack tolerances

=> TRL calibration with characteristic impedance calculation from EM simulation yields much smaller error

Comparison of compact model with deembedded measurements

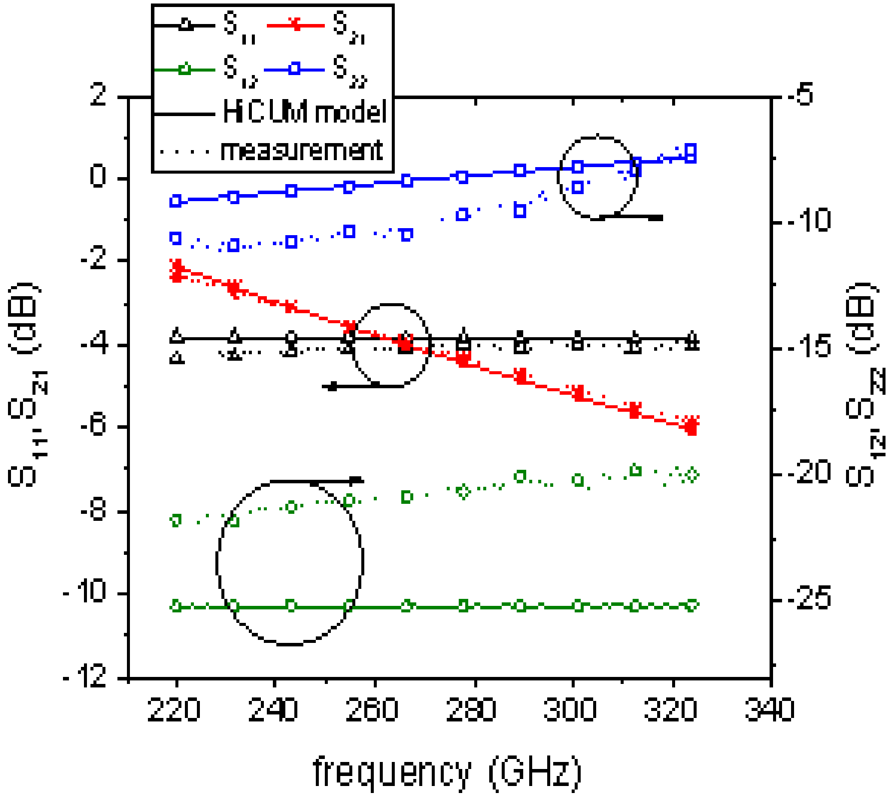
Investigated SiGe HBT

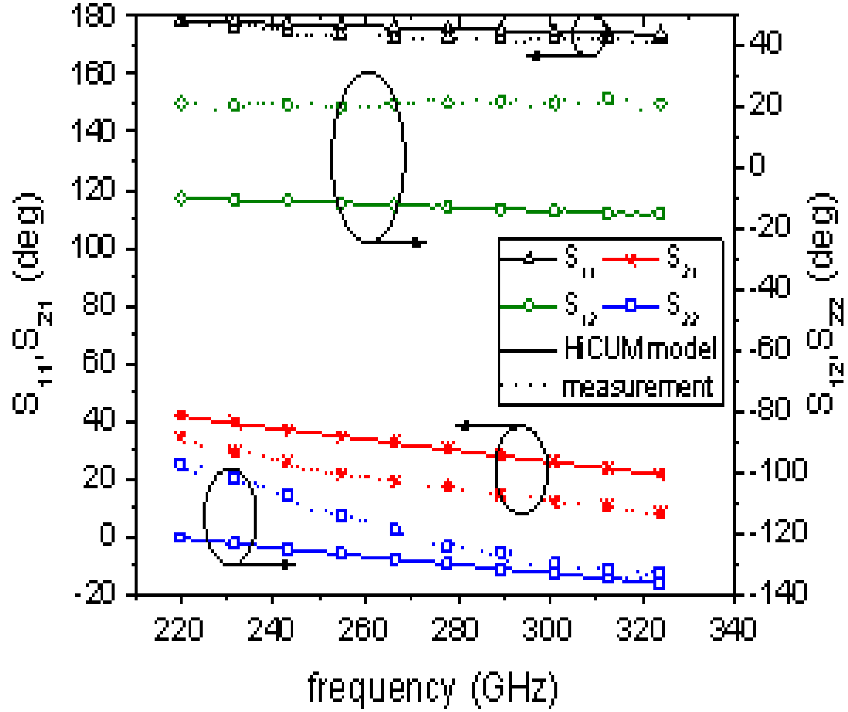
- device size: 2 x 0.22 μm x 5 μm
- operating point close to peak f_T: $(V_{BE}, V_{BE}) = (0.91, 1.5)V$
- HF layout
  - reference plane at end of CL-ICPW feed line
  - small additional "pad" and line required for connecting CL-ICPW to device
    => related S param. determined from EM simulation and used to correct measured device S-parameters
- direct calibration using corresponding fused silica substrate
- HICUM/L2 parameters not available in PDK
  => generated from scaling tool



HICUM/L2 comparison to measurements at 220 to 325 GHz

S parameters referred to system characteristic impedance $Z_{sys} = 50\ \Omega$

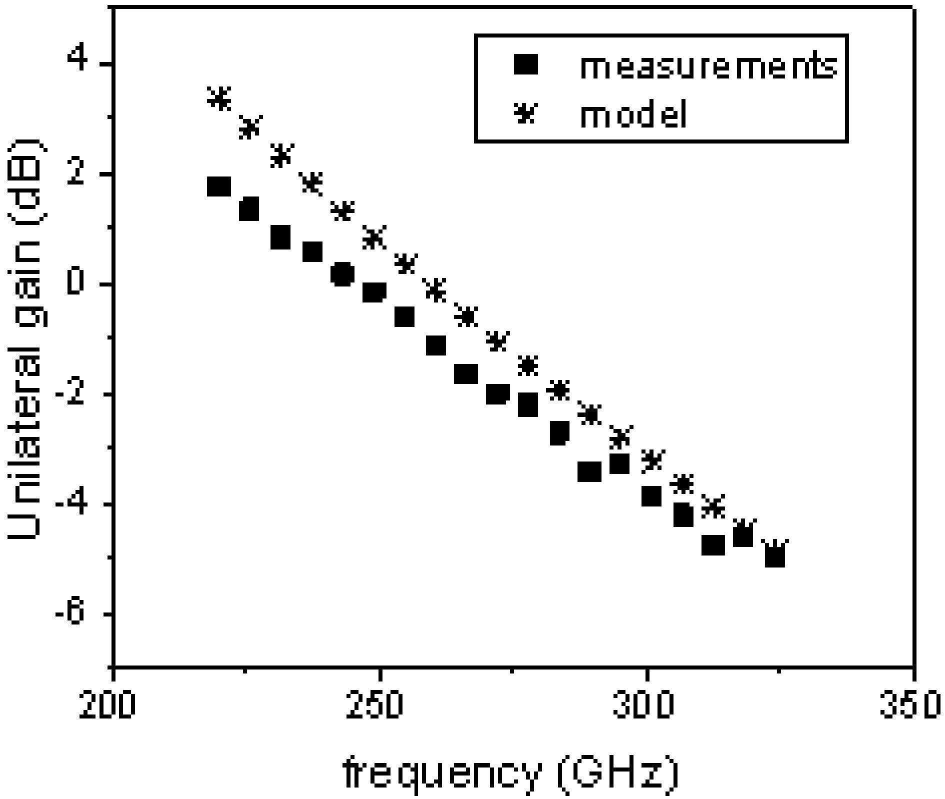




- excellent agreement for S_{21} and S_{11} with small phase difference in S_{21}
- reasonable agreement for S_{22} (missing Su coupling network)
- larger deviations in S_{12} (small absolute value)

HICUM/L2 comparison to measurements

unilateral power gain, **f = 220 .... 325 GHz**



=> good agreement between compact model and measurements

- deviations partially due to missing substrate coupling network and inaccuracy of predicted parasitic (external) capacitances

Conclusions

- Difficulty of conventional calibration/deembedding methods has been circumvented by direct on-wafer calibration up to DUT reference plane
- Proposed method is based on
  - CL-ICPW implemented on wafer to access DUT (at lowest metal level)
  - EM simulation for determining the characteristic TL impedance
  - dedicated calibration/deembedding kit in fused silica substrate
  - (m)TRL calibration
- Analytical model for CL-ICPW can be used for designing required test structures
- Measured S parameters from direct calibration have been used for first evaluation of SiGe HBT compact model (HICUM/L2) in 220 ... 325 GHz range

=> good agreement between model and measurement

Future work

- apply method to devices with different sizes
- investigate deviations in S_{22}, S_{12} between compact model and measured data
- extend method to higher frequencies

Acknowledgments

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