Circuit activities for compact model verification at mm-wave frequency

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Outline

- Introduction
- 95-195 GHz ultra wideband power amplifier
- 97 GHz low-power down-conversion mixer
- W-band low power narrow-band LNA
- Broadband Amplifier (BBA)
- 180-210 GHz (G band) frequency doubler
- 140-170 GHz LNA
- Conclusions

Introduction

- Device model verification beyond the typical standard characteristics by comparison to specially fabricated circuits
  - Design of small but practically relevant circuit blocks
  - Establishment of systematic design procedure to be used in other technology

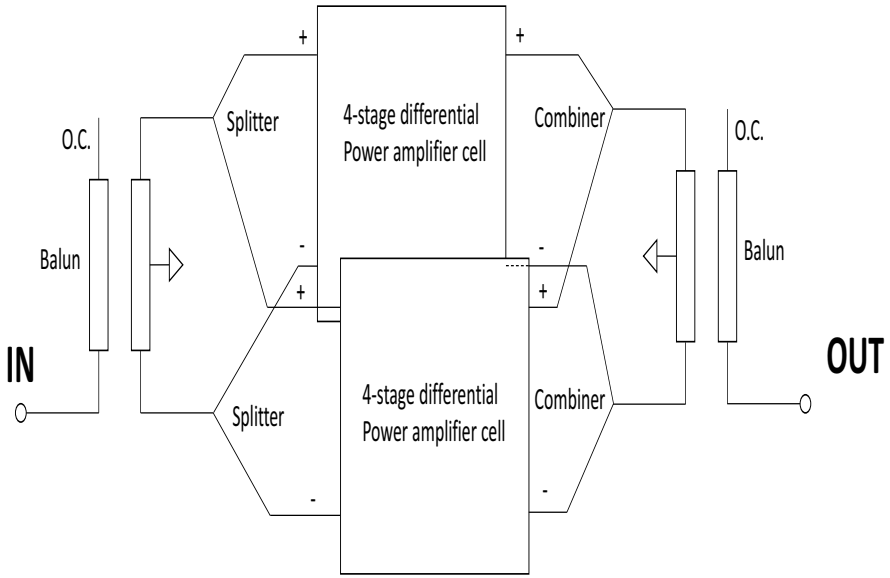
- Reducing the communication gap between modeling and circuit design engineers
  - most circuit designers lack device physics and modeling background
  - most modeling engineers lack circuit design background

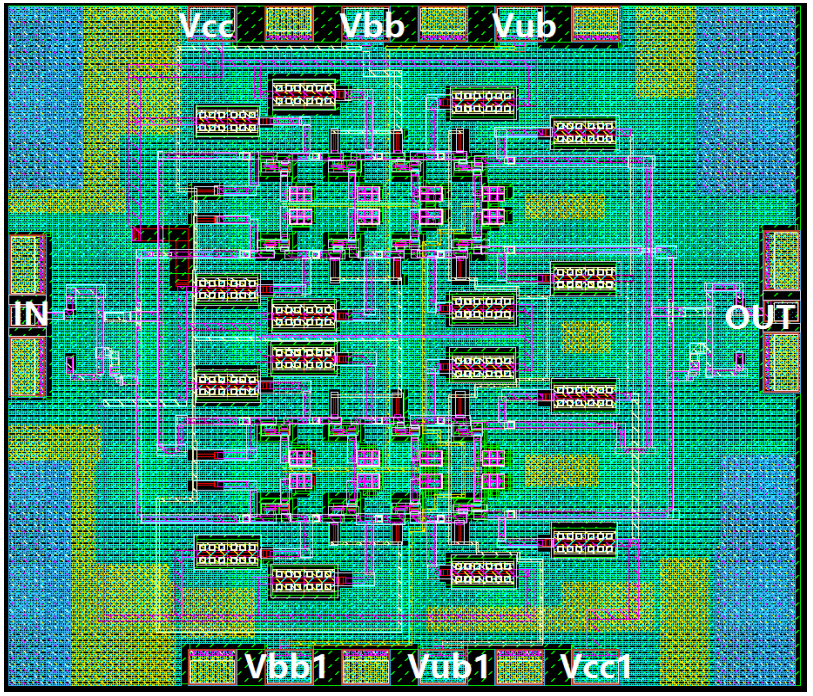
- Demonstrates model quality under realistic operating conditions
  => reduces *"blame game"*

- Well-designed circuits also allow process performance evaluation

95-195 GHz ultra wideband power amplifier

- Four-stage differential cascode configuration with two-way power combination
- Fabricated in B11HFC from Infineon
- Purpose: (i) integrated frequency extender for on-wafer small-signal device characterization (TARANTO WP 3.1); (ii) model verification

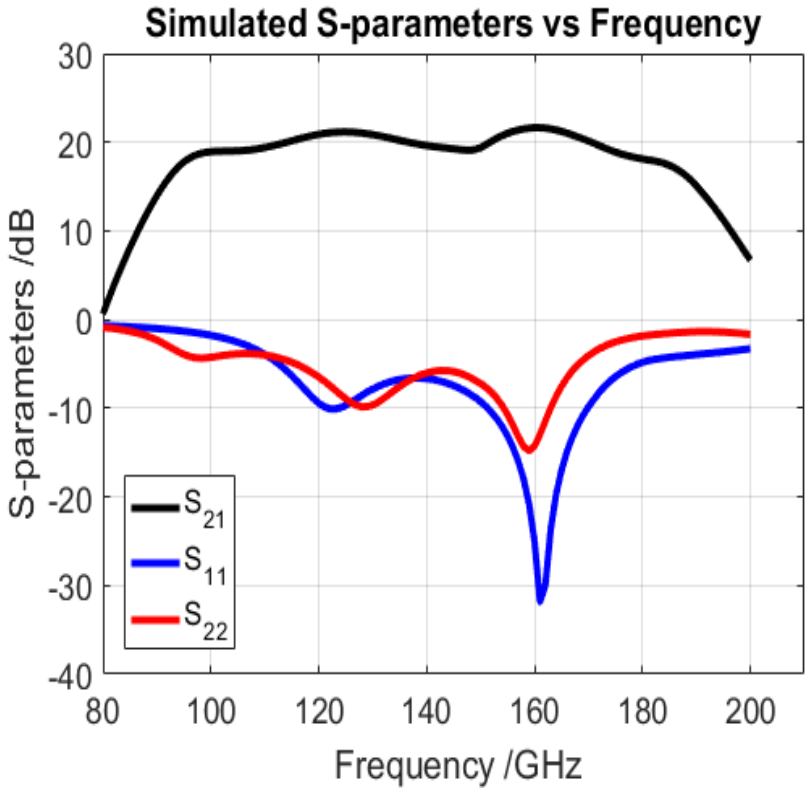


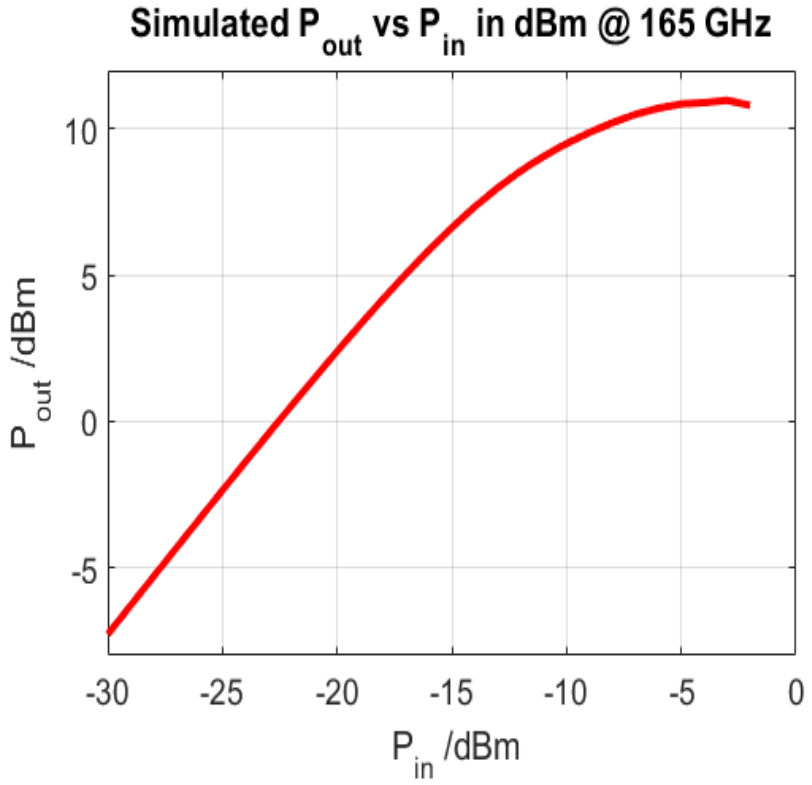


- Chip size ~ 1150 µm x 1300 µm

Electrical results (simulation so far)

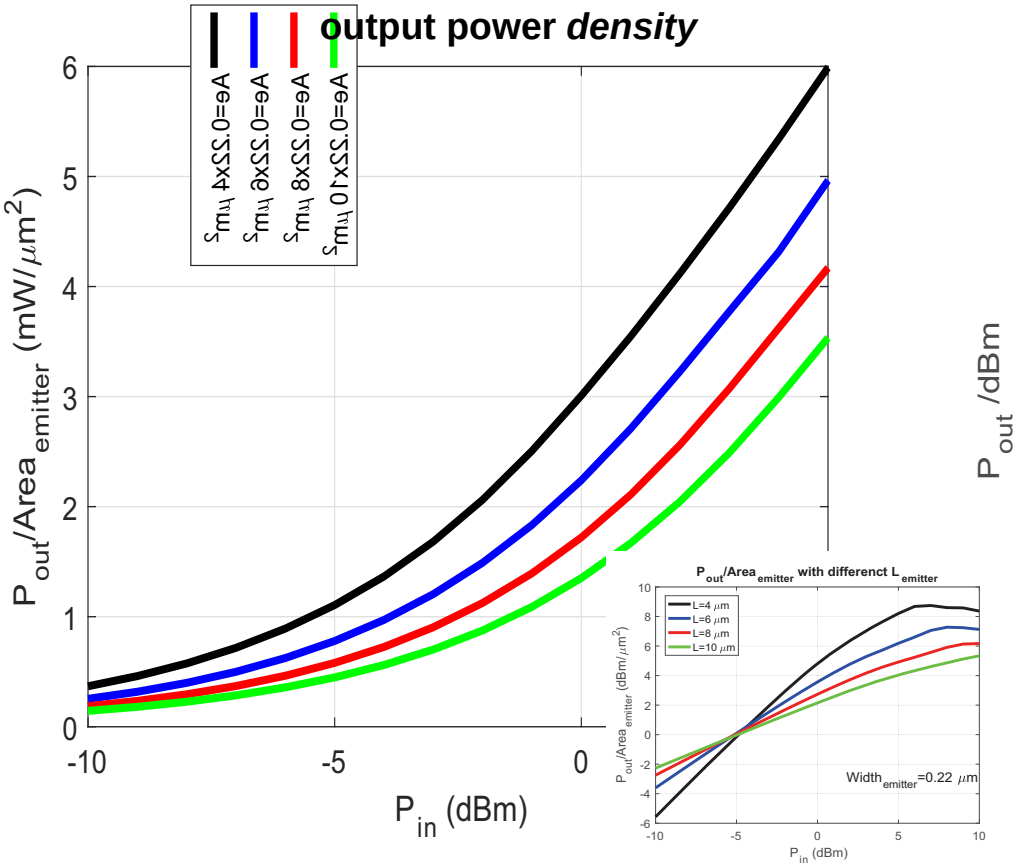
- In-band Gain of 21 dB; CBEBC configuration; Emitter size of 0.22 µm * 10 µm
- $P_{sat,out}$ = 10.7 dBm @ 165 GHz; $P_{1dB,in}$ = -13 dBm; $P_{1dB,out}$ = 6.4 dBm @ 165 GHz
- Sent for fabrication in May 2018, with an expected chip delivery in Sep 2018

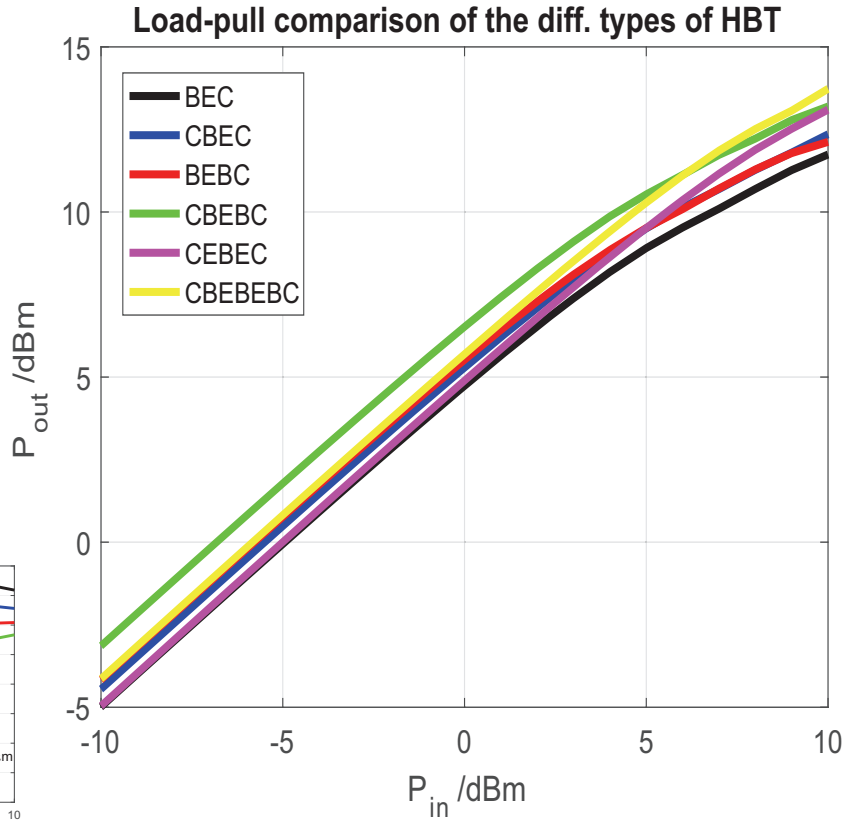




Impact of different layout configurations of HBTs

- Load-pull of a single transistor used in previous PA design (incl. s.h.)

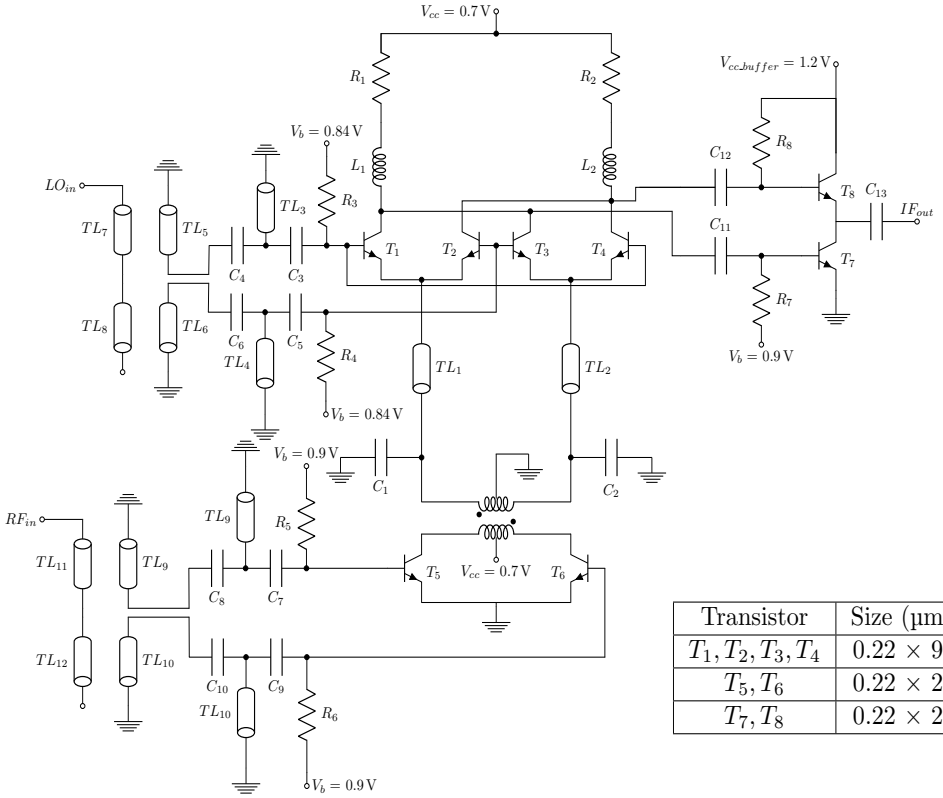




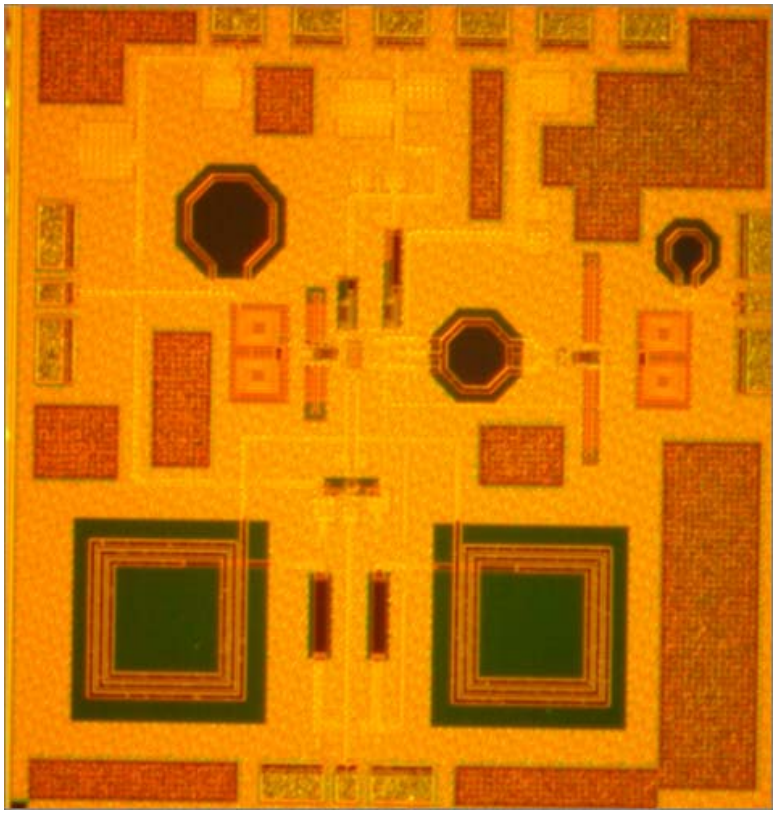
=> CBEBC and CBEBEBC HBT layouts offer higher $P_{sat,out}$ (about 2 ~ 2.5 dB) than default BEC HBT

97 GHz low-power down-conversion mixer

- 0.7 V supply voltage for the mixing core
- Transformer-coupled Gilbert cell with ~ 7 GHz output IF frequency
- Fabricated in B11HFC technology from Infineon



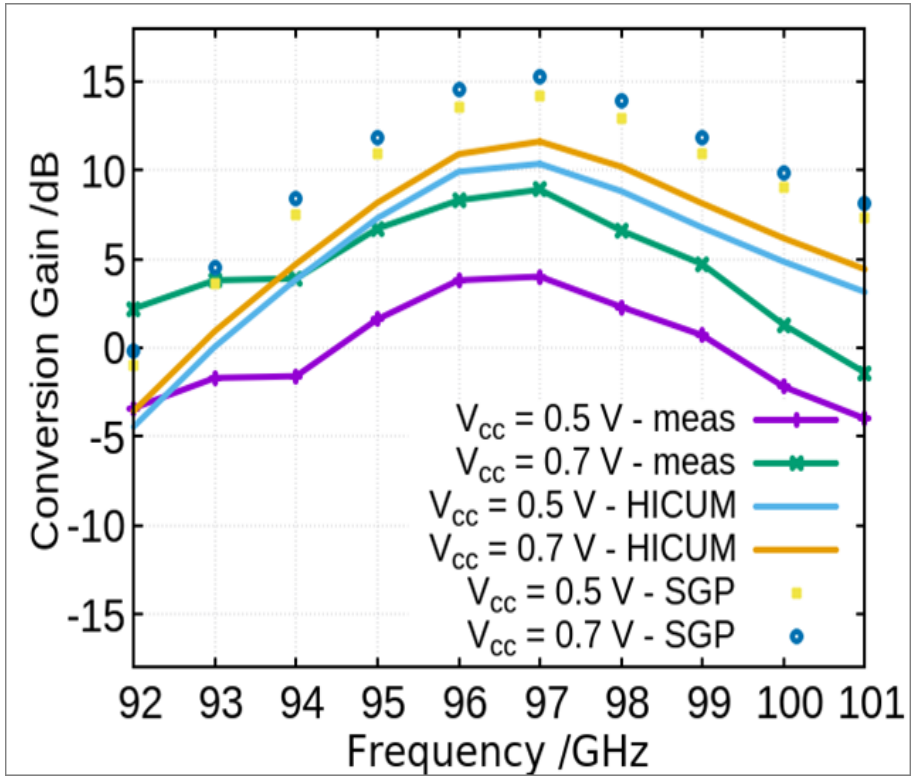
Transistor	Size (μm^2)
T_1, T_2, T_3, T_4	0.22×9.8
T_5, T_6	0.22×2.3
T_7, T_8	0.22×2.3

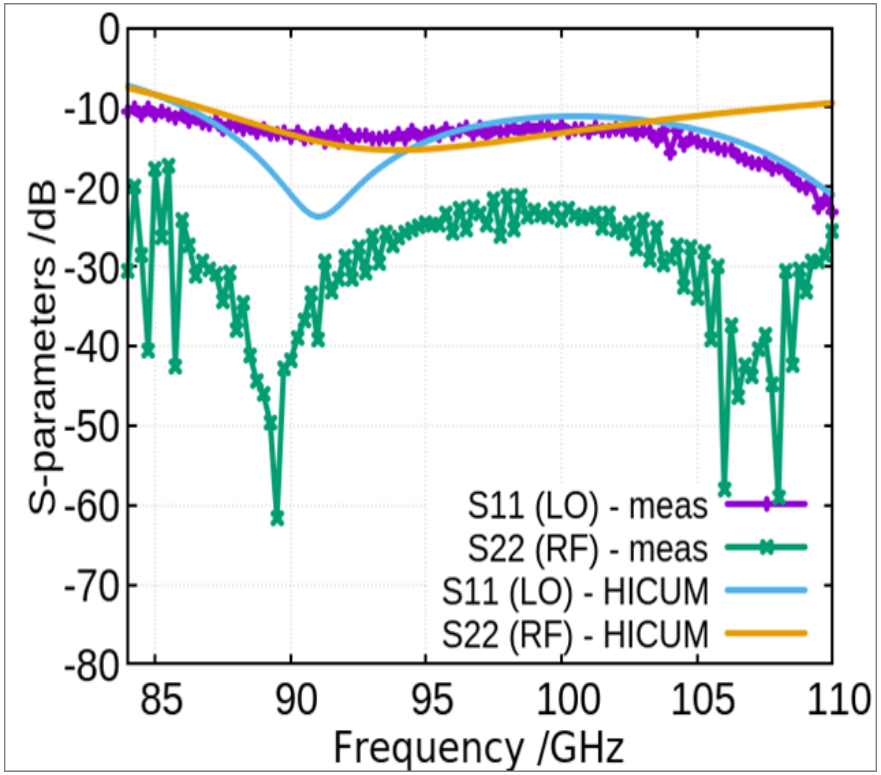


- Chip size ~ 1150 µm x 1200 µm

Results: experimental vs simulation

- V_{cc} = 0.7 V (mixer core), LO power = -2.9 dBm @ 90 GHz

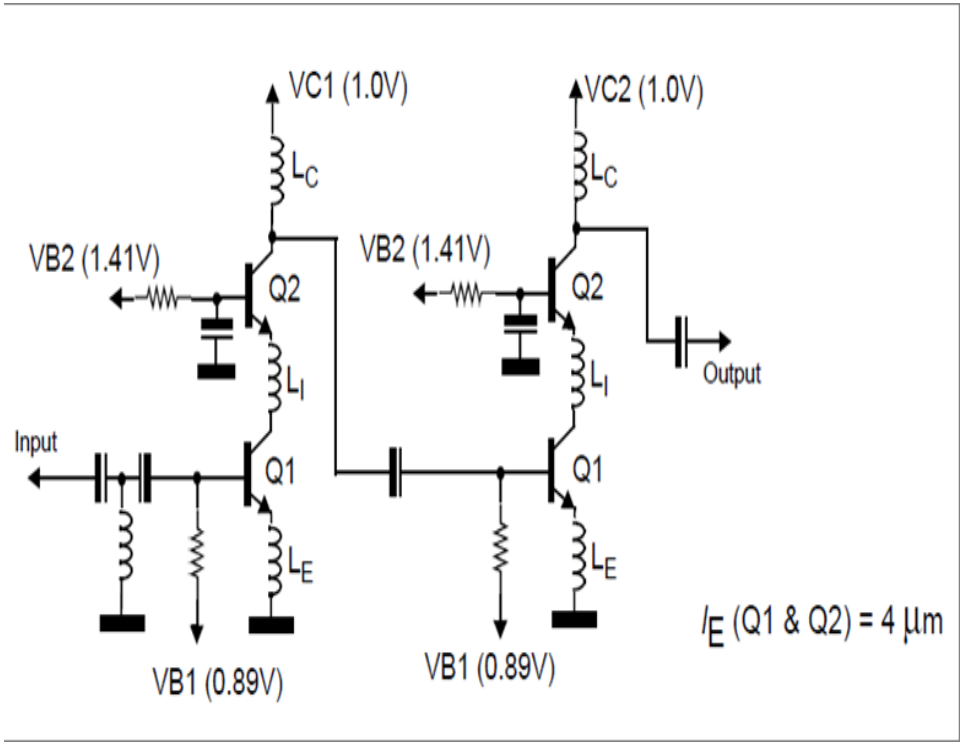


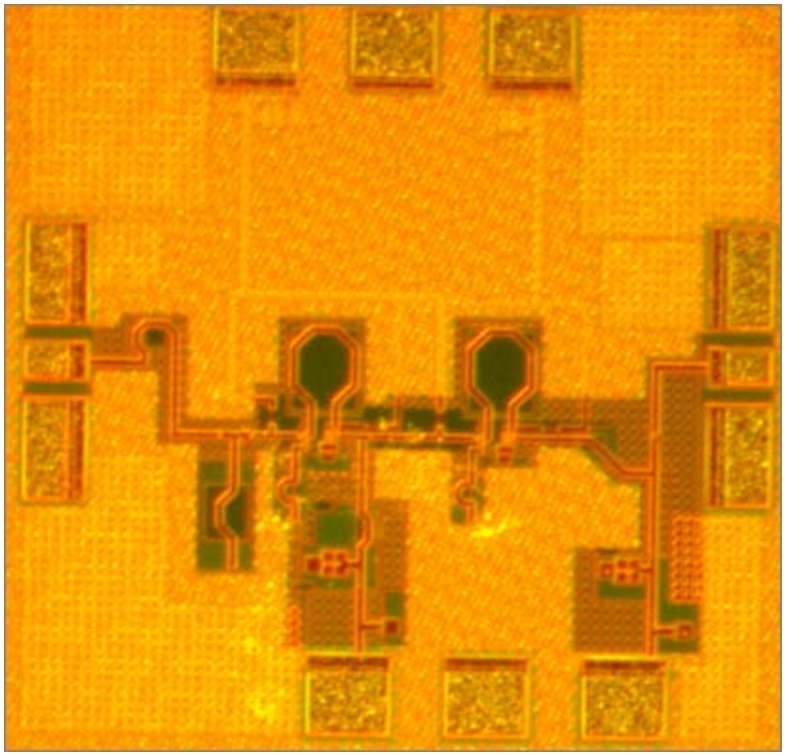


- SGPM significantly overestimates conversion gain
- Reasonable agreement with HICUM based simulation for G_C and S_{11} at V_{cc} = 0.7V
- Larger deviation when V_{cc} = 0.5 V, and the reason is unknown yet.

W-band low power narrow-band LNA

- Two-stage cascode configuration with 1.0 V supply voltage
- Both transistors biased in weak saturation (V_{BC} = 0.36 V)
- Fabricated in B11HFC from Infineon

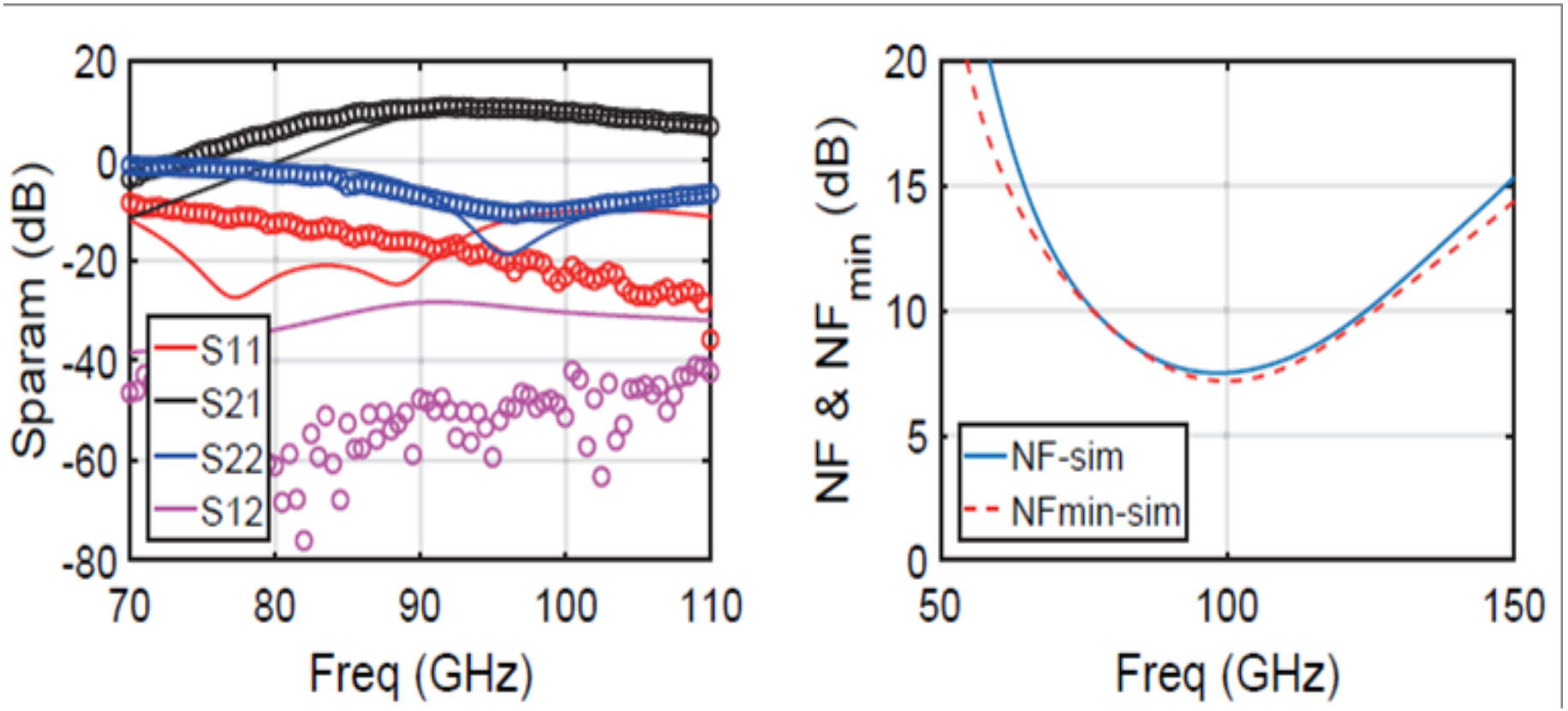




- Chip size ~ 680 µm x 700 µm

Results: experimental vs simulation

- 11 dB peak gain (measured) with only 1 V cascode supply voltage



- good agreement for S_{21} and S_{11}, larger deviations for S_{12} and S_{22}
- noise figure(s) yet to be measured

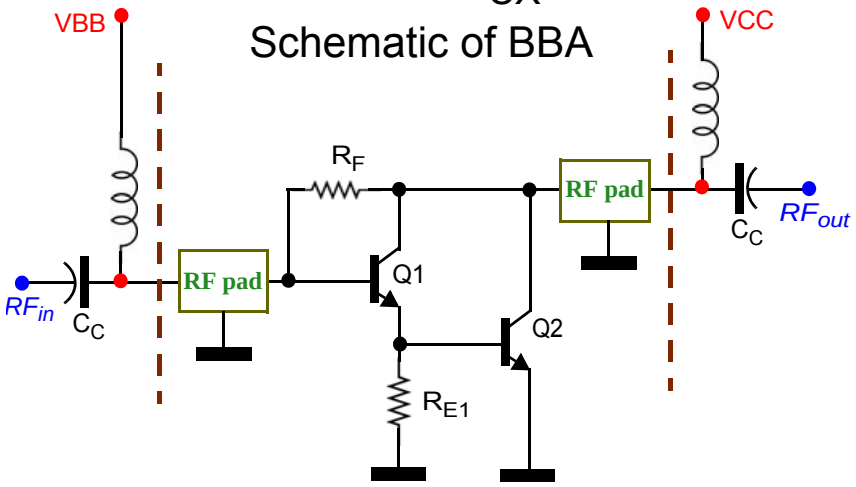
Broadband Amplifier (BBA)

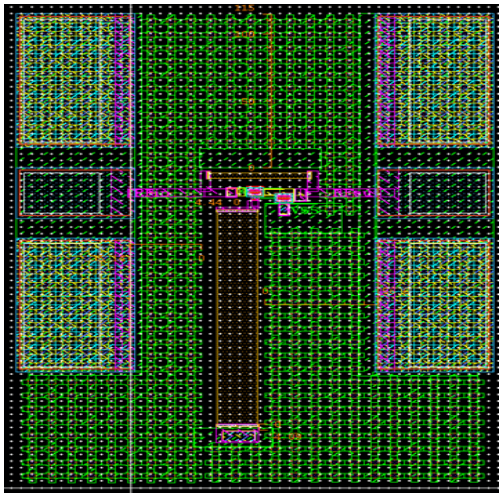
Goal: model verification

- BBA (w/o L_P) variants with three different transistor geometries:
  - CBEBC
  - BEC
  - CEBEC
  - Same A_E of Q1 & Q2 for all three variants; also:
    - R_{E1}=150 Ω and R_F=250 Ω
    - VCC=1.5 V and VBB=1.81 V
    - I_{CC} is higher for double collector device due to lower R_{CX} value

parameters	CBEBC	BEC	CEBEC
l_E (µm) (Q1, Q2)	4.2, 5	4.5, 5.2	2.3, 2.6
b_E (µm) (Q1,Q2)	0.2, 0.2	0.2, 0.2	0.2, 0.2
V_{BB},V_{CC} (V)	1.81, 1.5	1.81, 1.5	1.81, 1.5
S_{21} (dB)	12.1	12.05	12.05
3 dB BW (GHz)	43	37.5	36

Schematic of BBA



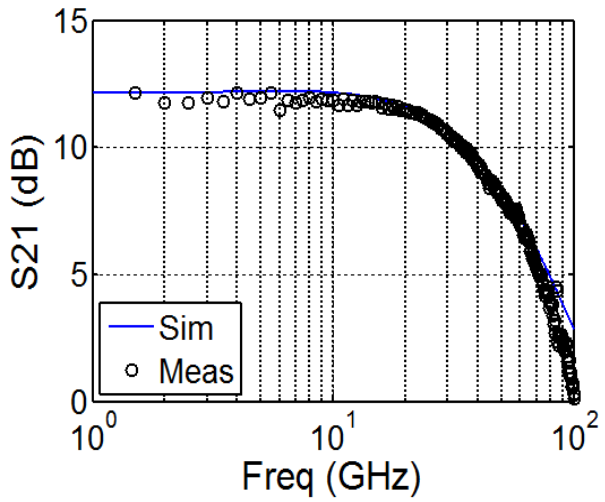


Results: experimental vs. simulation

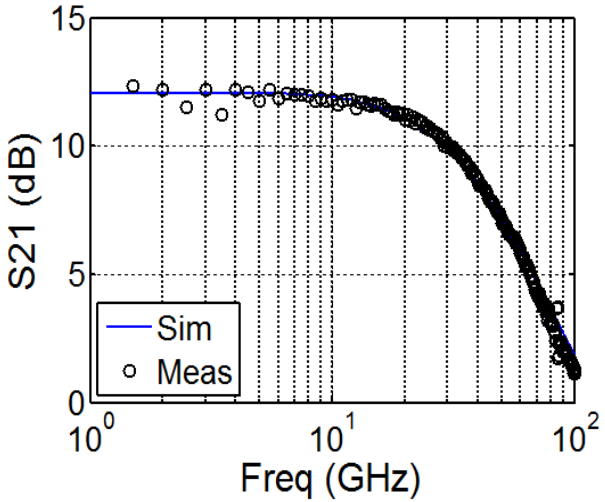
- Realized in B11HFC technology from Infineon
- Total die-size of each amplifier is 0.35 mm x 0.24 mm ~ 0.084 mm²
  => All three variants fit into regular transistor HF pad layout
- Transistor operating points set through external bias-tees

Simulated vs. measured small-signal gain (S_{21})

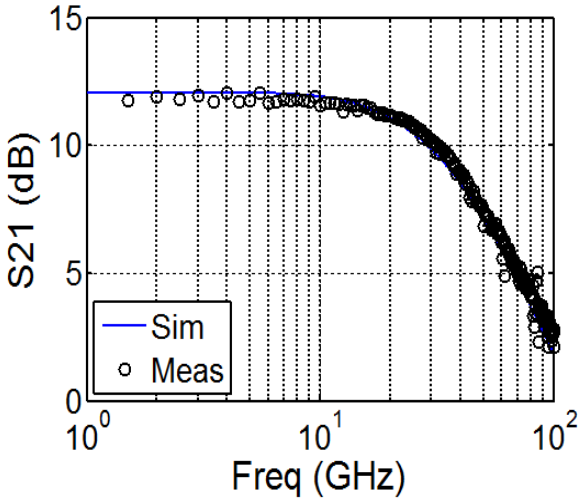
CBEBC device



BEC device



CEBEC device

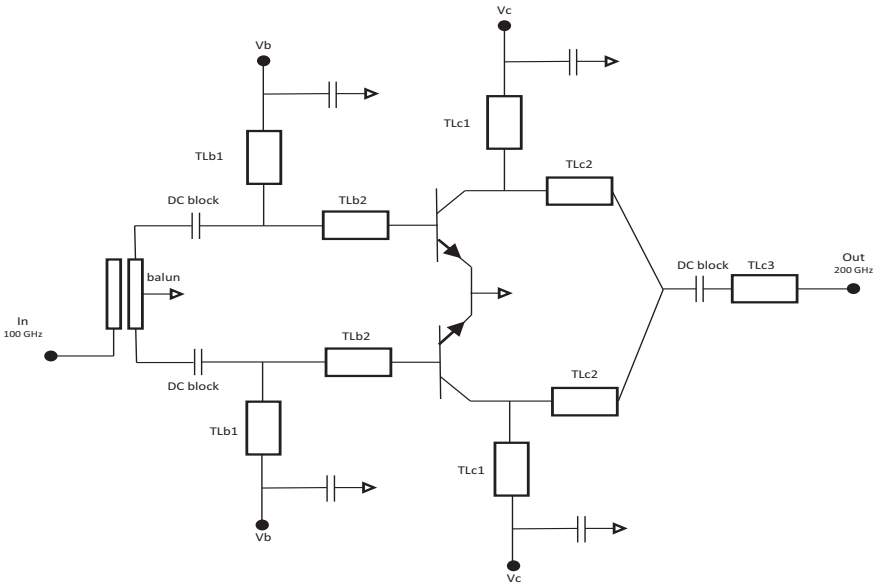


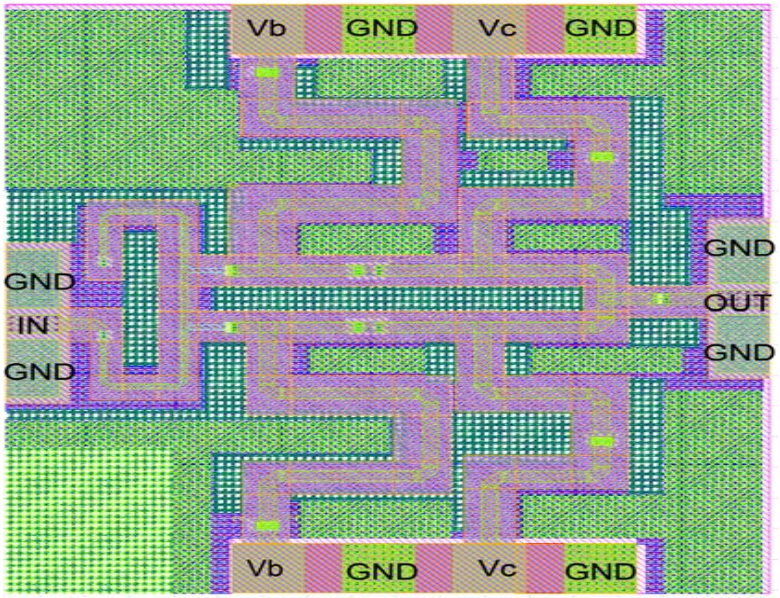
=> good agreement between simulation and measurement

- Bandwidth decreases from CBEBC over BEC to CEBEC

180-210 GHz (G band) frequency doubler

- Goals:
  - high output power around 200 GHz from 100 GHz signal source
  - integrated frequency extender for on-wafer small-signal device characterization (TARANTO WP3.1)
- Transistor size 0.07 µm x 3.6 µm
- Fabricated in 0.13 µm SiGe HBT technology from IHP

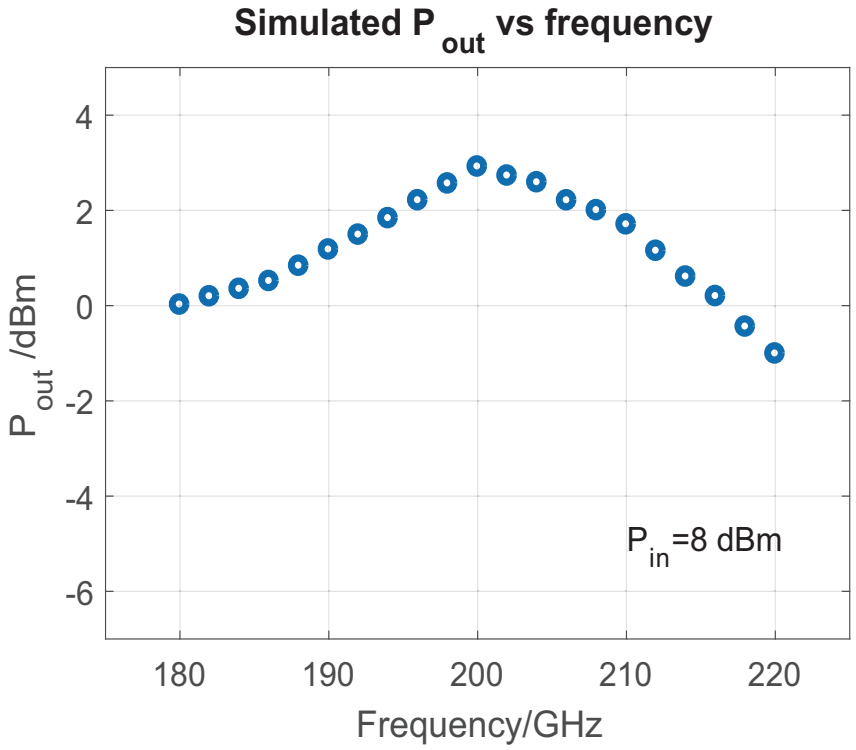


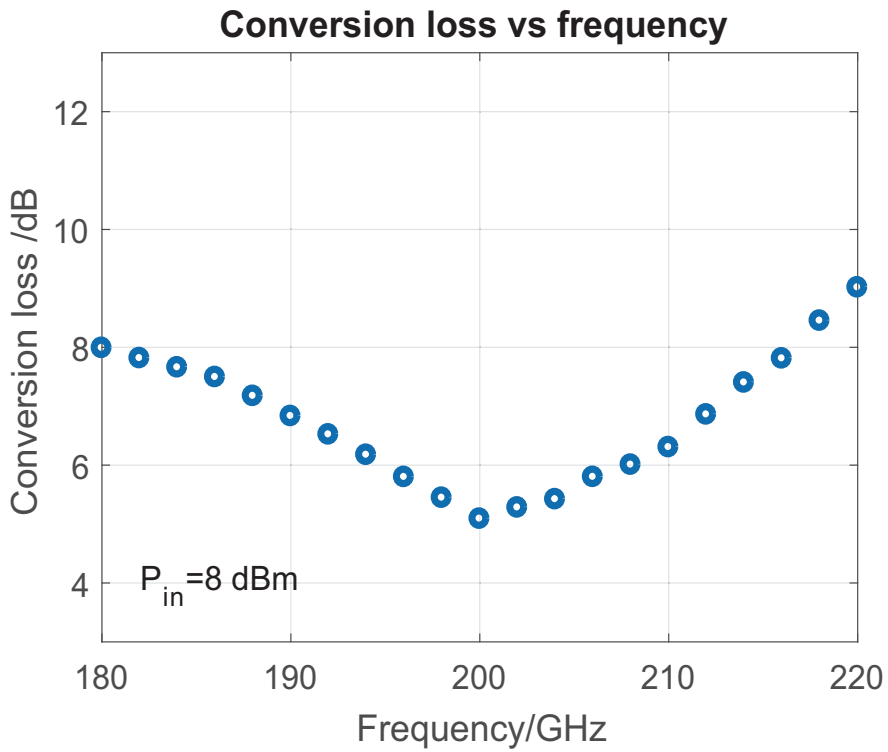


- Chip size ~ 860 µm x 980 µm

Simulated results

- Maximum 3 dBm output power @ 200 GHz with 8 dBm input @ 100 GHz
- Minimum 5 dB Conversion loss
- 3-dB bandwidth is around 35 GHz (180-215 GHz range)

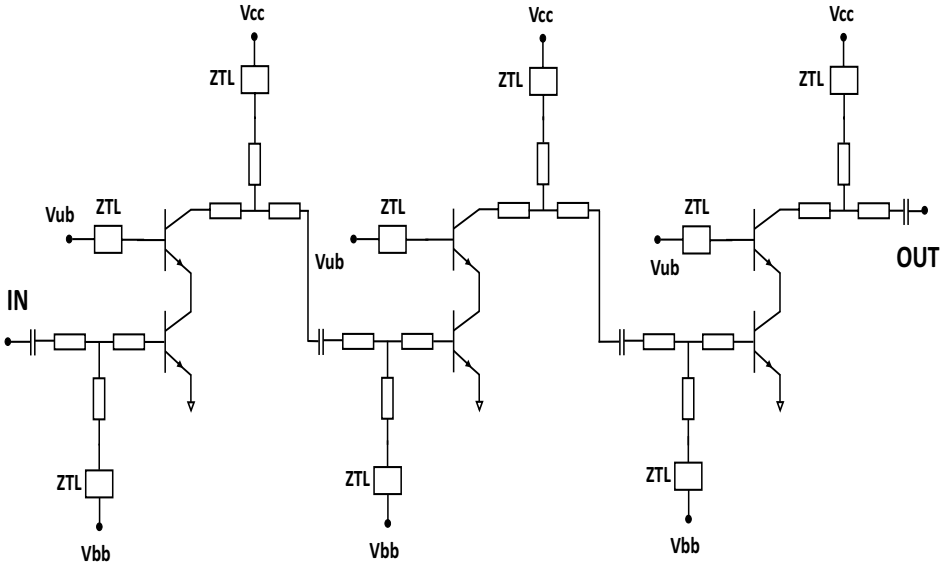


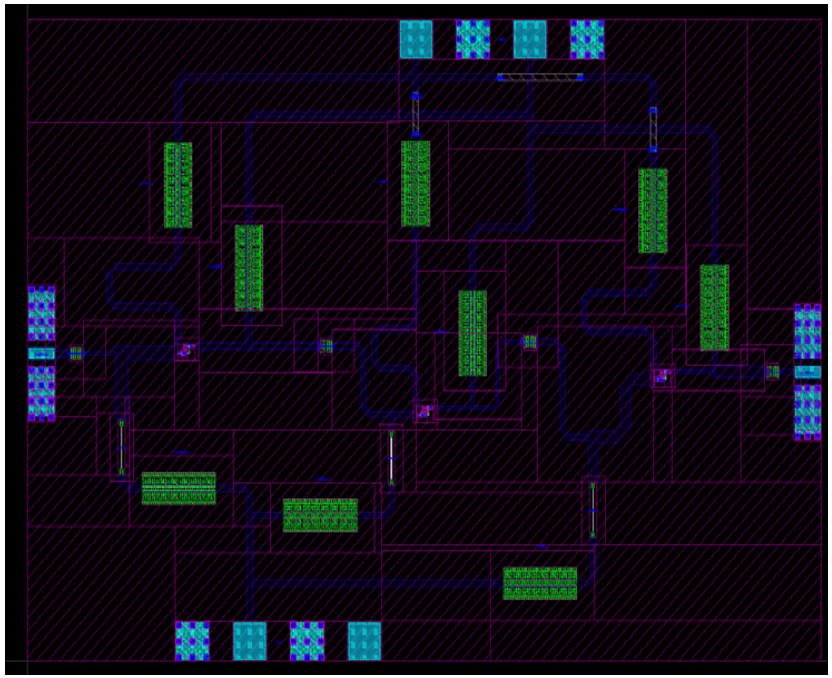


- Sent for fabrication in Aug 2017, already got the chip, waiting for measurement

140-170 GHz LNA

- Three-stage cascode configuration, transistor size 0.25 µm x 4 µm
- Fabricated in 0.25 µm InP HBT from Teledyne
- 1.8 V supply voltage (normally >3 V recommended in this technology)

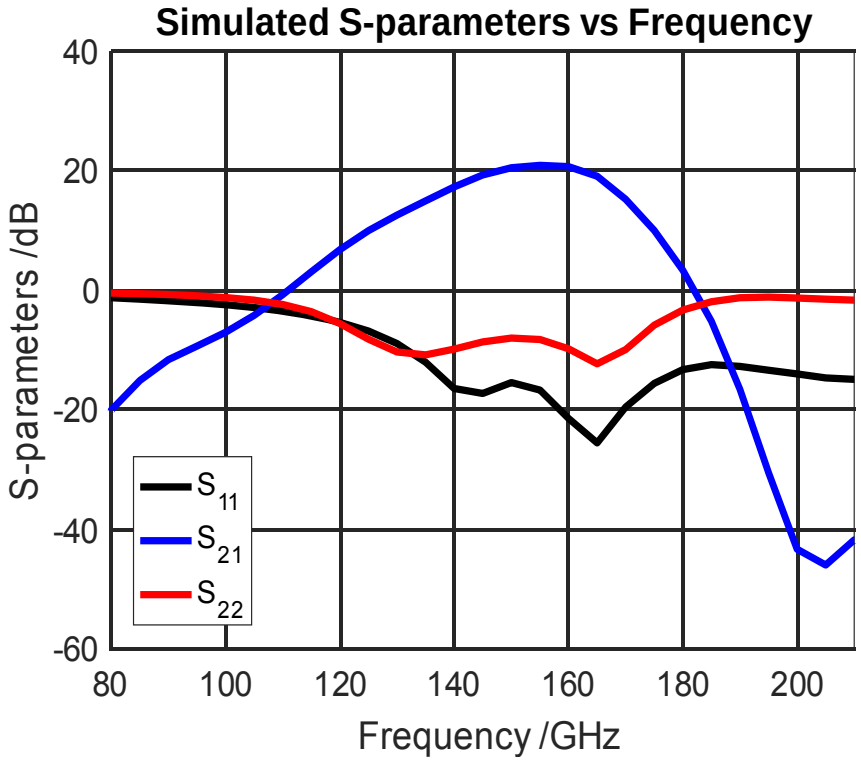


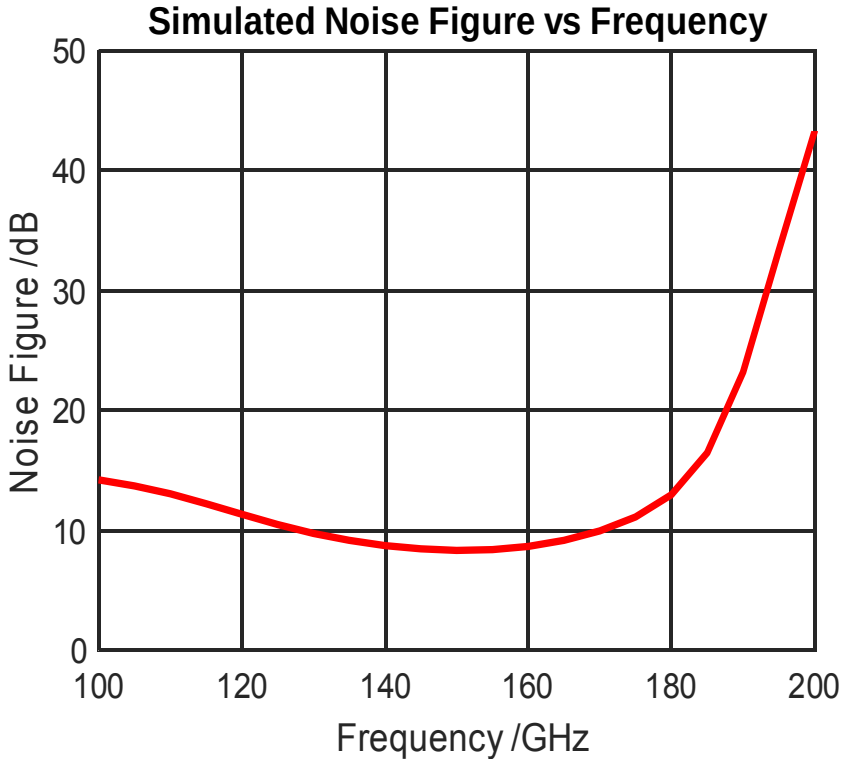


- Chip size ~ 1250 µm x 1800 µm

Simulated results

- >20 dB gain @ 160 GHz
- 8 dB minimum noise figure
- 30 GHz bandwidth over 140-170 GHz





- Sent for fabrication in Feb 2018, with an expected chip delivery in Aug 2018

Conclusions

- Design of mm-wave benchmark circuits
  => bridging gap between modeling and circuit design engineers

- Design of circuits beyond 160 GHz for on-chip frequency extension
  => to enable transistor characterization and model verification beyond 220 GHz

- Design of low-power mm-wave circuits
  => demonstrate potential of SiGe HBT technology for considerably reduced power consumption
  => model verification and demonstrate usefulness of operation in saturation region

Acknowledgements

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