

# Design of a C-Band CMOS Class AB Power Amplifier for an Ultra Low Supply Voltage of 1.9 V

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**Abstract** — Present day power amplifier (PA) design struggles with the fact that applicable supply voltages are continuously shrinking for short channel MOS transistors, which makes reaching high output power values increasingly difficult. This work develops a Class AB PA with an optimized load impedance for maximum output power with the help of a systematic load-pull analysis. It will display necessary trade offs for optimum output power and small signal gain. The presented PA, realized in CMOS, shows a measured output power of 19.8 dBm at 5.8 GHz for a supply voltage of 1.9 V. The drain efficiency at the 1 dB compression point reaches 28.1 %, the highest report up to today for this output power level.

**Index Terms** — Power Amplifier, low supply voltage, load pull analysis.

## I. INTRODUCTION

Power amplifiers for WLAN applications in the C band need to fulfill several crucial design specifications. Most important is a high output power value of typically around 20 dBm and higher. Furthermore, the architecture has to offer sufficient gain. Looking on the current climate debate, energy efficiency becomes increasingly important. Finally, the architecture should be producible with a low cost standard IC process in order to create a competitive product. While III/V semiconductor technologies can realize very high output power values together with comparably competitive efficiencies, they are still expensive in mass fabrication when compared to standard CMOS processes. MOSFETs, however, support only small supply voltages and therefore generally allow only small output power values for single amplifier stages. Furthermore, lower supply voltages simultaneously reduce the attainable efficiency levels. The ratio  $V_{\text{sat}}$  to  $V_{\text{Supply}}$  increases, which reduces the achievable RF voltage swing in relation to the available supply voltage and thereby decreases the obtainable drain efficiency of the amplifier. State-of-the-art power amplifiers are referenced by [1], [2] and [3]. One can clearly see the struggle between high output power and high efficiency.

As output power decreases approximately quadratic for lowered supply voltages, one way to increase the output power is to use an output matching network that converts a small load impedance seen by the transistor into the 50 termination needed. This transforms a low RF voltage – and high RF current – swing at the transistor drain into a high RF voltage and moderate RF current swings at the load. The load

pull analysis will screen the solution space of possible load impedance and helps choosing an optimum value with respect to output power level and small signal gain.

The PA presented is intended for mobile wireless terminals working according to the 802.11.a and 802.11n standard. Low supply voltage and high efficiency is a must for reduced battery count and prolonged battery lifetime. The potential application areas are WLAN and local positioning services as developed in the Resolution Project [4].

## II. DESIGN PROCESS

### A. Architecture Determination

The Class AB PA introduced here uses a supply voltage of only 1.9 V and is intended for the frequency range between 5 and 6 GHz. The applied process is the IBM-7WL CMOS process with minimum gate lengths of 180 nm and a  $f_T$  of up to 35 GHz for the MOS transistors

The starting point of the design is the choice of the intended technology, architecture and operating point. The choice of MOSFETs, supporting 1.9 V, is based on the need for a cost competitive architecture that uses an ultra low supply voltage.

The second selection is the chosen architecture and bias point. For output power levels of 20 dBm, a linearly amplifying PA biased in class AB with little distortion losses is a good choice for an one-stage PA design.

The next step is to look at the transistor width. The goal of around 25 to 30 % drain efficiency signifies a DC current of around 200 mA. This in turn leads to a transistor width of 1 mm for a gate bias between 1.1 V and 1.2 V.

### B. Load Pull Analysis

The output matching network is of major importance in order to achieve the intended power levels. It has not only to fulfill an impedance matching for the load termination but also to present an optimum impedance value to the transistor that leads to a maximum transferred power into the load. For a given transistor size, bias and fulfilled input matching, the load pull analysis sweeps the load impedance seen by the transistor and calculates the obtainable real output power across the resistive part of the load.

Fig. 1 shows a schematic representation of the load pull simulation structure. The impedance values of the bias elements have to be chosen sufficiently high in order not to be

visible at the C band. They comprise a large RF shunt inductance for the DC supply path and a large DC block capacitance, simultaneously a RF short cut for the load pull analysis. For each of the analyzed load impedance values, the input power is swept and the output power calculated in order to create a  $P_{out}$  versus  $P_{in}$  plot, scaled in dBm, in order to read out the 1 dB compression point ( $P_{1dB}$ ).

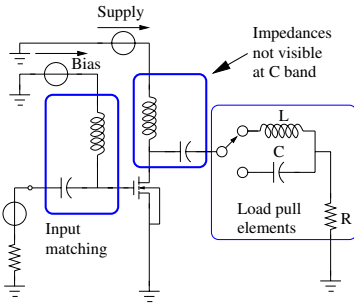


Fig. 1. Schematic representations of load pull simulation structure.

Simultaneously, one can extract the attainable large signal gain by subtracting  $P_{in}$  from  $P_{out}$  in the linear region. For perfect input matching conditions, the calculated large signal gain equals  $S_{21}$ .

### C. Load Pull Analysis Results

Fig. 2 shows the results for the load pull analysis for the given Class AB configuration described before.

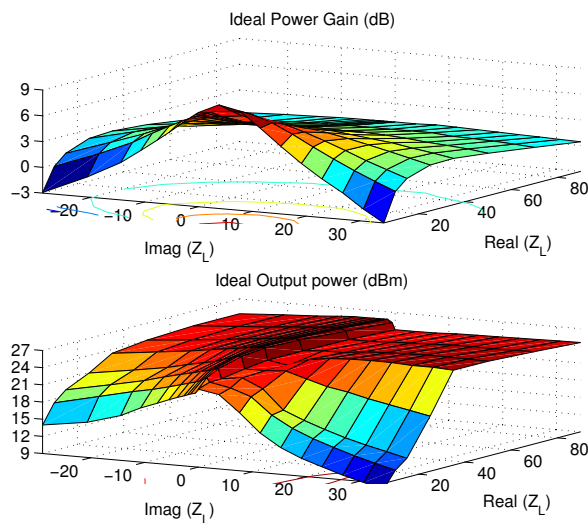


Fig. 2. Load-pull analysis results for the Class AB PA with transistor width of 2.5 mm, measured at 5.5 GHz.

The real part of the load impedance is swept from 5 to 90  $\Omega$ . Values below 5  $\Omega$  are prohibitive, because parasitic

impedances then increasingly influence the seen resistive load impedances and decrease efficiency, values above 90  $\Omega$  lead to negligible small signal gain. The imaginary part is swept on the one hand from 1 pF to 50 pF. Values below 1 pF would lead to decreasing  $S_{21}$  and output power values. On the other hand, the sweep is realized from 0 H to 1 nH. Values above 1 nH are prohibitive due to increasing parasitic losses. One can see that while  $S_{21}$  increases up to 9.1 dB toward the small resistive load impedance value of 5  $\Omega$ , the obtainable output power saturates to around 25 dBm for the opposite direction towards high resistive load impedances of 90  $\Omega$ .

These results are only a starting point for the design of the output matching network. Especially the negligence of the parasitic losses that come along with the use of inductive passive elements can decrease gain and output power, depending on the Q-factors of the inductance implementations available in the technology. Furthermore, by changing the gate bias voltage, one can fine tune the circuit toward varying efficiency and small signal gain values.

### D. Circuit Design

Fig. 3 shows the schematic representation of the final circuit.

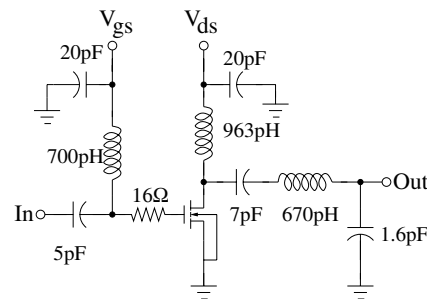


Fig. 3. Schematic representation of Class AB PA circuit.

The passive matching network, together with the 50  $\Omega$  termination not shown, was designed in order to present a load impedance at the transistor drain of :

$$Z_L = 5\Omega + j3.4\Omega \quad (1)$$

Comparing this load impedance with the results of the load pull analysis in Fig. 2, one can expect a small signal gain of 9.1 dB and a  $P_{1dB}$ -value of 22 dBm at 5.5 GHz.

The input and output matching networks assure matching conditions for the frequency range between 5 and 6 GHz. The 16  $\Omega$  resistor at the gate is introduced for stability reasons.

Fig. 4 shows the Class AB PA die photo. The input pad is on the left side, the output on the right side. The RF shunt inductance with a value of 963 pH for the DC supply is patterned as a left open 'U' using inductive line elements. Below the DC path, the RF output path is visible. A vast

ground realization can be seen at the lower side of the chip. The ground has to be realized as ideal as possible in order to avoid inductive degeneration in the transistor source due to parasitic inductances in the ground plane. This is especially important for this design, as this design trades the large output power value for a small value of  $S_{21}$ . Therefore, as many ground pads as possible as well as ample ground plane realization as visible in the lower part of the layout are crucial.

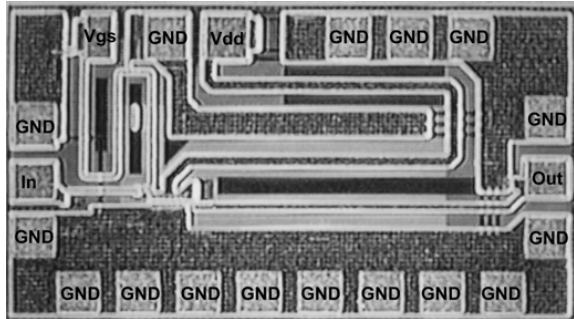


Fig. 4. The photo of the Class AB PA die, size: 1.45 x 0.85 mm<sup>2</sup>.

Fig. 5 shows the Q-factor simulations for the DC supply - as well as the RF output - path inductances. Q-factor values of 19.9 respectively 23.1 at 5.5 GHz show that the losses in the output matching network are manageable. The losses associated with the MIM capacitances are even smaller and can be neglected in comparison to the inductances.

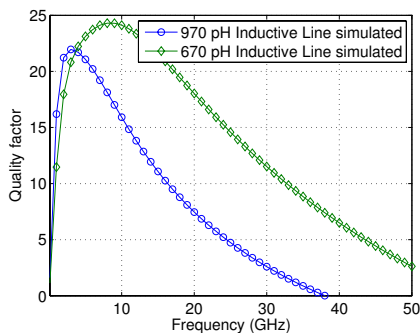


Fig. 5. Simulated performance of inductive line elements.

### III. MEASUREMENT VERSUS SIMULATION RESULTS

The following figures show the measured and simulated main figures of merit for the PA. While the measurements are obtained by on wafer measurements using network analyzer and power meter, the simulation results include the parasitic extracted capacitive and inductive elements of the drawn layout.

Fig. 6 shows the port reflection coefficients. Surprisingly, the measured matching peaks are slightly shifted to higher frequencies. An explanation could be that the parasitic extraction overestimated the parasitic capacitances of the matching networks in the simulation. This in turn shifted the peaks to higher values in reality.

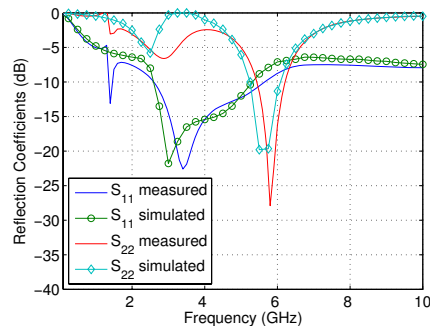


Fig. 6. Measured and simulated  $S_{11}$ - and  $S_{22}$ -parameters.

Fig. 7 shows both plots for simulated and measured small signal gain. While there is a very good consistency between simulated and measured gain results between 5 and 6 GHz, the simulation predicted higher gain values at 2.5 GHz, which indicated possible lower stability at this frequency.

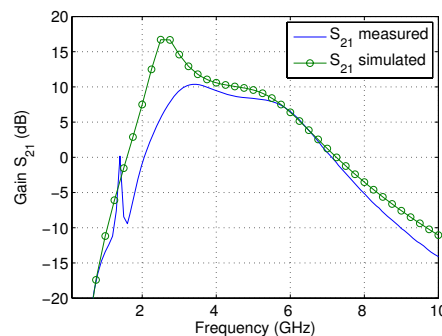


Fig. 7. Measured and simulated  $S_{21}$ -parameters.

This can also be seen, when looking at the simulated  $S_{22}$  values. One explanation for this mismatch could be a cross coupling between the U shaped DC supply path elements. Keeping in mind that the load pull analysis predicted 9.1 dB gain for the use of ideal passive elements at 5.5 GHz, the circuit simulation based on a layout extraction, including parasitic resistive, capacitive and inductive elements, predicted a value of 8.4 dB. The measured gain amounts to 8 dB and shows thereby a very good consistency to the simulated results.

Fig. 8 shows the simulated and measured plots for the 1 dB compression point, considered at 5.8 GHz. The measurement was carried out at 5.8 GHz, being the intended operation frequency for the Resolution project [4]. While the load pull analysis predicted around 22 dBm, the final layout extraction simulation showed a reached value of 20.6 dBm. The measured value of 19.8 dBm can be considered as a close match to the simulated results. The measured flowing current of 177 mA at  $P_{1dB}$  for a supply voltage of 1.9 V leads to an efficiency of 28.1 %. This value is a very satisfying result for a Class AB power amplifier.

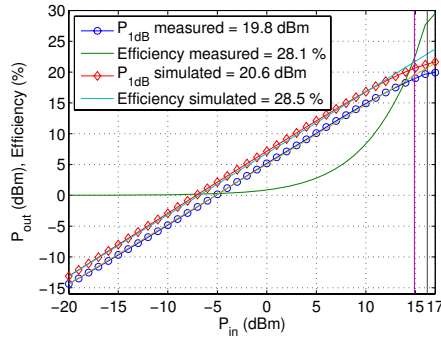


Fig. 8. Measured and simulated  $P_{1dB}$ -plots @ 5.8 GHz.

#### IV. COMPARISON WITH STATE OF THE ART

Table I shows the key performance characteristics for recent publications in the area of high output power PA design for ultra low supply voltages in CMOS. The results of the works referenced by [1] and [3] show 1dB compression point values that lie 2 and 1.2 dBm, respectively, above the work presented here. However, one can clearly see that these values are achieved for a significantly lower drain efficiency that will become more and more prohibitive with nowadays energy efficiency discussion. On the other hand, although the work

TABLE I  
COMPARISON WITH STATE OF THE ART AT C-BAND

Ref.	[1]	[2]	[3]	This work
<b>Techn.</b>	0.18 m CMOS	0.18 m CMOS	0.25 m CMOS	0.18 m CMOS
<b>Class/ # stages</b>	AB/3	AB/2	A/2	AB/1
<b>V<sub>Supply</sub></b>	1.8 V	1.8 V	2.0 V	1.9 V
<b>P<sub>1dB</sub></b>	21.8 dBm	17.4 dBm	21 dBm	19.8 dBm
<b>Gain</b>	21 dB	15.1 dB	> 6 dB	> 7 dB
<b>Drain efficiency</b>	13 %	27 %	22.5 %	28.1 %

referenced by [2] offers a comparably high efficiency, the  $P_{1dB}$  - value remains far below the 19.8 dBm presented in this work. To the knowledge of the author, the achieved 1 dB compression point value per V available supply voltage in combination with the high drain efficiency of 28.1 % is the highest value realized in CMOS, reported up to today. This work therefore contributes to the enhancement of the state-of-the-art.

#### V. CONCLUSION AND OUTLOOK

This paper highlights the use of the load pull analysis and shows the different steps and trade offs for the design of a power amplifier. The load pull analysis develops the possible solution space and shows the necessary trade off of a lower small signal gain value in order to reach high output power values for ultra low supply voltages. The Class AB PA design is developed toward the final layout and simulation and measurement results are compared. The measured PA shows an excellent 1 dB compression point value of 19.8 dBm for a supply voltage of 1.9 V.

Other architectures like switched PA design can achieve clearly higher efficiencies values than 28.1 %; however, they mostly trade this for lower output power values or use significantly higher supply voltages.

Towards a further development of the design, a preamplifier stage increasing the small signal gain seems very promising. The additional power needed for this stage could be made up by a shift of the main PA stage towards a class B operation point, thereby decreasing the DC power consumption of the main stage.

#### VI ACKNOWLEDGEMENT

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