Thermal Noise in MOSFETs: A Two- or a Three-Parameter Noise Model?

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***Abstract*—In this brief, it is clearly demonstrated that a two-parameter noise model is sufficient to accurately extract the MOSFET high-frequency noise performance, as long as channel uniformity is ensured (which corresponds to mainstream CMOS technology). Nevertheless, in the case of asymmetric channel-based MOSFETs, it is shown that a three-parameter noise model is required.**

***Index Terms*—Graded-channel MOS (GCMOS), mainstream MOSFETs, modeling, noise correlation coefficient, silicon on insulator (SOI), thermal noise.**

I. Introduction

THE MODELING of thermal noise has always been a challenge. In 1962, van der Ziel first introduced an understanding and a modeling of the thermal noise in field-effect transistors (FETs) [1], [2]. Based on this pioneering work, more models were introduced later on. In 1974, Pucel *et al.* proposed a three-parameter noise model, known as the PRC model [3], [4]. This noise model considers a gate noise current source i_g (induced gate noise) at the input and a drain noise current source i_d at the output, whose spectral densities are proportional to noise dimensionless coefficients R and P, respectively. These two noise sources are correlated, with a pure imaginary complex correlation coefficient $Cor = j.C$, explained by the capacitive coupling existing between the channel and the gate (in this brief, C is referred to as the correlation coefficient). For a recent technology node (gate length $\geq$ 65 nm) of MOSFETs, either in bulk or in silicon-on-insulator (SOI) technologies, the value of C is relatively weak (lower than 0.4) [5]–[7], in contrast to those usually observed in the case of III–V FETs or HEMTs (between 0.8 and 0.95) [4]. In 1989, Pospieszalski proposed a two-parameter noise model [8], [9]. In this model, two uncorrelated noise sources are considered: a gate noise voltage source at the input and a drain noise current source at the output. The spectral densities of these two noise sources are proportional to the equivalent noise temperatures T_g and T_d, respectively. The fact that the noise sources in the voltage–current representation are uncorrelated is equivalent to having the following relation between C, R, and P when considering the current–current representation:

$$C = \sqrt{\frac{R}{P}}. \tag{1}$$

This relation reduces, *de facto*, Pucel's noise model to two parameters. In order to study the validity of (1), Danneville *et al.* [10] introduced a complete analytical study of noise models of III–V FETs using a uniform active line theory and a more realistic set of results obtained by using the software HELENA [11].

The two-parameter noise model of Pospieszalski has widely been used within the III–V research community and within the Si MOSFET research community [12]–[15]. Nevertheless, a clear study justifying the use of this noise model for MOSFETs has not yet been reported. The importance of such a study inherits from the fast-growing trend to use the mainstream CMOS technology in high-frequency (HF) applications. Recently, as a result of aggressive scaling, mainstream CMOS technology can provide higher cutoff frequencies than HEMTs [16] while offering more flexibility in terms of technological parameters (e.g., equivalent barrier thickness [16]), device architecture (e.g., gate structure), or even design methodologies. These advantages put the MOSFET ahead compared to other alternatives such as HEMTs as a preferred choice for HF applications. Hence, a need is raised to verify the accuracy of the previously mentioned noise models for mainstream MOSFET devices.

It is also of interest to check these noise models for novel MOSFET structures. A wide variety of MOSFET architectures are continuously evolving and are preparing to replace the mainstream structures. In this context, the graded-channel MOS (GCMOS) transistor [17] is studied in this brief.

II. Discussions

The devices used in this brief are all fabricated on a partially depleted SOI 0.25-μm technology. The results shown are for an n-type conventional MOSFET and GCMOS of 0.5-μm channel lengths. Both devices feature gates with 12 fingers of 13.2-μm width each. In the GCMOS, the ratio of the lightly doped channel length to the total channel length (L_{LD}/L) is approximately 0.5 [18].

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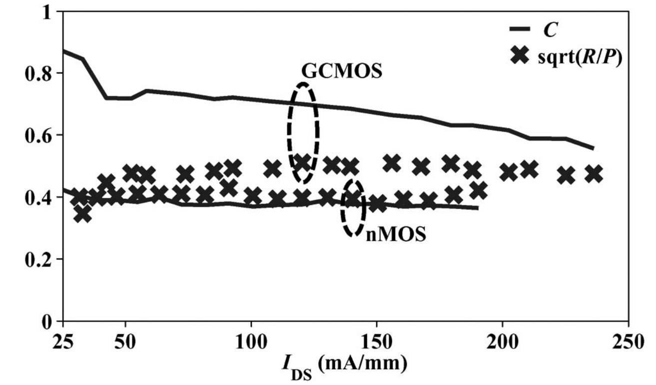

Fig. 1. Correlation coefficient C and $\sqrt{(R/P)}$ extracted at 6 GHz as a function of normalized drain current $I_{\rm DS}$ (with respect to the total transistor width) for conventional nMOS and GCMOS transistors.

All results are based on radio-frequency noise measurements achieved using a mechanical tuner system at a frequency equal to 6 GHz while the devices are biased in the saturation regime of operation ($V_{\rm DS} = 1.2$ V and $V_{\rm GS}$ varies from 0.5 to 1.5 V). The measured four noise parameters ($NF_{\rm min}$, R_n, and $Y_{\rm opt} = G_{\rm opt} + jB_{\rm opt}$) are used to extract the PRC model.$NF_{\rm min}$ is the minimum noise figure, R_n is the noise resistance, and $Y_{\rm opt}$ is the optimum noise admittance. A standard open deembedding is applied to the measured S-parameters, whereas the intrinsic noise parameters (and, thus, P, R, and C) are obtained through the well-known procedure explained in [19]. These measurements and extractions are presented in detail in [20].

In this brief, the current–current representation is employed since it is widely considered in the literature [5]–[7], [21]–[23].

A. Mainstream CMOS Technology

In the mainstream CMOS technology, the channel is uniformly doped in the lateral direction, i.e., from the source to the drain. In the following, this case is referred to as a conventional MOSFET (or nMOS).

In order to verify (1) in the case of conventional MOSFETs, the values of the correlation coefficient C and $\sqrt{R/P}$ as a function of normalized dc drain current ($I_{\rm DS}$) are shown in Fig. 1. The value of the correlation coefficient C for nMOS is approximately 0.4, which is in complete agreement with the value predicted by van der Ziel [2]. It is also obvious that $\sqrt{R/P}$ is almost equal to C over the whole range of operation of the conventional MOSFET, i.e., from weak to strong inversion. It is worth noticing that the same results is obtained when using PRC values of bulk MOSFETs calculated using technology computer-aided design (TCAD) simulations [24].

In order to further check the validity of (1), it is of interest to show the intrinsic noise parameters (after removing the effect of extrinsic resistance R_g and R_s). The expressions of $NF_{\rm min}$, R_n, and $Y_{\rm opt}$ given in [24] are employed to verify their dependence on C. Contrary to $NF_{\rm min}$ and $Y_{\rm opt}$, it is clear that R_n does not depend on C. On the other hand, instead of reporting $Y_{\rm opt}$, it is preferred, from the circuit design point of view, to present $\Gamma_{\rm opt}$—the optimum input reflection coefficient—in a Smith chart representation.

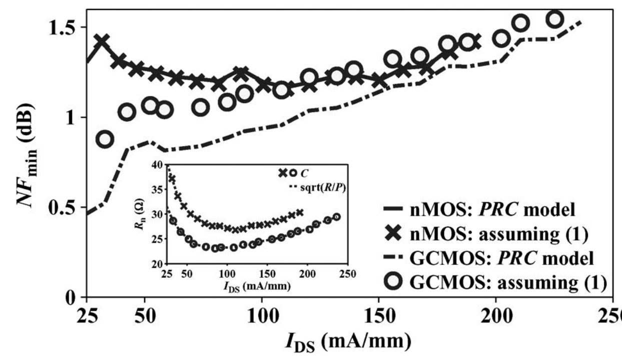

Fig. 2. Intrinsic minimum noise figure $NF_{\rm min}$ at 6 GHz as a function of $I_{\rm DS}$ for conventional nMOS and GCMOS transistors. In the inset, the noise resistance R_n is shown for both devices as a function of $I_{\rm DS}$.

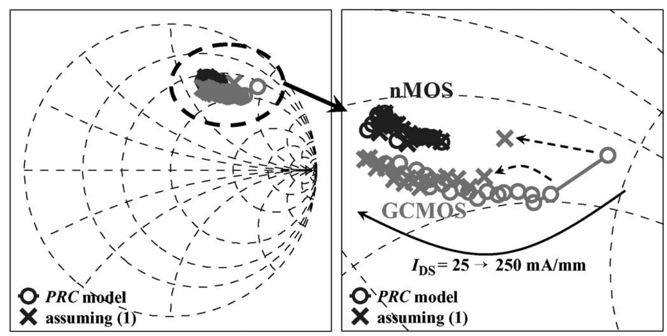

Fig. 3. Optimum input reflection coefficient $\Gamma_{\rm opt}$ (in a Smith chart) at 6 GHz as a function of $I_{\rm DS}$ for conventional nMOS and GCMOS transistors. Dashed arrows show the shift in $\Gamma_{\rm opt}$ in the case of a GCMOS.

Figs. 2 and 3 report $NF_{\rm min}$ (R_n in the inset) and $\Gamma_{\rm opt}$, respectively, as a function of the normalized drain current $I_{\rm DS}$, obtained from

– Pucel's PRC noise model (which gives a good agreement with experimental data [20]);
– Equation (1) to define C.

A perfect match is noticed between the values of $NF_{\rm min}$ and $\Gamma_{\rm opt}$ obtained from Pucel's PRC noise model and the values calculated when using (1) as an assumption.

These results clearly show that "two" noise parameters are sufficient to fully model/extract the four noise parameters ($NF_{\rm min}$, R_n, and $Y_{\rm opt}$) featured by a conventional MOSFET, independent of the chosen noise model (i.e., the extraction of P and R using Pucel's noise model or the extraction of T_g and T_d using Pospieszalski's noise model). It justifies as well why a simple noise figure measurement (as a function of frequency), when setting a 50-Ω source impedance at the input of the device under test, is sufficient to extract the four noise parameters [12]–[14], [21], [22].

B. GCMOS

In a GCMOS, the channel is highly doped near the source and lightly doped near the drain, with a gradual or abrupt step at the middle of the channel. From a noise perspective, this asymmetric doping profile leads to a higher C due to a localized distribution of the drain noise current near the source [23] (unlike a conventional MOSFET for which the distribution of the drain noise current is uniform [7], [23]). A higher C translates into a better HF global noise performance compared to a conventional MOSFET, as reported using HF noise measurements [20] and TCAD simulations [24]. Such a unique noise behavior is confirmed in Fig. 1 in which C and $\sqrt{R/P}$ are presented. Unlike conventional MOSFETs, C is not *equal* but higher than $\sqrt{R/P}$ over the whole range of operation (again, the same result is obtained using PRC values of bulk MOSFETs calculated from TCAD simulations [24]).

It is also of interest to evaluate the potential impact of employing the assumption of (1) in the case of a GCMOS. In the case of $NF_{\min}$, it turns out that an error as high as 0.2 dB (at $I_{\mathrm{DS}} = 50$ mA/mm and frequency $= 6$ GHz) is observed when comparing the values extracted using Pucel's PRC noise model and the values calculated assuming (1). Moreover, the values of Γ_{opt} extracted using Pucel's PRC noise model are quite different from those calculated assuming (1). This means that if (1) is used for a GCMOS, an important noise mismatch would occur when designing an LNA, leading to an important degradation of the LNA noise figure. From this study, it turns out that the use of Pucel's three-parameter noise model (PRC) is required when studying the HF noise performance of a GCMOS. This result is not limited to novel devices like a GCMOS, but also for state-of-the-art technologies, whenever a perfect uniformly doped channel is difficult to achieve.

III. Conclusion

In this brief, the concept of a "two-parameter noise model" has clearly been validated for a conventional MOSFET (mainstream CMOS), a device widely used in the HF domain, provided that the channel uniformity is ensured. Nevertheless, in the case of an asymmetric channel MOSFET (such as a GCMOS), whose noise physics is very different from the conventional MOSFET, it has been shown that a three-parameter noise model is more appropriate.

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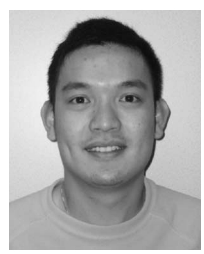

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