Compact Modeling of High Frequency Correlated Noise in HBTs

P.Sakalas[1,2], J.Herricht[1], A.Chakravorty[1], M.Schroter[1,3]

[1]CEDIC, Dresden University of Technology, Mommsenstrasse 13, 01062 Dresden, Germany, [2]Semiconductor Physics Institute, Vilnius, Lithuania, sakalas@iee.et.tu-dresden.de, [3]ECE Dept., University of California, San Diego, USA.

Abstract **---A compact model solution, consistent with the system theory for correlated base and collector shot noise sources, is derived and implemented in the bipolar transistor model HICUM using Verilog-A. Compiled (with Tiburon) Verilog-A model is simulated using ADS 2004A and the results are tested against measured noise parameters for high-frequency (f_T at 150 GHz) SiGe HBTs. Very good agreement between simulated and measured data is obtained.**

Index Terms --- **Noise, SiGe Heterojunction bipolar transistors, HICUM, correlation, shot noise, noise modeling, Verilog-A.**

I. Introduction

For bipolar transistor, noise behaviour at high frequency substantially differs from that at the low-frequency region due to the effect of correlation between the base and collector (i.e., the input and output) current shot noise sources [1][2][3][4][5][6][7][8][9]. The correlation between the base and collector shot noise sources in HBTs is well described analytically in [2]. For modern HBTs (e.g., SiGe-HBTs), the noise correlation becomes important at frequencies beyond ~1/10 of peak f_T [8]. Unfortunately, implementation of correlated noise in a compact model is not straight-forward, and from a system theoretical approach a consistent implementation has neither been investigated yet, nor been done for bipolar transistors. Conventional noise computation, implemented in all simulators, can only handle uncorrelated noise sources. Even through the adjoined network concept [10], noise calculation does not handle correlation terms. From the point of view of SPICE implementation, a possible Verilog-A solution of correlated noise for MOS transistors has recently been given in [11]. However, a complete and systematic analysis of the bipolar transistor noise from the perspective of SPICE-like implementation is still missing. In this paper, we deal with a complete theoretical analysis of noise behaviour in bipolar transistors. Our solution handles the correlation terms in such a manner that the existing SPICE-like simulators can additionally compute the correlated noise in a similar way they do for the uncorrelated noise sources. The problem was addressed almost two decades ago through the noise calculation of complex active filter circuits [12] and the corresponding solution provides a useful background for our investigation.

II. Theory and Verilog-A implementation

Transfer of the noise signal in the linear network in frequency domain is described as follows[13]:

$$\mathbf{S}_{YY}(j\omega) = \mathbf{G}(j\omega)\cdot\mathbf{S}_{XX}(j\omega)\cdot\mathbf{G}^{+}(j\omega) \quad (1)$$

where $\mathbf{G}(j\omega)$ is transfer function matrix of any noise source to a free of choice output in the circuit and $\mathbf{G}^{+}(j\omega)$ is the adjoint matrix of the transfer function. The $\mathbf{S}_{XX}(j\omega)$ is the power spectral density (PSD) matrix of noise sources and is defined as:

$$\mathbf{S}_{XX}(j\omega) = \begin{pmatrix} S_{i_{nb}} & \underline{S}_{i_{nb}i_{nc}} \\ \underline{S}_{i_{nc}i_{nb}} & S_{i_{nc}} \end{pmatrix} \quad (2)$$

Off-diagonal elements of the matrix correspond to the cross-PSDs, which are not taken into account by the conventioanl SPICE-like circuit simulators while simulating noise behaviour. Consequently, the correlation between noise sources is omitted in the noise computation. For the bipolar transistors, correlation between base and collector shot noise plays a significant role at high frequencies and, therefore, should be accounted for.

In order to force circuit simulators to compute correlation terms additionally, transformation of the input matrix into a diagonal matrix is performed. Here, the input matrix is expressed through a diagonal $\mathbf{D}_X(j\omega)$ and a transformation matrix $\mathbf{T}(j\omega)$:

$$\mathbf{D}_X(j\omega) = \begin{bmatrix} \mathbf{D}_1 & 0 \\ 0 & \mathbf{D}_2 \end{bmatrix}, \quad \mathbf{T}(j\omega) = \begin{bmatrix} 1 & 0 \\ \underline{t}_{21} & 1 \end{bmatrix} \quad (3)$$

$$\mathbf{S}_{XX}(j\omega) = \mathbf{T}(j\omega)\cdot\mathbf{D}_X(j\omega)\cdot\mathbf{T}^{+}(j\omega) \quad (4)$$

where $\mathbf{T}^{+}(j\omega)$ is the corresponding adjoint matrix. Now the modified input matrix becomes:

$$\mathbf{S}_{XX}(j\omega) = \begin{bmatrix} \mathbf{D}_1 & \mathbf{D}_1\underline{t}_{21}^{*} \\ \mathbf{D}_1\underline{t}_{21} & \mathbf{D}_1|\underline{t}_{21}|^2 + \mathbf{D}_2 \end{bmatrix} \quad (5)$$

Comparing matrix elements of eq. (5) and eq. (2), one obtains: $\mathbf{D}_1 = S_{i_{nb}}$, $\mathbf{D}_2 = S_{i_{nc}} - S_{i_{nb}}|\underline{t}_{21}|^2$. The cross-PSD is:

$$\underline{S}_{i_{nc}i_{nb}} = S_{i_{nb}}\underline{t}_{21} \quad (6)$$

Expression for the control factor $\underline{t}_{21}$ can be found later and associated with a controlled source in the equivalent circuit (EC).

Interpretation of the above matrix manipulation into a noise EC model can provide a better understanding for further implementation. After transforming $\mathbf{S}_{XX}(j\omega)$ into a diagonal matrix, the practically correlated noise sources i_{nb} and i_{nc} (see Fig. 1a) take the form of three uncorrelated ones $\overline{i_{nb}}$, $\overline{i_{nc}}$ and $\underline{t}_{21}i$ (see Fig.1b). The transformation yields an additional noise source, which carry the correlated terms. This is understood as the inclusion of the additional controlled source during the transfomation through the control factor $\underline{t}_{21}$. The control factor of this source contains the correlation between the noise sources i_{nb} and i_{nc}. This additional controlled current source is tagged in parallel to the output noise source (see Fig.1b) keeping consistency with the system theory [13].

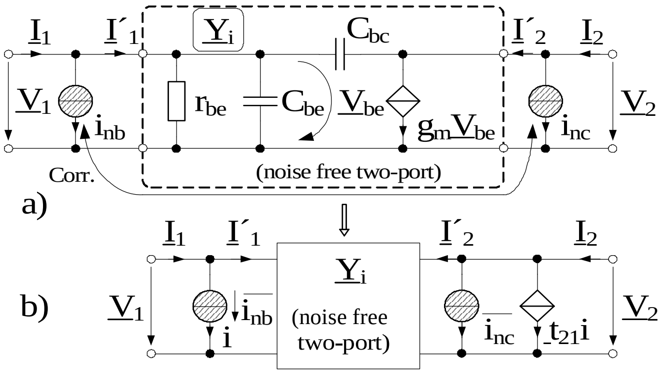

Fig. 1. a) Noise free two-port with small signal equivalent circuit (SSEC) of the internal BJT in the dashed box and correlated noise sources i_{nb} and i_{nc}, at the input and output respectively b) SSEC with three modified uncorrelated noise sources. Note that $i \equiv \overline{i_{nb}}$.

Now the input voltage noise source in Fig.2.b will be expressed as a function $v_{n\_ers} = f(\overline{i_{nb}}, \overline{i_{nc}}, \underline{t}_{21}i)$ of uncorrelated noise sources in Fig.2.a. This further analysis is carried out in connection with the noise computational methods adopted in conventional SPICE-like circuit simulators. Two-port Y-parameter representation for circuits in Fig.2a/b can be given by,

$$\underline{I}_1 = \underline{Y}_{11}\underline{V}_1 + \underline{Y}_{12}\underline{V}_2 + \overline{i_{nb}} \quad , \underline{V}_1 = v_{nRs} - R_S\underline{I}_1 \qquad \text{(Fig. 2a)} \quad (7)$$
$$\underline{I}_2 = \underline{Y}_{21}\underline{V}_1 + \underline{Y}_{22}\underline{V}_2 + \overline{i_{nc}} + \underline{t}_{21}i$$

$$\underline{I}_1 = \underline{Y}_{11}\underline{V}_1 + \underline{Y}_{12}\underline{V}_2 \ , \ \underline{V}_1 = v_{n\_ers} - R_S\underline{I}_1 \qquad \text{(Fig. 2b)} \quad (8)$$
$$\underline{I}_2 = \underline{Y}_{21}\underline{V}_1 + \underline{Y}_{22}\underline{V}_2$$

Setting $\underline{V}_2 = 0$ (output shorted) in both eq. (7) and eq. (8) and resolving expression for $\underline{I}_2$, one obtains,

$$v_{n\_ers} = \underbrace{1}_{G1} v_{nRs} + \left(\underbrace{\underline{t}_{21}\frac{1+R_S\underline{Y}_{11}}{\underline{Y}_{21}}}_{G3} + \underbrace{\left(-R_S\right)}_{G2}\right)\overline{i_{nb}} + \underbrace{\frac{1+R_S\underline{Y}_{11}}{\underline{Y}_{21}}}_{G3} \cdot \overline{i_{nc}} \qquad (9)$$

Expressing eq. (9) in terms of power spectral densities, i.e., in terms of eq. (1), one gets the final expression for PSD as,

$$S_{v_{n\_ers}} = |G_1|^2 S_{v_{nRs}} + |\underline{t}_{21}G_3 + G_2|^2 S_{\overline{i_{nb}}} + |G_3|^2 S_{\overline{i_{nc}}} \qquad (10)$$

The expressions for PSDs in eq. (10) are:

$$S_{v_{nRs}} = 4kTR_S, \ S_{\overline{i_{nb}}} = 2qI_B \qquad (11)$$

Note that $i \equiv \overline{i_{nb}}$ and R_S is the source resistance.

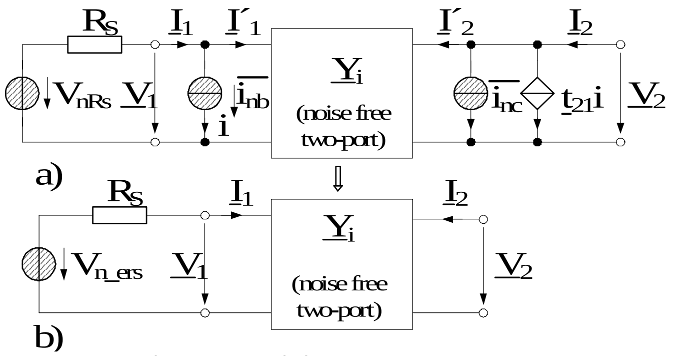

Fig. 2. a) modified SSEC (cf. framed part in Fig. 1 a)) with uncorrelated noise sources $\overline{i}_{nb}$, $\overline{i}_{nc}$ and $\underline{t}_{21}$i, b) SSEC with equivalent noise voltage source v_{n_ers} at the input (usually the input port source).

$$S_{\overline{i_{nc}}} = S_{i_{nc}} - |\underline{t}_{21}|^2 S_{i_{nb}} = S_{i_{nc}}\left(1 - B_f\left(\omega\frac{\tau_{Bf}}{3}\right)^2\right) \qquad (12)$$

with
$$S_{i_{nb}} = 2qI_B, \ S_{i_{nc}} = 2qI_C \qquad (13)$$

where B_f is dc gain and τ_{Bf} is base transit time. Control factor $\underline{t}_{21}$ for the eq. (10), following from eq. (6) is defined as,

$$\underline{t}_{21} = \frac{\underline{S}_{i_{nc}i_{nb}}}{S_{i_{nb}}} = -j\omega\frac{\tau_{Bf}}{3}\frac{I_C}{I_B} \text{ with } \underline{S}_{i_{nc}i_{nb}} \approx -2qI_C\left(j\omega\frac{\tau_{Bf}}{3}\right) \qquad (14)$$

where I_B and I_C are the direct base (intrinsic base emitter diode) and direct collector (forward transfer) currents, respectively. The drivation of the cross-PSD $\underline{S}_{i_{nc}i_{nb}}$ (eq. (14)) may be found in [1][2].

Now one may try to implement the above mentioned method of correlated noise computation through compact model and thereafter verify the implementation with a circuit simulator. Emergence of Verilog-A as a preferred language for writing compact models [14][15], enables the model developer to implement and test any new concept in a short period of time. For the noise simulation in Verilog-A, only a limited number of functions are supported, among which “white_noise ( )” and “flicker_noise ( )” are useful. The language reference manual (LRM)[15] has an example of correlated noise implementation with a real valued correlation coefficient. However, one can use the “ddt ( )” operator with a concept of capacitive coupling to implement any imaginary correlation [11]. Inside “white_noise ( )”, it is not obviously permitted to specify any argument that depends upon frequency, also the argument should not be negative in any case. As per our theoretical discussion, one requires to implement three controlled sources, one at the input and the other two at the output. The source at the input side is the same as the base current uncorrelated noise source. At the output side, one controlled source can be implemented by tagging a capacitor (with capacitance value of noise transit time) from the input noise source maintaining a proper sign of the control factor $\underline{t}_{21}$. However, the main problem, according to eq. (12), is to implement the remaining noise source in the output with the proper PSD, part of which depends upon the square of the frequency preceded by a negative sign!

According to [11], we understand that to obtain a "negative sign" inside the noise PSD is not possible from simple addition and subtraction of controlled sources and one can not multiply controlled sources in any SPICE-like implementation of noise. Therefore, it is not possible to straightforwardly realize the new PSD $S_{\overline{i_{nc}}}$ in Verilog-A, since it is clear that any noise PSD corresponds to a squared quantity cancelling any negative sign. However for this case, we can use an approximation as in eq. (15), which can imitate the theoretical prediction:

$$S_{\overline{i_{nc}}} \approx S_{i_{nc}}\left(1-\frac{B_f}{2}\left(\omega\frac{\tau_{Bf}}{3}\right)^2\right)^2 = S_{i_{nc}} - |t_{21}|^2 S_{i_{nb}} + \underbrace{\frac{|t_{21}|^4}{4B_f}S_{i_{nb}}}_{\text{error term}} \qquad (15)$$

It is found that an error (last term in eq. (15)) does not exceed a 10% limit up to one third of the peak transit frequency (for 150 GHz SiGe process HBTs). It is also worth to mention that this PSD is part of the total noise correlation, which is again part of the total noise of the transistor. In the calculation of the minimum noise figure (NF_{min}), ultimately the error remains very small up to the peak value of f_T. Putting eq. (15) into eq. (10), and re-arranging the terms, we obtain:

$$S_{v_{n\_ers}} \approx |G_1|^2 A + |G_2|^2 B + |G_3|^2 C + 2Re\left\{G_3 G_2^* t_{21}\right\} B + K \qquad (16)$$

$$A = S_{v_{nRs}}\ ,\quad B = S_{i_{nb}}\ ,\quad C = S_{i_{nc}}\ ,\quad K = |G_3|^2 \frac{|t_{21}|^4}{B_f} B$$

In eq. (12), factor 1/3 is relevant for pure diffusion transistors. In modern transistor models like HICUM, a bias dependent total transit time is formulated including the contributions from the emitter and the collector regions [16]. Therefore the factor 1/3 may be found a little smaller than the one actually required from device physics, if the total transit time is used in the implementation. To maintain consistency and generality for all other processes including Si-based ones, in our implementation we used the bias dependent total transit time and a parameter instead of the factor 1/3. The VCCSs, shown in Fig. 3, are dependent on the voltages V(b_n1) and V(b_n2):

$$I(bi, ei) = gV(b\_n1)\ ,\qquad V(b\_n1) = \frac{1}{g}\sqrt{2\cdot q\cdot i_{bei}}\ ,$$

$$I(ci, ei)_1 = \left(1-\frac{B_f}{2}(alit\cdot Tf\cdot\omega)^2\right)\cdot g\cdot V(b\_n2)\ , \qquad (17)$$

$$V(b\_n2) = \frac{1}{g}\sqrt{2\cdot q\cdot i_t}\ ,$$

$$I(ci, ei)_2 = -j\omega\cdot B_f\cdot alit\cdot Tf\cdot g\cdot V(b\_n1)$$

Fig. 3 shows a SPICE-like implementation of transistor noise (including correlation). where "g" corresponds to a uniform conductance of 1S, "*alit*" is a parameter dependent on the process technology (e.g. 1/3 for diffusion transistor), "*Tf*" is the bias dependent total transit time that takes into account the total delay for the carrier in emitte base, and collector regions, "q" is the elementary charge and "B_f" is equivalent to dc gain, "i_{bei}" is internal base and "i_t" is transfer currents, as defined in HICUM. Now we can get the PSDs as:

$$S_{I(bi,ei)} = 2qi_{bei} = S_{\overline{i_{nb}}} = S_{i_{nb}} \qquad (18)$$

$$S_{I(ci,ei)_1} = 2qi_t\cdot\left(1-\frac{B_f}{2}(alit\cdot Tf\cdot\omega)^2\right)^2 \approx S_{\overline{i_{nc}}}$$

$$S_{I(ci,ei)_2} = (2qi_{bei}(B_f\cdot alit\cdot Tf\cdot\omega)^2) = |t_{21}|^2 S_{\overline{i_{nb}}} = |t_{21}|^2 S_{i_{nb}}$$

,

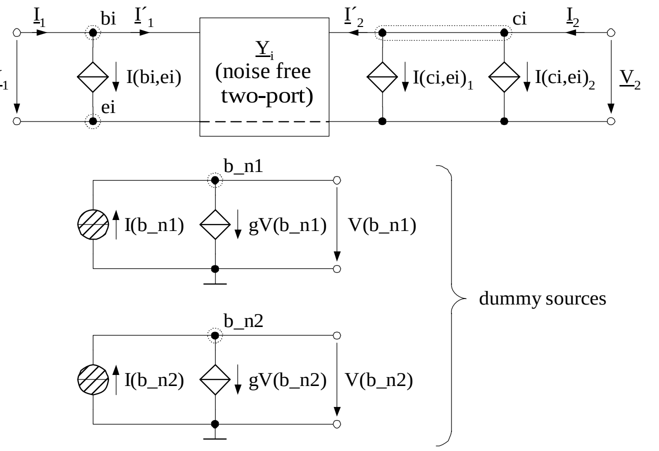

Fig. 3. Realization of correlation in compact models from a system theory perspective.

A Verilog-A implementation of corresponding correlated noise in bipolar transistors is given in Fig. 4. Note that for modular representation, p1 and p2 are used to indicate the input and the output node of the two-port network, that is to say, the branch b_p1 is equivalent to branch (bi,ei) and b_p2 to (ci,ei) of Fig. 3. The variable *betadc* is precalculated from the direct internal base current (*ibei*) and the transfer current (*it*) of the transistor. Two dummy noise current sources are created with spectral densities *2*Q*ibei* and *2*Q*it* at (n1,0) and (n2,0) branches. Connecting with 1Ω resistor, it is ensured that the noise currents are same as the noise voltages at the respective branches. In the input node, only the base current noise contribution is directly tagged. The output node is tagged with two separate noise contributions, one from the base current noise associated with frequency dependent control factor and other

```
inout   p1, p2;
branch (p1)      b_p1;
branch (p2)      b_p2;
branch (n1)      b_n1;
branch (n2)      b_n2
parameter real alit = 0.333 from [0:1];
I(b_n1) <+ white_noise(2*‘P_Q*ibei, “shot”);
I(b_n1) <+ V(b_n1);
I(b_n2) <+ white_noise(2*‘P_Q*it, “shot”);
I(b_n2) <+ V(b_n2);
I(b_p1) <+ V(b_n1);
I(b_p2) <+ V(b_n2);
k1 = alit*Tf;
I(b_p2) <+ 0.5*betadc*k1*k1*ddt(ddt(V(b_n2)));
I(b_p2) <+ betadc*ddt(-k1*V(b_n1));
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Fig. 4. Verilog-A implementation of HBT transistor correlated noise.

from the transfer current (or collector current) noise. Part of this second term is associated with a squared-frequency dependency preceded by a negative sign as shown in eq. (18).

III. Model verification

Noise parameters were measured for 0.18 µm SiGe-BiCMOS HBTs [17], with a peak transit frequency of f_T=150 GHz at V_{CE}=1.5V. Measured transistors have a CBEBC contact configuration with emitter window areas A_{E0}[µm^2]=0.2∗4.52, 0.2∗10.16. Measurements were performed in the 2-26 GHz frequency band. Noise parameters were de-embedded with the correlation matrix technique. Simulations were performed with ADS 2004A using compiled (with Tiburon) Verilog-A code. This piece (Fig.4) of Verilog-A code is introduced into the existing Verilog-A HICUM Level 2 model to test against the actual measured noise data. Using simulation results from both, the compiled Verilog-A HICUM as well as the simulator built-in HICUM level 2 model with the same set of model parameters, perfect agreement was obtained against the measured dc and high-frequency data. Since Verilog-A based model is very flexible, it can be easily modified and compiled over again, after any change. This opens a possibility to seek impact to noise parameters the effect of correlation between the base and the collector current shot noise sources by setting model parameter to desired value. For example at ("*alit*"=0) HICUM noise model does not account correlation effect. Measured and simulated results are presented in the Figures 5, 6. At microwave low frequency (2 GHz) no impact of correlation is observed, where both simulated curves (with and without correlation) coincide with

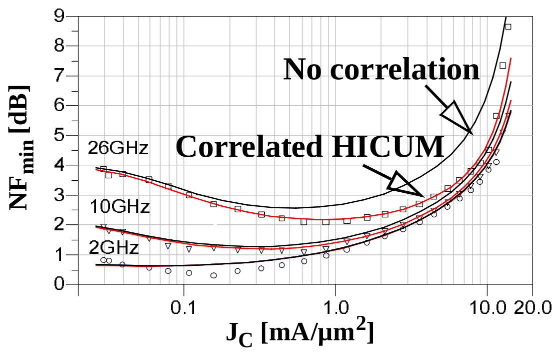

Fig. 5. NF_{min} vs. J_c for SiGe HBTs, symbols: meas., lines: sim.

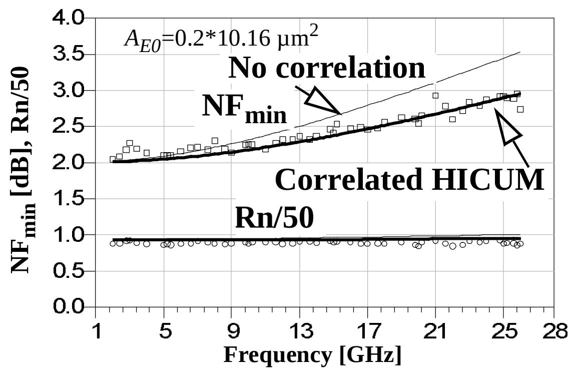

Fig. 6. NF_{min} and R_n/50 vs frequency at J_c=2.74mA/µm^2, V_{CE}=1.5 V, meas., lines: sim.

measured data. Beyond ~10 GHz, simulation results without the effect of correlation deviate from the measured data significantly, whereas those including the effect of correlation are found to be in a perfect agreement up to 26 GHz.

IV. Conclusions

Based on system theory, bipolar transistor noise is formulated. Developed equations include noise correlation terms in such a way that the approach can be implemented into a compact model to be used with any conventional SPICE-like circuit simulator. The concept is successfully realized in existing Verilog-A code for HICUM. Implementation is verified against measured high-frequency (f_T=150 GHz) SiGe-HBTs noise data. The corresponding results are found to be in perfect agreement.

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