Compact formulation for the bias dependent quasi-static mobile charge in Schottky-barrier CNTFETs

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***Abstract* - Carbon nanotube (CNT) field-effect transistors (FETs) are promising candidates for future high-frequency (HF) system-on-chip applications. Understanding and modeling mobile charge storage on CNTs is therefore essential for device optimization and circuit design. A physics-based compact analytical formulation is presented that enables an accurate approximation of the mobile charge in Schottky-barrier CNTFETs over the practically relevant bias range for HF circuit design. The formulation is C_∞ continuous and yields accurate results also for the capacitances. The new formulation has been verified for both ballistic and scattering dominated carrier transport by employing device simulation, which was calibrated to experimental data from multi-tube CNTFETs**

***Index Terms* - Carbon nanotube field-effect transistor, compact modeling, FET charge modeling.**

I. Introduction

High carrier velocity, thermal ruggedness, linearity adjustable by geometry, and excellent channel control, among others, make carbon nanotube (CNT) field-effect transistor (FET) technology a promising candidate for future high-speed/-frequency system-on-chip applications [1-4]. Recently, the development of CNTFETs built with single-walled tubes as channel material has made significant progress. On the digital application side, 3D integration of CNT based memory and logic gates for building a microprocessor has been demonstrated [5, 6]. On the analog high-frequency (HF) side, CNTFETs with 160 nm channel and 110 nm gate length were fabricated at wafer-scale that exhibit cut-off frequencies around 100 GHz [7]. This HF performance is now at the same level as that of RF CMOS with the same gate length (but shorter channel length!), despite an average density of just 50 CNTs/µm and an average current per CNT of only 5 µA. These results provide, for the first time, experimental proof for the great potential of CNTFET technology to achieve significantly better HF performance than RF CMOS for the same lithography node and also for co-integration with digital CMOS.

As a next step, the advantage of CNTFETs needs to be demonstrated also in integrated HF circuits. The design of such circuits requires, among others, compact transistor models that are available in circuit simulators. Although various CNTFET compact models have been published in the past, most of them have focused on just the description of the DC drain current for digital applications. The few proposed models, which also included a charge description, [8-12] either rely on idealized assumptions or too simple equivalent circuits [8-10] that make the proposed models far too inaccurate for HF circuit design, or require a numerical integration or an evaluation of a large number of summation terms or iterations [8, 10-12] which is not suitable for practical HF circuit design. The remaining practically suitable HF compact models [8, 13-15] include a sufficient equivalent circuit but with a description of the tube charge that is either a phenomenological or for classical MOSFETs or contain expressions with limited accuracy of derivatives for harmonic balance simulation. Finding a suitable compact analytical solution for the tube charge is challenging due to the Schottky-barrier (SB) that forms at the source and drain contact. This SB leads to tunneling as the major mechanism for carrier injection into the channel.

Presently, a compact continuous formulation describing the bias dependent mobile charge in SB-CNTFETs over the entire practical (I_D, V_{DS}) bias range sufficiently accurate for HF circuit design does not exist. There are several challenges for developing such a formulation. First, the carrier density integral does not have a closed-form analytical solution. Second, covering the complete bias range from subthreshold to high injection requires a smooth transition from Boltzmann to Fermi statistics. Third, for the charge on a single tube there are no measurements as a function of circuit relevant bias conditions[1], which can serve as reference. The last issue has been circumvented in this work by employing a CNTFET dedicated device simulator. Solving the first two issues is the main focus of this work.

This paper is organized as follows. The device simulation approach is briefly presented in Section II along with the definition of the simulated structure. The basic expression for the channel charge as a function of the tube ("surface") potential is derived in Section III, followed by a derivation of the tube potential as a function the internal terminal voltages of the CNTFET. These basic equations are then combined in Section IV into a compact formulation for the tube charge that is valid under all bias conditions. Comparisons between compact formulation and 3D device simulation for charge and capacitance as well as between complete compact model with the new charge formulation and experimental device data are shown in Section V.

II. Device Simulation

For the investigation pursued here, a single-tube within the 3D unit cell structure of a multi-tube CNTFET as shown in Fig. 1 was simulated with a channel l_{ch} of 100 nm and a length l_g of 80 nm for the buried gate electrode located symmetrically

1. There have been only (impedance bridge based) measurements for $V_{DS} = 0$ V [16, 17] - a bias condition that is of no relevance for circuit applications.

between source and drain contact. The buried gate structure has been chosen because of its best performance in terms of speed (i.e. lowest parastics [18]) and linearity [3]. The CNT with 1.3 nm diameter resides on a high-k gate oxide of 5 nm thickness (t_{ox}) and is surrounded by a low-k isolation oxide on top of the high-k gate oxide. Source, drain and gate contact are simulated as rectangular solid metal blocks with heights h_{con} larger than the CNT diameter. The unit cell width w_{uc} (equal to the tube spacing) was set 20 nm which is sufficient to avoid screening effects [19][2]. Without loss of generality, an n-FET was chosen since the mobility of electrons and holes is the same in CNTs. Also, the obtained characteristics enable a direct comparison to incumbent technologies, in which n-FETs prevail for RF applications.

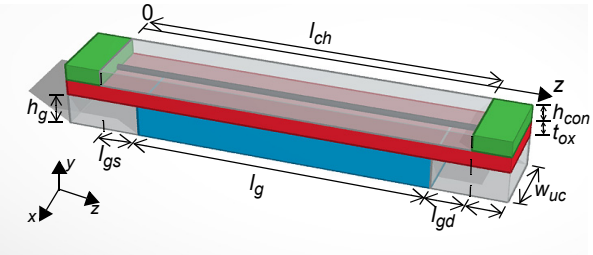

Fig. 1. 3D view of the simulated buried-gate CNTFET unit cell within a multi-tube channel HF structure. h_{con} = 6.3 nm, h_g = 15 nm, l_{gs} = l_{gd} = 10 nm.

For enabling device structure optimization and obtaining CNTFET terminal characteristics over a wide bias range relevant to circuit design, a computationally efficient simulation approach is required. Thus, augmented drift-diffusion transport (aDD) coupled with a 3D Poisson solver has been employed here. The CNT can be represented by a cylinder enabling the exploration of 3D electrostatic and transport effects or, as outlined in [19], also by a simple line charge if the tube potential is properly chosen. The latter approach was employed in this work. The physical parameters describing the aDD carrier transport were carefully calibrated to solutions of the Boltzmann transport equation, and Fermi statistics was included as well. The latter is essential for being able to properly model tube (i.e. channel) charge and current above threshold, especially in the bias region that is of interest for circuit design. The source and drain contact are described as a heterojunction between the metal covered CNT and its channel region [20, 21]. Tunneling and back scatttering at the corresponding heterojunction barriers are included in the aDD formulation via the recombination/generation term and the WKB approximation. More details on the simulator can be found in [22]. In this work, without loss of generality, a nFET is assumed and just the first subband is considered. The derived analytical expressions and reference results are valid for quasi-static operation.

The carrier density at the charge control point z_t in the middle of the gate is given by the pseudo-bulk approximation

$$n_t = n(z_t) = \int_{W_{Ct}}^{\infty} D_{tn}(W)\, f_n(W_{Fnt}, W)\, dW\,. \tag{1}$$

Here, W is the electron energy, D_{tn} the CNT density of states (DoS), f_n is the electron Fermi function with W_{Fn} as the electron quasi-Fermi energy, and $W_{Ct} = W_C(z_t)$ is the conduction band edge at the location z_t. These variables are visualized in Fig. 2.

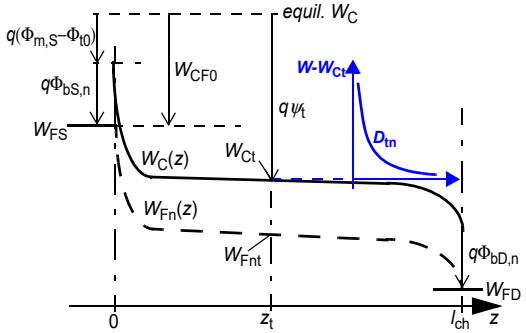

Fig. 2. Band diagram along the channel and definition of relevant variables; the tube surface potential ψ_t is defined against the equilibrium level of the conduction band. The inset at the conduction band edge $W_C(z)$ shows the DoS at the channel location z. W_{Fnt} is the electron quasi-Fermi-level at z_t in the middle under the gate.

In the device simulator, the Mintmire Approximation [23] for the DoS is used. However, this does not enable an efficient solution of the carrier density integral in (1). Thus, for the analytical treatment, the DoS resulting from assuming a parabolic band structure is assumed,

$$D_{tn}(W) = \frac{D_0}{\sqrt{W - W_{Ct}}} \quad \text{for } W > W_{Ct}, \tag{2}$$

with the prefactor D_0 as a material constant that can be calculated from the effective mass but will be absorbed later in a model parameter. With (2), the carrier density can be written as

$$n(z_t) = N_C\, F_{n,-1/2}(\eta)\,. \tag{3}$$

Here, $F_{-1/2}$ is the Fermi integral of order -1/2 with the argument

$$\eta = \frac{W_{Fnt} - W_{Ct}}{k_B T}, \tag{4}$$

and N_C is the *effective* density of states of the conduction band,

$$N_C = 2\frac{\sqrt{8\pi m_n^* k_B T}}{h} b_{NC} \tag{5}$$

with the tube temperature T and the effective electron mass m_n^*. The factor b_{NC} accounts for the difference in the DoS between the parabolic band approximation (b_{NC} = 1) and the Mintmire DoS employed in the simulator (b_{NC} > 1). Note that N_C will be absorbed in a model parameter.

2. Note that a spacing of 20 nm corresponds to a tube density of 50/µm which matches values obtained in fabrication.

III. CNT Charge

The electron channel charge in a selected subband is given by

$$Q_n = -q\int_0^{l_{ch}} n(z)dz = \int_0^{l_{ch}} Q'_n(z)dz \tag{6}$$

with the electron channel charge density $Q'_n(z) = -qn(z)$. Since it is not possible to find an analytical expression for the *spatial* dependence of the carrier density, the considerations are reduced, for the time being, to the carrier density at the spatial location z_t. Comparing the corresponding charge density

$$Q'_{tn} = -qn(z_t) \tag{7}$$

with the total channel charge calculated from device simulation in Fig. 3 reveals that (7) captures the bias dependence quite well except for some scaling factor close to 1. There is also little difference in the behavior and deviation of (7) with the reference charge between a buried gate and a gate-all-around FET structure. In a compact model, the charge elements are controlled by the internal potentials which are related to the potentials at the device terminals via series resistances. Hence, in this and the next section, primed node designations are used to indicate internal voltages.

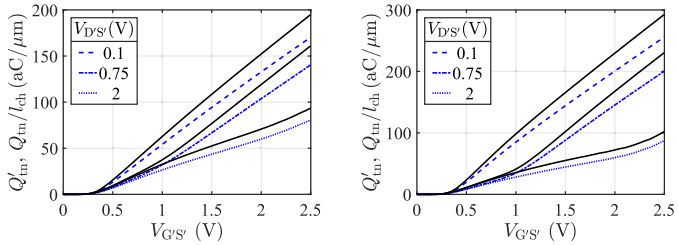

Fig. 3. Total tube charge Q_{tn} normalized to the channel length (broken lines) and tube charge density Q'_{tn} defined by (7) (solid lines) as function of $V_{G'S'}$ at $V_{D'S'}$/V = 0.1, 0.75, 2 for (a) a buried gate CNTFET and (b) a gate-all-around CNTFET.

The Fermi integral $F_{-1/2}(\eta)$ in (3) has closed-form analytical solutions only for the asymptotic cases of low carrier density ($\eta \to -\infty$) and high carrier density ($\eta \to +\infty$), respectively. However, a suitable analytical approximation of the Fermi integral over the entire bias range that smoothly links these two asymptotic solutions is

$$F_{-1/2,\,an}(\eta) \cong \frac{f_h \exp(\eta)}{f_h + c_h \exp(\eta)} \tag{8}$$

with the function

$$f_h = \sqrt{1 + \frac{2c_h^2}{\pi}(\eta + \sqrt{\eta^2 + c_\eta})} \tag{9}$$

and the parameters $c_h = 3.2$ and $c_\eta = 8$. Formulation (8) with (9) covers the entire bias range $\eta = [-\infty, \infty]$ as compared to the approximation proposed in, e.g., [24]. Investigations have shown that the maximum error of 4% in (8), (9) at the transition from Boltzmann to Fermi statistics has negligible impact on the accuracy of the compact charge formulation.

IV. Compact Model Formulation

Combining (3), (7) and (8) gives for the total electron charge on the tube

$$Q_{tn} = -Q_{tnC}\, F_{-1/2,\,an}(\eta), \tag{10}$$

where the prefactor

$$Q_{tnC} = qN_C l_Q \tag{11}$$

can be adjusted to measured data and l_Q is an effective length. The latter represents the spatially non-constant carrier density along the tube and can be used for geometry scaling purposes. Typically, l_Q is slightly smaller than the channel length.

Next, η in (4) is expressed by potentials. According to Fig. 2, the conductance band edge can be converted to a tube potential,

$$\frac{W_{Ct} - W_{F0}}{-q} = \psi_t - V_{CF0} \tag{12}$$

Here, V_{CF0} represents the energy difference between the equilibrium conduction band edge under the gate and the equilibrium Fermi level W_{F0}, i.e.

$$\begin{aligned} V_{CF0} &= W_{CF0}/(-q) \\ &= \Phi_{bS,n} - (\Phi_{m,S} - \Phi_{t0}) \\ &= \Phi_{bD,n} - (\Phi_{m,D} - \Phi_{t0}) \end{aligned} \tag{13}$$

with Φ_{t0} and $\Phi_{m,(S/D)}$, respectively, as work function of the CNT and source/drain metal, respectively. Defining the electron quasi-Fermi potential (QFP) $\varphi_{nt} = (W_{Fnt}\text{-}W_{F0})/(\text{-}q)$ then allows to express (4) by potentials,

$$\eta = \frac{\psi_t - V_{CF0} - \varphi_{nt}}{V_T} \tag{14}$$

with $V_T = k_B T/q$ as thermal voltage.

The relation between ψ_t and the applied gate potential $V_{G'}$ can be determined from a voltage loop under the gate. Fig. 4 shows on the left the band diagram in axial (i.e. horizontal) direction for the CNT region and on the right the band diagram for a cut in radial (i.e. vertical) direction under the gate at z_t. In bulk FETs, the voltage loop perpendicular to the gate is referenced to the equilibrium electrostatic potential at the bulk contact. This approach cannot be applied to CNTFETs due to the lack of a bulk region. Instead, the applied potentials are defined against the equilibrium Fermi potential $W_{F0}/(\text{-}q) = 0$ as a reference. According to Fig. 4, the voltage loop then reads

$$\psi_t = k_{Gt} V_{G'S'} - \psi_{ox} - \Phi_{bG,n} + V_{gt}/2 \tag{15}$$

Here, $V_{G'S'}$ is the voltage between the internal gate and internal source electrode with $V_{S'} = W_{F0}/(\text{-}q)$ as reference. Furthermore, ψ_{ox} is the voltage drop across the gate oxide, $V_{gt} = W_{gt}/q$ is the CNT bandgap voltage, and $q\Phi_{bG,n}$ is the difference between the gate metal work function $q\Phi_{mG}$ and the CNT affinity $q\chi_t$. The additionally introduced empirical parameter

k_{Gt} takes into account the non-ideal coupling between gate electrode and channel due to, e.g., fringing effects, which can lead to a non-ideal subthreshold slope.

The unknown ψ_{ox} can be determined considering the charge density balance along the radial CNT direction at z_t in Fig. 4,

$$Q'_{Gt} + Q'_{ox} + Q'_{tn}(\psi_t) = 0\,, \tag{16}$$

with the charges per length on the gate electrode (Q'_{Gt}), of the gate oxide (Q'_{ox}) lumped together at the oxide interface to the CNT, and in the channel ($Q'_{tn} < 0$). With $\psi_{ox} = Q'_{Gt}/C'_{ox}$ and C'_{ox} as electrostatic gate oxide capacitance per length, the voltage loop (15) can be written as

$$\psi_t = k_{Gt} V_{G'S'} - V_{tmc} + \frac{Q'_{tn}(\psi_t)}{C'_{ox}}\,, \tag{17}$$

where the material constants have been lumped together in the auxiliary voltage

$$V_{tmc} = \Phi_{bG,n} - \frac{V_{gt}}{2} - \frac{Q'_{ox}}{C'_{ox}}\,. \tag{18}$$

Eq. (17) establishes a nonlinear relation between tube potential and charge according to (10) and (14). Its solution can be found iteratively and requires a suitable expression for φ_{nt}.

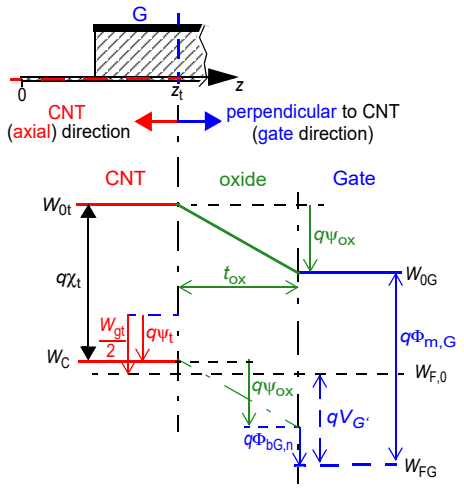

Fig. 4. Band diagram in a CNTFET along the axial direction (left red arrow) and, with applied gate bias, along the radial direction perpendicular to the gate (right blue arrow).

The electron quasi-Fermi level φ_{nt} can be determined according to the following considerations. Within the source barrier region, the electron density results from carriers emitted over and tunneling through the barrier. In the aDD framework, tunneling is modeled via carrier generation, which causes the electron density in the barrier region to increase from very small values at $z = 0$ towards the density level close to n_t at the end of the barrier. Hence, the resulting diffusion gradient in $-z$ direction must be overcome by a large enough electric field to drive the electron flux towards the drain. This causes W_{Fn} to drop within the source barrier region from the source level W_{FS} to the level under the gate as shown in Fig. 5. For ballistic transport W_{Fn} remains spatially constant under the gate (Fig. 5(a)), while for scattering transport the associated voltage drop causes a gradient there (Fig. 5(b)). Towards the drain, W_{Fn} approaches the drain contact Fermi level W_{FD}.

More details on the bias dependence of the energy levels at z_t is provided in Fig. 6. At low $V_{G'S'}$, i.e. in the subthreshold region, the charge is negligible and, according to (17), W_{Ct} drops from its equilibrium value directly proportional with $V_{G'S'}$ while W_{Fnt} remains bias independent at W_{FS}. Beyond subthreshold, W_{Fnt} starts also to drop with a slightly smaller slope than W_{Ct} until it coincides with $-qV_{D'S'}$ at approximately $V_{D'S'} + V_{CF0}$, from whereon its $V_{G'S'}$ dependence remains negligible. This point, at which W_{Ct} also changes to a branch with much lower slope, marks the transition from Boltzmann to Fermi statistics and a much more rapid increase of the carrier density and tube charge as compared to the high-voltage branch (e.g., $V_{D'S'} = 2$ V) in Fig. 3.

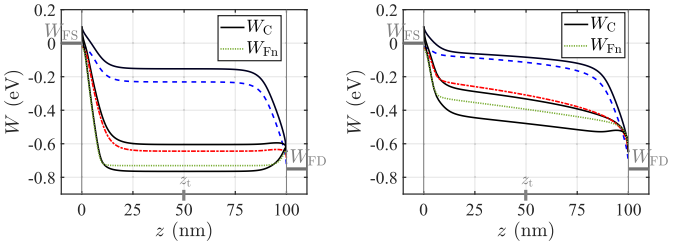

Fig. 5. Conduction band edge (solid lines) and electron quasi-Fermi level (broken lines) along the CNT channel of a buried gate CNTFET for $V_{D'S'} = 0.75$ V, $V_{G'S'}/V = 0.5$, 1, 1.5: (a) ballistic transport and (b) scattering transport.

The exact $V_{G'S'}$ dependence of W_{Ct} is determined by (17) in conjunction with (10). The transition from Boltzmann to Fermi statsistics marks the $V_{G'S'}$ range, from which on W_{Ct} drops below $W_{FD} + q\Phi_{bD,n}$ and the injection of carriers (electrons here) from the drain starts. In addition to the carrier injection from the drain, back scattering at the heterojunction barriers further increases the carrier density and tube charge, resulting in weaker gate control of the channel and thus lower slope of W_{Ct} with $V_{G'S'}$. In Fig. 6 two differences between ballistic and scattering transport are noticeable, which are both caused by carrier scattering and the resulting larger channel charge density. First, in Fig. 6(b) the transition to Fermi statistics is shifted towards lower $V_{G'S'}$ as compared to the ballistic case in Fig. 6(a). Second, the drop of W_{Fnt} towards W_{FD} with $V_{G'S'}$ extends over a wider bias range for scattering transport, which is a consequence of the gradient of W_{Fn} due to scattering, causing W_{Fnt} to be visibly above W_{FD}.

Based on the above discussion, a smooth and flexible description of W_{Fnt} or, equivalently, φ_{nt} is obtained with

$$\frac{W_{Fnt}}{-q} = \varphi_{nt} = s_{Fn}\left[V_{Fnt}\ln\left(1+\exp\left(\frac{V_{nt}}{V_{Fnt}}\right)\right)\right. \tag{19}$$
$$\left. - V_{FnB}\ln\left(1+\exp\left(\frac{V_{nt}-\beta_{Fn}V_{D'S'}}{V_{FnB}}\right)\right)\right]$$

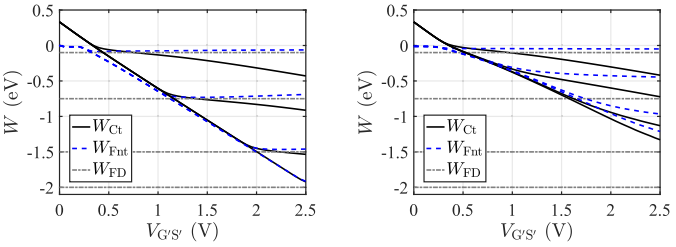

Fig. 6. Conduction band edge W_{Ct} (solid lines) and electron quasi-Fermi level W_{Fnt} (dashed lines), both at z_t, versus $V_{G'S'}$ of a buried gate CNTFET for $V_{D'S'}$/V = 0.1, 0.75, 1.5, 2 (also indicated by W_{FD}): device simulation results for (a) ballistic transport and (b) scattering transport.

with the argument $V_{nt} = V_{G'S'} - V_{Fnth}$. The voltage V_{Fnth} marks the first drop of W_{Fnt} when W_{Ct} reaches $W_{FS} + q\Phi_{bS,n}$ and tunneling starts at the source. The parameter s_{Fn} allows to adjust the slope, i.e. the proportionality with $V_{G'S'}$. The voltage parameters V_{Fnt} and V_{FnB} just determine the smoothness of the transitions and are in the order of a few V_T. The parameter β_{Fn} allows to model the deviation of W_{Fnt} from W_{FD} after the transition from Boltzmann to Fermi statistics. This deviation is very small for ballistic transport but clearly visible for scattering transport.

The nonlinear relation (17) between Q_{tn} ($= \boldsymbol{Q}'_{tn}\boldsymbol{l_Q}$) and ψ_t for a given bias point ($V_{G'S'}$, $V_{D'S'}$) can be written in the form

$$\boldsymbol{f}_{Q_{tn}} = \boldsymbol{Q}_{tn}(\psi_t, \varphi_{nt}) + \boldsymbol{C}_{ox}[\boldsymbol{k}_{Gt}\boldsymbol{V}_{G'S'} - \boldsymbol{V}_{tmc} - \psi_t] = 0 \qquad (20)$$

with Q_{tn} from (10), φ_{nt} from (19), and C_{ox} ($= \boldsymbol{C}_{ox}\boldsymbol{l_Q}$), V_{tmc} as model parameters. In the compact model, above relation is solved iteratively applying a Newton-Raphson algorithm with a fixed damping factor of 0.7. Assuming as initial value $\psi_t = V_{G'S'}$, convergence is achieved within maximal 10 iterations for a relative error below 10^{-6}. Since the equations involved in solving (20) are quite simple, the number of arithmetic operations is fairly small. The new model formulation has been implemented in Verilog-A in the framework of CCAM [15].

V. Results

The new model formulation has been compared to the results from device simulation. In both cases also the bias dependent channel capacitance,

$$\boldsymbol{C}_{gg} = \left.\frac{\boldsymbol{dQ}_{tn}}{\boldsymbol{dV}_{G'S'}}\right|_{V_{D'S'}}, \qquad (21)$$

will be compared, since it is of practical relevance and since the derivative is a good indicator for possible model inaccuracies. The capacitance was calculated numerically here for both device simulation and compact model. Since a change in tube charge Q_{tn} induces a gate charge change, the capacitance defined by (21) corresponds to the one seen (and measured) at the internal terminals of the CNTFET; i.e. (21) should not be confused with the quantum capacitance.

Table 1 summarizes the model parameters of the charge formulation for both the ballistic and the scattering transport case and for measured multi-tube HF CNTFET. Nonlinear optimization was used for determining the parameter values for a given set of $Q_{tn}(V_{G'S'},V_{D'S'})$ data from device simulation. The parameters V_{CF0}, V_{tmc}, C_{ox} were determined here directly from the device structure. In practice, all parameters will be determined from measured electrical data, which has been the case for the experimental device considered here. In particular, the total channel charge can only be measured indirectly through the capacitance C_{gg} and subsequent integration.

Table 1: Model parameters of the compact charge model and corresponding extracted values for both ballistic and scattering transport of the simulated buried-gate CNTFET as well as for the measured multi-tube HF CNTFET [25].

Param.	symbol	unit	description	ball.	scat.	Exp.
qtnc	Q_{tnC}	aC	tube charge prefactor	4.553	3.765	35.5
kgt	k_{Gt}	-	factor accounting for non-ideal coupling of gate and tube	0.965	1.0	0.551
vcf0	V_{CF0}	V	electrostatic potential in thermal equilibrium	0.33	0.33	0.24
vfnth	V_{Fnth}	V	voltage indicating electron QFP drop with $V_{G'S'}$	0.24	0.39	0.457
vtmc	V_{tmc}	V	Material dependent voltage defined by (18)	0	0	0.2
cox	C_{ox}	aF	gate oxide capacitance	9.83	9.83	56.84
sfn	s_{Fn}	-	slope parameter for electron QFP	0.816	0.617	0.391
vfnt	V_{Fnt}	V	smoothing voltage for electron QFP (first transition)	0.113	0.215	0.151
vfnb	V_{FnB}	V	smoothing voltage for electron QFP (2nd transition)	0.101	0.195	0.299
betafn	β_{Fn}	-	V_{DS} dependence. of electron QFP	1.17	1.04	0.486

A. Ballistic transport

Fig. 7 shows the comparison of the total tube (i.e. channel) charge and capacitance for a wide bias range that is of interest for high-frequency circuit design. Excellent agreement is obtained for both charge and capacitance, demonstrating that all relevant features have been preserved in the analytical model.

Notice that especially the nonlinear transition region between Boltzmann statistics (low capacitance) and Fermi statistics (high capacitance) is described very accurately (see Fig. 7(c)) for all $V_{D'S'}$ values. Also the shape of the curves, including the small overshoot, is properly captured in C_{gg} and, as expected, no discontinuities are visible. Further verification showed that the new formulation exhibits also a quite reasonable accuracy in the subthreshold region.

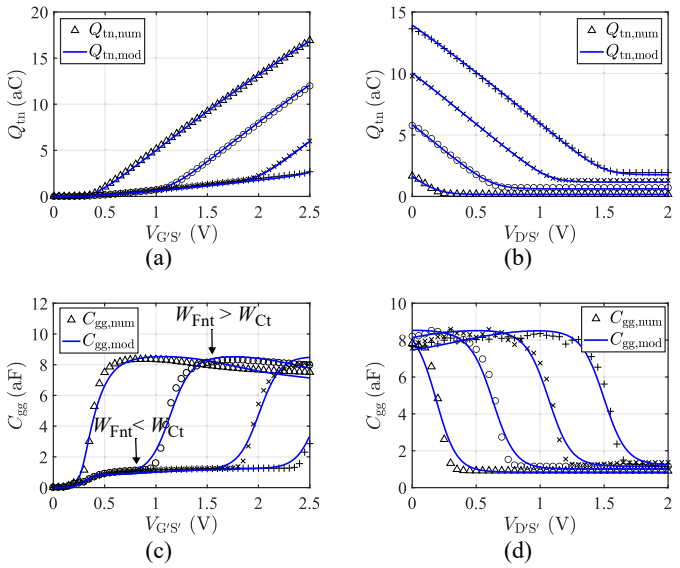

Fig. 7. Comparison between analytical calculation (solid lines) and device simulation (symbols) of a buried-gate CNTFET with ballistic transport for (a), (b) the channel charge and (c), (d) the associated capacitance. Parameter for (a), (c) $V_{D'S'}$/V = 0.1 (Δ), 0.75 (o), 1.5 (x), 2 (+) and for (b), (d) $V_{G'S'}$/V = 0.5 (Δ), 1 (o), 1.5 (x), 2 (+).

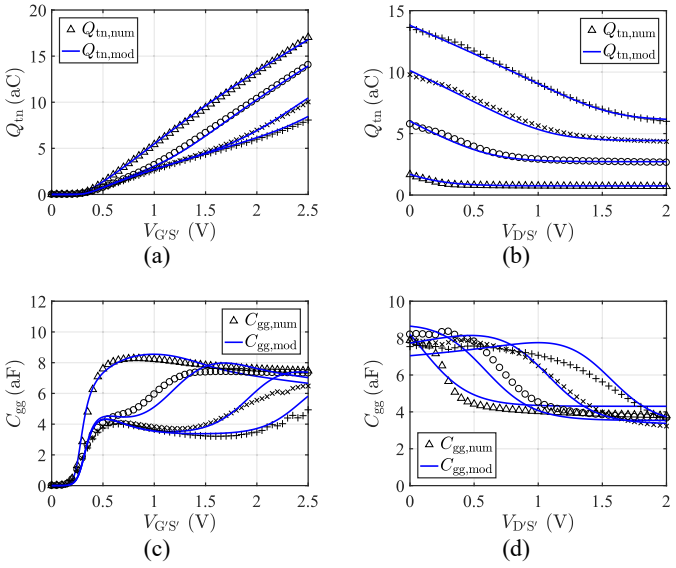

Fig. 8. Comparison between analytical calculation (solid lines) and device simulation (symbols) of a buried-gate CNTFET with scattering transport for (a), (b) the channel charge and (c), (d) the associated capacitance. Parameter for (a), (c) $V_{D'S'}$/V = 0.1 (Δ), 0.75 (o), 1.5 (x), 2 (+) and for (b), (d) $V_{G'S'}$/V = 0.5 (Δ), 1 (o), 1.5 (x), 2 (+).

B. Transport including carrier scattering

Channel charge and capacitance resulting from scattering transport are shown in Fig. 8 for the same bias range as before. Carrier scattering causes a significant increase in the source injected charge contribution, which is clearly indicated by the much larger slope of Q_{tn} and the corresponding larger capacitance for the high $V_{D'S'}$ branch (see Fig. 8(c)). The slope of the strong charge increase with $V_{G'S'}$ after the onset of carrier injection at the drain does not differ much from that of the ballistic transport as is evident from the similar peak C_{gg} values and the corresponding plateau. However, the transition from low to high capacitance value extends over a much wider $V_{G'S'}$ range, which has also been observed experimentally for multi-tube high-frequency CNTFETs [15].

C. Different gate topologies and contact types

The charge formulation developed in this work is not limited to any specific device structure or contact type. In Fig. 9, the formulation is compared to the simulation data of a top-gate single-tube CNTFET with otherwise the same structural dimensions as for the buried-gate CNTFET shown before. In addition, the barrier height at the source and drain contact is set to $\Phi_{bS,n}$ = -0.05 V. This corresponds to an ohmic contact and leads to sharp increase in the carrier injection around the threshold voltage. Excellent agreement is obtained for both charge and capacitance, including the small peak in the capacitance near the threshold voltage. This proves that the new formulation is general enough to account for different gate topologies and contact types.

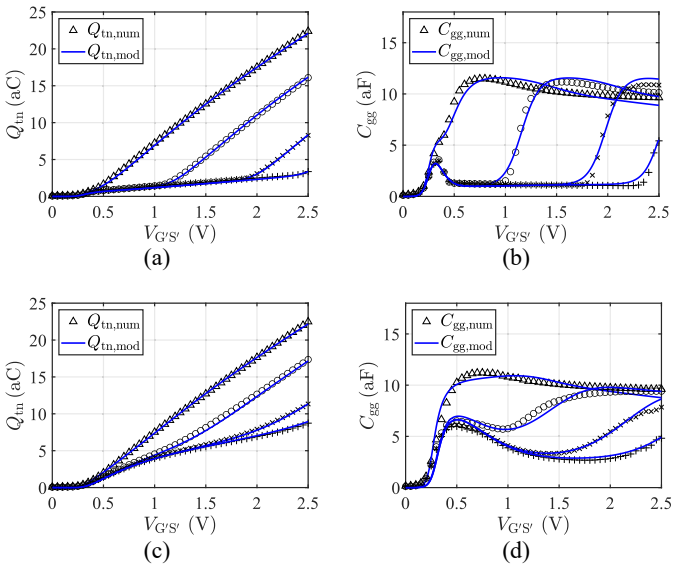

Fig. 9. Comparison between analytical calculation (solid lines) and device simulation (symbols) of a top-gate CNTFET with ohmic contact. (a), (b) Ballistic transport and (c), (d) scattering transport for the channel charge and the associated capacitance. $V_{D'S'}$/V = 0.1 (Δ), 0.75 (o), 1.5 (x), 2 (+).

D. Experimental model verification

Charges in transistors are typically determined from capacitances or time constants, which in turn are obtained from S-parameter measurement taken over a wide range of circuit relevant bias conditions. Performing S-parameter measurements on a single-tube CNTFET is impossible due to the far too large impedance mismatch to 50 Ω, the reference impedance of HF equipment. Hence, capacitance information has to be obtained

from measuring HF CNTFETs with a sufficiently large number of CNTs in parallel.

For the experimental verifcation of the developed charge formulation, the measured bias and frequency dependent S-parameters of the multi-tube HF CNTFET published in [25] were used. After removing the parasitic elements of the test layout (pad and connection capacitances, probe and pad series resistances), the resulting de-embedded Y-parameters only include the metallization layers of the transistor which are essential for its operation in a integrated circuit. The total gate capacitance is then obtained from

$$C_{GG} = \Im(\underline{Y}_{11})/2\pi f. \tag{22}$$

In addition, the transit frequncy f_T was determined from the common-source current gain $\underline{h}_{21}$ by extrapolating its quasi-static (i.e. single-pole) frequency dependence towards unity gain, yielding

$$f_T = |\underline{h}_{21}(f_m)|f_m, \tag{23}$$

with $\underline{h}_{21} = \underline{Y}_{21}/\underline{Y}_{11}$.

The new charge formulation was integrated into the compact carbon CNTFET model CCAM [15], replacing the old formulation. From the available DC and small-signal terminal measurements, the parameters of the complete compact model were extracted. In particular, the parasistic capacitances were determined from the measured "off" state Y-parameters. The resulting parameter values for the new charge model are listed in Table 1. The large tube charge prefactor and gate oxide capacitance are mostly due to the much larger gate width of the measured device. Compared to the simulation data, the fringing field related coupling factor k_{Gt} is less than 1 due to the larger gate metal overlap in the fabricated device.

Fig. 10 shows the comparison of the gate capacitance and the *extrinsic* transit frequency between measurements and model for a wide V_{GS} range[3]. Excellent agreement for both C_{GG} and f_T is observed, confirming the suitability of the new charge formulation also for fabricated devices. Note that a comparison of the complete compact model, including series resistances consisting of contact and metal layer components, with measurements is shown and thus device terminal voltages are now being used.

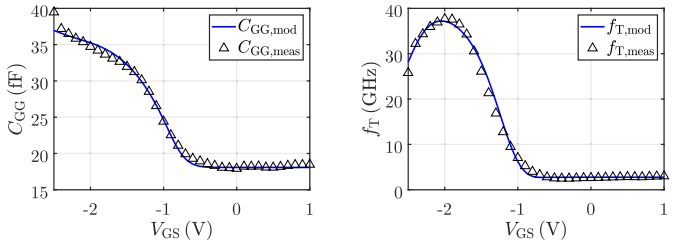

Fig. 10. Comparison of (a) total gate capacitance and (b) extrinsic transit frequency as a function of external GS voltage between the charge model integrated into the compact model [15] (line) and the measurement data (symbols) of a multi-tube HF CNTFET [25] for V_{DS} = -1.5 V.

3. The measurements (taken in 2019) contain only a single V_{DS} value that is suitable for the purpose of this work.

VI. Summary and Conclusions

A physics-based and continuous formulation of the total channel charge in CNTFETs has been presented that does not require the evaluation of tunneling transmission factors and bias case dependent partitioning of an integral solution with their higher-order discontinuities. The formulation includes the impact of the Schottky barriers via a bias dependent description of the quasi-Fermi potential under the gate. Compared to 3D device simulation results of a realistic single CNTFET unit cell structure excellent agreement for both the charge and the channel capacitance has been obtained for ballistic transport and for scattering transport along the tube over a wide bias region relevant to analog high-frequency circuit applications. Further, the model has been integrated into a complete CNTFET compact model. The parameters of the model can be obtained from electrical characteristics obtained at the internal transistor terminals. Additional subbands can be easily included in the model by applying the same formulations to each subband with a change in the electrostatic potential in thermal equilibrium, V_{CF0}, which would be larger for higher subbands and then summing up the charges obtained from each subband. It is planned to release the new compact model once its accuracy and convergence has been sufficiently tested during circuit design.

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