

Device modeling tools and their application to SiGe HBT development

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Abstract - The enabling role of device simulation (TCAD) and compact modeling for the structural optimization of SiGe HBTs during process development is discussed. It is shown that employing a Boltzmann and an augmented drift-diffusion solver in combination with a physics-based compact model and geometry scalable parameter extraction can successfully support process development. As application examples, two particular use scenarios are discussed along with practical examples, and corresponding results are presented.

Index Terms - compact modeling, device modeling, TCAD, geometry scaling, SiGe HBT

I. INTRODUCTION

Silicon-germanium (SiGe) heterojunction bipolar transistors (HBTs) have found widespread use in high-frequency (HF) applications, mostly in HF front-ends co-integrated with MOSFETs in a BiCMOS process technology. The latter combines on a single chip the capability of ultra-high-speed front-end circuits with the high integration density of CMOS for digital signal processing. Applications of SiGe HBTs range from cell phones [1] over automotive radar [2] and mm-wave data transfer [3, 4] to (sub-)mm-wave sensing and imaging [5, 6]. Most recent progress in SiGe HBT performance demonstrated a current gain transit frequency f_T beyond 500 GHz and a maximum oscillation frequency f_{max} of more than 700 GHz [7, 6, 8], and predictions yielded (f_T , f_{max}) up to (0.8, 1.9) THz [9, 10]¹, making this technology attractive for the rapidly emerging field of THz electronics with application areas in, e.g., transportation, health, security, and high-bandwidth communications (e.g. [11, 12]).

The performance predictions in [9, 10] were obtained with a hierarchy of simulation tools. Starting with semi-classical device simulation based on the solution of the Boltzmann transport equation (BTE) [13], the carrier transport properties in one-dimensional (1D) HBT structures² with reduced vertical dimensions and associated optimized doping and composition profiles were predicted. The BTE results were then used to calibrate the parameters of a drift-diffusion (DD) transport model, which - due to its significantly higher computationally efficiency - was employed for optimizing the lateral (i.e. two-dimensional (2D)) scaling of HBT structures [9]. Finally, the electrical characteristics from DD simulation were approximated by a physics-based compact transistor model that allows capturing the properties of realistic three-dimensional (3D)

structures (cf. Fig. 1(a)). This way, all relevant electrical and electro-thermal parasitic effects are included, enabling the simulation of the corresponding terminal characteristics and of complete circuits [9].

The measured performance achieved in [7] corresponds to technology node N3 in the roadmap [9], which was predicted a few years earlier for the ITRS 2014. In fact, the doping profile of N3 was a guide for eventually achieving the electrical targets of the EU DOTSEVEN project. A detailed analysis with a physics-based compact model, which allowed to determine the electrical characteristics of the 1D transistor by de-embedding all parasitic effects from the measured terminal characteristics, yielded very similar values for the internal base sheet resistance, area-specific depletion capacitances, collector current density and f_T as node N3 [14]. Recently, the approach sketched above was successfully applied in the DARPA T-MUSIC project for developing a new SiGe HBT process generation within production facilities. These results underline the capability and usefulness of today's device simulation tools. Proper application of the available tools enables fast device design optimization and thus helps to accelerate process development, which in turn leads to significant cost savings. Considering the increasingly complicated and costly fabrication process, device modeling, including technology computer-aided design (TCAD) and physics-based compact modeling, has become an important part of process development.

This work discusses the present status of various device modeling tools and, in particular, their use for different purposes. Hence, first an overview on the various tools and their limitations is given in Section II. Information on the extraction of detailed device related data from measurements is provided in Section III. The two major use scenarios for the application of device modeling and its tools are out-lined in Section IV and V, while Section VI briefly discusses device modeling at cryogenic temperatures.

II. DEVICE MODELING TOOLS AND THEIR ROLE

The importance of device modeling and associated tools for semiconductor technology development has increased over time. This section discusses first semi-classical TCAD tools and then compact modeling along with the pros and cons of each for various applications. The last section touches on additional simulation tools that have become increasingly important for successfully designing modern integrated circuits.

A. Numerical device simulation (TCAD)

The traditional goal of TCAD is the investigation of the im-

1) Obtained within the former International Roadmap of Semiconductors (ITRS), which now has become the International Roadmap for Devices and Systems (IRDS; <https://irds.ieee.org>).

2) All discussions refer to npn transistors.

part of process changes on electrical device performance in order to save fabrication cost. One of the goals in the nineties was the so-called virtual fab that aimed at the simulation of all fabrication processes and resulting device characteristics for developing process recipes before committing to the fabrication based on the optimal “virtual” recipe. This goal has never been achieved though, at least for HBTs, due the lack of predictability of process simulation: the physical effects of material compositions, increasing doping concentrations, introduction of new materials and associated lattice strain on electrical characteristics are apparently too difficult to predict sufficiently accurately. However, based on short-loop experiments and repeated calibration of transport parameters, doping and composition profiles can be tuned or extracted that can serve for device simulation. A comprehensive overview on various device simulation approaches can be found in [15].

The most important task of device simulation is the calculation of terminal currents and associated internal charges as a function of the voltages applied at the device contacts. Carrier transport simulation on a broader basis started out with the DD formulation. At the same time, various efforts existed to solve the much more rigorous BTE using the Monte Carlo method. However, such a statistical solution method makes resolving the minority carrier concentration difficult and is thus unsuitable for bipolar transistors. More recently, deterministic solution methods have been developed [13] and successfully been demonstrated for predicting device characteristics for new process generations [9, 10, 16].

With shrinking dimensions, moments of the BTE were developed, such as energy transport (ET) and energy balance equations, that resulted in a variety of formulations, typically known as ET and hydro-dynamic (HD) transport simulation [17-19]. For capturing quantum mechanical effects like carrier transport through very thin layers, the Schrödinger equation has to be solved. This has already become necessary for advanced SiGe HBTs operating at cryogenic temperatures in circuits for, e.g., quantum computing and space exploration. Generally, the calculation of carrier transport has to be accompanied with the solution of the Poisson equation for yielding a self-consistent electrostatic field distribution.

Over time, the purpose and use of device simulation has been extended beyond its traditional goal. Inverse modeling employs device simulation in combination with measurements for determining doping and composition profiles as well as material properties. Here, the physical parameters that define the material parameters in a simulator are adjusted based on electrical measurements until simulated and measured result (e.g. current, capacitance) agree.

Since device simulation offers fundamental insights into device operation, it is being heavily utilized today for both developing and verifying compact models as well as for optimizing device performance. As a side application of this, device simulation enables the development of special test structures and the evaluation of the accuracy of the obtained results from their measurements.

More recently, compact model parameters in preliminary

process design kits (PDKs) for new technology generations have been determined based on device simulation. For MOSFETs, even predicting the impact of process tolerances (“statistical” simulation) due to random doping atom distribution has been attempted [20].

Finally, in future the utilization of atomistic simulation tools is expected. This has already occurred for developing and understanding emerging devices based on, e.g., carbon-nanotubes or two-dimensional channel materials. Here, the non-equilibrium Green’s function (NEGF) approach [21] has been employed for calculating the impact of atomic layer changes on the transport properties.

B. Compact modeling

Compact models (CMs) are defined by a lumped equivalent circuit and a (preferably) closed-form analytical formulation for the current through each lumped element as a function of node potentials. In physics-based CMs, the parameters of the current-voltage formulation depend on properties of the physical device structure, such as dimensions, (average) doping concentrations, carrier mobility, bandgap etc.. Hence, each element in a physics-based CM represents a specific physical region in a device structure as shown in Fig. 1(b).

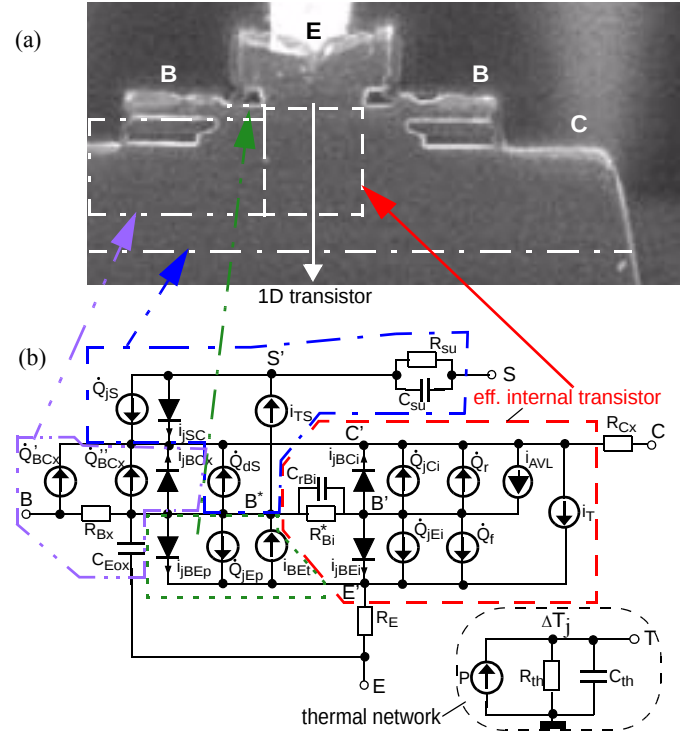


Fig. 1: (a) TEM cross-section of a SiGe HBT [22] and (b) large-signal equivalent circuit of a CM (HICUM/L2 [23]) with self-heating adjunct network. Not shown here are additional adjunct networks for vertical NQS effects and high-frequency noise correlation.

The traditional use of CMs is the representation of the electrical characteristics of fabricated devices during circuit design and optimization. Computational efficiency and associated simplifications have been driving the development of CMs. Hence, any CM is always a compromise between an

as accurate as possible description of physical effects and a minimal number of arithmetic operations. In addition, ease of parameter extraction is important for foundries and providing PDKs. In combination with device simulation and related tools (see section C. below), CMs today also predict device performance in preliminary PDKs. This topic will be expanded on in section IV.

Physics-based CMs have also been used for debugging process technology. The physical relation of each equivalent circuit element of a model to the device structure allows to draw conclusions from the extracted model parameters and element values regarding the properties of the corresponding device region. Going one step further, once the external regions of a device structure (and other parasitic effects) are described accurately by the CM, their impact on the electrical characteristics can be evaluated. Here, more recently, the role of compact modeling in process development has been extended further. By stripping off the model elements associated with the external transistor regions, the electrical characteristics of the intrinsic device structure can be obtained. In case of bipolar transistors, this corresponds to the vertical 1D line under the emitter as defined in Fig. 1(a). The resulting “1D measurement data” can then be used for comparison with and calibration of device simulation results as well as for verifying the 1D doping and composition profile [24–28]. This topic will be discussed in more detail in section V.

The accurate determination of equivalent circuit element values is of utmost importance for process debugging. Thus, a very important part of compact modeling is parameter extraction, which is a combination of data management and nonlinear optimization. Parameter extraction software must provide not only the capability of data importing, processing and visualization as well as interfaces to circuit and TCAD simulators but also CM-specific procedures for reliably obtaining parameters from processed data sets. Preferably, a process and model specific parameter extraction flow should be quickly repeatable for data from different dies and wafers of the same process. This topic is discussed in more detail in section III.

Finally, physics-based CMs have been used for many years for statistical modeling. Here, the fabrication tolerances are captured by those model parameters that have a “built-in” relation to structural and material parameters.

C. Other related simulation and modeling tools

Besides carrier transport in semiconductors, additional effects need to be often taken into account during device modeling and circuit design. Parasitic capacitances of complicated device structures can be calculated in a computationally efficient way with a stand-alone 3D-Poisson solver. The impact of self-heating due to phonon scattering has been investigated by solving the BTE for phonon transport [6]. While this gives detailed insight into the temperature distribution within the device, the large computational effort limits the results typically to the 1D structure. For a realistic 3D device structure, a more practical approach is to solve the heat equation, consisting of Fourier’s law and an energy balance equation includ-

ing time dependent heat generation and storage, in three dimensions. The results can be converted into an electrically equivalent multi-pole network consisting of thermal resistances and capacitances.

Signal coupling between a substrate contact somewhere on the chip surface and a single device or also coupling between different devices (so-called substrate coupling) becomes more pronounced with device scaling and higher frequencies. Its effects can be captured by a 3D solution of the majority carrier continuity equation with drift transport in combination with Poisson’s equation.

The design and optimization of HF circuits has to include the signal interaction between metal layers of the back-end-of-line (BEOL) and the substrate and also between different BEOL layers. While for these electro-magnetic problems generally the solution of Maxwell equations in three dimensions is required, for planar structures the computational effort can often be reduced by quasi-3D solvers.

For compact modeling, sufficiently accurate parametric analytical equations for representing the parasitic capacitances as well as the element values of the self-heating and intra-device substrate coupling networks are desirable. Based on conformal mapping techniques, closed-form analytical formulations for parasitic capacitances and substrate network elements can be obtained for various topologies [29]. The difficulties here though lie in (i) the sometimes too complicated topologies of fabricated devices, which require simplifications with reduced accuracy, (ii) the constantly necessary effort of adapting existing equations to new device architectures, and (iii) the fact that some solutions lead to elliptic integrals which can only be evaluated numerically. Thermal effects are typically represented by a single-pole adjunct network hooked up to an external node of the transistor model. Multi-pole networks increase the number of nodes and are thus considered by the circuit design community as too time consuming. The development of geometry dependent equations has focused mostly on the thermal resistance while much less is known about the geometry dependence of the thermal capacitance. Element values of a multi-pole thermal network even for multi-finger devices, i.e. including intra-device thermal coupling, can also be calculated numerically efficiently from a Green’s function solution. A sophisticated geometry preprocessor is needed for calculating the full set of HBT model parameters for a large variety of emitter dimensions and contact configurations (e.g. BEC, CBEB, CEBEB etc.) [30, 31].

As a final note, it should be mentioned that one has to be careful when defining the physical boundaries of a device that is supposed to be represented by a CM. Otherwise, important parasitic effects may be counted twice (via the parasitic extractor and EM simulation) or are ignored. Typically, only the first two metal layers of the BEOL are used for contacting the device to make it functional. Also, the elements of the substrate coupling network can only be included in a compact model parameter set if the location of the substrate contact relative to the device is known. Often circuit designers re-

move the substrate contacts of the transistor layout used by the modeling engineers for parameter extraction and place a common substrate contact somewhere on the chip surface. In that case, the intra-device substrate network in the PDK device needs to be disabled.

III. GEOMETRY-SCALABLE PARAMETER EXTRACTION

With a proper set of special DC test structures and transistors with different geometries in HF and DC pads it is possible to determine the bias, temperature, frequency and geometry dependent value of each element of a physics-based equivalent circuit accurately. Table 1 contains a list of test structures that are recommended for geometry scalable parameter extraction.

Table 1: List of test structures for geometry-scalable CM parameter extraction. (CE: common-emitter)

Structure	Layout / Purpose
contact chains	DC / sheet and contact resistances
tetrodes	DC, diff. E widths / intern. base sheet res.
HBT	DC, small & large / substrate transistor I-V
CE HBT	HF, diff. E widths / C-V, I-V, transit time
CB HBT	HF, diff. E widths / C-V, I-V, transit time
open, short	HF / deembedding
transm. lines	HF / on-wafer calibration (D band and up)
multi-E HBT	HF / scaling, TEM

Given the relatively large number of model parameters in modern CMs, the overall parameter extraction flow is typically broken up into a sequence of smaller steps, each of which targeting the determination of a small subset of parameters related to the measured characteristics of, e.g., an equivalent circuit element. One may distinguish two basic types of extraction steps. First, process- and model-specific parameters are determined from special test structures and under specific operating conditions [32-35]. In contrast to these direct methods, parameters describing operating regions in which several physical effects are superimposed and hence are difficult to separate, are often determined by numerical optimization, possibly involving circuit simulation. While numerical optimization is easy to implement in software, it is advisable to reduce the number of parameters extracted that way to a minimum, since the optimization of multiple variables is more prone to yielding unreliable (and ambiguous) results.

A widely used parameter extraction software in industry is Keysight's ICCAP, which also includes equipment drivers. However, ICCAP's interfaces focus heavily on the company's equipment and circuit simulation tools, and its set-up strongly favors visual curve fitting for a single device (geometry). A common issue of commercial software is the license cost and the lack of adaptability of its core infrastructure to, e.g., other external tools or specific extraction approaches and to a geometry-scalable physics-based parameter extraction. These problems have been addressed recently by new software for both data acquisition [36] and model parameter extraction [37]. The latter allows the user to systematically

process measurement data, automatically generate reports using PyLatex and manage circuit and TCAD simulations with different simulation tools in a highly efficient and extendable way. As a next step, existing in-house parameter extraction modules are planned to be transferred to the open-source part of DMT, including classes for parameter extraction and to enable extraction re-runs as batch job for new data of the same or a similar process. The parameter extraction implemented in DMT and roughly sketched in Fig. 2 proceeds in three major steps [26]:

- Process-specific parameters, such as the sheet resistances and the contact resistivities as well as capacitances and currents associated with the junction areas and perimeters, are determined first from special test structures (e.g., contact chains, tetrodes, transistors with different sizes) and by applying special measurement conditions. The results are used in the subsequent extraction steps for determining, e.g., the series resistances as well as split of internal and external capacitances and currents for a given HBT structure.
- Next, the parameters for the reference device are extracted. This step yields in particular all non-scalable parameters.
- Finally, parameters that are not directly related to physics or difficult to extract analytically, such as smoothing parameters, are set by fine-tuning and numerical optimization.

All compact model results shown in this overview have been based on the above parameter extraction procedure.

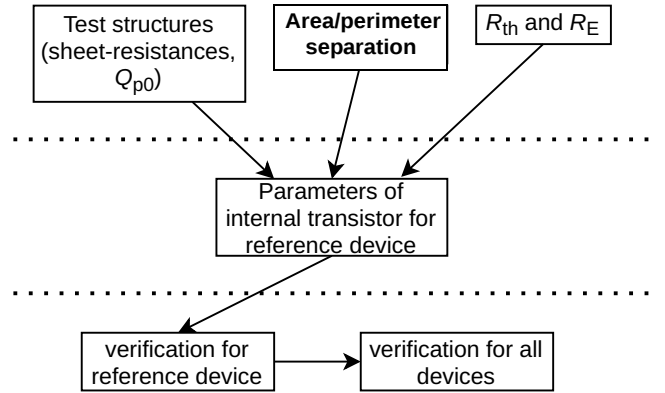


Fig. 2: Flow-chart for extracting the parameters of a physics-based compact model from measured (or simulated) data.

IV. FROM DEVICE SIMULATION TO PDK LIBRARY

At the beginning of the DOTFIVE project in 2008 it was already known that DD transport yielded too pessimistic results in terms of device speed (i.e. too low f_T) due to the inability to capture velocity overshoot in the BC depletion region. It was believed though that ET would give correct results and could be used as vehicle for both optimizing device design and model development [38]. However, it turned out that ET/HD transport yielded (partially far) too optimistic performance compared to BTE simulations using a deterministic solver [13], the results of which served as reference for calculating the electron transport current and densities in the intrinsic (1D)

transistor³.

Typical results for the transit frequency f_T are illustrated in Fig. 3 for different doping profiles that represent subsequent technology generations [9]. It can be observed that ET consistently predicts higher f_T than the BTE and that the deviation grows with vertical scaling. The main origin for these deviations has been attributed to the empirical parameters used in the carrier temperature gradient term, the Wiedemann-Franz law and the closure term in the energy flux [38]. These parameters depend in unknown way on the device structure and cause a significantly larger electron velocity at the BE junction and in the entire base compared to BTE results. On the other hand, f_T from DD transport is consistently too low with a deviation that also grows with vertical scaling. This is mainly due to the limited carrier saturation velocity, the bulk value of which is lower than the local value in the BC depletion region. Similar results have been obtained also for fabricated transistors and corresponding experimental data [39]. As a consequence, either of the two moment based transport models needs to be re-calibrated for any significant change in the doping and composition profile.

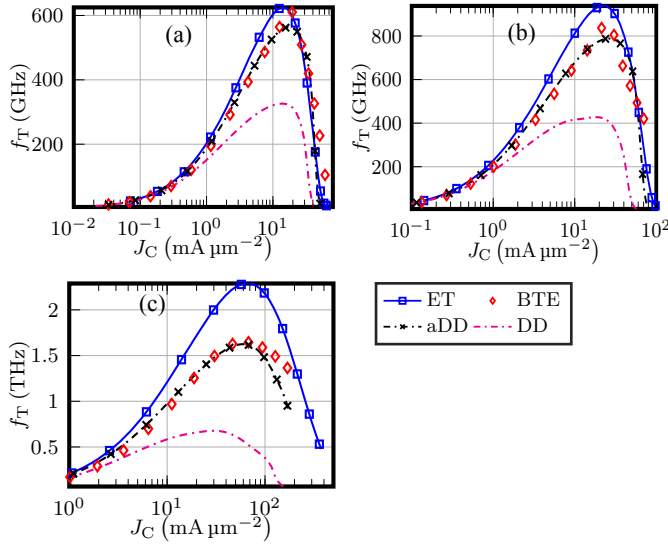


Fig. 3: Transit frequency vs. collector current density (at $V_{BC} = 0V$) for the SiGe roadmap HBT generations [9] (a) N2, (b) N3 and (c) N5. Comparison between BTE, ET, DD and aDD simulation results.

The long simulation time for solving the BTE makes the approach inefficient for optimizing the doping and composition profile of a given process node and also for generating the terminal characteristics that are necessary for CM parameter extraction. The latter requires I-V curves for a wide J_C and V_{CE} range. Hence, both ET and DD transport parameters were adjusted (“calibrated”) so as to match the BTE results as accurately as possible over a wide bias range. It turned out that ET characteristics were quite sensitive to the empirical parameters mentioned earlier [38]. In particular, certain combinations that gave a good agreement for f_T resulted in a non-physical nega-

tive output conductance. For traditional DD transport, just the mobility and saturation velocity can be adjusted. More recently, a non-local model for the field dependent carrier velocity was derived, leading to an augmented DD (aDD) transport formulation with the energy relaxation length as additional parameter [39]. Compared to ET (i) calibrating aDD transport to the BTE is much easier, (ii) aDD is computationally more efficient, (iii) all CMs are based on DD transport. Hence, for these reasons and since (a)DD transport using the concept of ballistic mobility appears to work well even for nanoscale devices (e.g. [40]), further use of ET simulation was abandoned and just aDD simulation has been utilized in recent projects for simulating both SiGe and III-V HBTs. Numerical aDD simulation is considered the most suitable stepping stone in between BTE and CM. The latter, from a practical point of view, requires even further simplifications of the DD formulation.

This choice of simulation approaches is further confirmed in Fig. 4. It shows a comparison between the results of the compact model HICUM, aDD transport and BTE. Quite good agreement is achieved for the DD-based models despite the strong simplifications. Of course, a CM contains many parameters that enable the adjustment of its electrical characteristics to those of a wide range of HBT technologies. Hence, the question is rather, how “physical” the extracted CM parameters are. As it turns out, the key model parameters of HICUM/L2 are still reasonably close to the average values that can be obtained from aDD simulation for a given transistor structure since the fundamental formulations of the CM (for transfer current and charge) have a strong relation to the DD transport model and device structure.

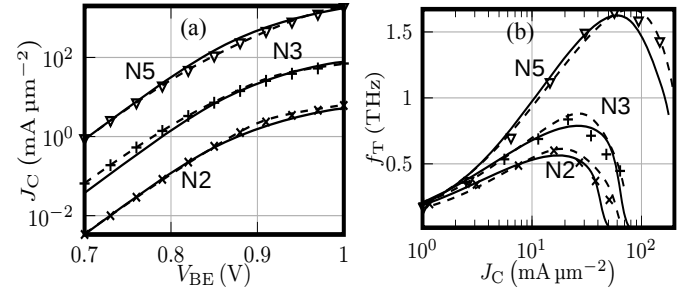


Fig. 4: (a) Transfer characteristics and (b) transit frequency $f_T(J_C)$ (all at $V_{CE} = 0.8V$) for the SiGe HBT roadmap generations N2, N3 and N5 [9]. Comparison between BTE (symbols), aDD (solid lines) and HICUM/L2 (dashed lines). In (a), for a separation and clearer view, J_C of N2 and N5, respectively, was multiplied with 0.1 and 10, respectively.

Due to the large computational effort, the BTE is usually solved just for the vertical (1D) HBT structure⁴. Although even for highly scaled HBTs the 1D structure strongly determines the intrinsic nonlinear transistor behavior (given by the transfer current and mobile charge), the impact of the carrier injection across the emitter perimeter junction and of the external regions on the HF device performance is significant.

3)Note that DD transport is still used for holes.

4) But a 3D k-space still has been used.

Hence, an additional reason for switching from BTE simulation to aDD simulation is the computational efficiency of the latter for 2D and 3D structures. While it is possible to simulate a 3D HBT structure [41], there is no need to spend that effort since (i) the external regions can be easily described by Ohm's law, bias independent parasitic capacitances and bias dependent depletion capacitances and (ii) long emitter stripes (corresponding to the 2D case) are used for HF applications and provide all necessary information for extracting CM parameters.

The process-specific model parameters of the emitter perimeter region can be determined from 2D aDD device simulation, while the relevant sheet resistances of the external regions and the contact resistivities for the new process node are already reasonably well known by the process engineers. A 3D Poisson-solver is then used for determining the parasitic capacitances of the external HBT regions and a 3D thermal solver yields the element values of the thermal network, all a function of emitter or device geometry. Once all process-specific parameters have been determined, analytical equations are used to calculate the model parameters for a given actual transistor structure the geometry of which is defined by its dimensions and its contact configurations. Fig. 5 summarizes the corresponding procedure with the various TCAD tools used.

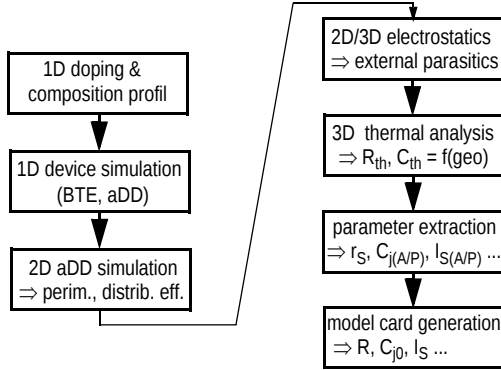


Fig. 5: Flowchart for generating predicted model cards using a variety of TCAD tools.

V. FROM MEASUREMENTS TO 1D CHARACTERISTICS

Once the first two steps of the CM parameter extraction procedure outlined earlier have been completed, the model parameters for various specific HBT structures with different emitter dimensions can be generated. The parameter calculation is based on the actual (rather than drawn) dimensions and includes structural effects such as emitter window corner rounding. A detailed model verification is performed by comparison of the CM simulation with measured DC and HF characteristics, including Y-parameters and, preferably, also large-signal (e.g., load-pull) data. When, after possible further fine tuning, the comparisons show satisfactory results over bias, geometry, frequency and temperature, the probability is very high that each EC element accurately represents its associated device structure region and occurring physical effects there. Then, by stripping off one element at a time, its impact on the

electrical characteristics can be evaluated. Finally, the “1D measurement” data obtained from this approach can be used for verifying and also calibrating device simulation results as well as for inverse modeling (using a calibrated simulator).

As an example, Fig. 6 displays the corresponding results for f_T of two different process generations in terms of doping profiles. Here, groups of external elements, such as all external series resistances or all parasitic capacitances, have been removed step by step. It is interesting to note that there is a factor of 1.5 improvement in the 1D f_T (cf. Fig. 6(b) vs. (a)), but this factor drops to 1.3 for the external f_T due to the larger impact of parasitic effects. The data shown in Fig. 6(b) were from a preliminary process version developed during the DOTSEVEN project. The detailed analysis of the impact of parasitic effects, showing in particular a sufficient margin in the 1D doping profile, then helps process engineers to decide which structural improvements are most important to work on for achieving the target device performance.

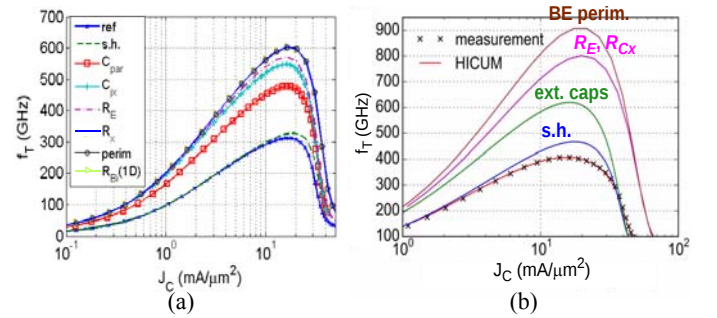


Fig. 6: Transit frequency vs. collector current density for two different process generations showing the impact of parasitic effects and external regions on the device characteristics.

That same approach was pursued successfully more recently in the DARPA T-MUSIC project [16]. The device structure of the Tower Semiconductor production process SBC18H5 was improved using (i) BTE simulation due to significant changes in doping, (ii) aDD device simulation for optimizing the vertical doping and composition profile and (iii) a scalable HICUM/L2 model for optimizing the lateral device structure. For reliably deploying aDD simulation, a geometry-scalable parameter extraction was performed based on fabricated SBC18H5 structures. Then, the impact of the external regions was analyzed, thus not only providing the 1D transistor characteristics but also enabling the identification of those external regions that most severely degraded device performance.

Next, based on measured initial doping data, the doping profile of the 1D structure was adjusted as follows. The base peak doping level was slightly adjusted according to the measurement of the internal base sheet resistance obtained from tetrodes. Then the collector doping concentration was slightly adjusted to match the drop of f_T at high current densities. The corresponding BTE results served as reference for calibrating the aDD transport solver. The latter was then utilized for examining profile changes that would lead to the highest possible increase in transit frequency. Fig. 7 shows the measured and simulated 1D transit frequency for different stages of the

process development. Deviations of the BTE from measurements may be due to uncertainties in the doping and composition profiles and the associated lattice strain.

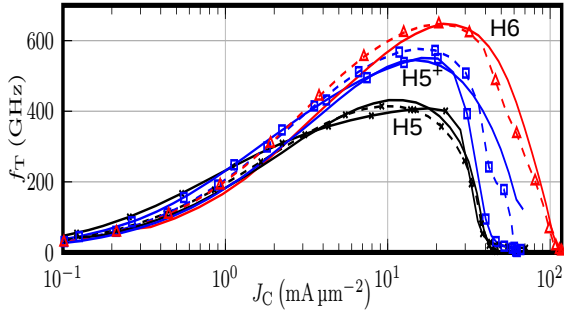


Fig. 7: Transit frequency vs. collector current density for different process versions. Comparison of 1D aDD device simulation (dashed line with symbols) with 1D measurement data (solid lines with symbols, H5 and H5⁺ only) and BTE simulation data (solid lines).

VI. MODELING AT CRYOGENIC TEMPERATURES

SiGe HBTs have been demonstrated to be well-suited for low-temperature applications [42]. More recently, there has been significant interest in using SiGe HBT technology also for building readout circuits in quantum computers. The design of these circuits requires physics-based large-signal CMs, which unfortunately do presently not exist. Their development is hampered in part by both the lack of low-temperature transport models implemented in device simulators and convergence issues.

DD transport leads to extremely low current densities at low temperatures. This causes convergence problems for both numerical device simulation and CMs in circuit simulation below about 25K or even higher. However, for advanced SiGe HBTs with a thin base layer, the significant intra-band tunneling through the base region and also trap assisted tunneling associated with the junctions dominates the terminal currents at cryogenic temperatures. Adding these tunneling mechanisms increases the simulated currents to their measured levels [43, 44]. The also increased conductances improve the convergence down to even 4K.

VII. SUMMARY AND OUTLOOK

The combination of selected TCAD tools and compact modeling along with proper test structures for model parameter extraction enables time and cost efficient device design for SiGe HBT process development. Frequent comparisons of simulation results with experimental data also facilitates very useful cross-fertilization between TCAD, compact modeling and process development. Since for predicting the electrical characteristics of an actual (3D) HBT structure in a new process generation no single tool or technique is suitable, a simple push-button approach does not exist and the device engineer must rather have a deep understanding of the relevant physics covered by each tool.

Future scaling of SiGe HBT structures towards presently predicted generations [9] and possibly beyond will have to ad-

dress increasing process tolerances due to the increasing impact of lattice strain and random distributions of doping and composition atoms. Fig. 8 illustrates the problem. Each Ge distribution within the very thin Si base layer will produce different material properties such as density of states, bandgap and mobility. The atomistic simulation results of such a highly scaled structure have to be translated to semi-classical TCAD tools in order to obtain the electrical characteristics of a complete 1D and 3D transistor structure. Including such random variations in compact models will also be challenging.

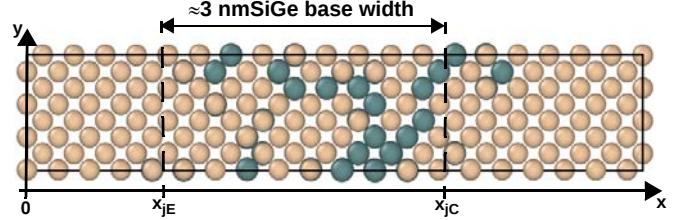


Fig. 8: Cross-sectional vertical plane through a Si-SiGe-Si slab used for simulation exhibiting a possible (random) distribution of Ge atoms (ramped from 0% at x_{JE} to 30% at x_{JC}) within a Si host lattice.

VIII. ACKNOWLEDGMENTS

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