Latest developments of HICUM/L2 for mm-wave applications

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Outline

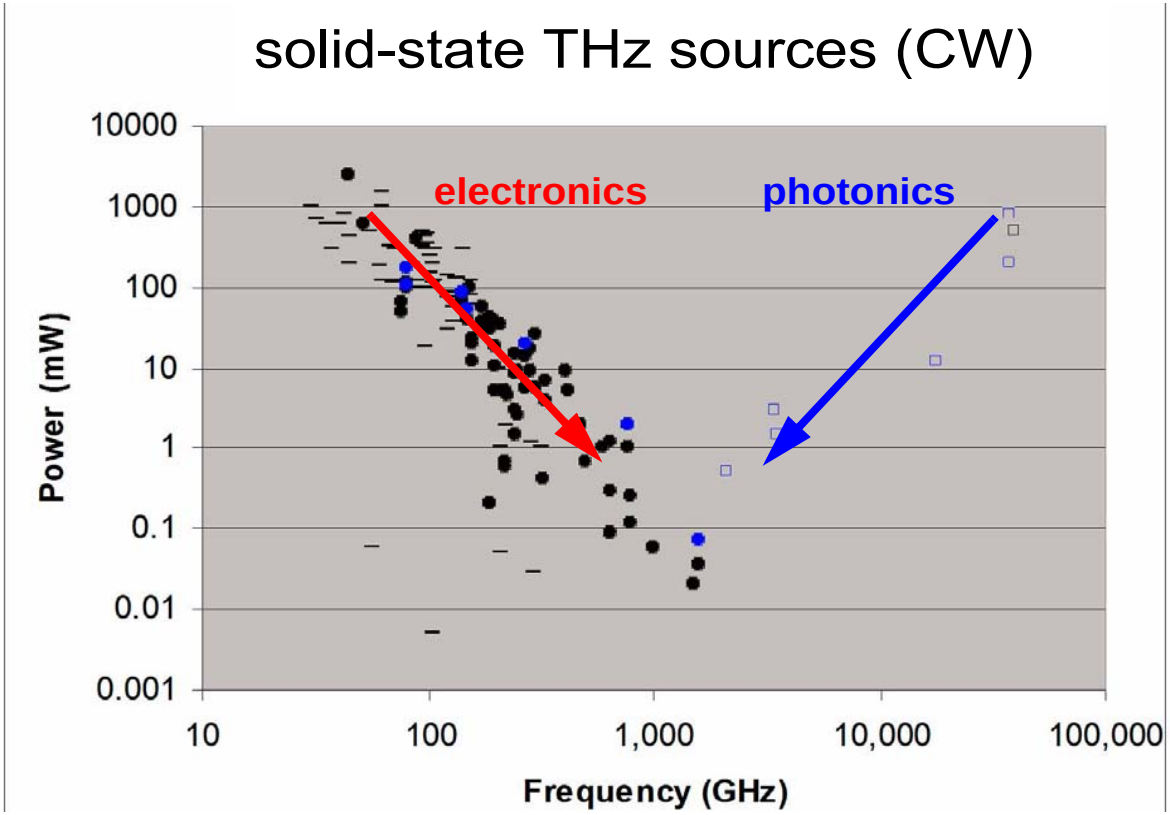
- Introduction
- HICUM/Level2 extensions
- Model verification
- Summary

Introduction

Major challenge for mm-wave and THz operation:

generating sufficient output power

solid-state THz sources (CW)



=> need to exploit process limits by careful *device* and *circuit optimization*

=> need *accurate compact models* for active and passive devices

HBT modeling challenges

... to be addressed for mm-wave and THz circuit design

- self-heating => thermal stability, reliability
- breakdown => reliability, stability
- high-current effects & quasi-saturation => PAE, operating frequency
- substrate effects => PAE, jitter, operating frequency
- large-signal operation => distortion
- distributed effects: high-frequency, breakdown, thermal, substrate
- g_m drop (technology dependent) => drive capability/circuit speed

ALSO: model *verification* issues ...

- process development is outpacing measurement equipment availability
  => how to verify large-signal modeling at multi-100 GHz?
  (incl. distortion!!)

Modeling approaches

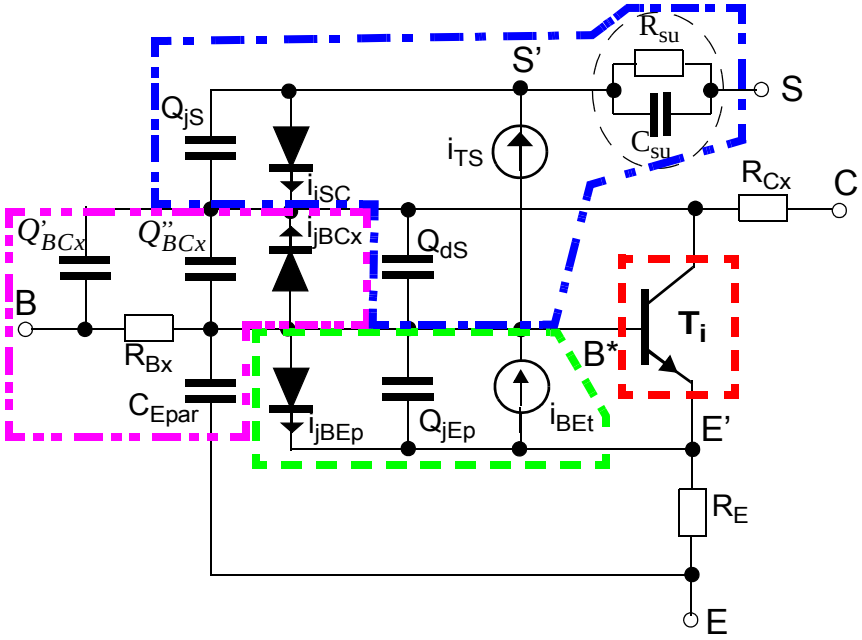
Criteria	Behavioral, X-par.	Physics-based
accuracy	high (within narrow ranges)	moderate to high over wide range
numerical stability	compromised outside fitting ranges	high (for standard models)
fabricated devices	need every possible layout used in circuits	only few devices (6 HF trs, 6 test structures)
measurement effort	moderate to high	moderate to low
par. extraction effort	moderate to low (per device) very high for library	moderate to low (per device) very low for library
geometry scaling	inconsistent (typically)	consistent
predictive capability	none	moderate to high
statistical modeling	none (very high effort)	good to excellent

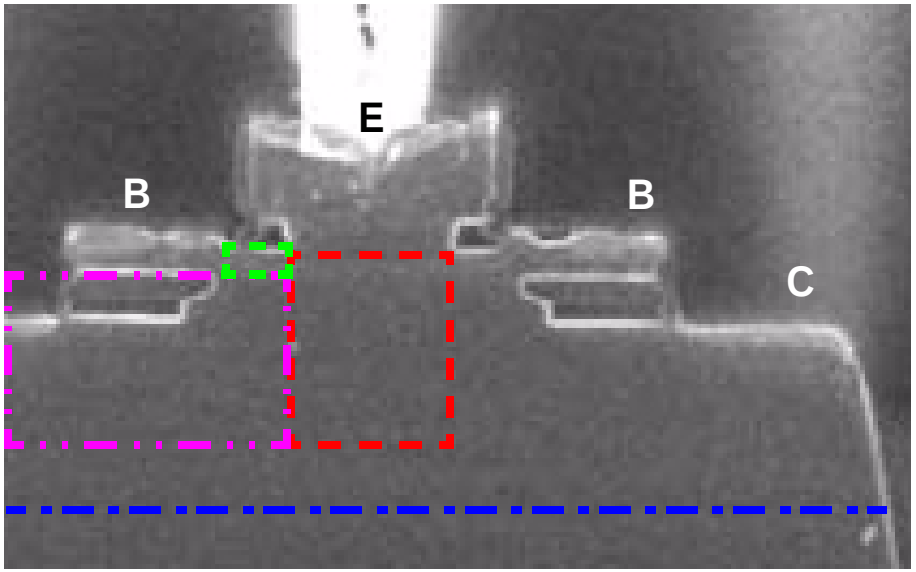
***Goal*: cover large variety of applications & circuit optimization (bias, T, f)**

=> *Physics-based* model (cuts design cycle, supports process dev.)

Physics-based compact model

... definition



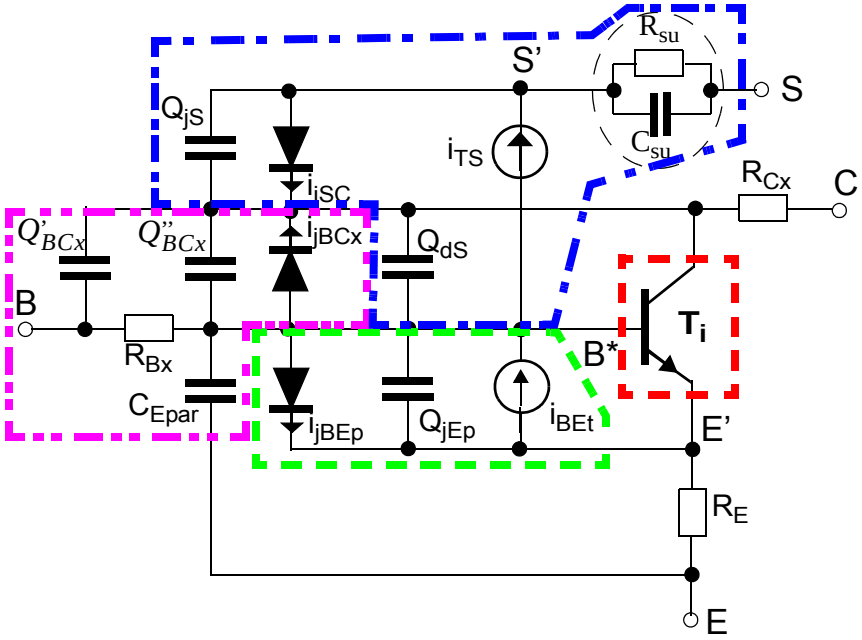


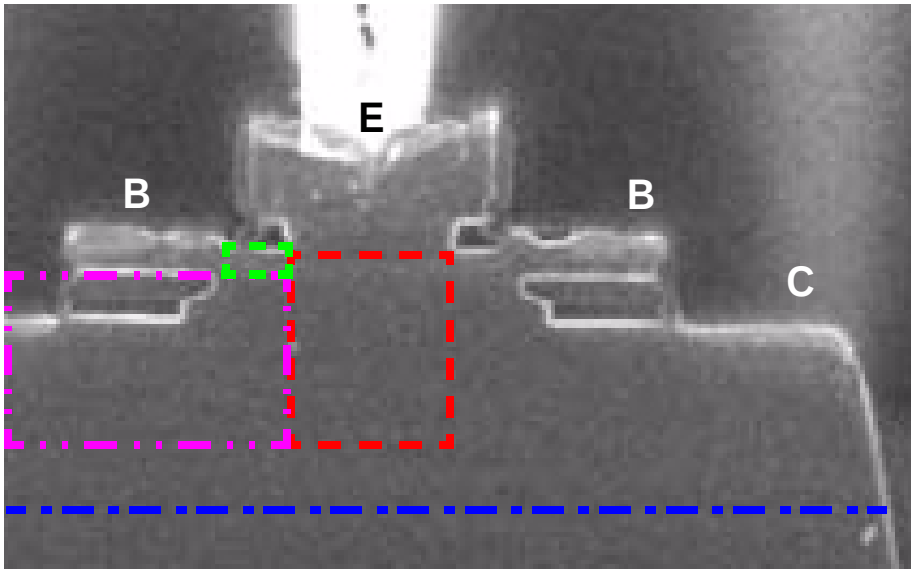
each spatial region is represented by corresp. equivalent circuit element

- each EC element value is a function of bias, T, structural and physical parameters

Physics-based compact model

... definition





each spatial region is represented by corresp. equivalent circuit element

- each EC element value is a function of bias, T, structural & physical parameters

=> realized in HICUM/Level2 (from the beginning)

=> supports circuit optimization, statistical modeling, process development

HICUM/Level2 extensions

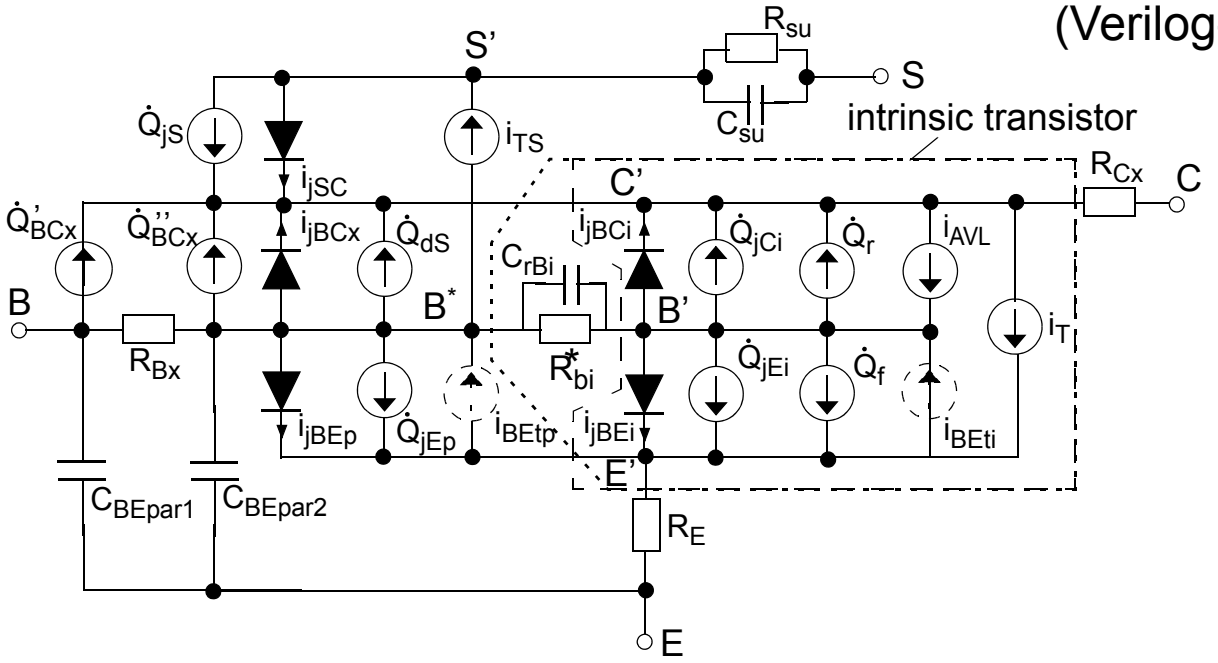
... recent development work during DOT5, DOT7, RF2THz

- transfer current and g_m drop (technology dependent)
  - bias dependence of reverse Early effect => g_m degradation at low injection
  - weight factor for low-current mobile charge => g_m degradation at medium injection
  - temperature dependence of weight factors
- explicit formulation of BC barrier effect
- flexible CE voltage dependence of critical current
- temperature dependence of thermal resistance
- simplification of AC emitter current crowding implementation
- exact implementation of correlated HF noise (verified up to at least 500GHz)
- simplification of input NQS effect description (and verification)

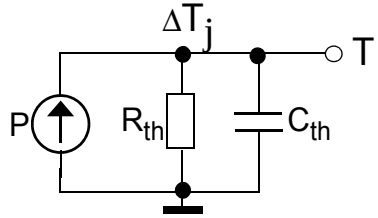
... and: reliable model parameter extraction methods

Complete HICUM/L2 equivalent circuit

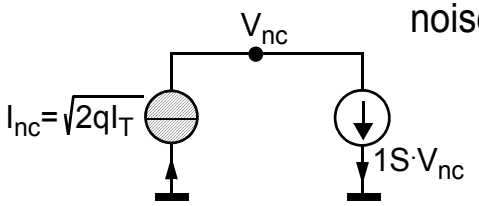
(Verilog-A implementation)

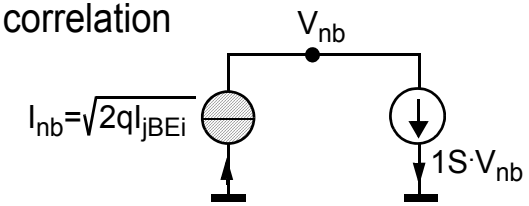


thermal network



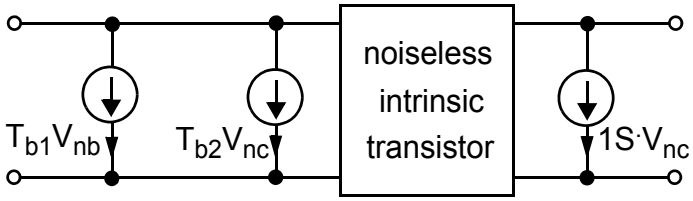
noise correlation



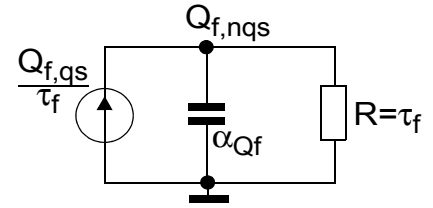


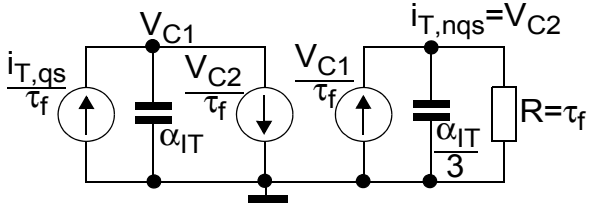
$T_{b1}=1+j\omega\tau_f\sqrt{B_f(2\alpha_{qf}-\alpha_{IT})^2}$

$T_{b2}=j\omega\tau_f\,\alpha_{IT}$



vertical NQS effects





Model features

- large-signal model
  => small-signal, noise, distortion follow automatically!!

- includes all relevant SiGe HBT related effects
  (e.g. Ge dependence, BC barrier)

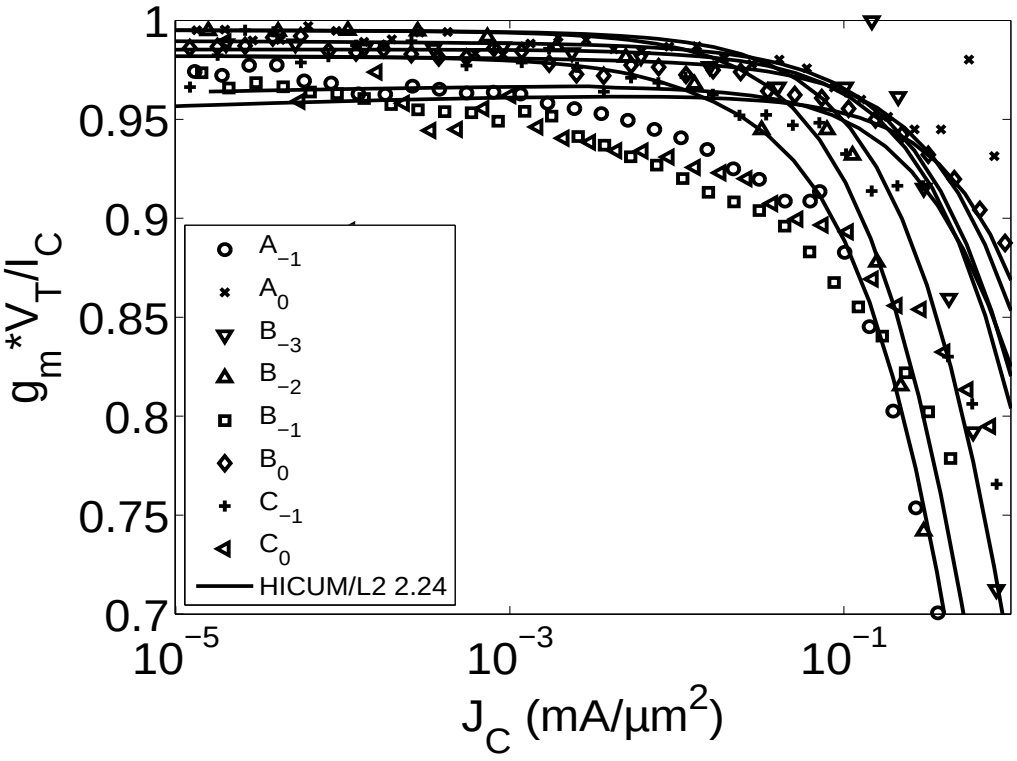
- physics-based
  => geometry scalable, predictive (statistical simulation) capability

- available in all mainstream simulators (ADS, ELDO, MWO, SPECTRE ...)
  - vs. "special" models available in only a single simulator

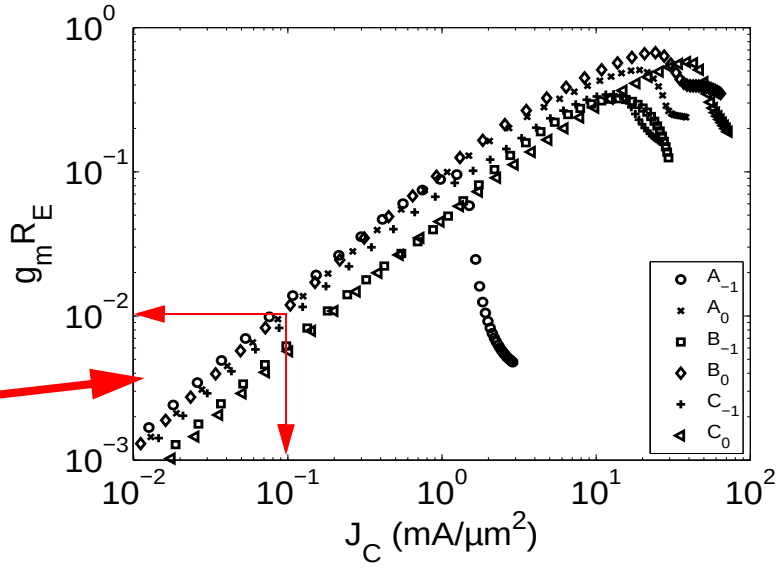
- applied to every Si BJT and SiGe HBT process node since early eighties
  => spans 90(55)nm to 1µm lithography, 10 to 400 GHz transit frequency

  => continuous model development and improvement

Transfer current



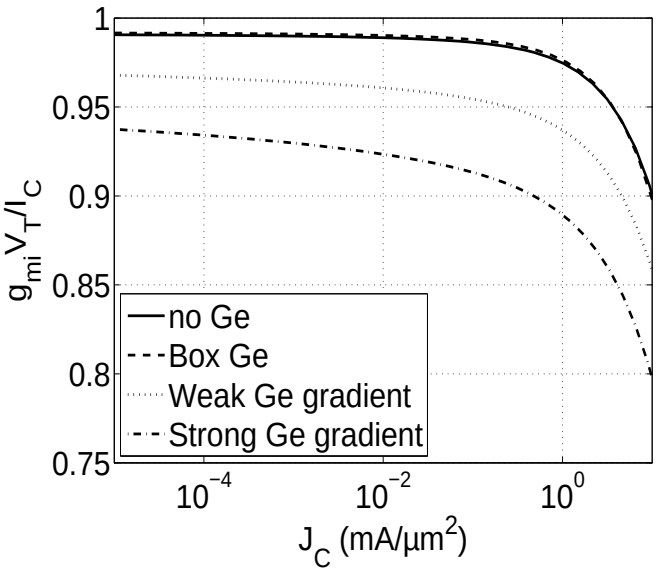
- g_m degrades at low-injection for some technologies
- degradation is *not related* to process generations



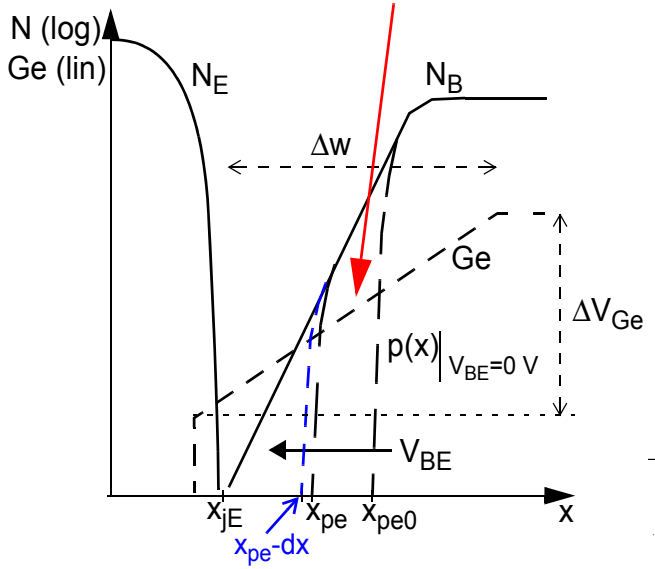
- not caused by emitter resistance
- not caused by BGN or quantum effects

=> g_m degradation difficult to capture accurately with existing models

Transconductance

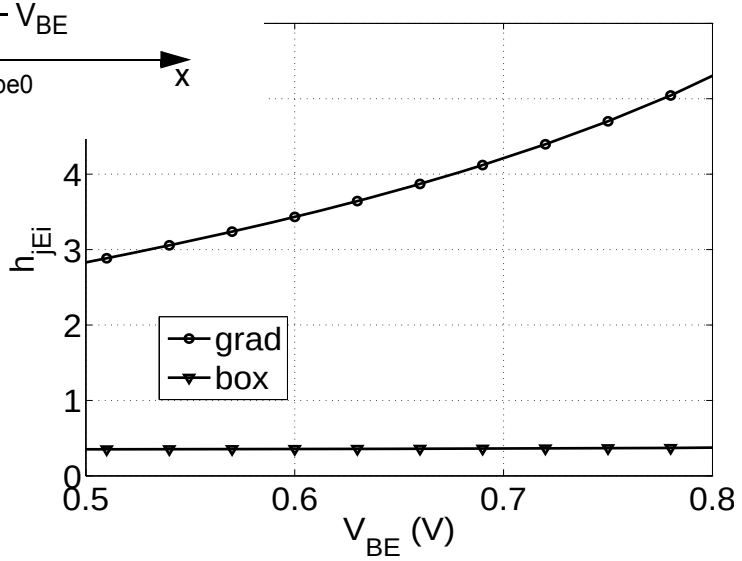


similar trend observed from device simulation for graded Ge profile in BE SCR



=> Ge grading causes bias dependence of GICCR weight factor h_{jEi} for BE depletion charge Q_{jEi}:

$$I_T = \frac{c_{10}}{Q_{p0} + h_{jEi} Q_{jEi}} \left[\exp\left(\frac{V_{B'E'}}{V_T}\right) - \exp\left(\frac{V_{B'C'}}{V_T}\right) \right]$$

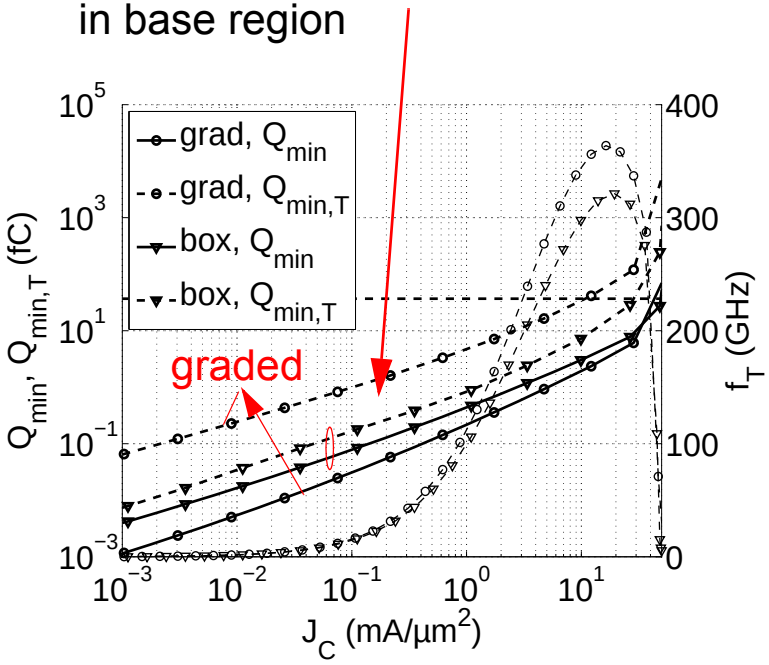


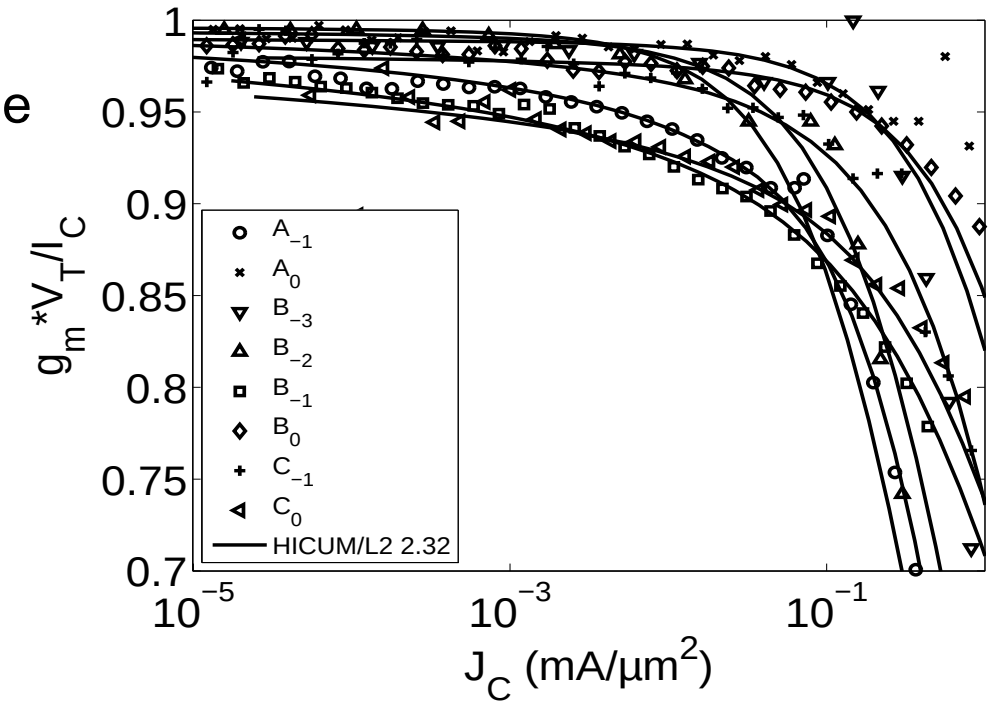
Transconductance

- h_{jEi} voltage dependence $h_{jEi}(V_{B'E'}) = h_{jEi0}\dfrac{\exp(u)-1}{u}$

  with $u = a_{hjEi}\sqrt{1 - V_{B'E'}/V_{DEi}}$

- h_{f0}: weight factor for mobile charge
  - graded Ge causes *shift in weighted mobile charge center of gravity* in base region





$$\Rightarrow\ I_T = c_{10}\frac{\exp\left(\dfrac{V_{B'E'}}{V_T}\right) - \exp\left(\dfrac{V_{B'C'}}{V_T}\right)}{Q_{p0} + h_{jEi}(V_{B'E'})Q_{jEi} + h_{f0}Q_{f0}}$$

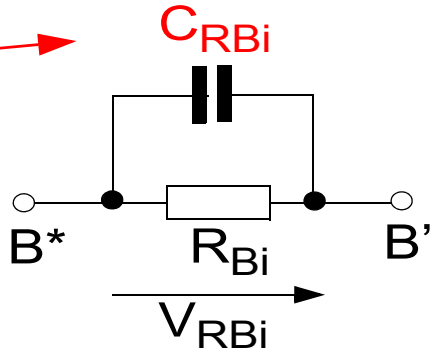
=> very accurate modeling of transconductance

AC emitter current crowding (Lateral NQS effect)

Issue: generates 2.3MB of code for derivatives!

- AC analysis by using

$$C_{RBi} = f_{CRBi}(C_{jEi} + C_{jCi} + C_{dEi} + C_{dCi})$$



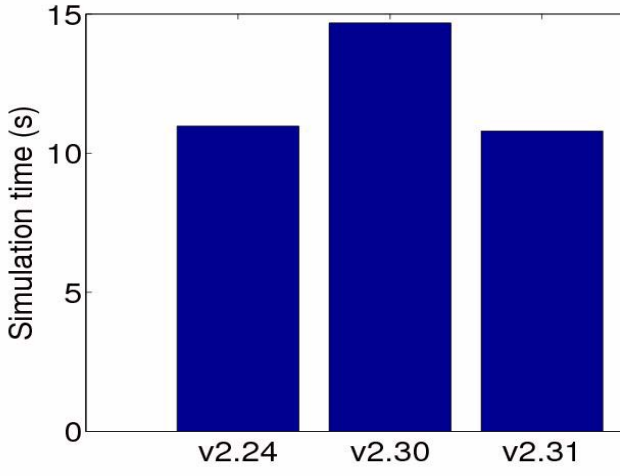
- Previous calculations of diffusion capacitances

$$C_{dEi} = \left.\frac{dQ_{dEi}}{dV_{BE}}\right|_{V_{BC}} \quad \text{and} \quad C_{dCi} = \left.\frac{dQ_{jCi}}{dV_{BC}}\right|_{V_{BE}}$$

=> calculated using ddx-operator

- Simplification avoiding ddx operator

$$C_{dEi} = \frac{dQ_{dEi}}{di_{Tf}}\frac{di_{Tf}}{dV_{BE}} \approx \tau_{f0}\frac{i_{Tf}}{V_T} \quad \text{and} \quad C_{dCi} \approx \tau_r\frac{i_{Tr}}{V_T}.$$



- g_m overestimation by i_{Tf}/V_T partially compensated by using τ_{f0} instead of τ_f

=> reduces code size (ADMS) to 0.3 MB(2.31)

Temperature dependence of thermal resistance

- For potential numerical stability reasons, modeling of $R_{th}(T)$ was changed from nonlinear to linear formulation:

$$R_{th}(T) = R_{th}(T_0)\left(\frac{T}{T_0}\right)^{\zeta_{Rth}} \quad \text{to} \quad R_{th}(T) = R_{th}(T_0)(1 + \alpha_{Rth}\Delta T)$$

- For backward compatibility, the present implementation reads

$$R_{th}(T) = R_{th}(T_0)(1 + \alpha_{Rth}\Delta T)\left(\frac{T}{T_0}\right)^{\zeta_{Rth}}$$

  where the previous term and parameter have still been kept

  - Setting
    - $\alpha_{Rth} = 0$ and $\zeta_{Rth} > 0$ recovers the previous formulation
    - $\alpha_{Rth} > 0$ and $\zeta_{Rth} = 0$ gives the new formulation

- Planned: no further support for previous implementation (and parameter ζ_{Rth}) but requires to add prevention of negative R_{th}

Thermal and emitter resistance

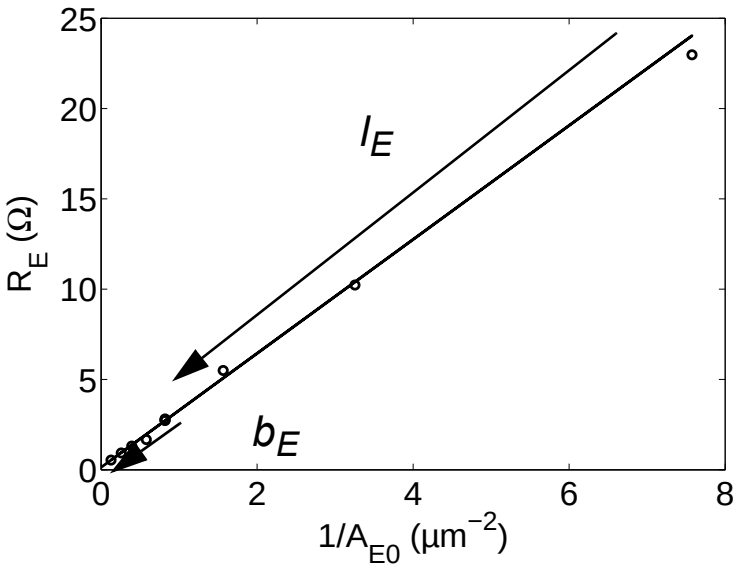
... from a joint extraction

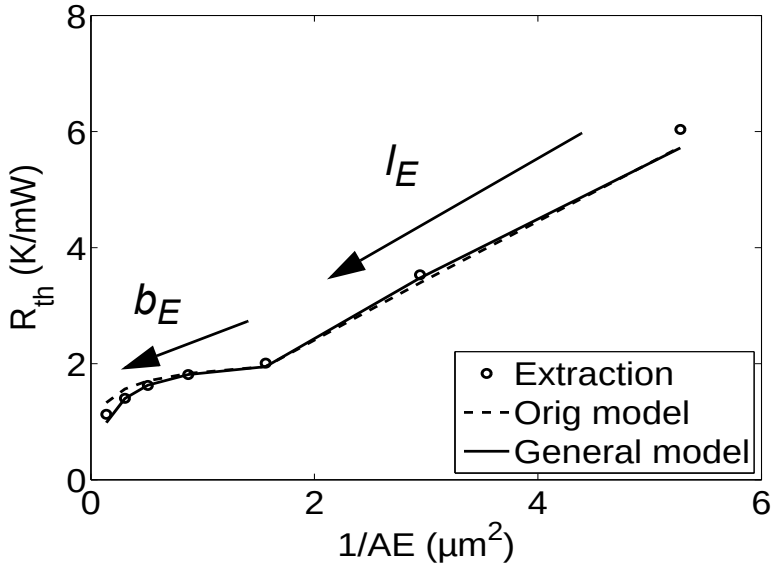
- Scaling of thermal resistance was changed from

$$R_{th} = \frac{\ln(4l_E/b_E)}{l_E} r_{th} \quad \text{to} \quad R_{th} = \frac{R_{th0}}{1 + a_{rthb} b_E + a_{rthl} l_E}$$

  to give better results for width scaled devices

- Emitter resistance scaling almost ideally linear





Correlated noise

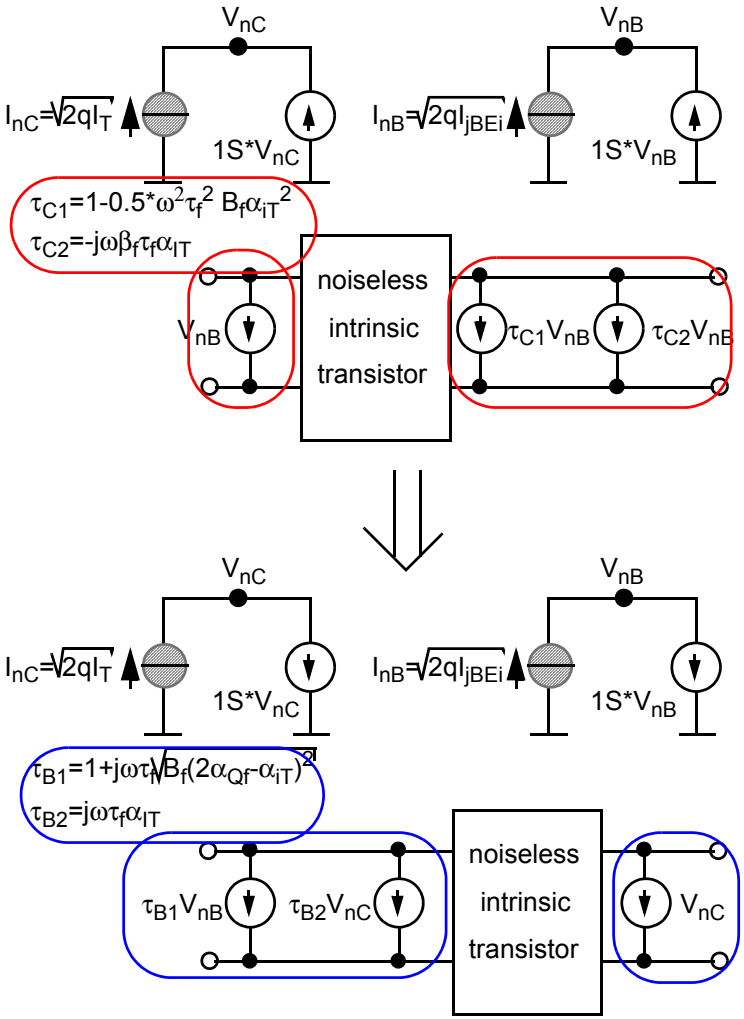
- New formulation for correlated noise modeling
  - modeling at the transistor input, not output
  - flag ***flcono*** turns correl. noise **on (1) and off (0)**
  - conditional statement for calculation of square root

IF $2\alpha_{Qf} > \alpha_{iT}$ => $\tau_{b1} = 1 + j\omega\tau_f\sqrt{2\alpha_{Qf} - \alpha_{iT}^2}$

otherwise => $\tau_{b1} = 1$

  - no use of nested ***ddt*** operators anymore
  - ***default*** values of α_{Qf} (*alqf*) & α_{iT} (*alit*) have been changed to physically meaningful values
  - ***Range*** of *alqf & alit* modified from [0:1] to **(0:1)**

- Generic method for constructing correlated noise networks see:
  - *J. Herricht et al., "**Systematic** compact modeling of correlated noise in bipolar transistor", accepted in IEEE Trans. MTT, 2012.*



Model verification

- standard characteristics: DC, small-signal y-parameters
  occasionally noise (often limited 26 GHz), sometimes load-pull & harmonics

=> typically in (foundry) characterization labs

=> issues for mm-wave & THz technologies

  - need (large) arrays for achieving suitable impedances => impact of interconnect parasitics
  - *distortion*/harmonics, load-pull: coupler & passive tuners limit frequency to below 50...75GHz
  - ***on-wafer*** S-parameter measurement: limited to 110GHz in foundries, rarely 220GHz, none at higher frequencies; pulsed AC difficult (bias Tees, meas. interval)
  - severe self-heating limits usable bias region for parameter extraction

=> how to verify compact models beyond equipment limitations?

  - device simulation: small-signal, noise, large-signal characteristics
    => limited to basic 1D or 2D device structure without major parasitic regions
  - use in-band distortion from two-tone load-pull => limited to magnitude

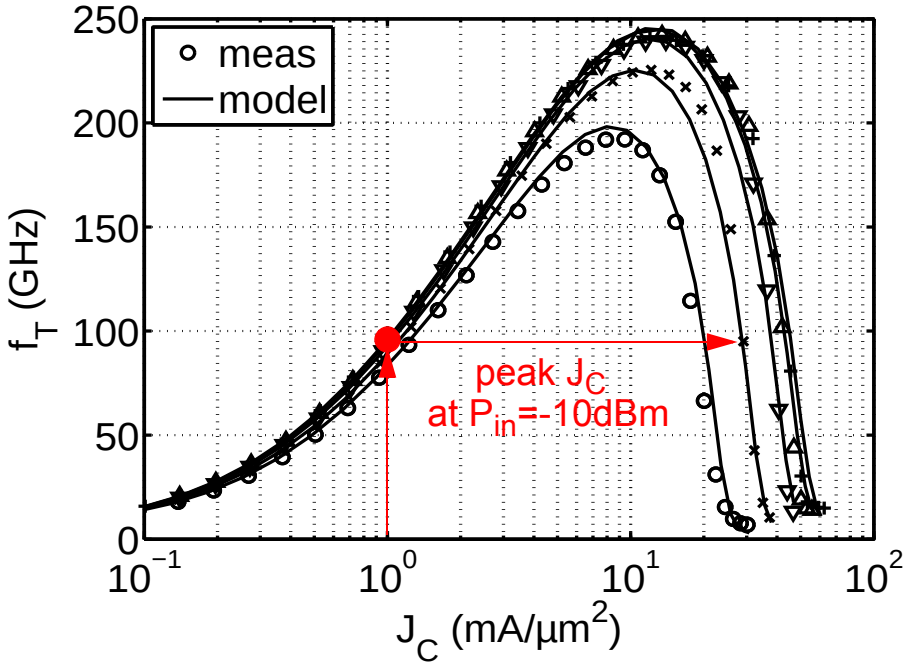
=> use *physics-based* models for extrapolating beyond equipment limits

=> Really needed:
pulsed mag & phase (or time domain) measurement capability up to 1THz

High-performance SiGe HBT (cont'd)

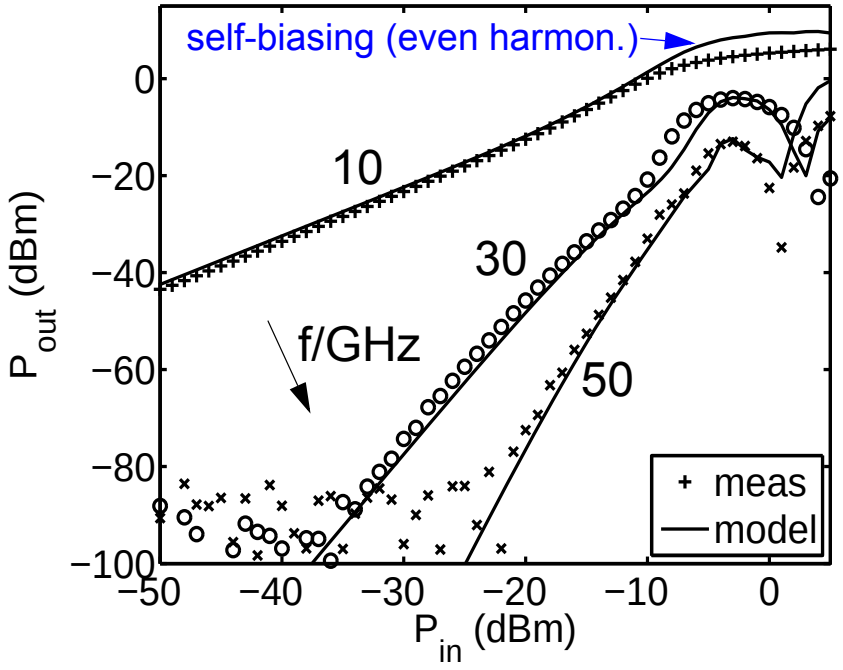
B7HF500 (IFX) *high-performance* BEC transistor with A_{E0}=2x0.1x4.88µm²

transit frequency



V_{CB}\V = -0.5, -0.3, 0, 0.3, 0.5

output vs. input power



(V_{BE}, V_{CE}) = (0.8, 0.8) V

=> excellent agreement up to high input power and third harmonics

Summary

- Need for pushing process limits => accurate compact HBT modeling
- HBT compact modeling approaches (physics-based vs. behavioral models)
- HICUM/L2 latest developments
  - released as CMC model v2.33
  - available in all commercial circuit simulators and many industry PDKs
- Experimental examples for small and large-signal behavior
  - high-performance (low breakdown voltage) HBTs
  - similar results were obtained also for high-voltage (low speed) HBTs
  - used in industry (e.g. WCDMS, OFDMA, CD/DVD laser drivers, OC192, GSM and GPS receiver front ends, wireless entry systems, UWB, DBS(SAT), radar, OC768...)

Planned extensions and improvements

- improved substrate coupling network (incl. *compact* geometry scaling)
- *BTB, TAT* in BC SCR and *BTB* in forward-biased BE SCR
- *reliability* model
- additional model verification on benchmark *circuits*
- CPU time reduction

Acknowledgments

Compact modeling

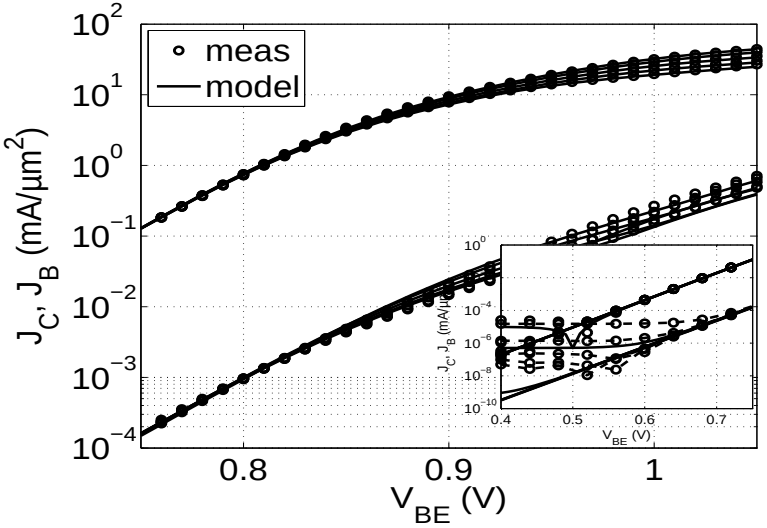
- EU FP7 IP DOTFIVE (financial support; SiGe HBT technology)
- EU Catrene RF2THz(SiSoC) (financial support; SiGe HBT technology)
- German Science Foundation SFB 912 (financial support; SiGe HBT technology)
- German Science Foundation SCHR695-3 (financial support; InP HBT research)

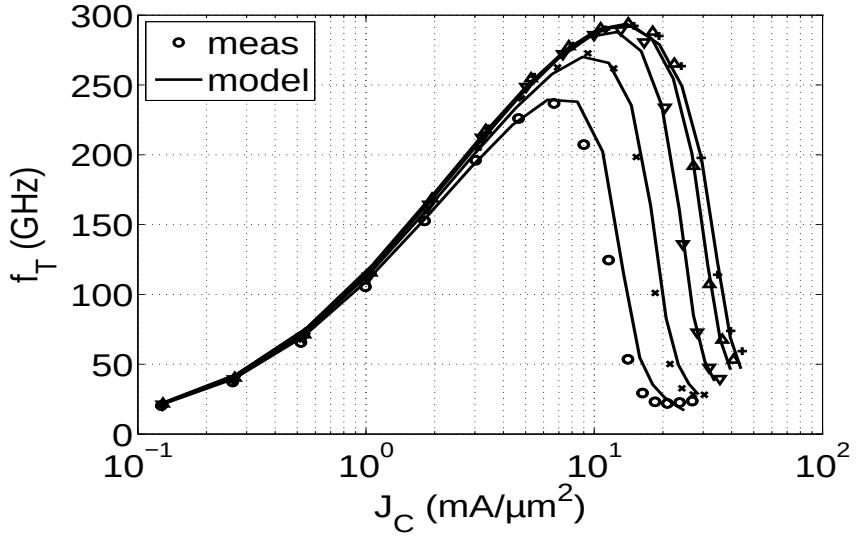
Users and user support

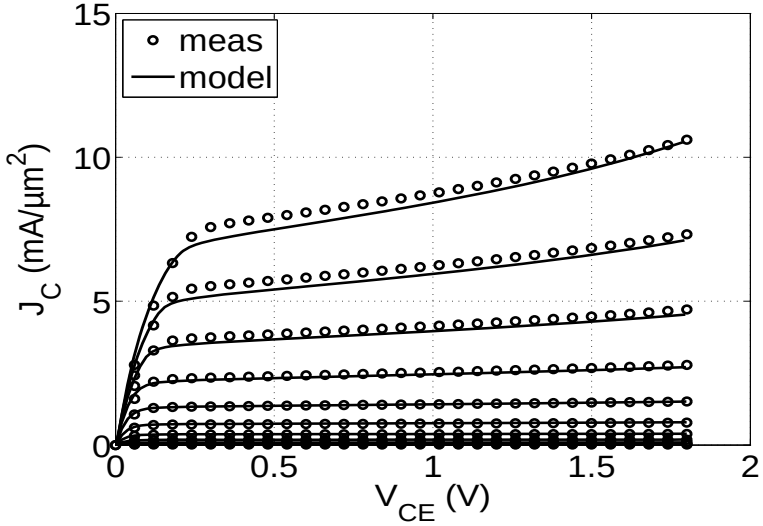
- IHP, Infineon, GCS, Skyworks, ST Microelectronics, TowerJazz (wafer supply)
- AWR, Cadence, Mentor Graphics (software)
- Agilent, AIST, Analog Devices, Atmel, IBM, ProPlus Solutions, Qualcomm, Renesas Electronics, RFMD, Samsung, Silvaco, SK Hynix, Synopsys, Texas Instruments (National), TelefunkenSemi, Toshiba, TSMC, UMC

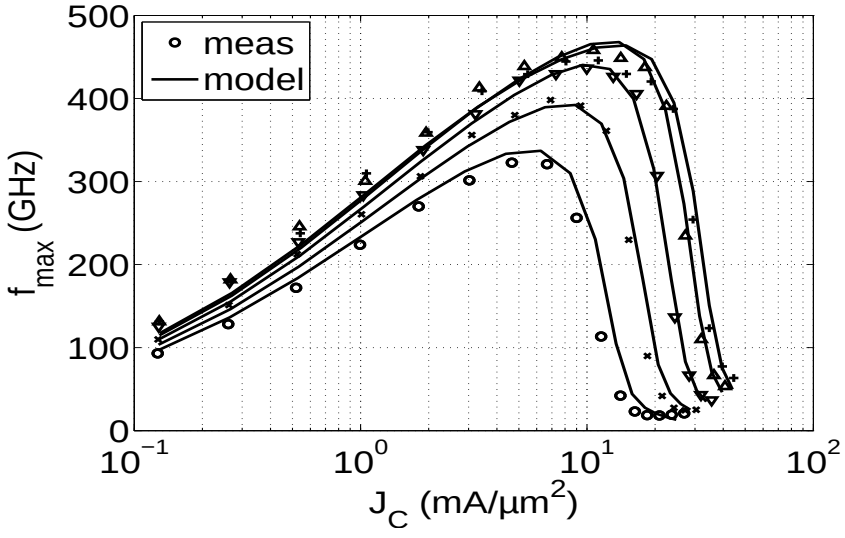
Appendix

- SG13 (IHP) CBE transistor with A_{E0}= 8 x 0.12 x 1.1µm²: DC, f_T, f_{max}



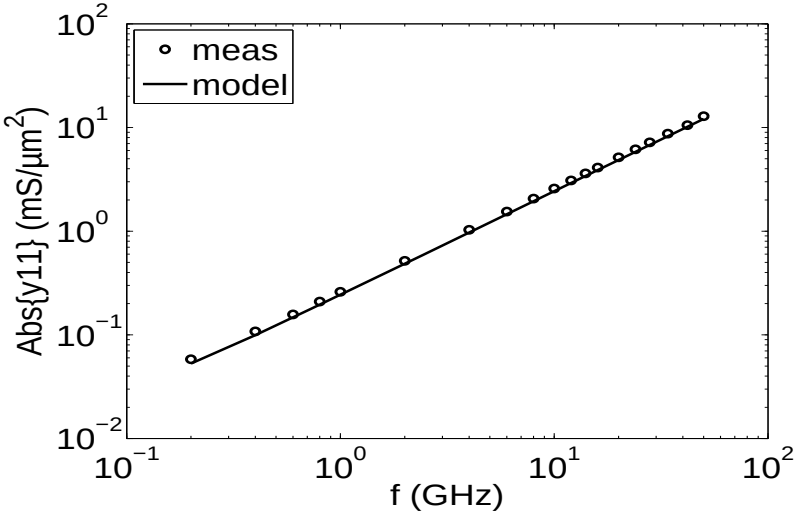


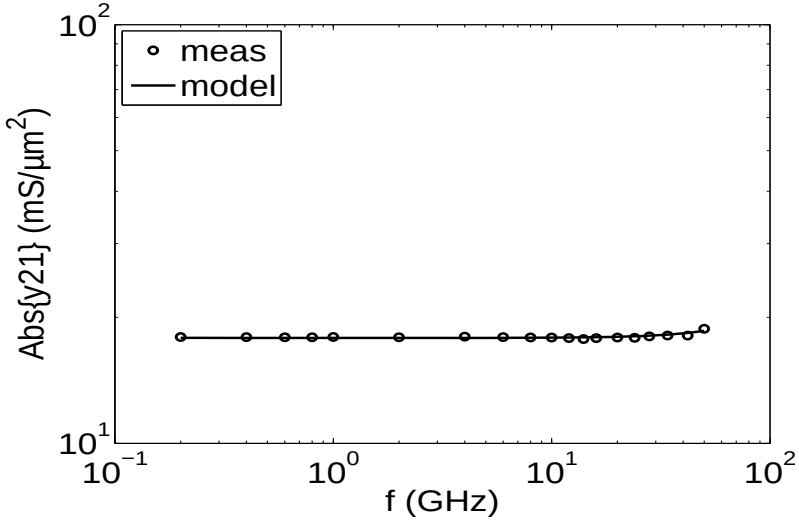


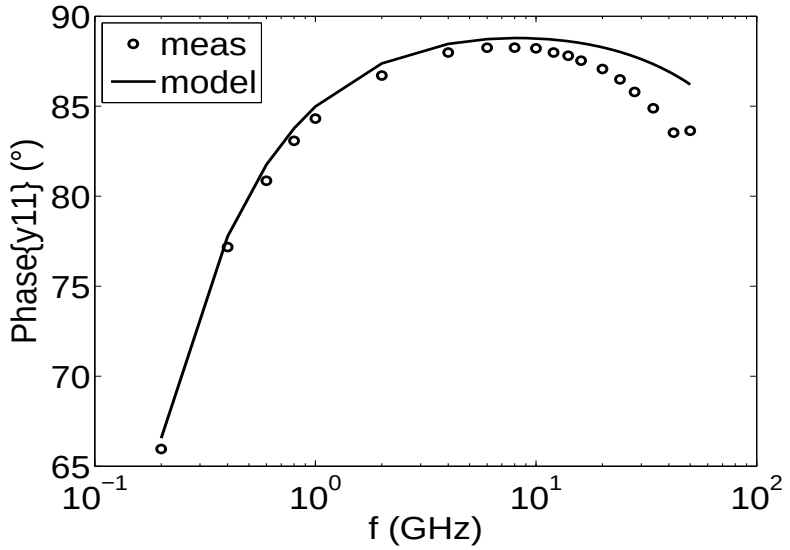


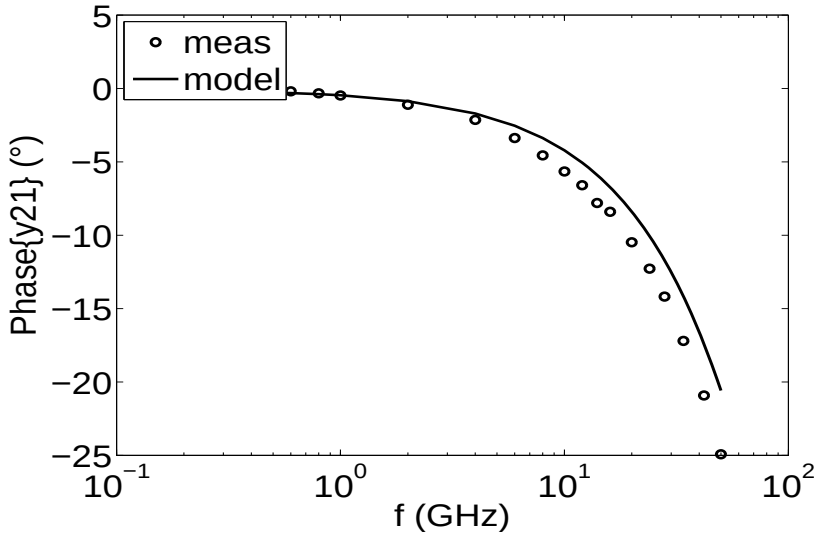
Model verification (cont'd)

- SG13 (IHP) CBE HBT, A_{E0}= 8x0.12x1.1µm²: y-parameters at peak f_T









Model verification (cont'd)

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