Tools and Environment for Sub-THz Circuit Design:

- What Can Be Done From a Modeling Perspective -

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Open Bipolar Workshop
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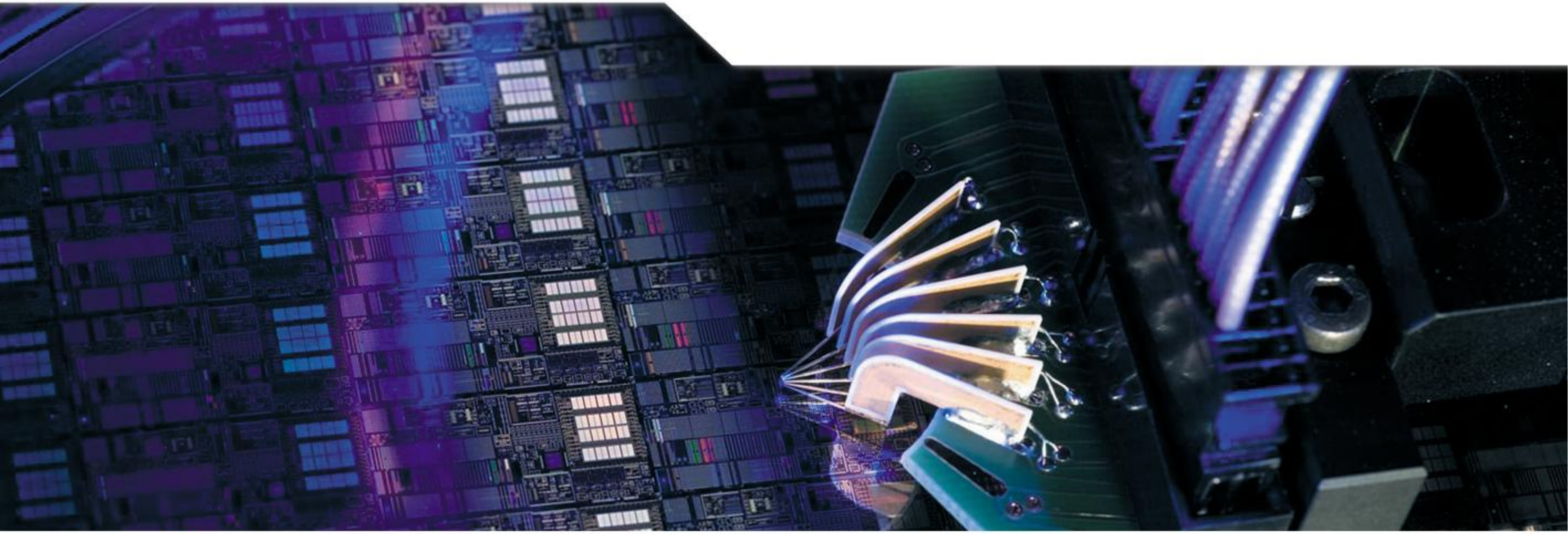

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OUTLINE

- INTRODUCTION
- CONTEXT
- SOURCES OF SIMULATION INNACURACY
  - CORE MODEL
  - SCALABLE MODELING & PARAMETER EXTRACTION
  - MEASUREMENTS
  - TEST KEY DESIGN
  - DESIGN / MODELING TARGET
- PROPOSED VALIDATION METHOD
- CONCLUSION

INTRODUCTION

GOAL OF THIS WORK:

- Identify modelling issues to improve circuit design environment
- Set up model validation methodology @ mmWave / Sub THz frequencies

Designer’s feedback is very important but often does not allow to track down the source of the problems (Many possible sources of innacuracy exist)

- Designers may not have modeling background
- Model engineers don’t know the designer’s circuits
- Even small circuit building blocks may be too complex to identify root cause

CONTEXT

- **DOTSEVEN FP7 PROJECT**
  Towards 0.7 Terahertz Silicon Germanium Heterojunction Bipolar Technology

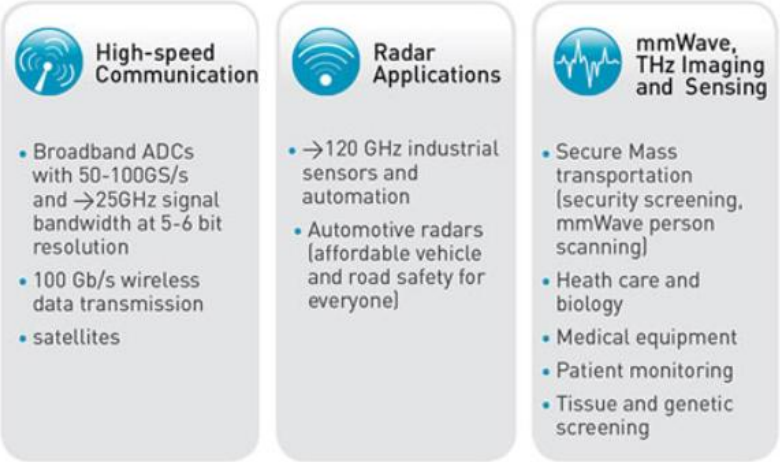


Illustration of mm-Wave and THz applications

This is a research project context
Concurent iterations in :

- process technology
- Circuit design
- Modeling

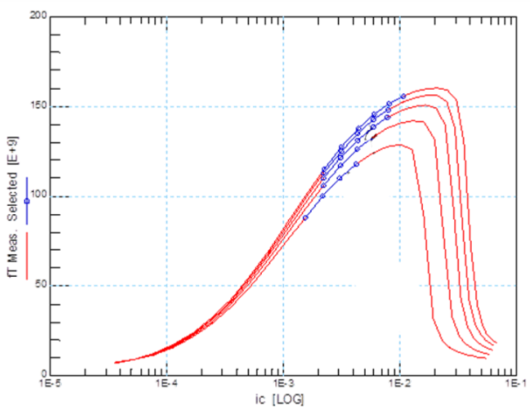
Process iteration **i** → Models of iteration **i** → Circuit Design (with models of iteration **i)** → Process iteration **i+1** → Circuits of iteration **i+1**

MODEL VALIDATION IS DIFFICULT

CORE MODEL

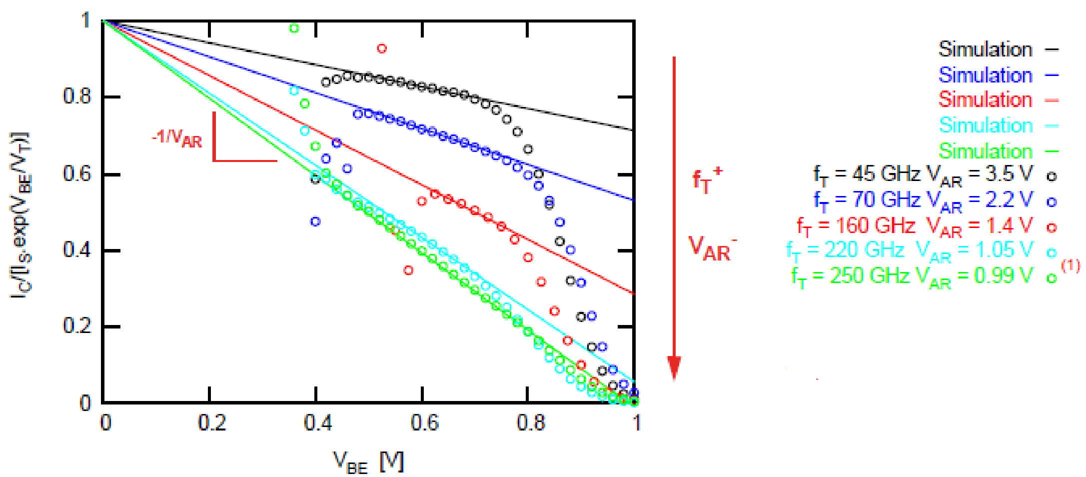
- Why HiCuM model in the beginning (for SiGe HBTs) ?
  - Accurate physics based capacitance model (intrinsic/perimeter/oxide & metal)
  - base current ideality factor independent of collector current (no BETA)
  - Transfer current described via self consistent GICCR [SCHR1993]
    - Accurate Kirk effect / quasi-saturation description
    - Self consistent AC/DC formulation (based on charges)
    - Self consistent Early effect (output conductance)
    - Bandgap engineering accounted for through meaningful weighting factors
  - Accurate transit time model (rapid f_T falloff @ high current and voltage dependence)
  - Self Heating model
  - Base resistance formulation
  - Substrate current & parasitic substrate network
  - … and more

For more details cf. [SCHR2005]



CORE MODEL

- HiCuM model in DOT7 (& DOT5)
  - Continuous improvements based on leading edge processes
  - Example: steep Ge profiles in the base of HBTs lead to increased (& bias dependent) reverse Early voltage -> led to new HiCuM L2 v2.3 formulation

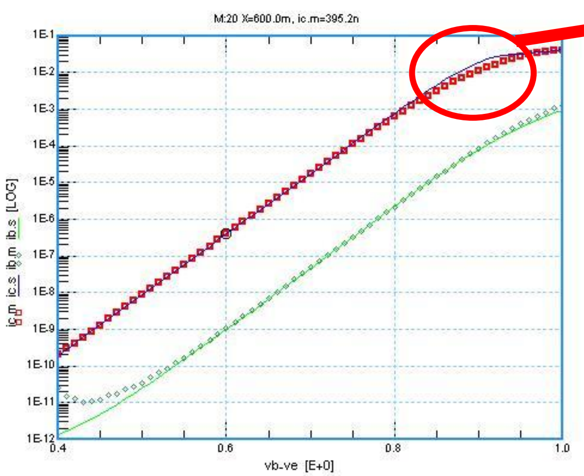


source [CELI2010]

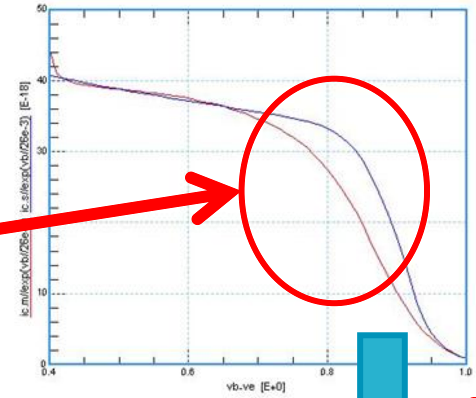
CORE MODEL

- Example (cont'):
  - Transition between low & high current densities is critical

Forward Gummel Plot $I_C(V_{BE})$, $I_B(V_{BE})$

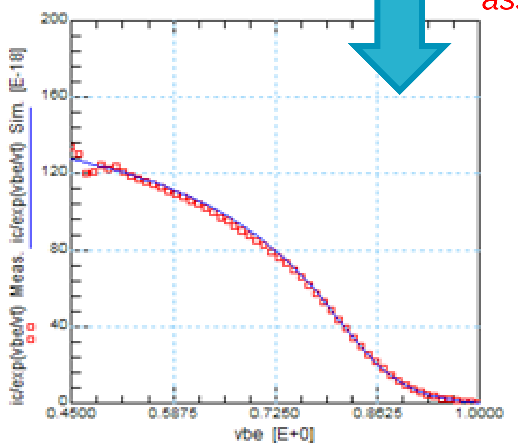


Normalized Collector Current
(Magnifying the observed discrepancy)



HiCuM L2 v2.2 formulation

NEW Formulation & associated parameter extraction

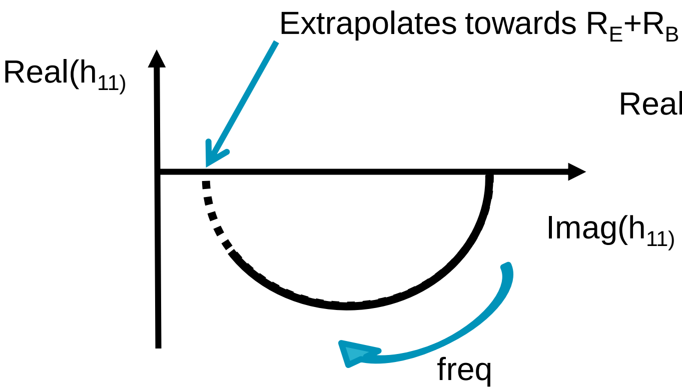


HiCuM L2 v2.3 formulation

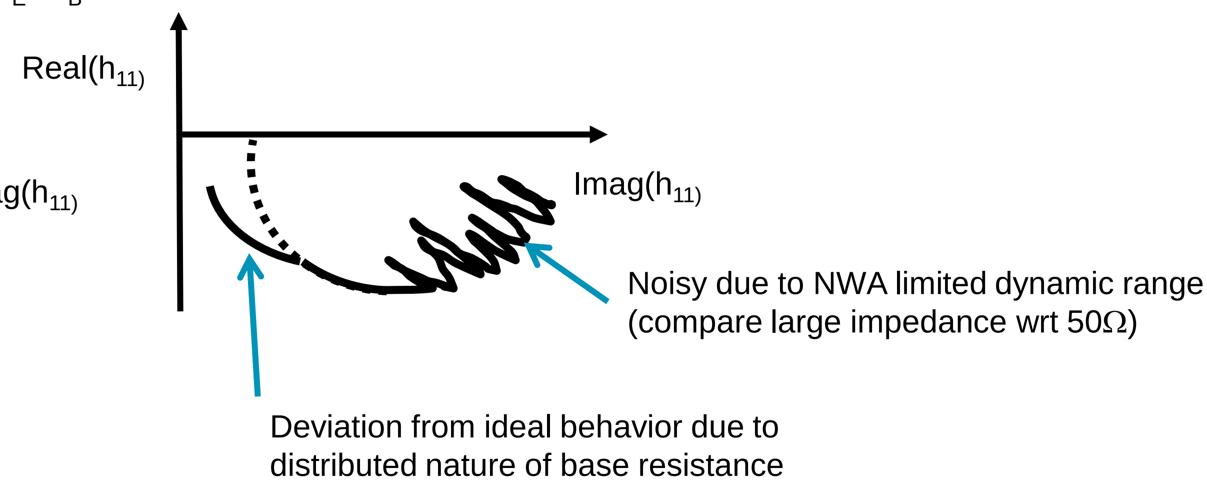
SCALABLE MODEL & PARAMETER EXTRACTION

Some critical model parameters are difficult to extract from HBT measurements:
Example: base resistance extraction from impedance circle method (e.g., [KLOO1999])

Theoretical



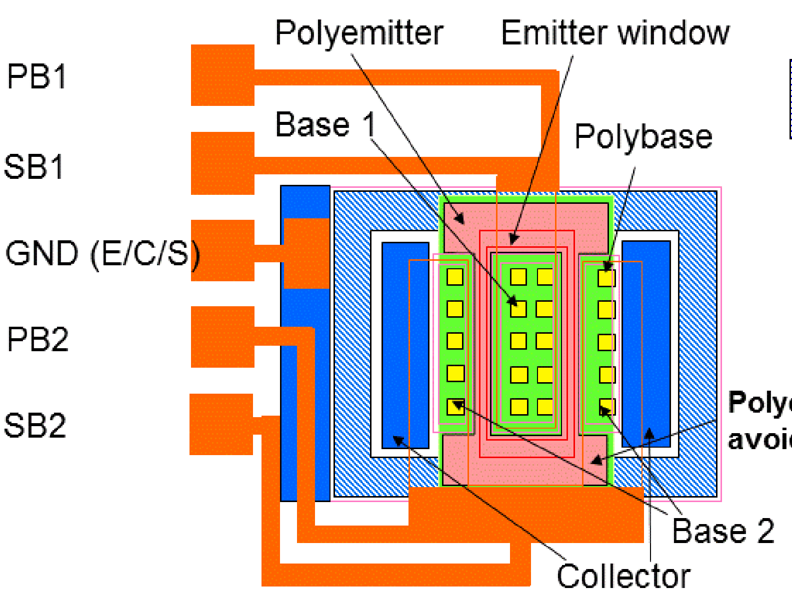
Practical

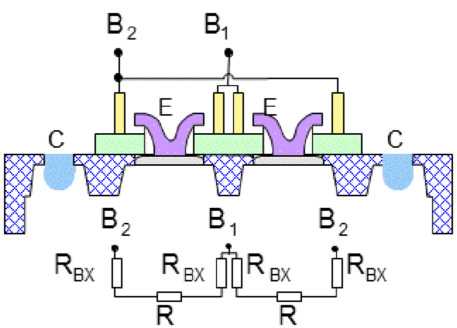


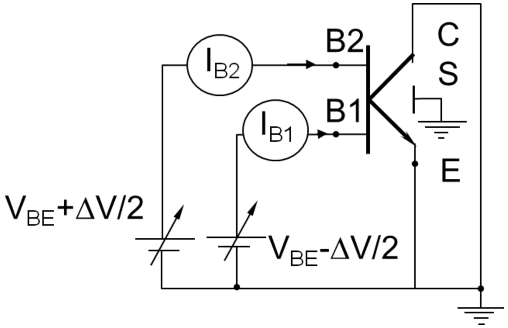
SCALABLE MODEL & PARAMETER EXTRACTION

Use specific test structures for physics based parameter extraction

Example: Tetrodes for base resistance [REIN1991]



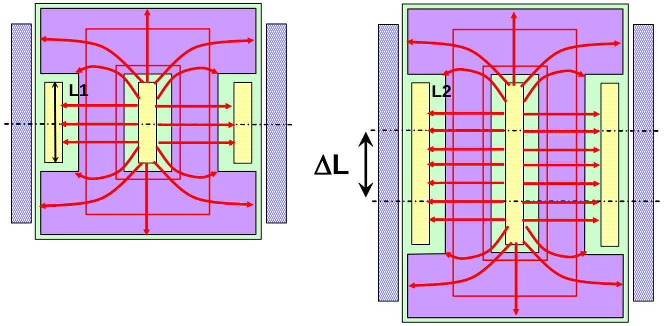


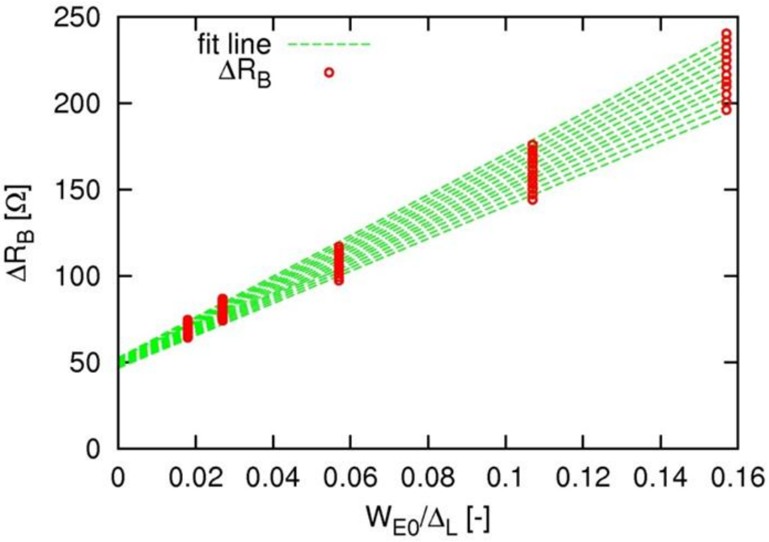


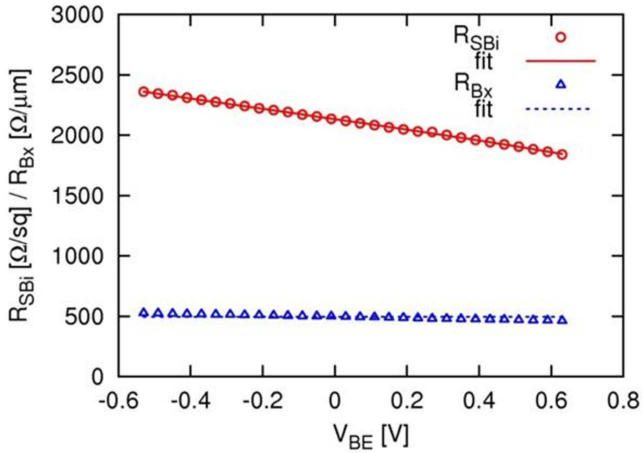
SCALABLE MODEL & PARAMETER EXTRACTION

Use specific test structures for physics based parameter extraction
Example: Tetrodes for base resistance

- Two different length to remove 2D effects
- Several widths to separate intrinsic and extrinsic base resistance from geometry variation







SCALABLE MODEL & PARAMETER EXTRACTION

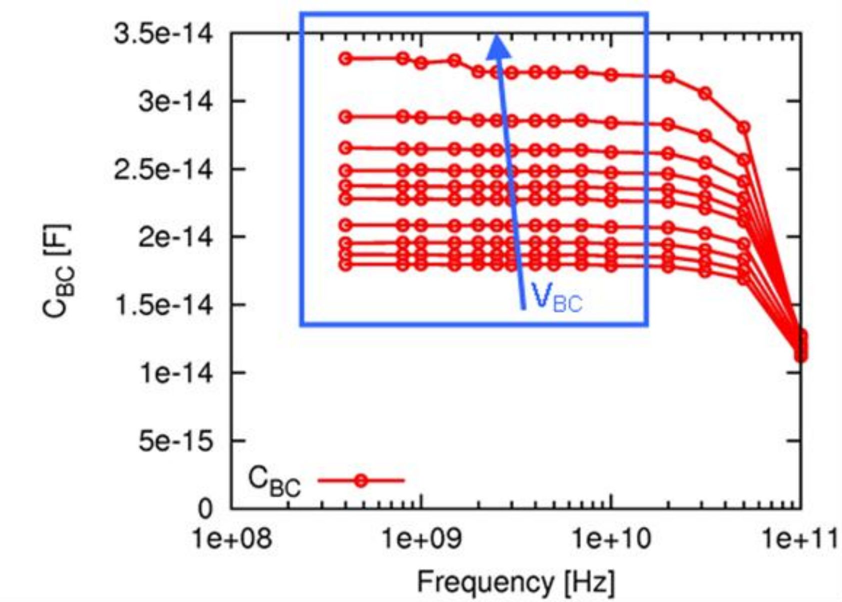
Scalable model principle
Example 1: Junction capacitances

From de-embedded S parameters measurements,
obtain capacitance versus frequency then apply averaging:

$$CBE = \Im \frac{(Y_{11} + Y_{12})}{\omega}$$

$$CBC = -\Im \frac{(Y_{12} + Y_{12})}{2\omega}$$

$$CCS = \Im \frac{(Y_{22} + Y_{12})}{\omega}$$



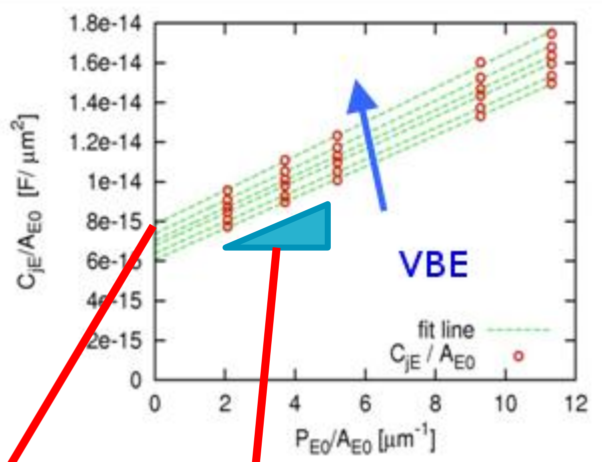
SCALABLE MODEL & PARAMETER EXTRACTION

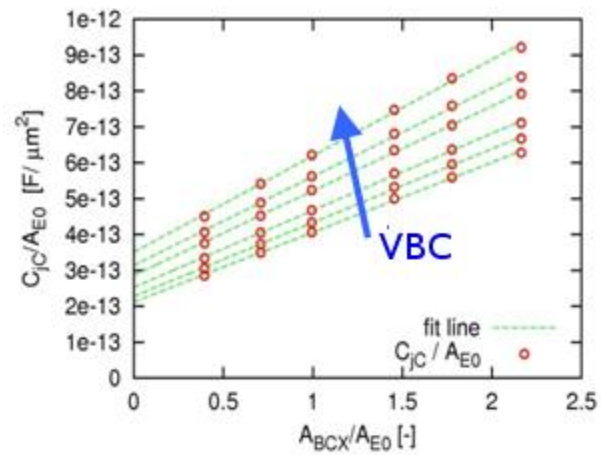
Scalable model principle

Example 1: Junction capacitances

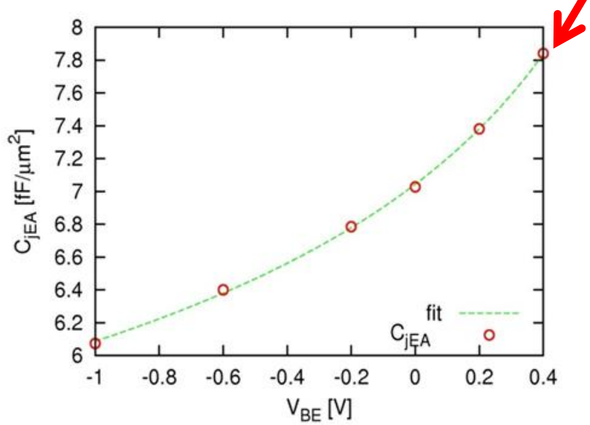
$$C_j = C_{jA}\,A + C_{jP}\,P$$

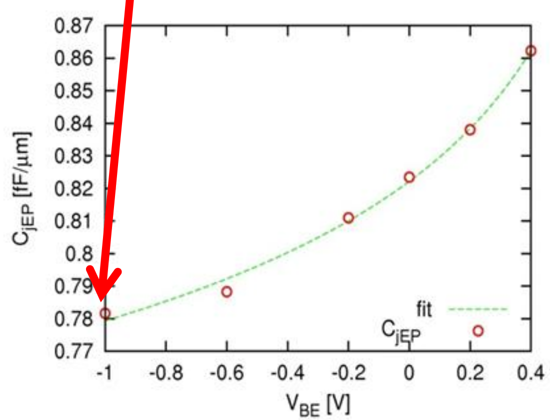
$$\Rightarrow \quad \frac{C_j}{A} = C_{jA} + C_{jP}\,\frac{P}{A}$$





From slope and Y intercept, obtain capacitance components versus bias





2 different physics based sets of parameters (built in voltage, grading coefficient, specific capacitance) each related to well defined doping region

SCALABLE MODEL & PARAMETER EXTRACTION

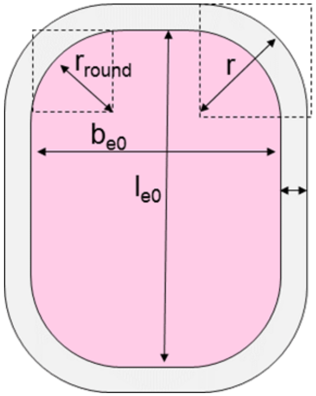
Scalable model principle
Example 2: collector (transfer) current
Different principle:

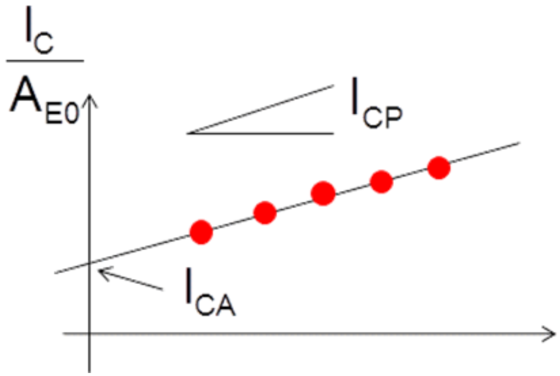
- Similarly extract effective parameters from geometry
- But merge 2 different regions (intrinsic / perimeter) into a single effective area

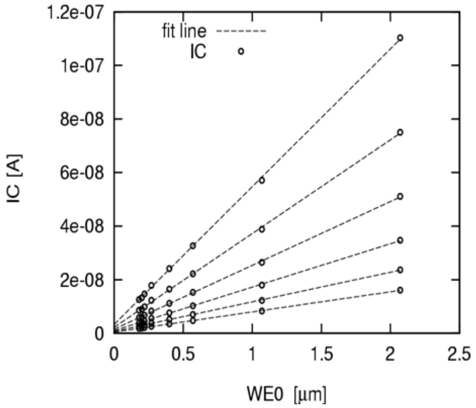
$$I_C = I_{SA} \cdot A_{E0} + I_{CP} \cdot P_{E0} = I_{CA} \cdot A_{Eeff}$$

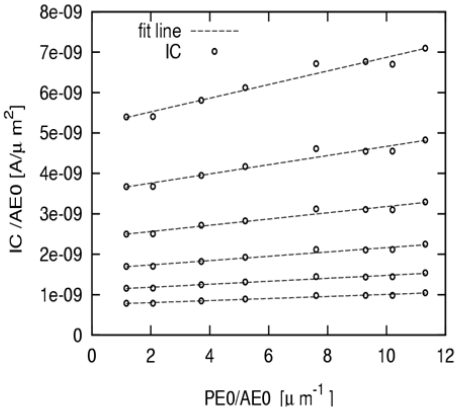
$$A_{Eeff} = A_{E0} + \gamma_C P_{E0}$$

$$\gamma_C = \frac{I_{SP}}{I_{SA}}$$



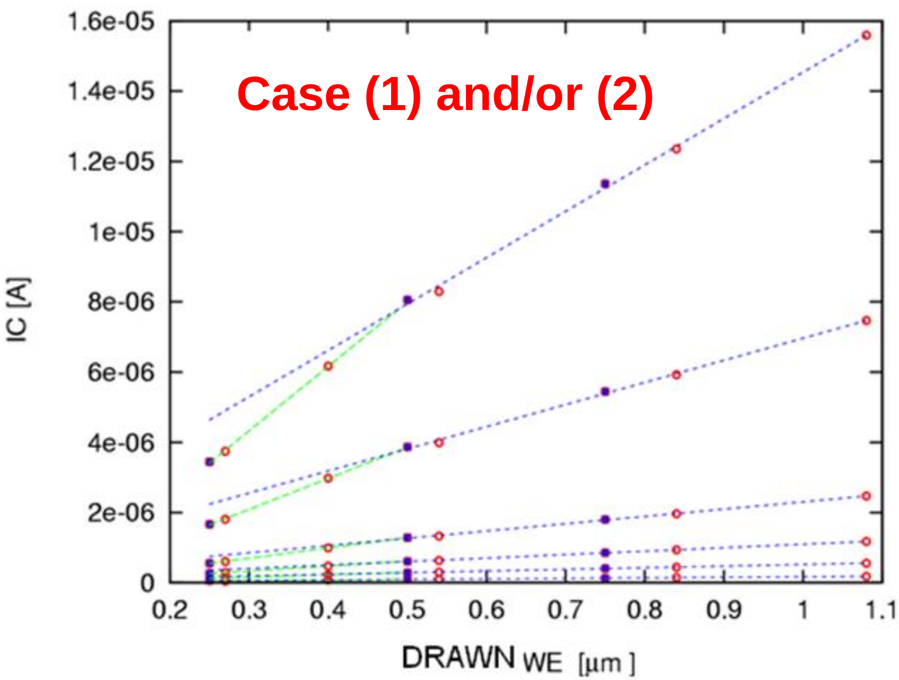






SCALABLE MODEL & PARAMETER EXTRACTION

- Problem occurs when scaling is compromised
  1. Vertical doping (or Ge) profile not constant with geometry
  2. Real (silicon) junction dimension unknown or not following drawn dimensions
  3. De-embedding / test key issue



Observed issue with width scaling:
- If case (1), this is “real” scaling issue not a measurement problem
- If case (2) this is a “false” scaling issue

Difficult to answer without SEM pictures

SCALABLE MODEL & PARAMETER EXTRACTION

- Problem occurs when scaling is compromised
  1. Vertical doping (or Ge) profile not constant with geometry
  2. Real (silicon) junction dimension unknown or not following drawn dimensions
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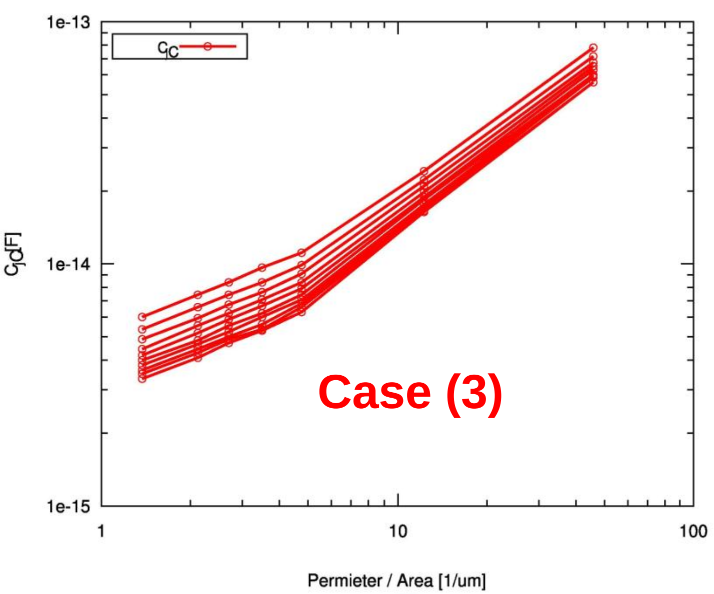
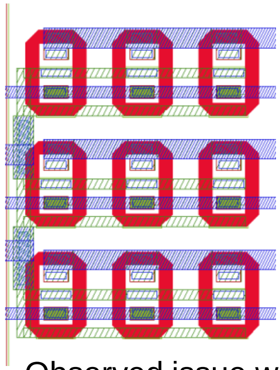
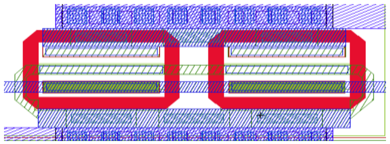


Short transistors (in parallel)



Long transistors (in parallel)



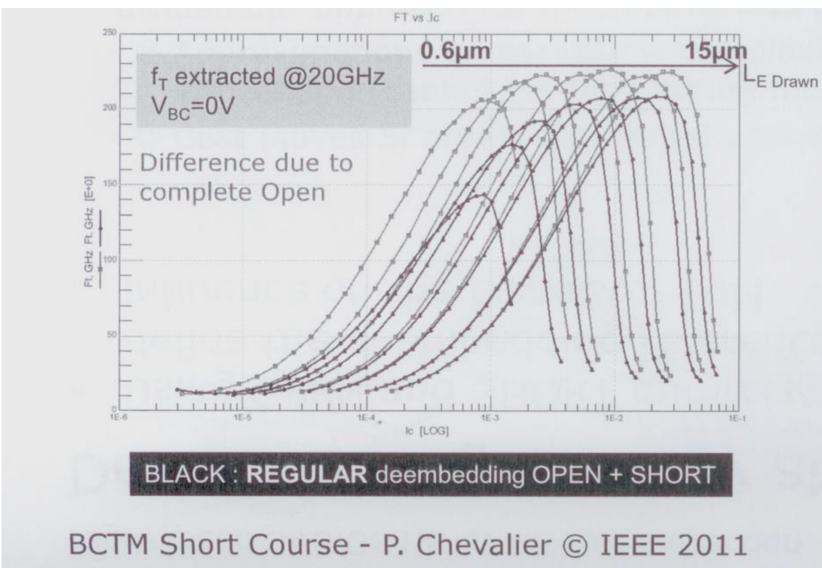
Observed issue with Junction capacitance scaling due to test structure problem and inconsistency with DUMMY OPEN
Backend connection lines (not scalable) are not fully de-embedded

Measurements of short transistor become more **precise** but less **accurate**

SCALABLE MODEL & PARAMETER EXTRACTION

- Problem occurs when scaling is compromised
  1. Vertical doping (or Ge) profile not constant with geometry
  2. Real (silicon) junction dimension unknown or not following drawn dimensions
  3. De-embedding / test key issue

Case (3)



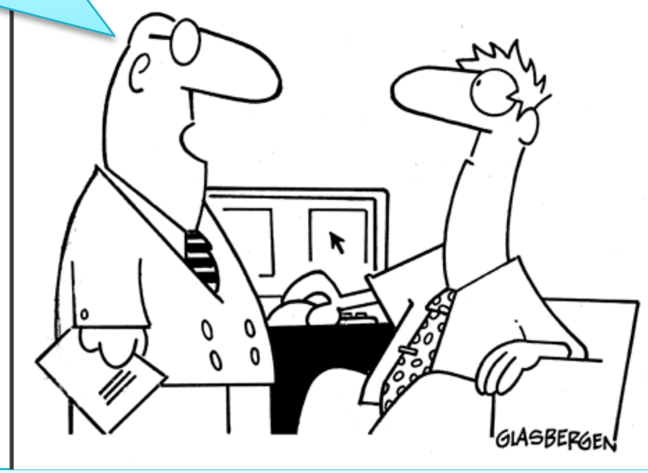
Observed issue due to de-embedding: where to stop de-embedding (M6 or M1?)

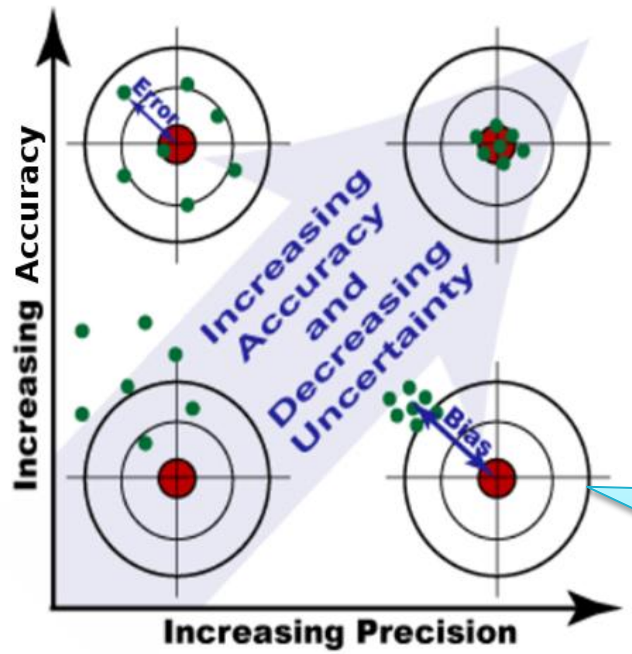
See later paragraph on de-embedding

source N. Derrier , P. Chevalier, ST

MEASUREMENTS

The marketing guys want more of
your over optimistic measurements

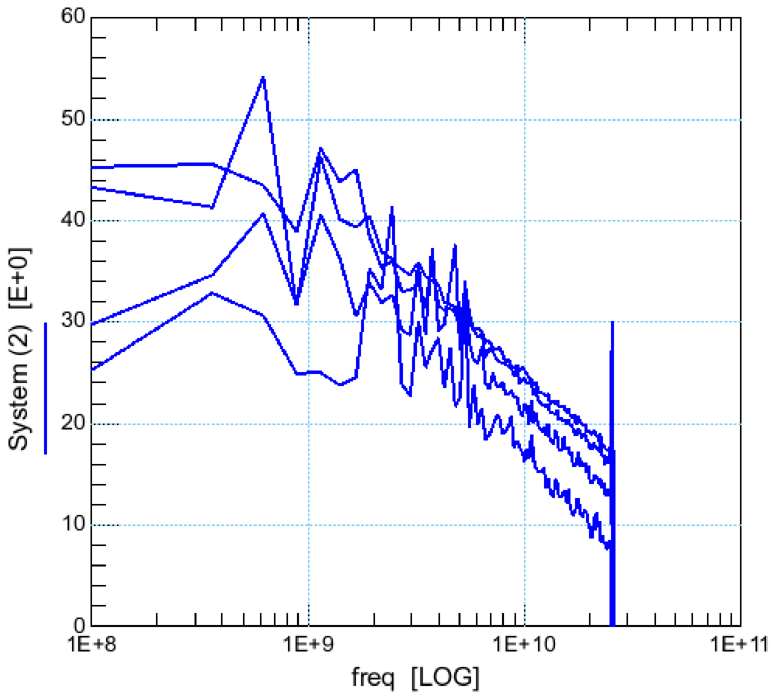




This case is the worst possible case:
Results “look” good but have systematic error
Absence of measurement noise, nice trend and reproducibility can be a misleading Indicator

MEASUREMENTS

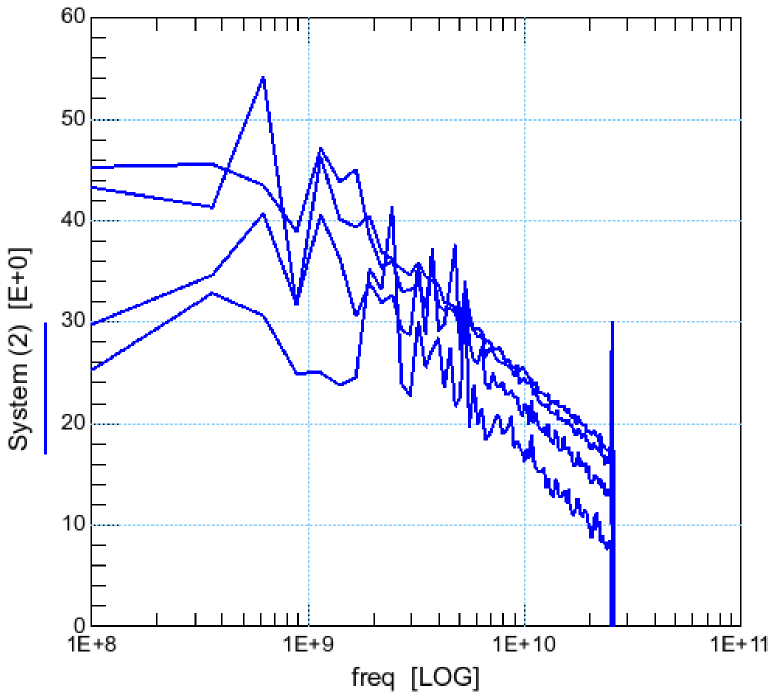
MASON's Gain Measurement: can be quite Noisy !

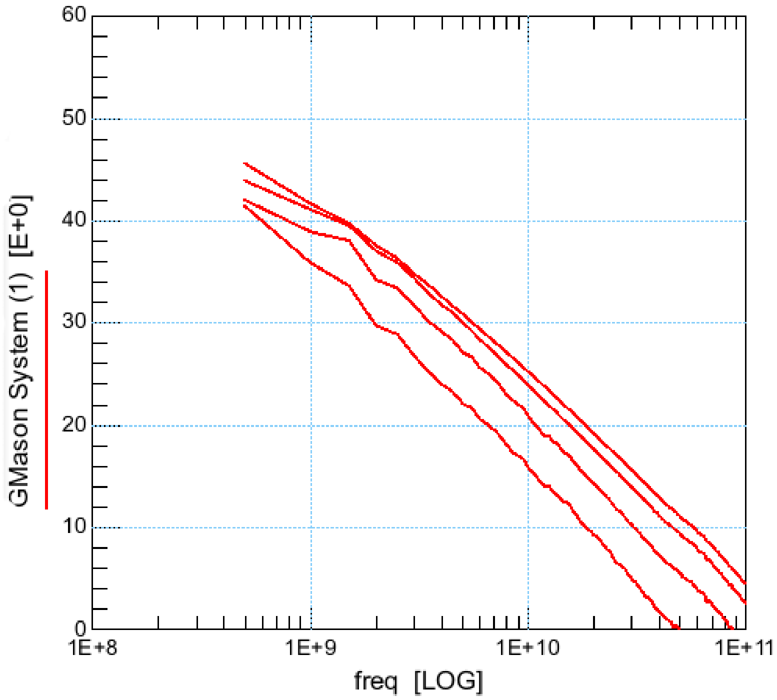


MEASUREMENTS

MASON's Gain measurement on another test bench: looks much better !

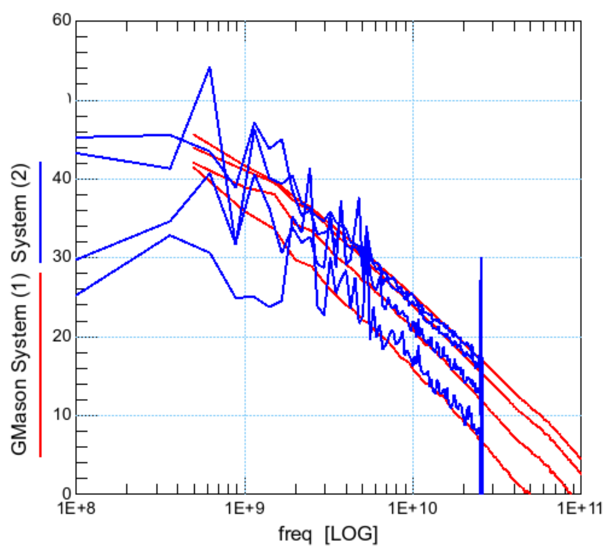
IN YOUR OPINION WHICH ONE IS BETTER ?

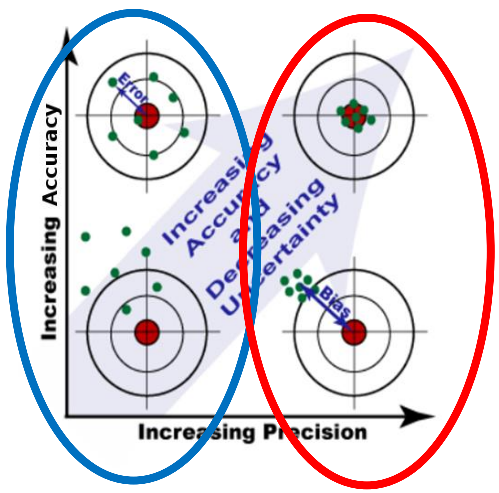




MEASUREMENTS

When Averaged, Both Give Same Result : They have same accuracy





Red: precise
Blue: not precise
When averaged,
both give same result but:
Can't conclude on
ACCURACY

Absence of measurement noise, nice trend and reproducibility can be a misleading Indicator

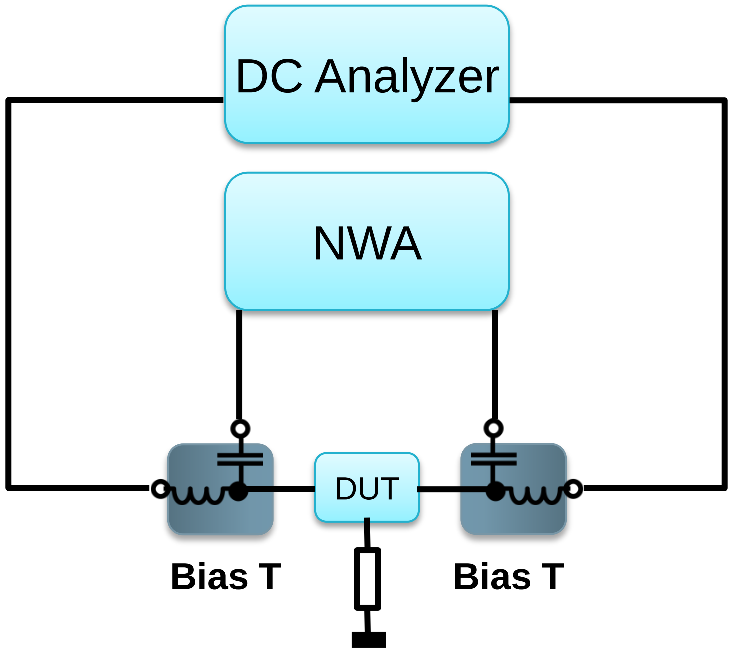
"ACCURACY" mostly depends on:

- Calibration (Type, Standards, environment, etc.)
- De-embedding quality & strategy (up to where do we de-embed?)
- Test key design (mostly consistency between device & Dummies)

Nothing straight forward to verify

MEASUREMENTS

Even DC measurements are not straight forward



DC path is usually longer, with more series resistance due to bias Tees

Ground return path has to be considered too

J_C @ peak f_T ~ 10mA/µm²
A_E = 0.2 x 10 µm²
I_C ~ 20 mA @ peak f_T

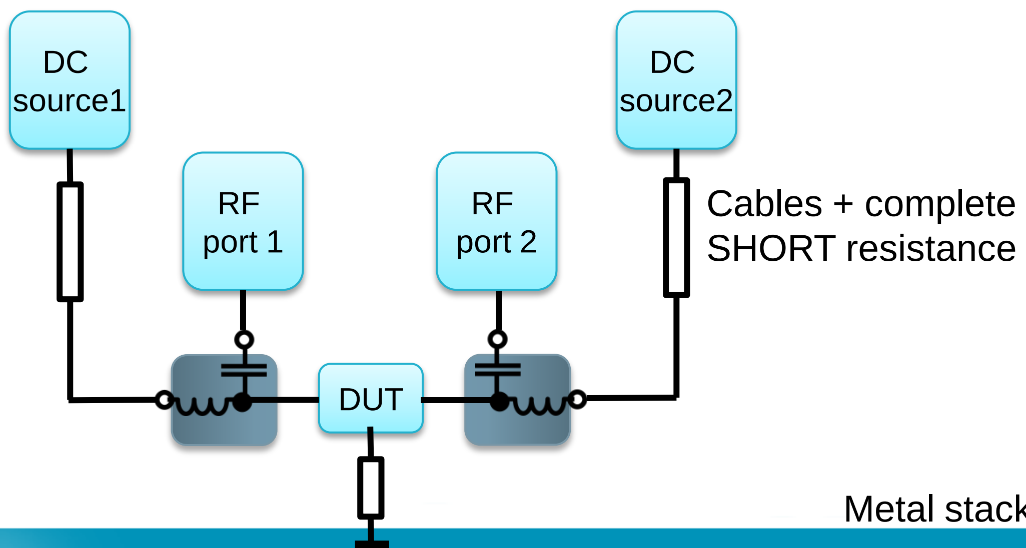
Consider 1Ω additional series resistance in the emitter DC path
ΔV ~ 20 mV

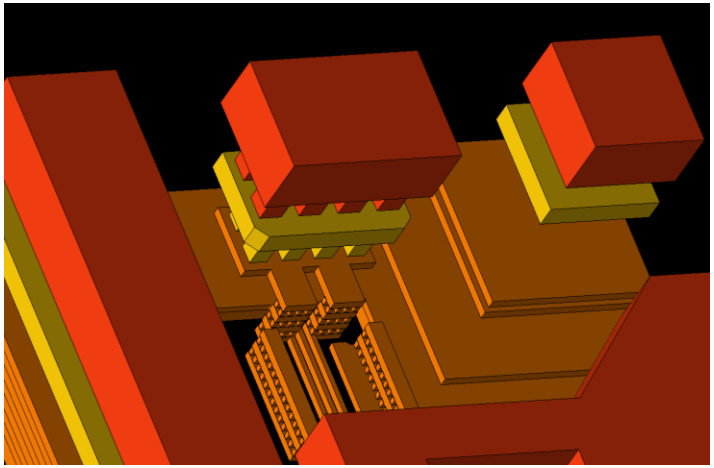
I_C has exponential dependence on V_{BE}:
exp(-20mV / V_T) ~ factor 1/2 @ room temperature

MEASUREMENTS

Even DC measurements Are Not Straight Forward

- Cables, access lines and vias series resistance down to the DUT (on chip) in the DC path need to be considered
- They are removed from AC path by calibration but are unavoidable in DC
- The only solution is to modify the simulation set up (for model / measurement comparisons) in order to emulate bias tees.
- Need to measure the complete SHORT dummy in DC!



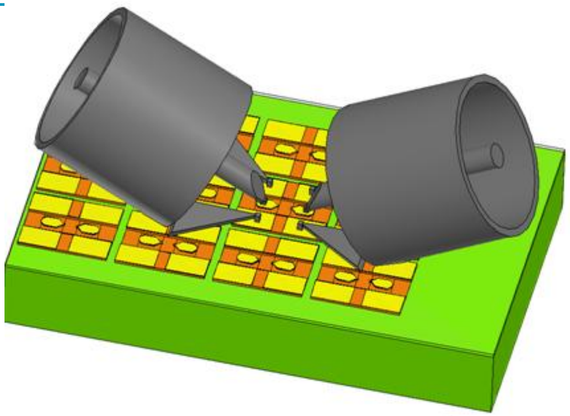


Metal stack down to transistor adds series resistance

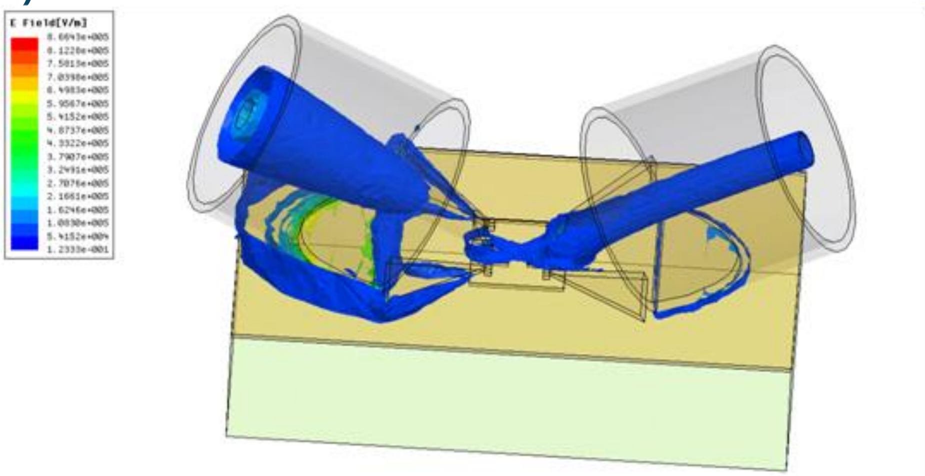
MEASUREMENTS

- Probe bottom coupling with material underneath

- Environment below the probes matters
- Impact of test structures surrounding
- Impact on calibration (Calibration on ISS / Measurement on Silicon Wafer)

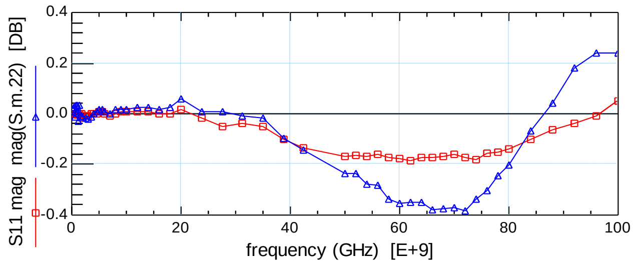


On-Wafer Calibration [MANG2006]
[DERR2012] (or similar) required
at high frequency
or
Ground plane on ISS ?



MEASUREMENTS

- Probe bottom coupling with material underneath



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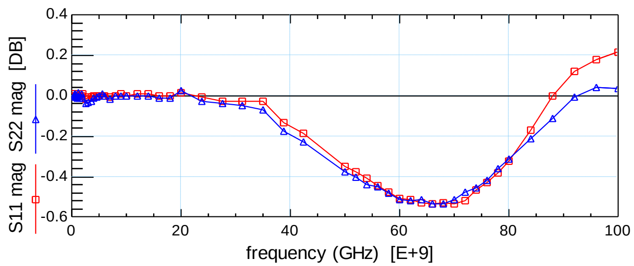

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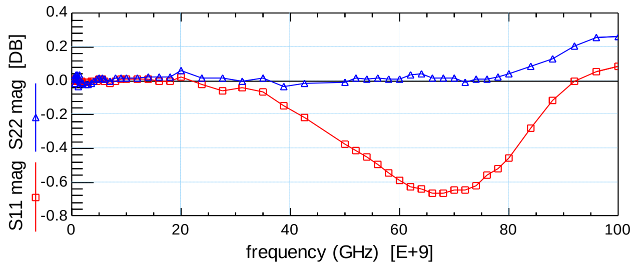

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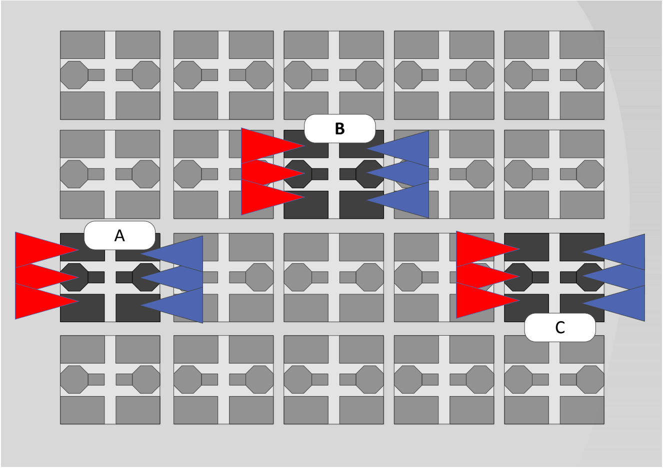
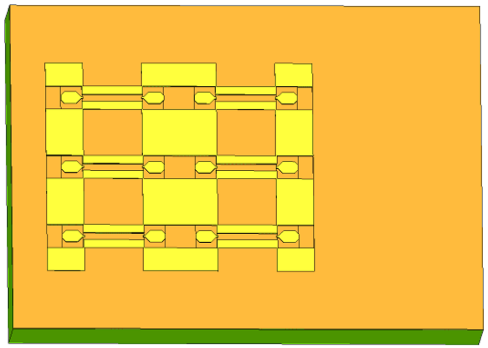


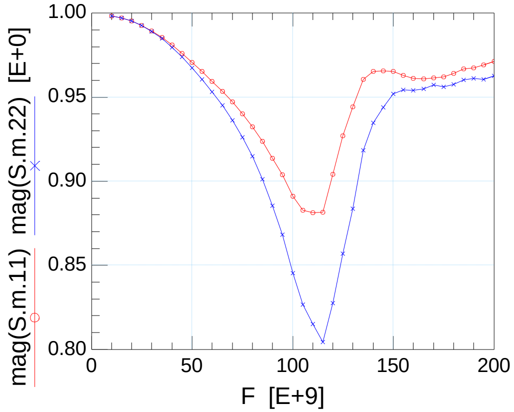
3 identical OPEN DUMMIES => SYMETRICAL STRUCTURE
S_{11} and S_{22} differ depending on position (i.e. depending on surrounding environment)

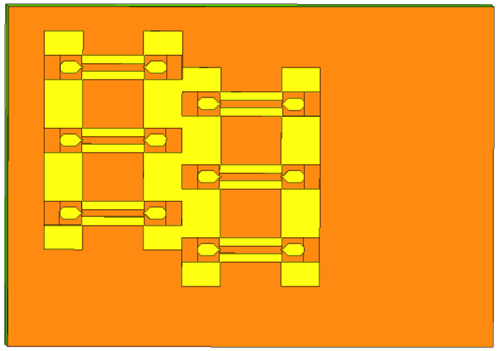
- Ground plane everywhere or/and
- Interleaved structures or/and
- Ground plane extension below the probes or/and
- Don’t put critical structures close to chip edge

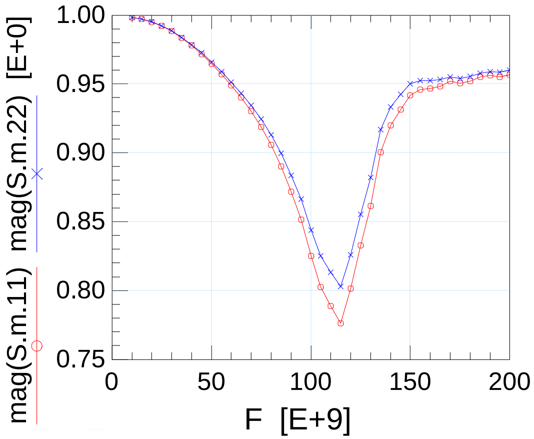
MEASUREMENTS

- Probe bottom coupling with material underneath









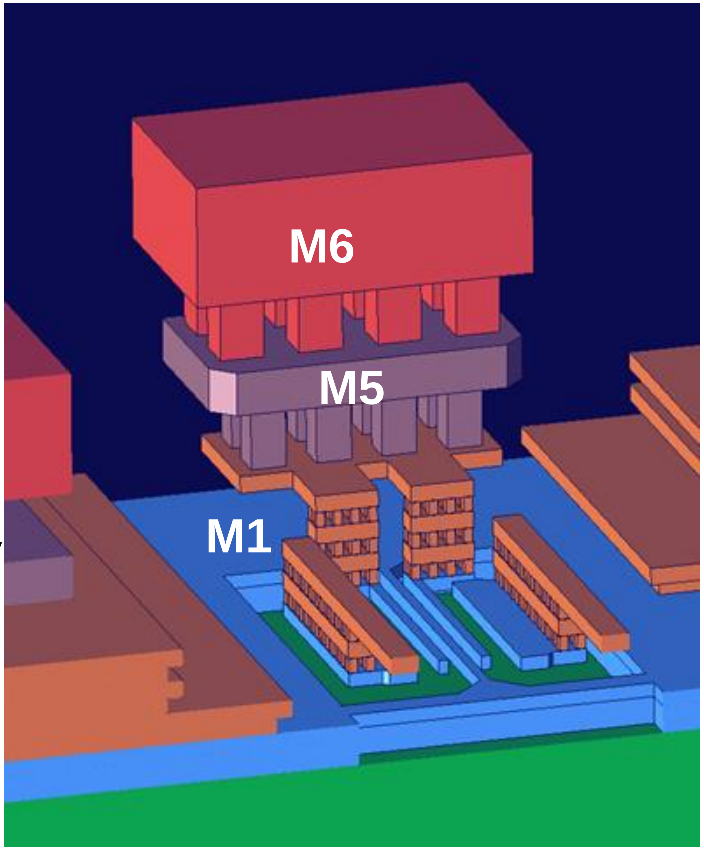
- Ground plane everywhere or/and
- Interleaved structures or/and
- Ground plane extension below the probes or/and

- Don't put critical structures close to chip edge

MEASUREMENTS

- De-embedding
  - De-embeding up to M6 (“regular” Open)
  - De-embedding up to M2 (ITRS compliant)
  - De-embedding up to M1

- Implications for OPEN/SHORT dummies
  - Complete OPEN/SHORT are more accurate but have more distributed effects
  - Distributed dummies modeled by lumped elements lead to unphysical de-embedding @ high frequency
  - Need Multi-Steps de-embedding (use after Pad & top metal de-embedding)
  - Or (better) Scalable de-embedding (need shielding to prevent substrate coupling)



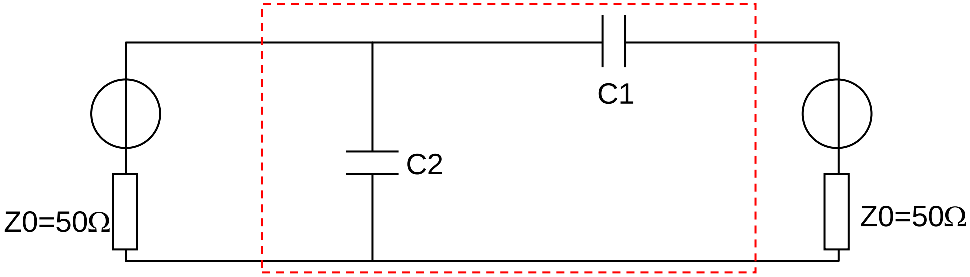
Optimized structure for minimum parasitics

MEASUREMENTS

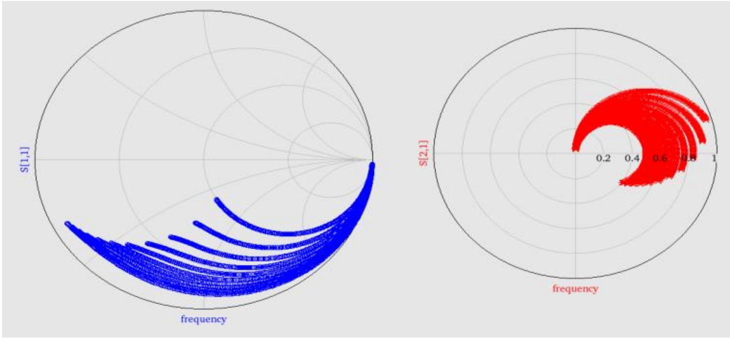
- De-embedding verification is difficult due to lack of known reference
- All papers on de-embedding show different methods comparisons and physical trend analysis
- Would be better to use simulations (EM)
- But indeed, active devices can’t be simulated with EM simulators
- New paradigm: find a suitable reference
  - Passive device (can be simulated with EM simulator)
  - Behavior not too far from transistors so that S parameters are in the same range of magnitude and phase (so that conclusions can be transposed to transistors)
  - Behavior is reasonably predictable from low frequency measurements
  - Behavior does not depend on critical fabrication steps (good matching / reproducibility)
- This is the idea behind the virtual load
  - Simulate the reference embedded in pads & access lines, simulate de-embedding dummies, apply de-embedding on simulations then compare with reference simulation alone: observed error gives the accuracy of de-embedding method

MEASUREMENTS

- Virtual LOAD: original idea

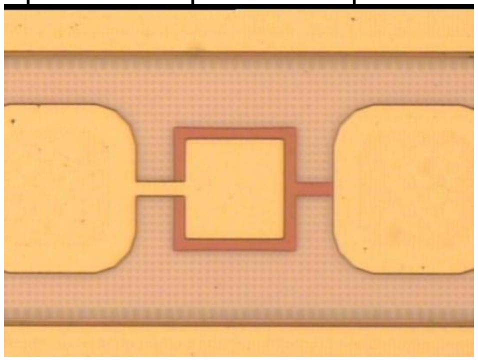


S parameters of the virtual load simulated with different C1/C2 ratios

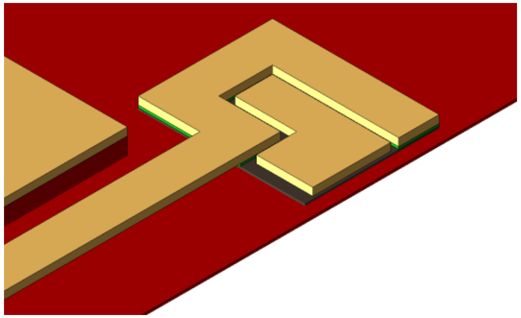


S11 pretty much similar to S11/S22 of transistors
S21 has same trend as S12 of transistors

The virtual load is a metal plate capacitor C1. Bottom plate has a parasitic capacitance C2



Improved virtual load (half structure) to allow access on both sides with top metal



MEASUREMENTS

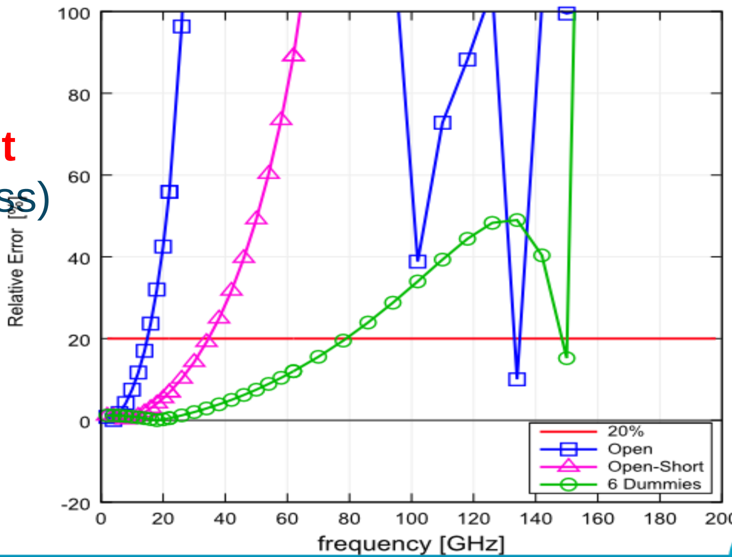
- 3D FEM EM simulations of virtual load with pads
- 3D FEM EM simulations of de-embedding dummies (OPEN, SHORT, LINE)
- 3D FEM EM simulations of virtual load (w/o pads)
- Apply different de-embedding methods to the simulations and compare results with simulations of the intrinsic device
- Error between de-embedded device with respect to reference is shown for simple OPEN, OPEN / SHORT and “6 dummies” de-embedding methods

[RAYA2013]

CONCLUSIONS are backend & layout dependent

- The shown results are not DOT7 (under-progress)

- Simple OPEN valid up 15GHz
- OPEN/SHORT valid up to 40GHz
- “6 dummies” valid up to 80GHz



TEST KEY DESIGN

Models refer to what is measured on the test chip :
Designers may not use exactly the same layout

Metal Routing:

- If de-embedding only up to M6: issue since transistor model contains M1-M5 capacitances, even if transistor is routed in M1 only
- If de-embedding up to M2/M1: routing parasitics accounted for by parasitic extractors (but what is the accuracy at mmWave frequencies in the presence of complex 3D EM effects? How to verify model accuracy for modeling engineers? If discrepancy is found what is root cause (model or parasitic extractor?) Initial schematic simulations too far from real performance? Inflation of modeling flags, i.e., inflation of model validation needs !

Layout of test keys can’t be dissociated from De-embedding strategy !
(Need strong cooperation of modeling team, PDK team, Measurement team, …)

TEST KEY DESIGN

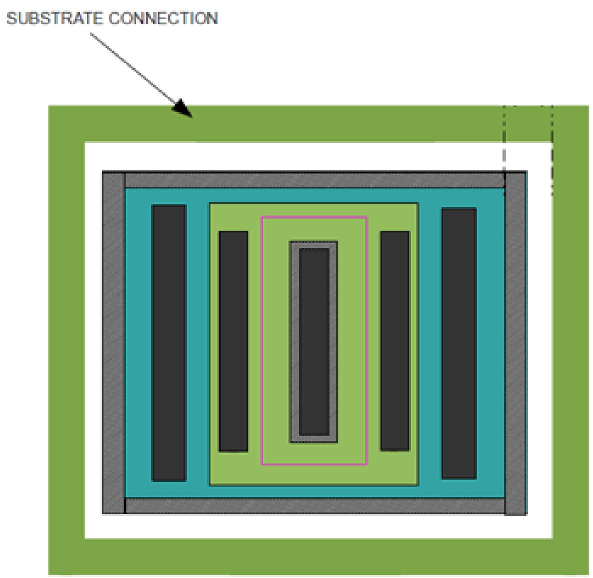
Models refer to what is measured on the test chip :

Designers may not use exactly the same layout

Substrate ring:

- HBT Test structures usually have a substrate ring
- Designers need more flexibility so that Pcells have no substrate ring (or optional substrate ring)
- Problem: intra / inter device substrate coupling is critical a mmWave frequencies
- Substrate coupling is a complex 3D problem not taken into account by post layout extraction tools

See later in circuit design section



DESIGN / MODELING TARGET

Designers don’t have same target as modeling engineers:

- Modeling engineers want consistent comparisons between measurements & models
- Designers want working circuit with best possible performance

DESIGN / MODELING TARGET

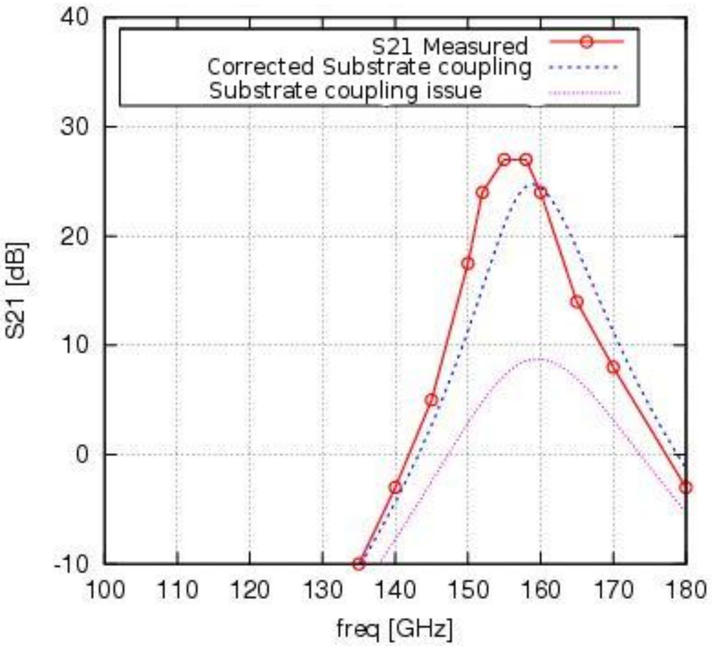
Circuit example :

- Initial Model /measurement discrepancy of 7dB
- Bias offset in measurement setup not in simulation + simulation issue due to S-parameters block revealed problem was even worse (17dB)
- After a lot of work, problem could be tracked down to substrate coupling issues

- Errors can compensate each others
- Extremely difficult to debug
- Questions remains for this circuit example:
  - Passive devices, integrated transformer, process generation i+1, input/ouput baluns, bias adjustment, simulator issues, substrate connections, process variations, other layout specific issues

Corrective action needed in verification methodology !

160 GHz 3 stage differential LNA, with integrated baluns (Ullrich Pfeiffer et al, DOT5)



PROPOSED VALIDATION METHOD

Many possible issues in the complex task of modeling:

- Measurement / de-embedding / Test structure design
- Model limitations (race between model development & technology)
- Parameter extraction errors / Scaling issues

Final validation step is a must !

Validation on circuits (done by design teams) is difficult (even simple circuits)

- Measurability (Multi-stage, differential, variability, biasing, frequency band, …)
- Dependence on other devices (passives, transmission lines, baluns, transformers)
- Custom layout (variations from Pcells, specific T lines, in house EM simulations, ground planes continuity, …)
- Etc.

PROPOSED VALIDATION METHOD

Need specific circuits for sub-THz & mmWave model validation:

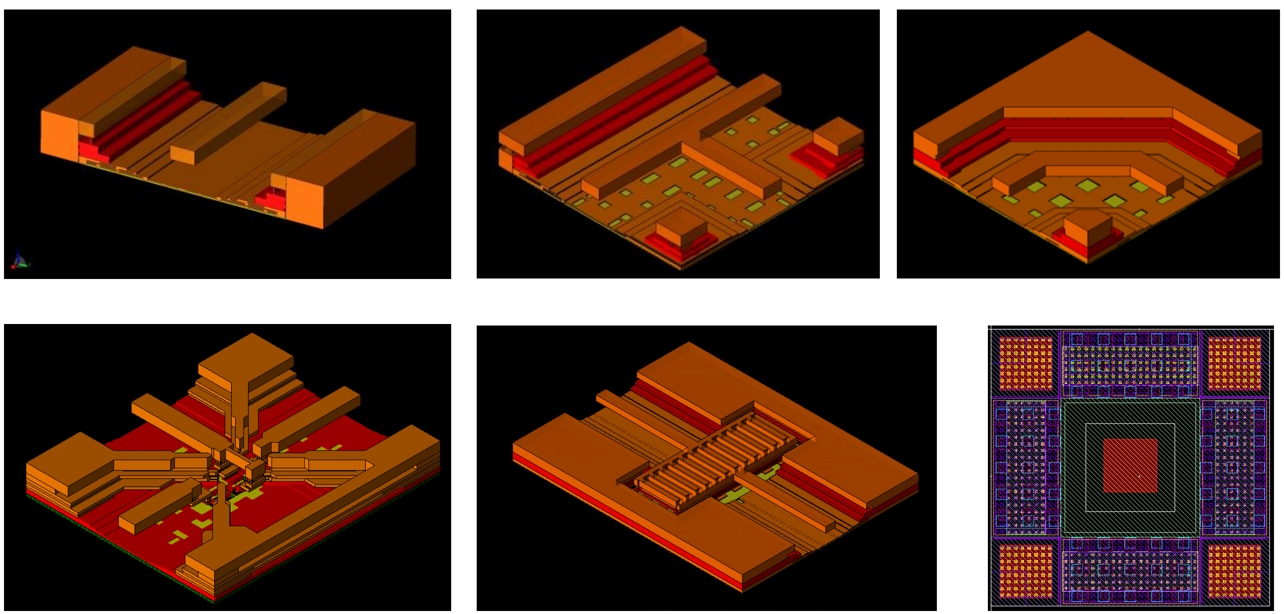
- Designed by modeling team (need to know circuit details)
- Simple circuit blocks, tailored for measurability
- Sensitive to the model to be verified (e.g. HBTs)
- Hierarchy of circuits (Small signal / noise, large signal, highly non linear)
- Extra components (passives, Tlines, etc.) need to be well known (EM simulations) or have limited impact
- HBT samples (of exactly similar layout than the one used in the circuit) available on the SAME wafer to be re-measured & re-modeled

This is the required condition to make fair comparisons

- Requires measurements and modeling skills
- Requires Design skills
- Requires EM simulation skills

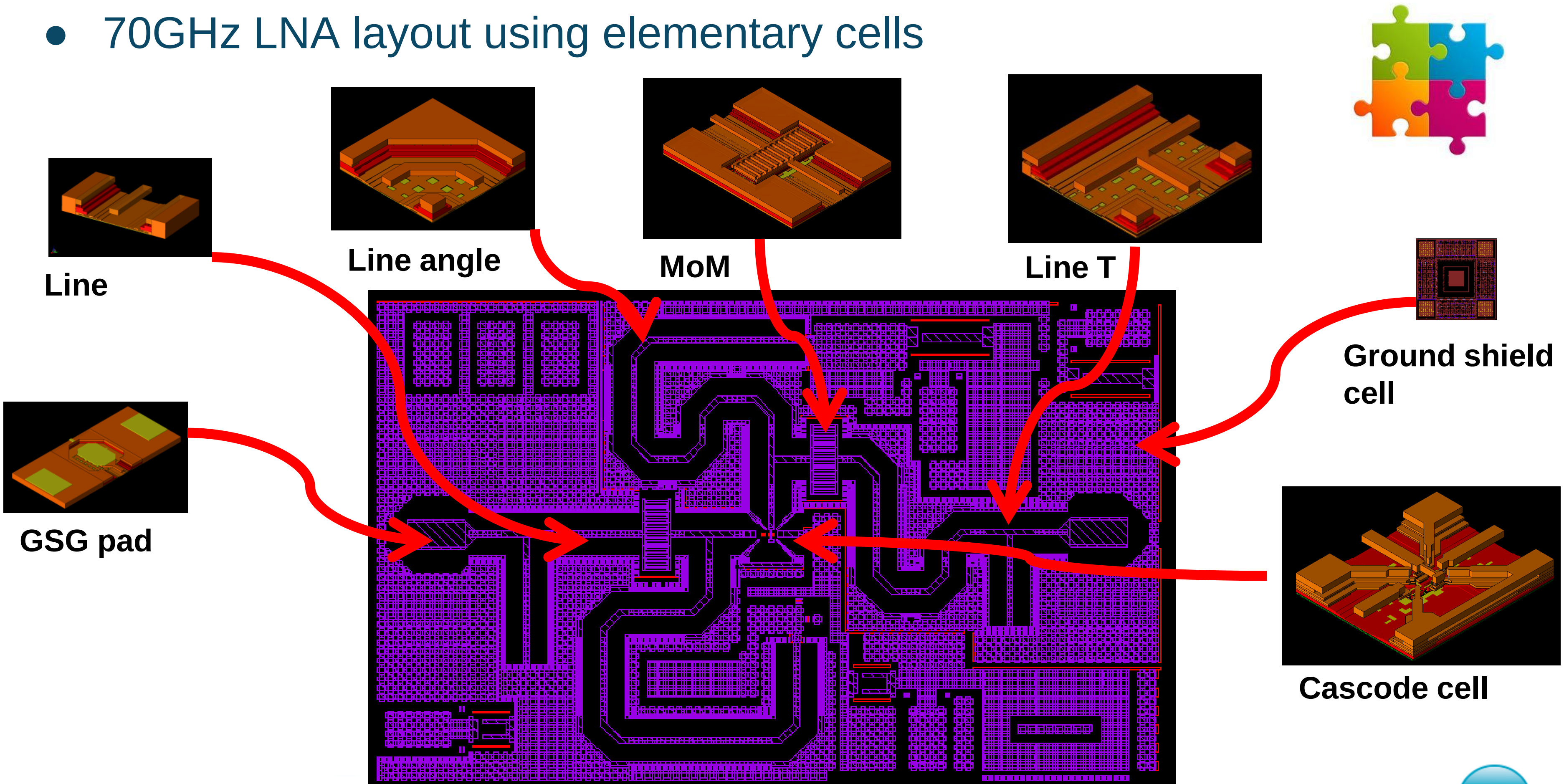
PROPOSED VALIDATION METHOD

- Example of ongoing work: Circuit blocks based on “puzzle parts”
  - Each part is (metal) density compliant : don’t use automatic filling / cheesing
  - Each part is simulated with EM simulator (3D generated from automatic scripting from GDSII) and available as single element on chip
  - Use ground shield everywhere to avoid substrate coupling and differences wrt measured test structures



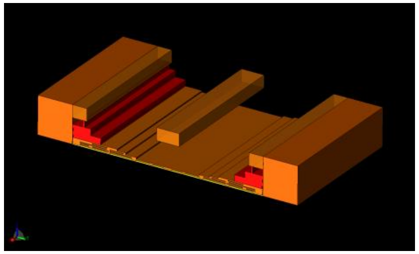
PROPOSED VALIDATION METHOD

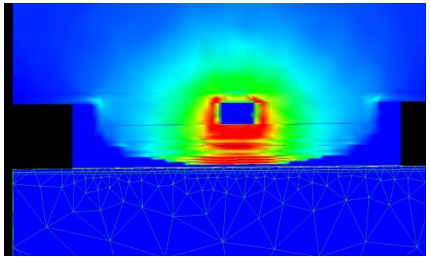
- 70GHz LNA layout using elementary cells

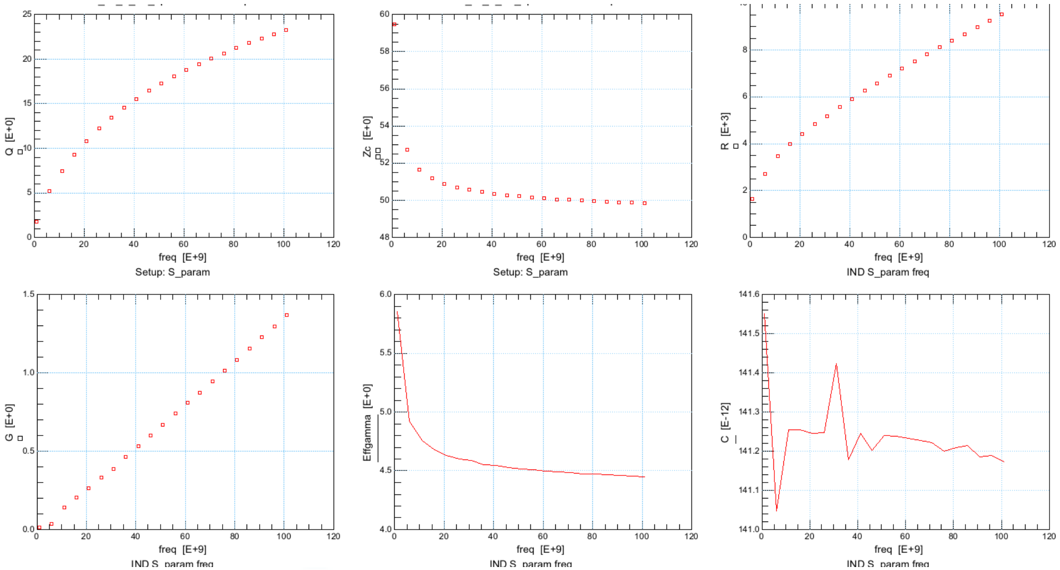


PROPOSED VALIDATION METHOD

- Transmission line work



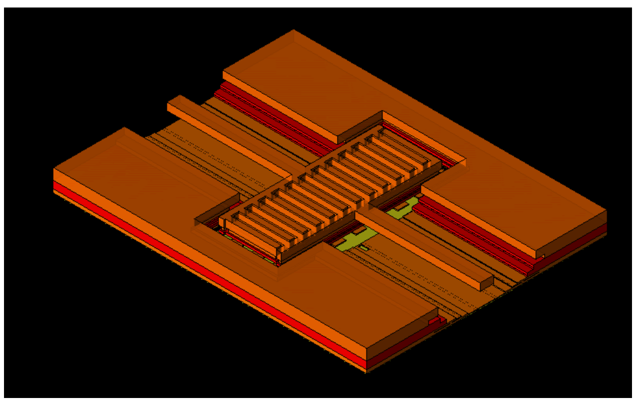


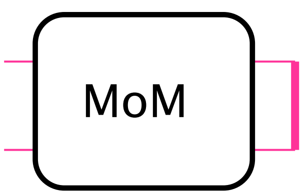


- Optimized design to avoid metal holes in the “visible” return path of the ground shield (EM simulation closer to reality)
- EM simulation of small length
- Compact model from EM simulation
- Measure single structure on chip within HF pads (and de-embedding structures)
- Re-calibrate EM simulator for next run

PROPOSED VALIDATION METHOD

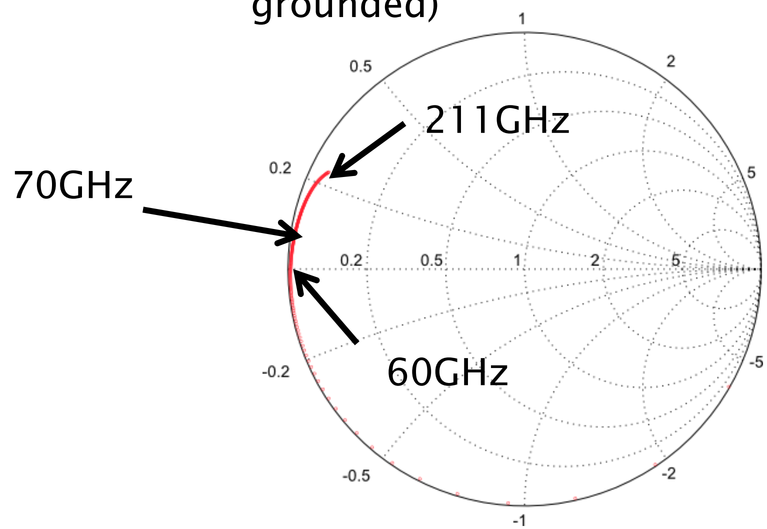
- MoM capacitor work
  - Short circuit around 60GHz
  - Input/output have same cross section than the T line





“Elephant” size margins to make sure the passives won’t play a negative role in the verification process

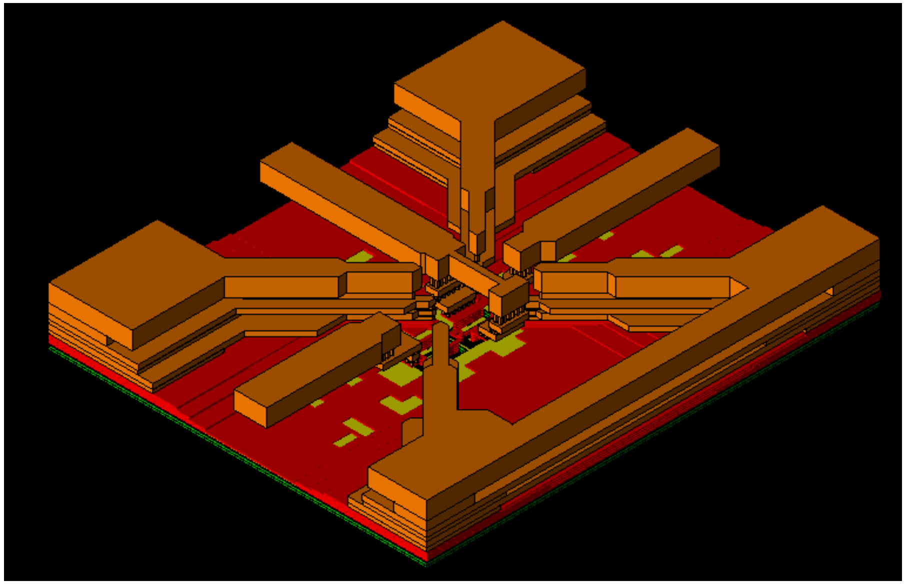
S11_1port (Port 2 is grounded)

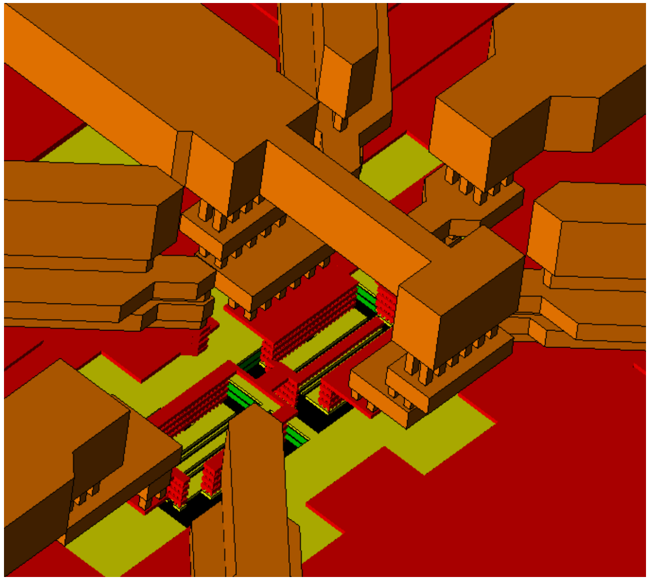


PROPOSED VALIDATION METHOD

- MoM capacitor work
  - Cascode backend simulation up to 210 GHz
  - Input/output have same cross section as the transmission line
  - Result is multi-port S parameter block to be inserted in the simulation

Do not rely of parasitic extractor





CONCLUSION

- Many sources of model inaccuracy are difficult to identify
- Thorough modeling work may not be enough
- Need modeling specific circuit blocks for validation at Sub-THz and mmWave frequencies
- Proposed methodology to design those necessary circuit blocks
  - Obtain sensitivity with respect to the device / model to validate and reduce sensitivity to other devices
  - Reduce mismatch between design environment and modeling environment (layout differences, simulation tools, process variations, …)
  - Design choices allow splitting the verification problem into smaller independent problems
- This work is on-going: still a lot of lessons to learn
- Verification work to be done
- Add new circuit blocks (increase frequency, add mixers, oscillators, …)
- Add circuits with specifications closer to real designs

AKNOWLEDGEMENT

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