

CATRENE – CT209 – RF2THZ SiSOC

Application Scenarios from RF2THzSiSoC

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Outline

- ☐ Demonstrators in RF2THZSiSoC - Goal Setting and Work Procedure; Summary
- ☐ Application Scenario 1: Fast Converters f. Optical Communication and Test & Measurement (Demo1)
- ☐ Application Scenario 2: Mobile Communication – Photonic Radio Transmitter (Demo 2)
- ☐ Wideband 240GHz Imaging System With Excellent Spatial Resolution
- ☐ 2-way Satellite Terminal for Consumer Application
- ☐ Application Scenario 3:
79 GHz and 120 GHz Radar Sensor Components and 120 GHz Radar System With Improved Angular Resolution
- ☐ Acknowledgement

Goal Setting and Project Work Procedure

❑ **Define, design, characterize demonstrators which demonstrate state and superior performance of the developed SiGe BiCMOS technologies**

❑ **Ambitious Future Applications from ...**

- ... Measurement: Agilent (Demo1b), Synview (Demo3a)
- ... Telecommunication: Alcatel-Lucent (Demo1a, Demo2)
- ... Consumer Market/Satellite Communication: NEWTEC (Demo4)
- ... Automotive and Industrial: Bosch (Demo3b, Demo5)

❑ **Project Work Procedure**

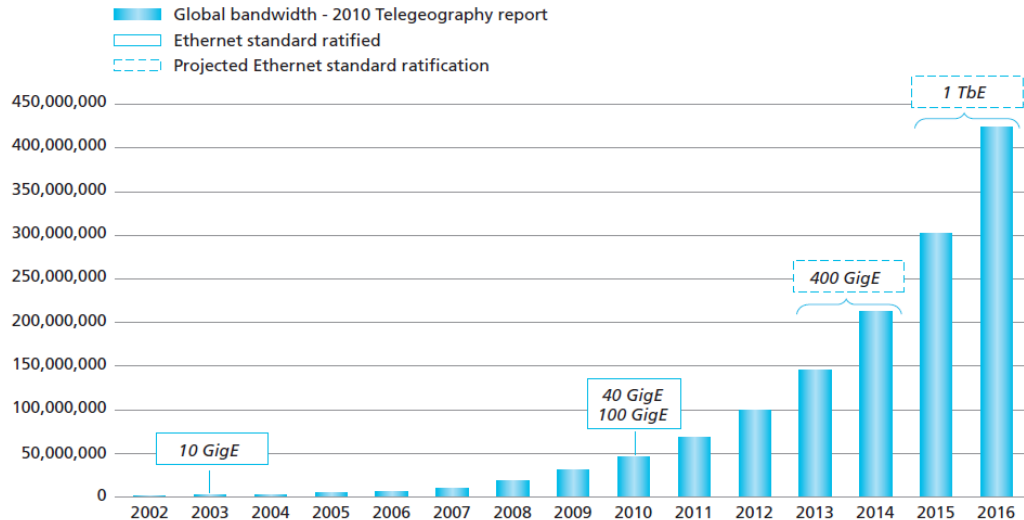
- System level requirements -> concept / architecture definition and specification
- Definition and design of test structure circuitry ("Phase 1"), based on preliminary design kit and models
- Chip-level tests, measurements, and characterization (after first Si available)
- Design of demo circuit considering experiences from preceding step ("Phase 2"), based on more mature design kit and device models
- Chip level test and measurement
- System integration and system level characterization and tests

The Demonstrators

- ❑ **Demo1: Fast Converters** (Alcatel-Lucent, Agilent, Micram, Univ. of Saarland)
 - Demo1a: Fast Converters for 400Gb/s Optical Transmission Systems
 - Demo1b: Fast Converters for AWG Measurement Systems
- ❑ **Demo2: Photonic RF Transmitter for 4G BTS** (Alcatel-Lucent, IHP, TU-Berlin)
- ❑ **Demo3: 240GHz and 120GHz Sensor Platforms** (Synview, Silicon Radar, Bosch)
 - Demo3a: 240GHz wideband imaging system with high spatial resolution
 - Demo3b: 120GHz radar system for sensing applications
- ❑ **Demo4: Two-way satellite Communication for Consumer Application**
(Bruco, ESIEE, ENSICAEN, MASER; NEWTEC, NXP, SALLAND, TU Delft, TU Eindhoven)
- ❑ **Demo5: Application of Radar Sensor Components for 79GHz and 120GHz**
(Bosch, ASTUS, TU-Delft)
 - Demo5a: swept signal source
 - Demo5b: digitally controlled phased TX array
 - Demo5c: all-digital FMCW receiver
 - Demo5d: wideband RX downconverter for wireless sensing

Demo1 Exploitation: Data Traffic Growth

□ Yearly growth of telecommunication core and access networks >40%



*Machine-generated application data is expected to grow at least **50 percent** a year for the next several years (Forrester Research, 2011)*

- *Cloud represents only **11 percent** of data center traffic today. That number will **grow to 34 percent** by 2015.*
- *Overall cloud traffic is set to grow from **130 Exabytes** today to **1.6 Zettabytes** in 2015.*

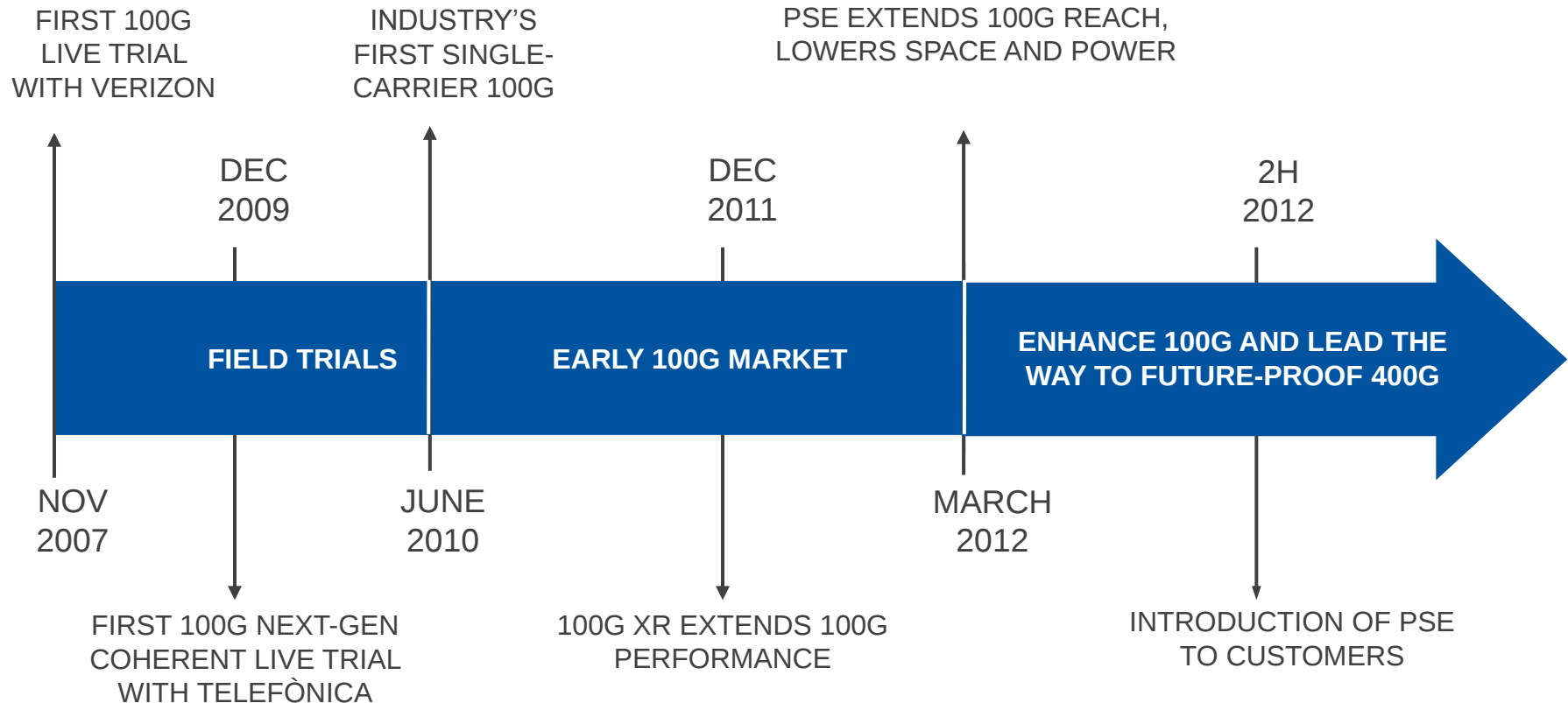


"Facebook Sees Need for Terabit Ethernet"

*"Facebook's data centers already need 100-Gigabit Ethernet and ideally could use 1-Terabit Ethernet, according to a senior network engineer at the company. ... servers can process data so fast, that they could fill **64 Terabit Ethernet pipes in the backbone of one data center...**" PC World, Feb. 2nd, 2010)*

Demo1 Exploitation: THE ERA OF 100G AND BEYOND

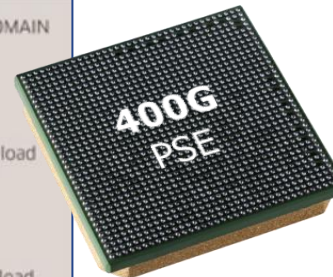
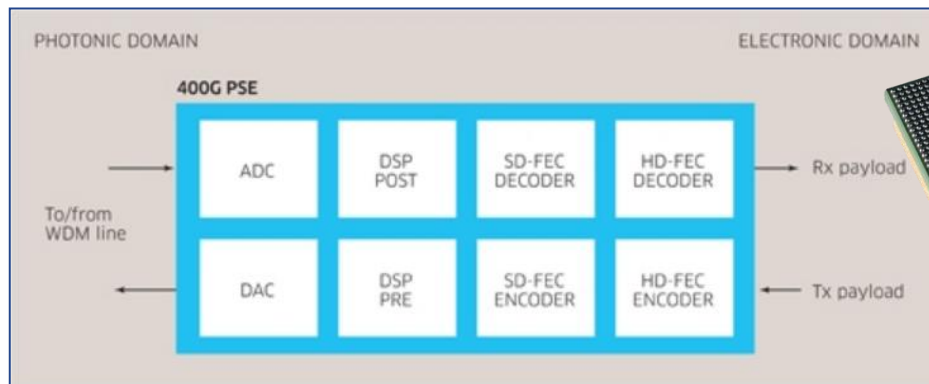
□ Evolution of Optical Communication Systems (Alcatel-Lucent)



Demo1 Exploitation: 400G Evolution

❑ Alcatel-Lucent 1830 PSS-64 (Photonic Service Switch)

- 32 slots a' 120 Gbps
1.92 Tbps universal switching matrix
- Supporting future 400GE and 1 Terabit interfaces
- 400G Photonic Service Engine



- Further Evolution (converter): Increase symbol rate and bandwidth, reduce power consumption, reduce costs ... → SiGe BiCMOS
- RF2THzSiSoC addressing technical bottleneck of optical high speed TX-systems
 - Realise ultra-fast ADC and DAC feat. high bandwidth and resolution, cope with extreme high data throughput (600Gb/s)

Application Fields for High End Arbitrary Waveform Generators:



General Purpose

- Education & Research
- R&D, Design Verification and Manufacturing
- Digital Video



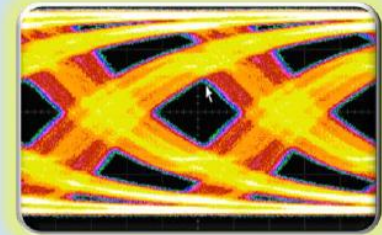
Communications

- UWB
- IEEE 802.11ad
- Satellite



Aerospace

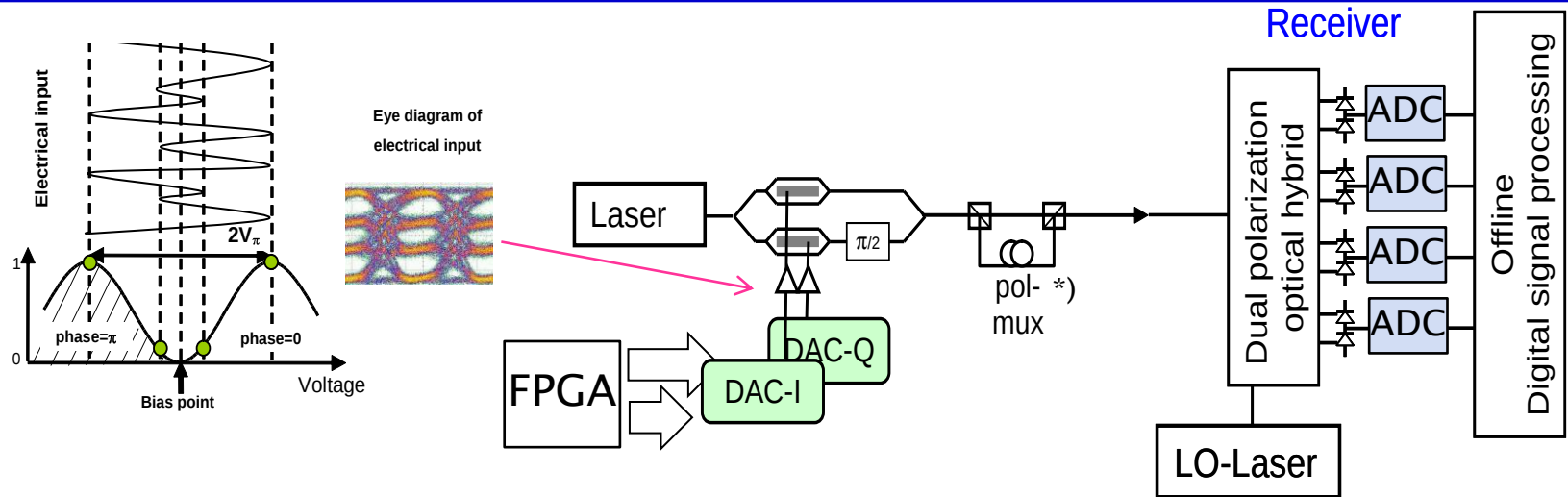
- Radar
- Electronic Warfare
- Satellite



Serial Bus Standards

- e.g. PCIe, USB, SATA, ...
- Multilevel Signals
- Jitter Margin Tests

Demo1a: 400Gbit/s 16QAM PolMUX Optical Transceiver

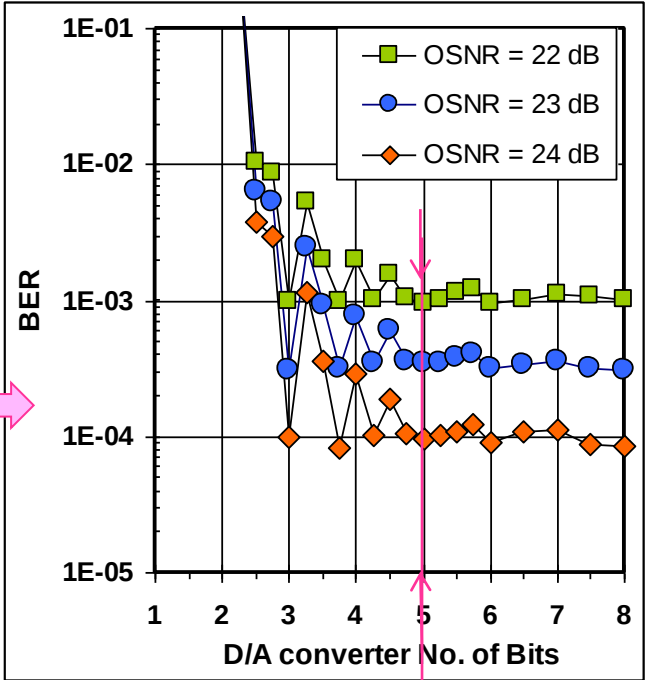


*) PolMUX will be emulated in test bed by means of split-delay-add stage

➤ 16QAM Polarisation Multiplex

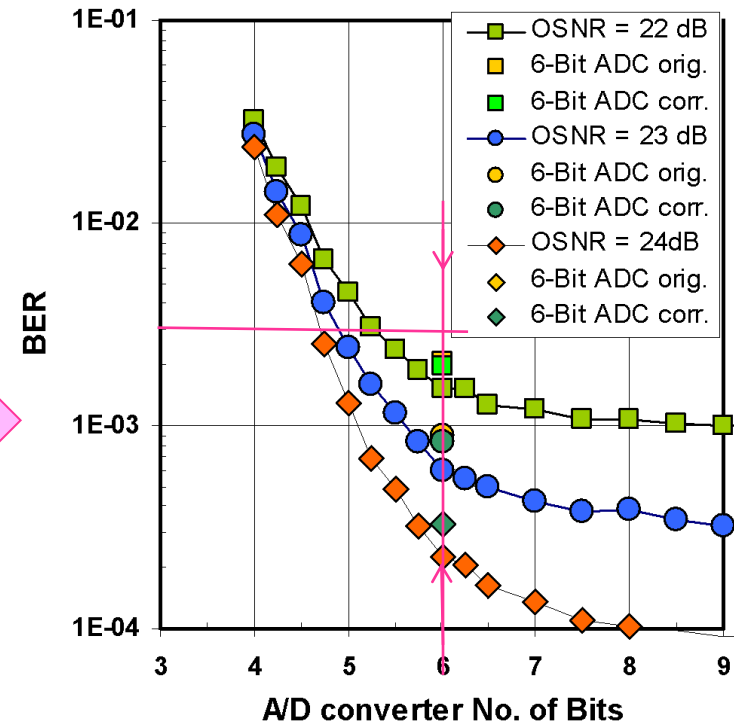
- Using two optical polarisations; per polarisation:
 - 4 bits coded into 1 symbol (i.e. 2 in In-Phase (I) and 2 in Quadrature (Q) comp.)
=> Modulator is driven by electrical four-level signal
 - After 90° phase rotation optical Q-signal is superposed with I-signal
- 8 bits transmitted per symbol interval
- 512 Gbit/s targeted (incl. FEC overhead)
- => Symbol rate = 64 Gbaud

Demo 1: DAC Requirements

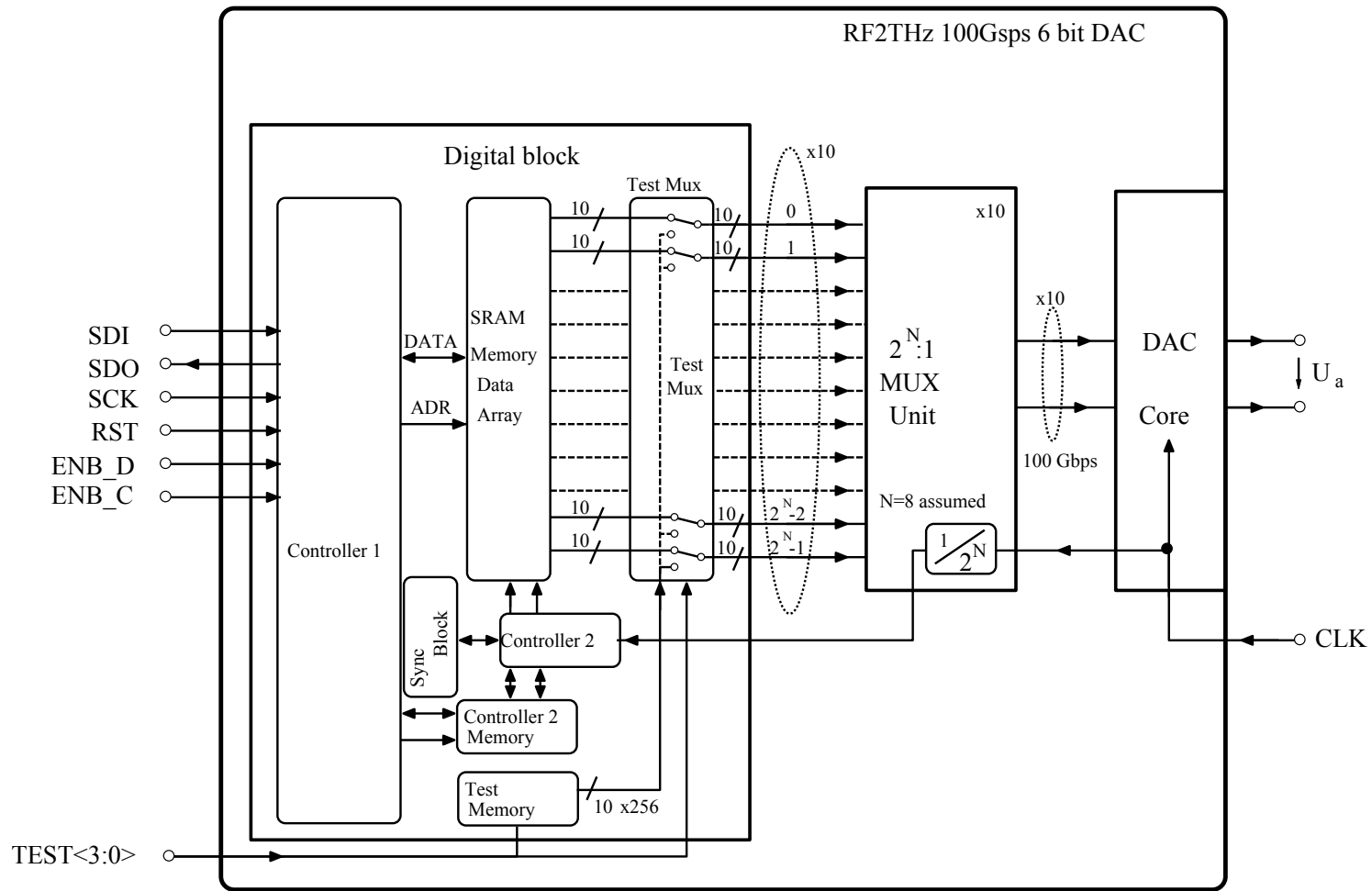
- Two parallel DACs drive child modulators of a LiNbO3 Mach-Zehnder IQ modulator
 - $V_{2\pi} \sim 5$ V, BW ~ 35 GHz $\Rightarrow$ need modulator driving amplifiers
 - Sampling rate ≥ 64 GS/s
 - Bandwidth $>$ Nyquist frequency (= Baudrate/2)
 - >6 bit resolution for correction of channel- and modulator nonlinearities (pre-distortion)
 - System level simulations yielded ENOB > 5 bit (assuming no pre-distortion, ideal 8 bit ADC on RX side)
 - 64 Gbaud @ 6 bit, hence 384 Gbit/s input capacity, need 24 differential Inputs, each 16 Gbit/s $\Rightarrow$ *today not viable*
 - Compromise solution: Off Line demonstration using *integrated memory buffer*: Need to store $2^{11}-1$ PRBS
memory size = $6 \text{ bit} \cdot (2^{11}-1) \cdot \text{sampling rate} / \text{memory speed}$
- (A pink arrow points from the text "integrated memory buffer" to the graph below)*
- 
- The graph shows the Bit Error Rate (BER) on a logarithmic scale (from 1E-05 to 1E-01) versus the D/A converter No. of Bits (from 1 to 8). Three data series are plotted for different OSNR values: 22 dB (green squares), 23 dB (blue circles), and 24 dB (orange diamonds). The BER generally decreases as the number of bits increases, with higher OSNR values resulting in lower BER. A vertical pink line is drawn at 5 bits, with a pink arrow pointing to it from the text 'integrated memory buffer'.
- | D/A converter No. of Bits | BER (OSNR = 22 dB) | BER (OSNR = 23 dB) | BER (OSNR = 24 dB) |
|---------------------------|--------------------|--------------------|--------------------|
| 2 | ~0.1 | ~0.05 | ~0.03 |
| 3 | ~0.01 | ~0.005 | ~0.002 |
| 4 | ~0.001 | ~0.0005 | ~0.0002 |
| 5 | ~0.001 | ~0.0005 | ~0.0001 |
| 6 | ~0.001 | ~0.0005 | ~0.0001 |
| 7 | ~0.001 | ~0.0005 | ~0.0001 |
| 8 | ~0.001 | ~0.0005 | ~0.0001 |
- Synchronization of four DACs incl. individual de-skewing within $<5\%$ of symbol duration (800 fs)
 - + Eval Board Requirements

Demo1 : ADC Requirements

- Sampling rate $\geq 2 \times \text{Baudrate}$
 - Bandwidth $>$ Nyquist frequency ($= \text{DAC Baudrate}/2$)
 - Calculated BER of 16QAM system at 32.5 Gbaud for different OSNR values versus
 - resolution of *idealized* RX ADC, and
 - additionally for 6-Bit ADC with ENOB=5.7, DNL=-0.36, before and after calibration resp.
(based on a simulated transfer characteristic of VEGA ADC, provided by partner MICRAM)
 - Targeted BER $\sim 2 \times 10^{-2}$ to 10^{-3} for error free transmission
 - DNL calibration saves equivalent of 0.5...0.3bit in resolution
 - OSNR of 22dB needed for 2×10^{-3} BER @ 6 Bit resolution
-
- Memory Size $\geq 500\text{k samples} \times \text{resolution} \times \text{oversampling factor}$
 - Sampling time synchronisation: 4 ADCs within $< 3\%$ of $1/\text{sampling frequency}$
 - Phase shift for sampling clock de-skewing 40 ps
 - + Eval Boards Requirements



Demo1: DAC Block Diagram



Block diagram

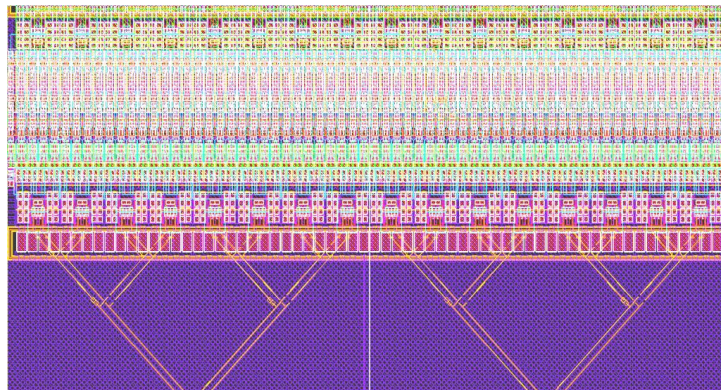
Demo1 – Feasibility Studies

□ ADC Target specification:

- 100 Gsps, 6 bit, Nyquist BW, flash architecture, on-chip memory

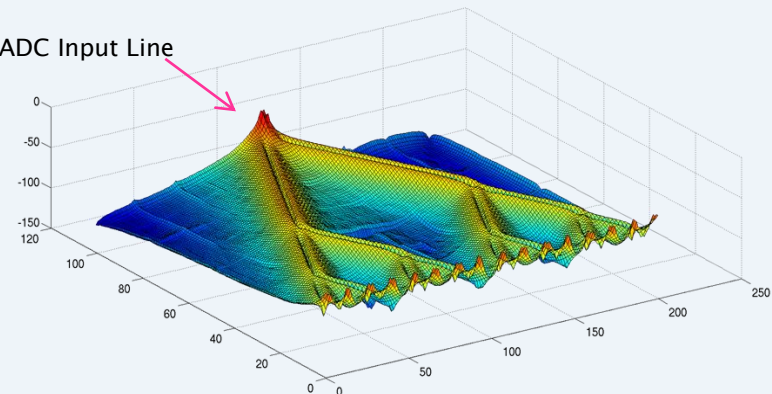
□ Feasibility studies on

- Energy efficient passive data distribution tree,
- Impact of Emitter-Follower non-linearity on ADC resolution
- Impact of comparator clipping induced timing error on ADC res. (Results published in Electronics Letters, vol.49, 2013)



Energy efficient signal and clock distribution concept

ADC Input Line



- Challenge: Guarantee for optimal matching conditions and transfer function over entire bandwidth
- Energy efficient approach, *purely passive* (w.o. buffer amplifiers)
- Simulation of current distribution in ground plane under ADC input signal tree

Demo2 Exploitation: Wireless Data Traffic Growth



Smartphone Density

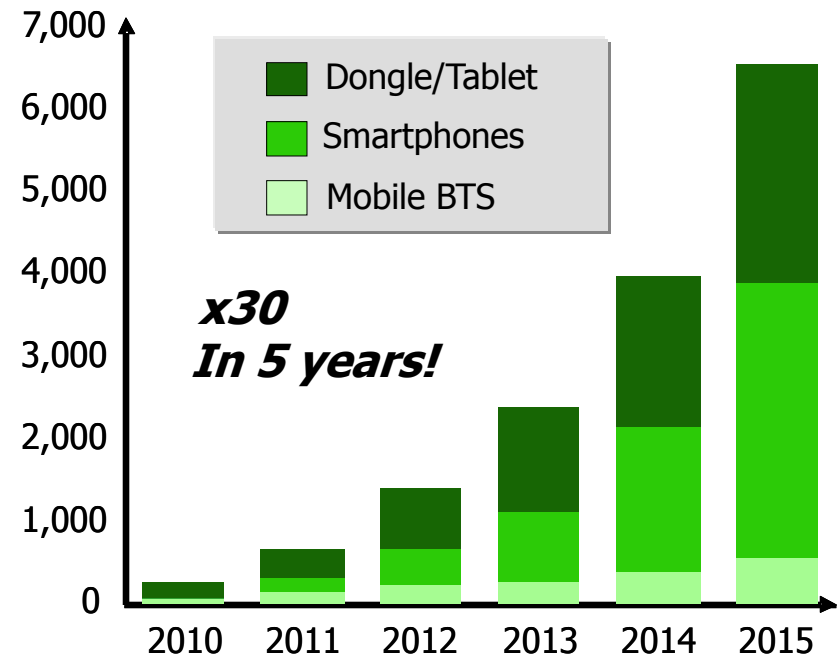
32x usage per km² until 2015

- Smart phones:
- 80%-85% of Data Calls
- 40% of all 3G Terminals

Mobile Internet

70% of Data Exchange in 2014

Pbytes/Month



**Number of Base
Stations
X25 in 2015**

Demo2 Exploitation: Small cell networks

- Expected growth of WW mobile data usage ~x30 in the coming 4...5 years, and x500 in coming 10 years
- Photonic rf transmitter targets energy efficient wireless small cell networks (femto)
- Distributed remote antenna base station
- Concepts merge into future ALUD products like e.g. Light Radio® systems.
- related to ALUDs involvement in CATRENE project **CT 206 UTTERMOST**

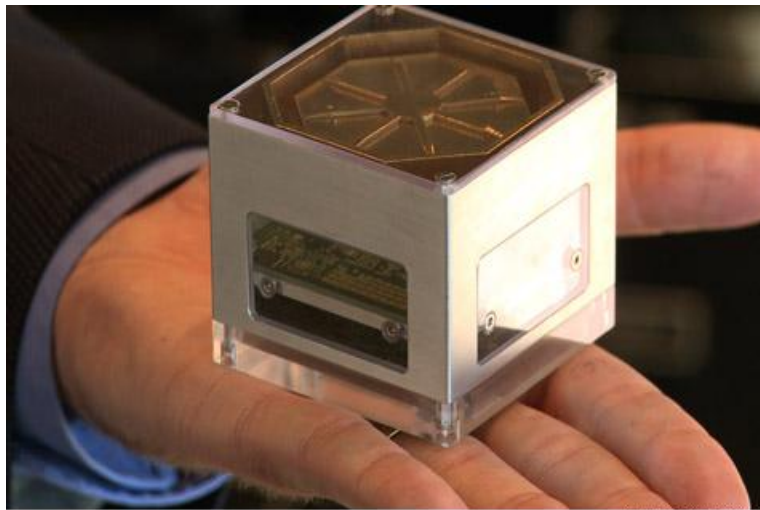
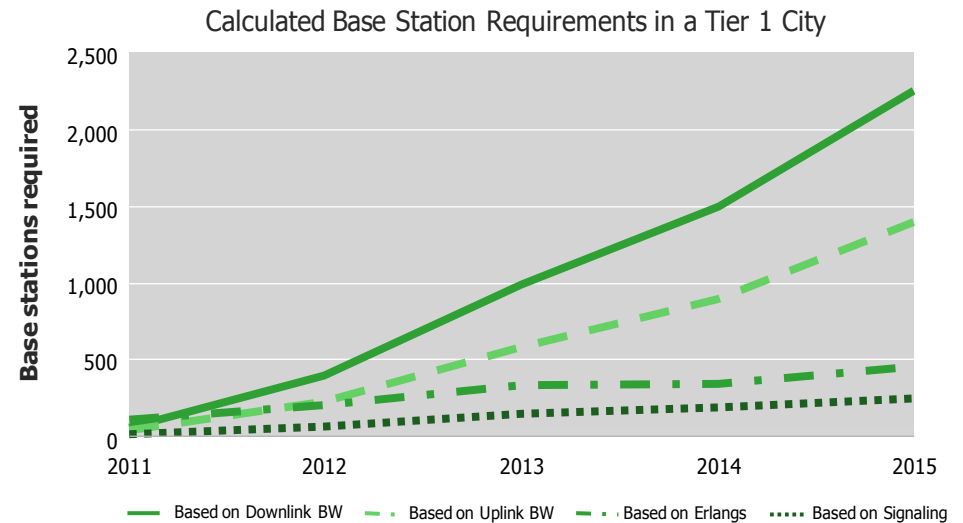


PHOTO: CNNMONEY

The Cube (Alcatel-Lucent Light Radio® combined system/antenna element)



Demo2 Exploitation: A-Lu Light Radio® Scenario

Virtual BTS

Technology agnostic

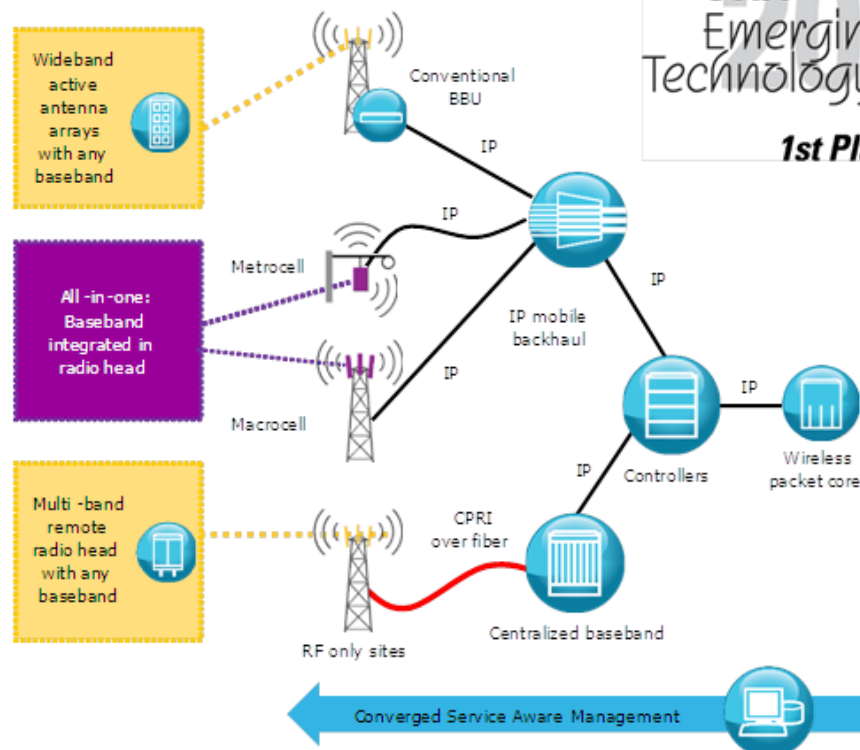
- Active Antennas and MB-RRH
- RF in all bands 700-2600 MHz
- SoC-based BBU (2G/3G/LTE)

Flexible and scalable

- Different deployment options (conventional, clustered or pooled)
- Virtualization and processing aggregation

Ultra compact

- Near Zero footprint BTS
- New generation cabinets



Virtual control

Processing Optimization

- Virtualization of applications
- Standardization on open platforms
- Supporting multiple technologies and multiple topologies

Convergence

Wireline and Wireless Network Convergence

- Integration with broadband Small Cells
- Integration with Optics (WDM, PON) and xDSL

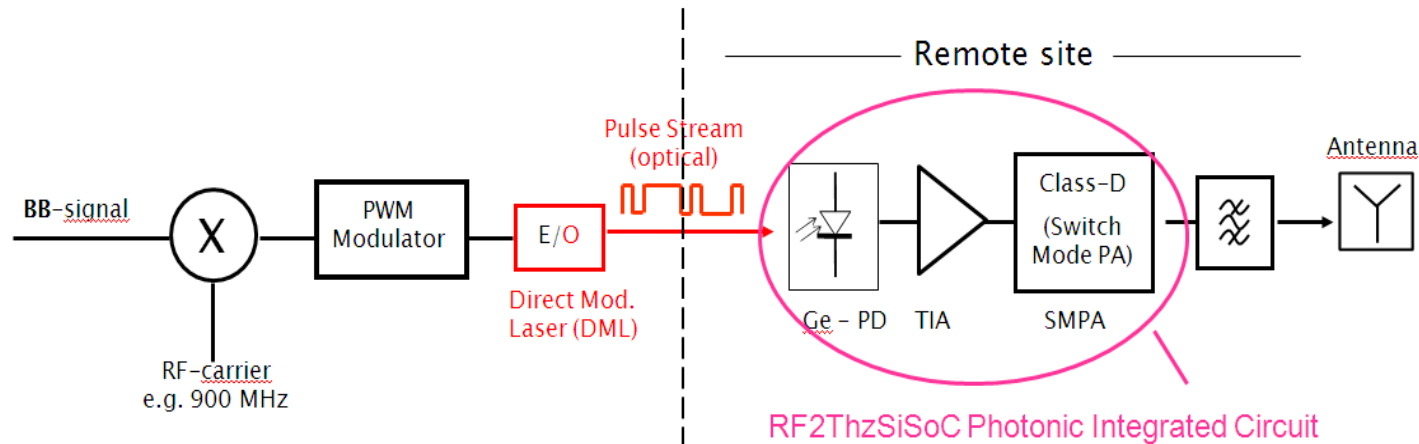
IP Convergence

- Consistent IP service quality and management between Wireless and Wireline

Demo 2: Photonic RF-Transceiver for 3G/4G BTS

□ Low cost remote rf-antenna TX-unit for femto cell BTS

- Reducing hardware effort by PIC integration combining Ge-PD with SiGe BiCMOS TIA and switch mode PA, (TX: 15dBm @ 900GHz)



- Status:
 - System level requirements defined, SiGe BiCMOS Process technology Identified
 - Test structures realised

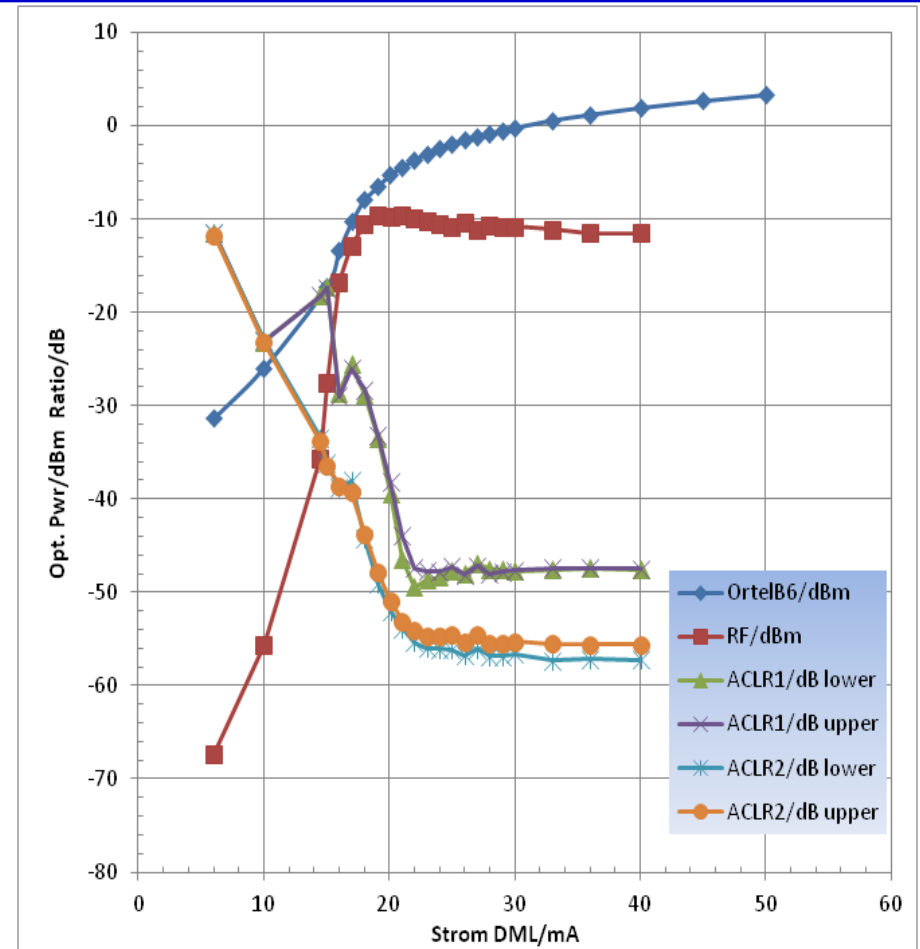
Demo 2: Influence of DML modulation on UMTS signal quality (ACLR)

□ Characterised vs. DML Bias current

- Laser Output Power
- Received rf-power at FSQ8
- ACLR1 ($f_c \pm 5$ MHz) and ACLR2 ($f_c \pm 10$ MHz)

□ First Results

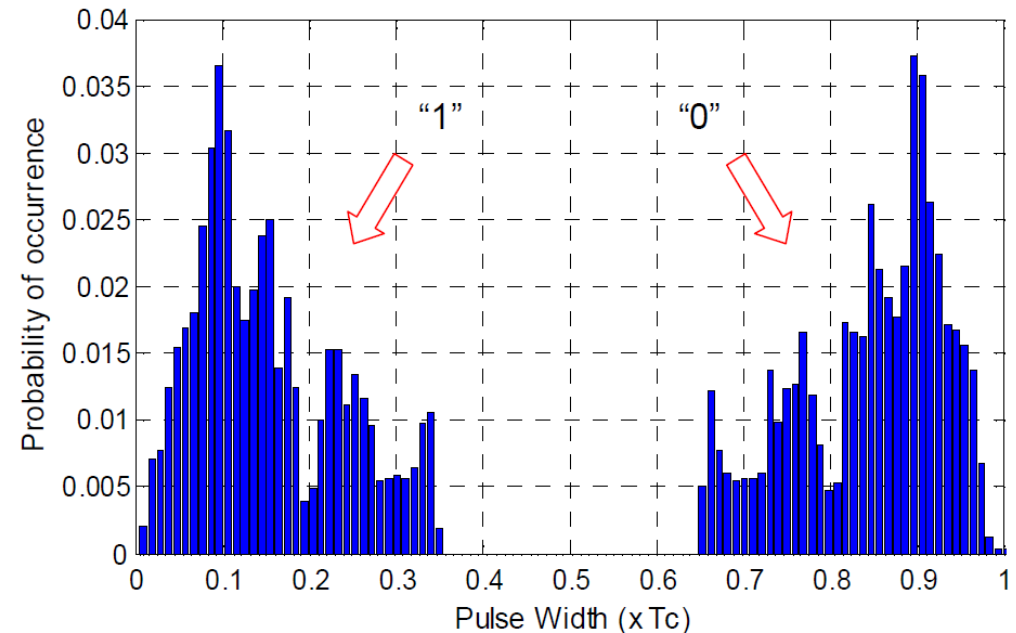
- $I_{DML} > 22$ mA:
ACLR of received signal nearly flat and similar to DML modulation signal
- Detected rf saturates at $I_{DML} \sim 20$ mA
- -10dbm at TIA to be expected



Demo 2: Component Selection for RF-SMPA (1/2)

□ Procedure

- Review of available transistor component options at IHP
- PWM modulated UMTS signal samples provided by ALUD
- Simulated different devices in single ended switch configuration
- Evaluate for power and efficiency



RF pulse-width modulation (PWM) pulse statistic

- Assuming PIN rise/fall time $\tau_{\text{rise,fall}} = 50 \text{ ps}$ -> open eye requires 100 ps data period = $0.2\tau_c$ @ $f_c = 2 \text{ GHz}$
- VDD measurements show that pulses below $0.2T_c$ won't switch completely in on/off state -> power/efficiency losses
- Signal pre-conditioning desirable

Demo2: Component Selection for RF-SMPA (2/2)

- Investigated components from IHP technologies SG25H1 and SG25H3 under ideal driving signal conditions ($\tau_{\text{rise,fall}} = 0$) using PWM modulated rf signal ($f_c = 920$ MHz):

Tech	Transistor	Vcc, V	Pch, dBm	η_{ch} %	RI Ohm
H1	50 x npn200_1	1.5	4.4	38.2	50
H3	100 x npnh3_shp1	1.5	4.9	40.3	50
H3	20 x npnH3_MV	3.5	5.7	55.5	580
H3	140 x npnH3_MV	3.5	8.4	38.3	110
H3	100 x npnH3_HV	5	9.9	41.2	200

Chosen →

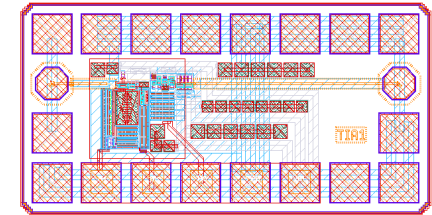
- npnH3_HV device (with $BV_{\text{CEO}} = 7$ V) provides highest output power; (chosen)
- Switches total efficiency was $> 70\%$, but when considering channel efficiency ($\eta_{\text{ch}} = P_{\text{ch}}/P_{\text{DC}}$) best value (55%) is achieved by combining npnH3_MV devices
 - Reduction of efficiency because collector voltage not returning to zero between short pulses)
- Re-characterized npnH3_HV with 2 GHz PWM modulated signal:

Tech	Transistor	Vcc, V	Pch, dBm	η_{ch} %	RI Ohm
H3	80 x npnH3_HV	5.4	6.3	28.9	180

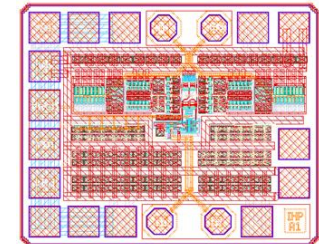
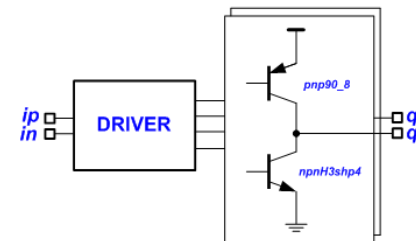
Demo2: Building Blocks and Test Structures

□ Circuits realized and characterized so far (2 Tape Outs at IHP)

➤ TIA

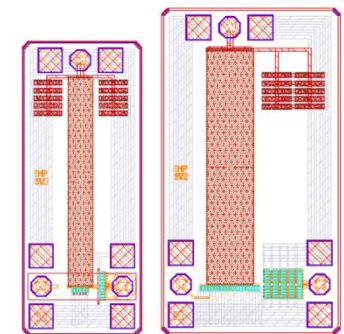
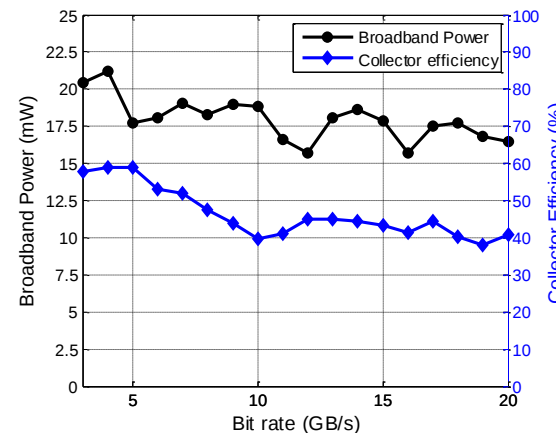
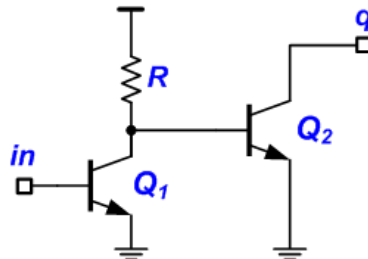


➤ H-Bridge



➤ Test Switches

- 2 variants with different transistor sizes
- Output swing 2.4 V @ 50 Ohm

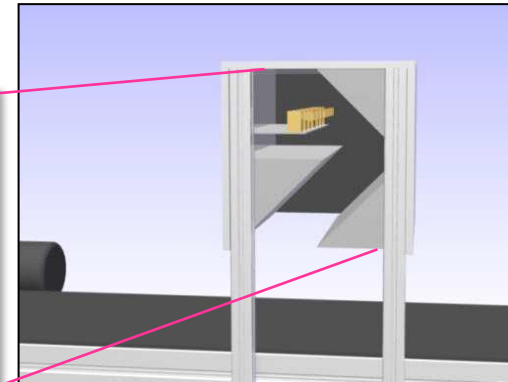
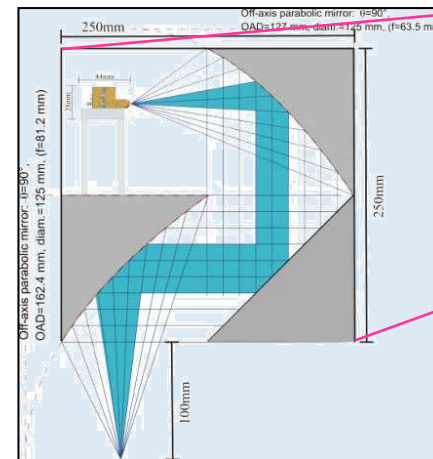
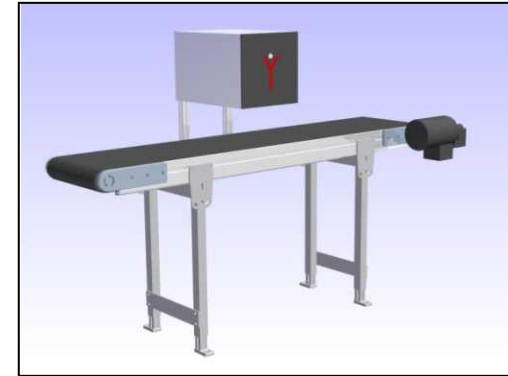


Demo3a:

Wideband 240GHz imaging system with excellent spatial resolution

❑ THz Image scanner for material and product testing

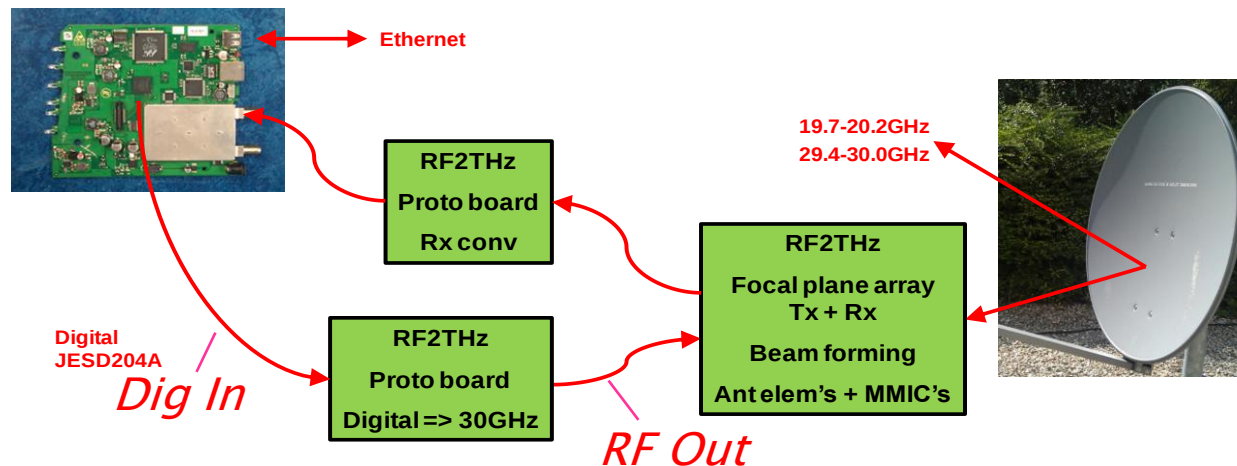
- 3D-imaging system using coherent THz-TX and -RX for synthetic aperture radar imaging (reflection imaging)
- Imaging system setup (conveyor belt and THz- line scanning unit)
- Integration of 32 Rx + 32 Tx Modules at 240 GHz
- Aiming for horizontal and vertical imaging in reflection
- Conveyor belt-velocity ca. 0.5 - 1 m/s
- Image generation with CUDA® based SAR algorithms
 - Status: Line of 50x50 voxels processed in 125 ms



Demo4: 2-way Satellite Terminal f. Consumer Application

□ Demonstrate use of prototype MMIC's in a 2-way internet broadband terminal for consumer market and verify MMIC's in 'real world'

- Transmit MMIC covering digital baseband to 30GHz
- Highly integrated 20 GHz **Rx front-end** and **Focal plane array** for beam forming / steering



- “One Box” = ethernet ↔ satellite; modem on the dish
- Demo concepts from ‘Tx-path only’ to ‘Rx + Tx path + focal plane array’, use stepped approach
- Co-development of antenna and μ -wave ICs

➤ Addressing Mass Market -> high volumes , low prize

Demos 3 and 5: Markets addressed by activities on RADAR components

□ Automotive market, driven by

- Future roadmaps of various international consortia (EuroNCAP, NANCAP+, JNCAP+) require increasing amount of active security features
- Increasing availability of driver assistance systems
- Increasing consumer awareness about traffic safety
- Radar is technology of choice, incl. radar/video sensor data fusion
- Observation of high benefit/cost factor for SiGe BiCMOS

□ Consumer goods market

- Sensors in buildings, appliances, and measurement equipment
 - High integration is important
 - Low cost is important
- High integration and low cost only feasible with high integration

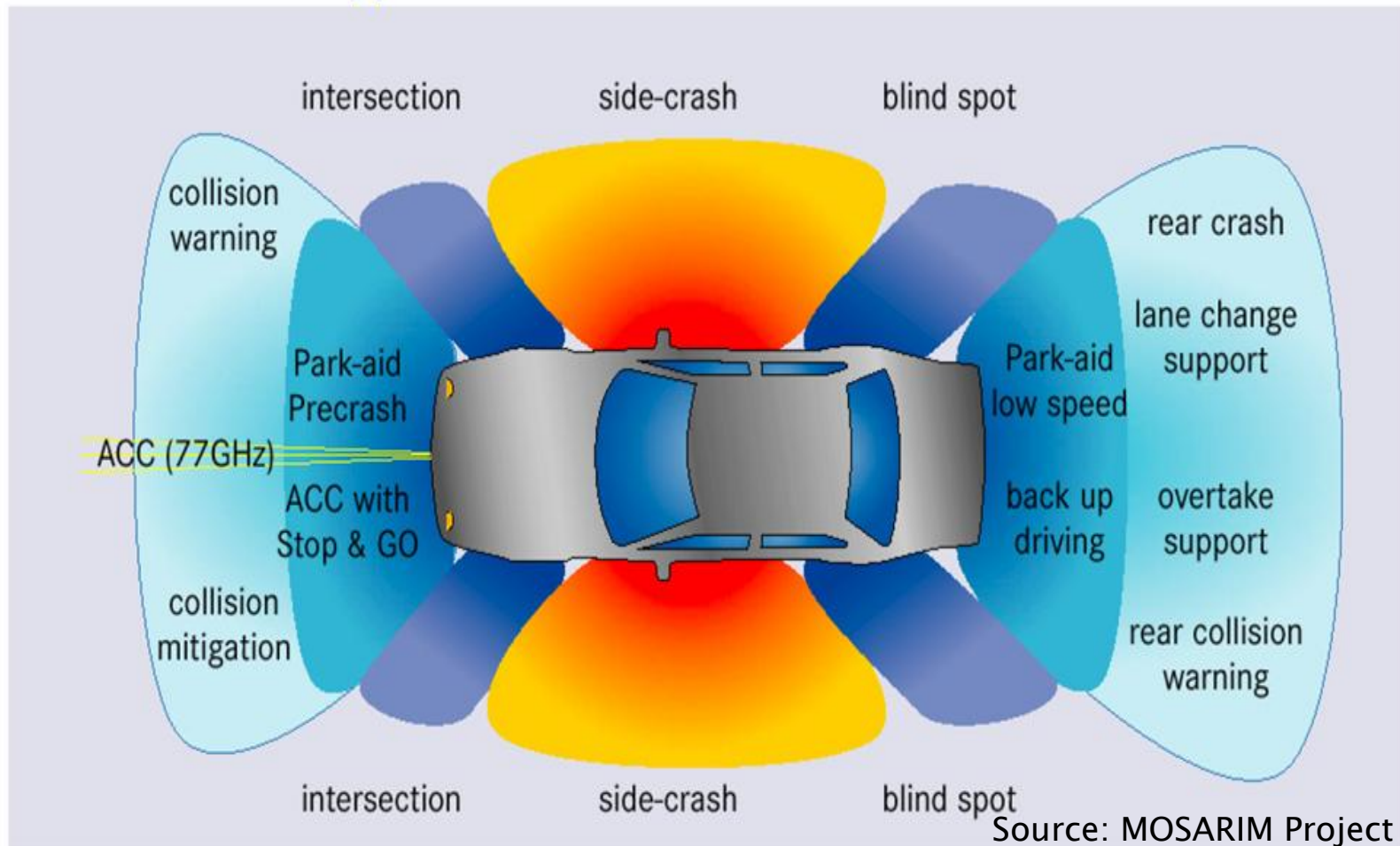
Automotive RADAR Technology SWOT Analysis

Strengths	Weaknesses
Robust performance Strong industry in Europe Superiour to video in fog and rain conditions	Angular resolution (video superior)
Opportunities	Threats
Huge volume by deployment of radar in all car categories	Alternative sensor concepts: LIDAR, ultrasound, video

- Highly complex driver assistance functions will require Radar as one sensor in the sensor data fusion due to superiority in foggy and rainy conditions.
- Great opportunity: huge volume market for Radar sensors

Driver Assistance Functions

- Many driver assistance functions require robust performance of RADAR AND high angular resolution



Consumer RADAR Technology SWOT Analysis

Strengths	Weaknesses
Robust performance for different environments Hidden mounting possibility (design freedom)	Invisible measurement spot with larger aperture compared to laser
Opportunities	Threats
Introduction of new measurement principles not yet found in market	More mature alternatives: laser, IR, ultrasonic, video

- Radar measurement principle not yet found in consumer market applications.
- Robust performance and additional mounting possibilities (hidden) for increased design freedom.

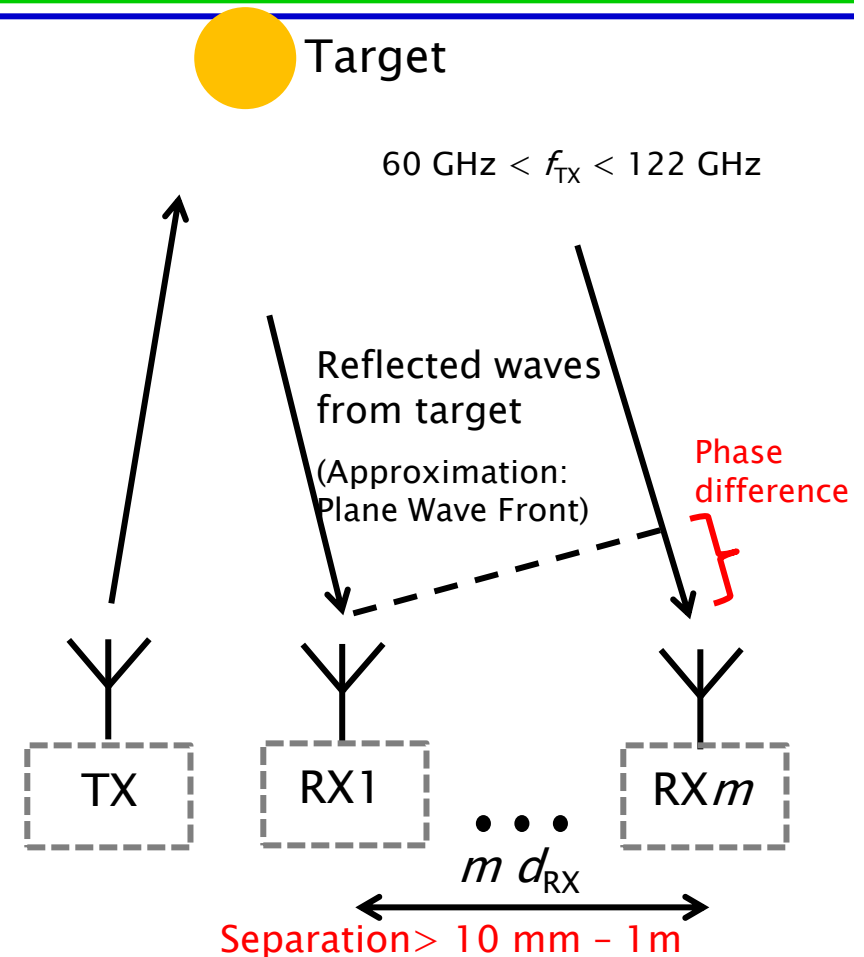
Demo3b: 120 GHz Radar system f. sensing applications w. improved angular resolution

□ Motivation:

- Detection of angular resolution requires coherent phase estimation of received signal across RX-channels.
- Larger aperture desirable to improve angular resolution
- For cheap products no off-chip RF-signals are feasible. Such signals on PCBs are expensive in production and material cost.

□ Therefore: three conceptual classes for synchronization

- Distribution of intermediate frequency over PCB
- Transmission of pilot tone over the air
- Phase estimation of free-running RX-VCO using knowledge about sent signal



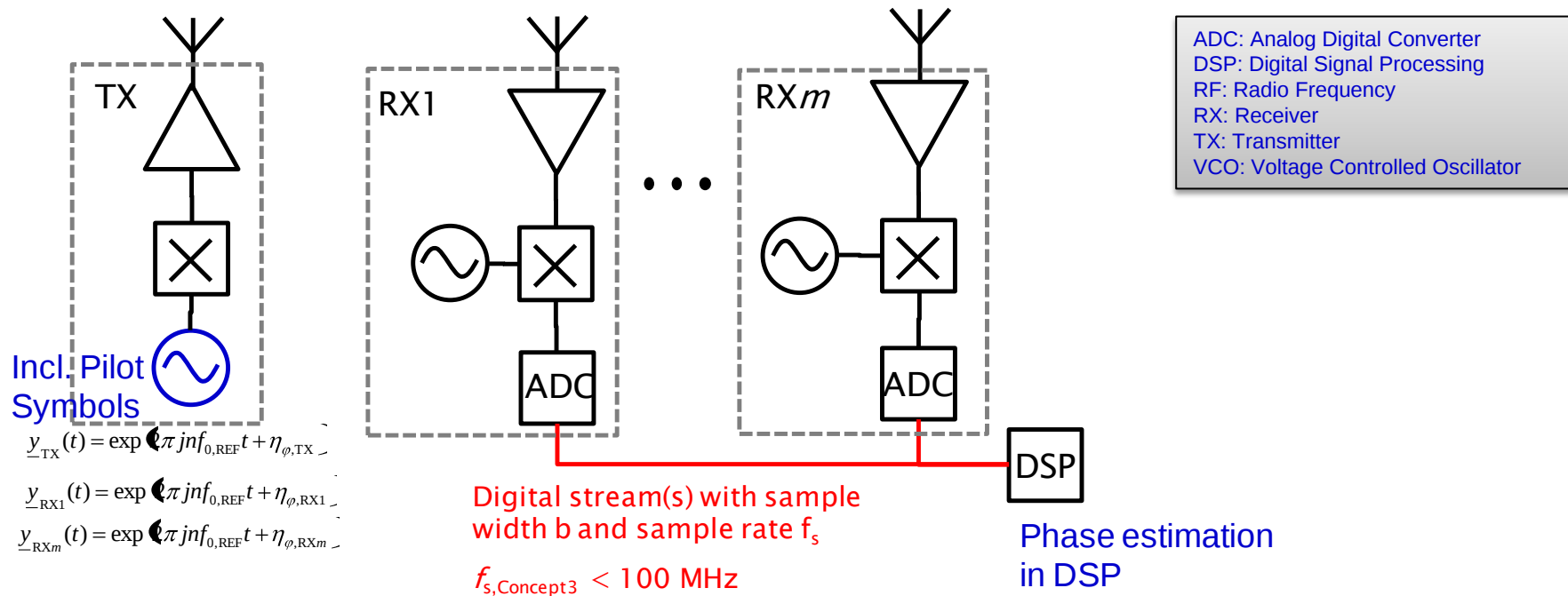
ASIC: Application Specific Integrated Circuit
PCB: Printed Circuit Board
RX: Receiver
TX: Transmitter
VCO: Voltage Controlled Oscillator

Demo3b:

120 GHz Radar system f. sensing applications w. improved angular resolution

❑ Coherent Phase Estimation of Free-Running Rx-VCO in Digital Domain

- Precise synchronization of individual antenna element MMICs' local oscillators RX SNR, element placement
- Simple rf-design
- Requires large bandwidth in digital stream due to free running VCOs



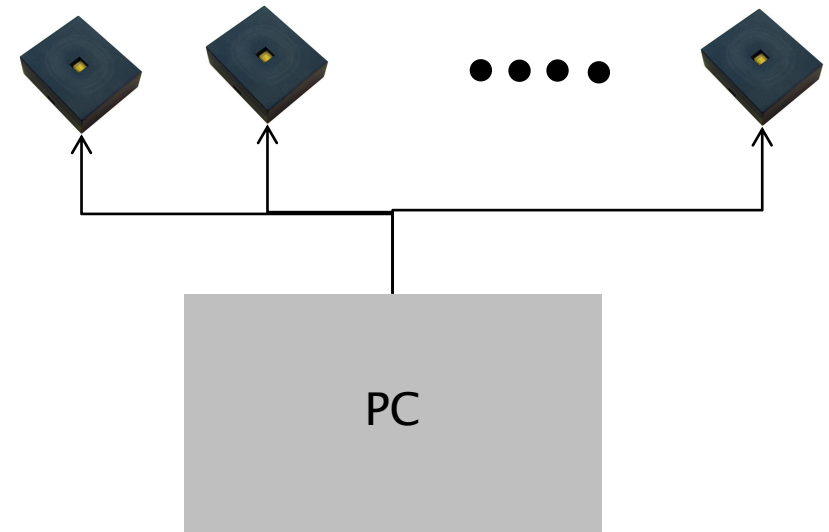
Demo3b: 120 GHz Radar system f. sensing applications w. improved angular resolution

□ Test-System for Implementation:

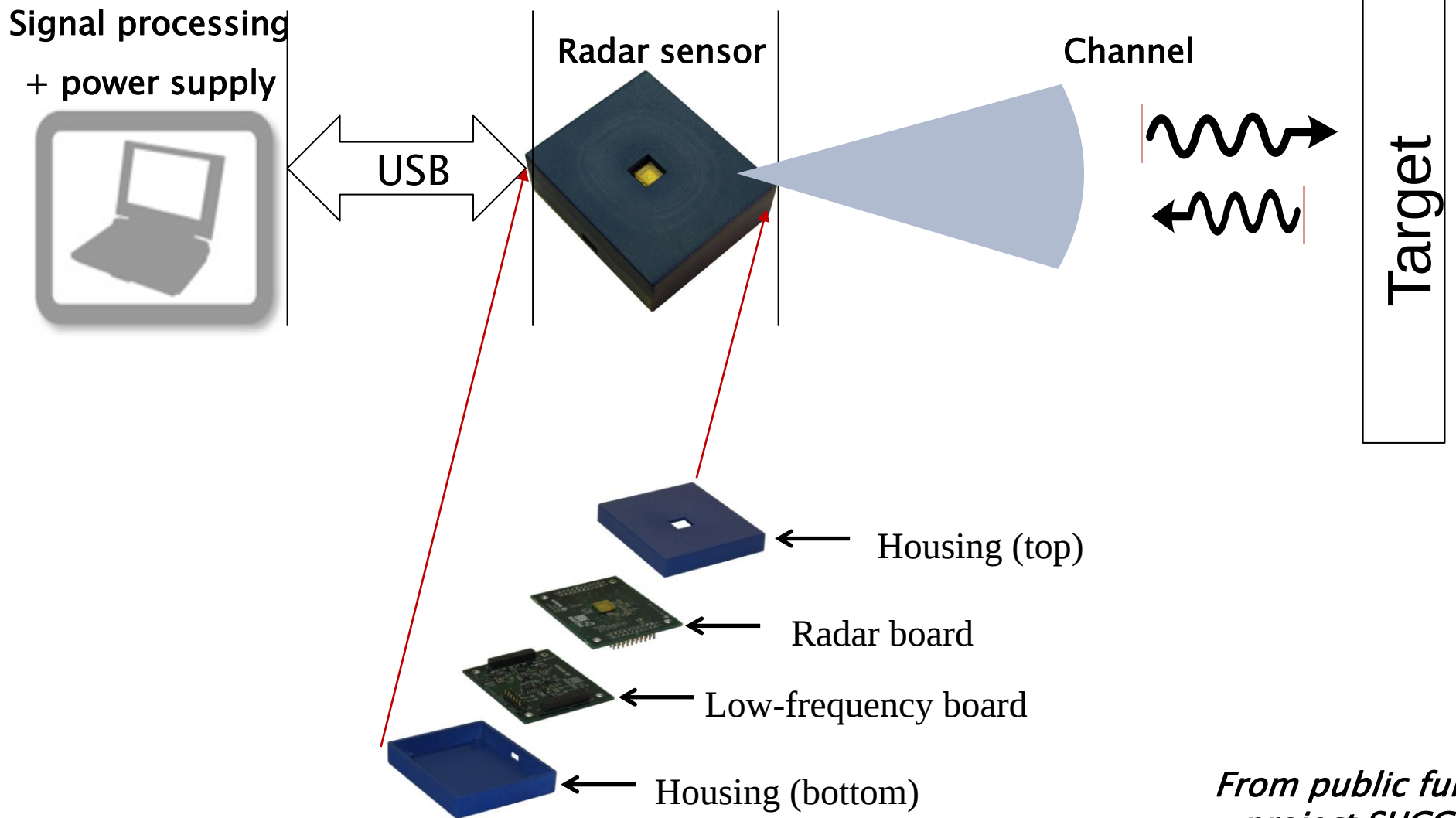
- Resorting to 122GHz TRX from Silicon Radar from SUCCESS-project
- Currently building H/W for tight timing control of coordinated measurements of up to 10 sensors



Photo illustrating appearance of the array setup



Demo3b: 120 GHz Radar system f. sensing applications w. improved angular resolution



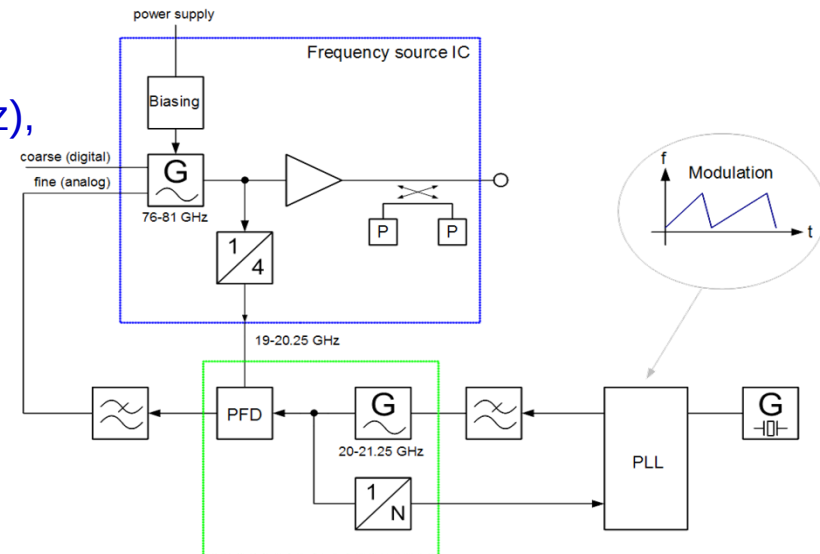
*From public funded
project SUCCESS*

Demo5: Radar Sensor Components for 79 GHz and 122 GHz

❑ (a) Swept signal source, (b) digitally controlled phased TX antenna array (Bosch, Astus)

➤ Frequency synthesizer:

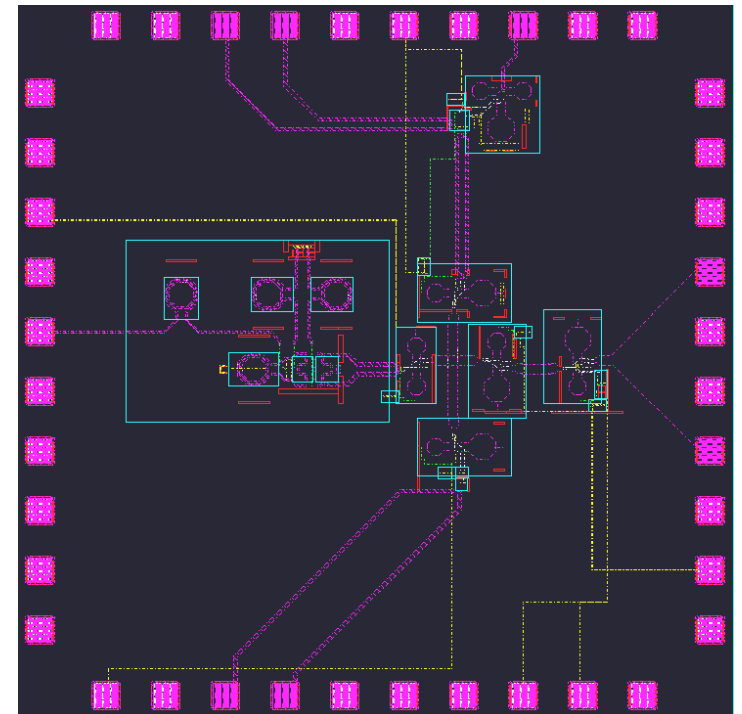
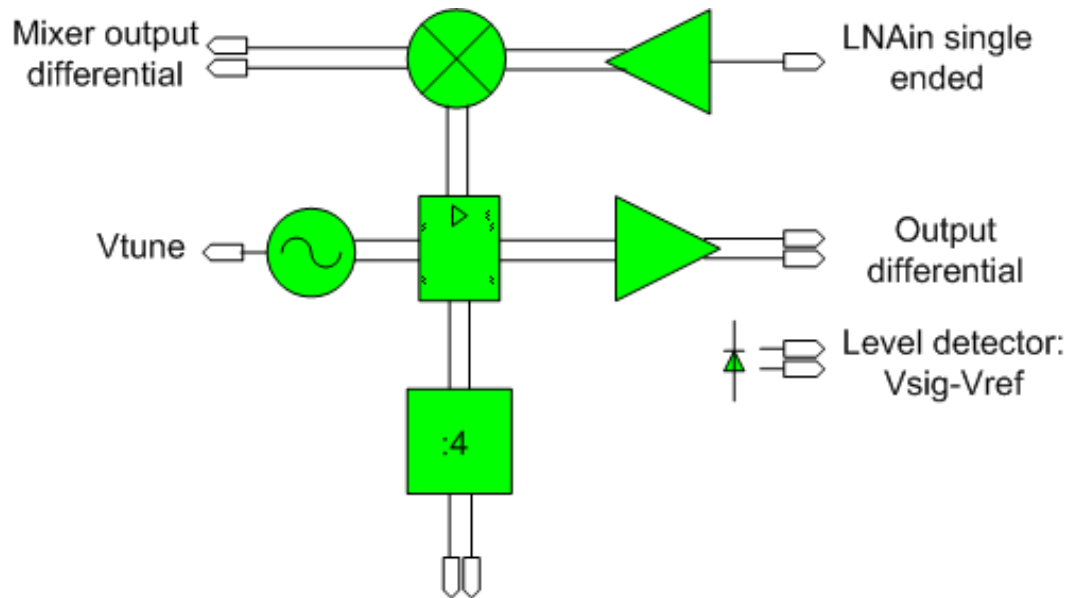
- Dual loop PLL w. very low noise VCO (77-81GHz), divider, and very fast PFD+VCO (20GHz)



❑ (c) All-digital FMCW synthesizer (TUD), and (d) wideband RX down-converter for wireless sensing (TUD)

- #### ➤ Building Blocks demonstrating integration of high performing rf circuitry up to 90GHz
- High Bandwidth, Low phase noise

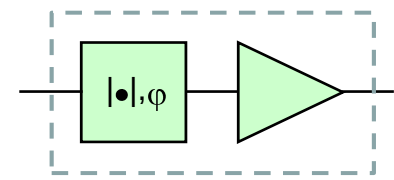
Demo 5a Design Blocks: Oscillator and Mixer



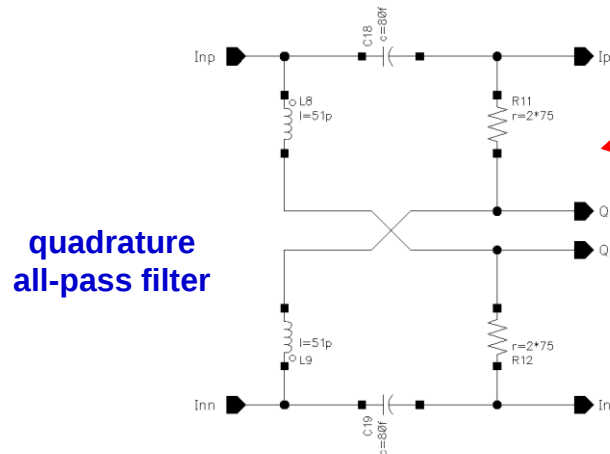
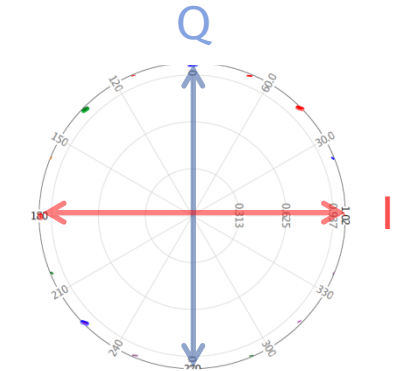
Design blocks:

- Oscillator, buffer and output buffer with level detector
- Divide by 4
- Rx: LNA + Mixer

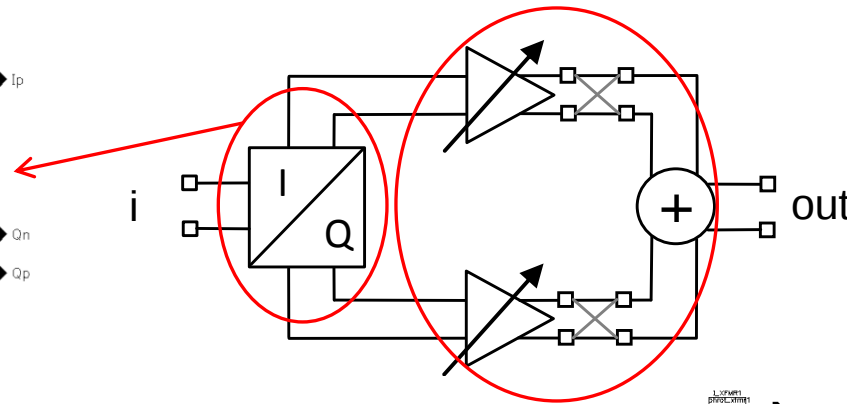
Demo 5b: Design Blocks: Phase Shifter



phase interpolation
topology



quadrature
all-pass filter

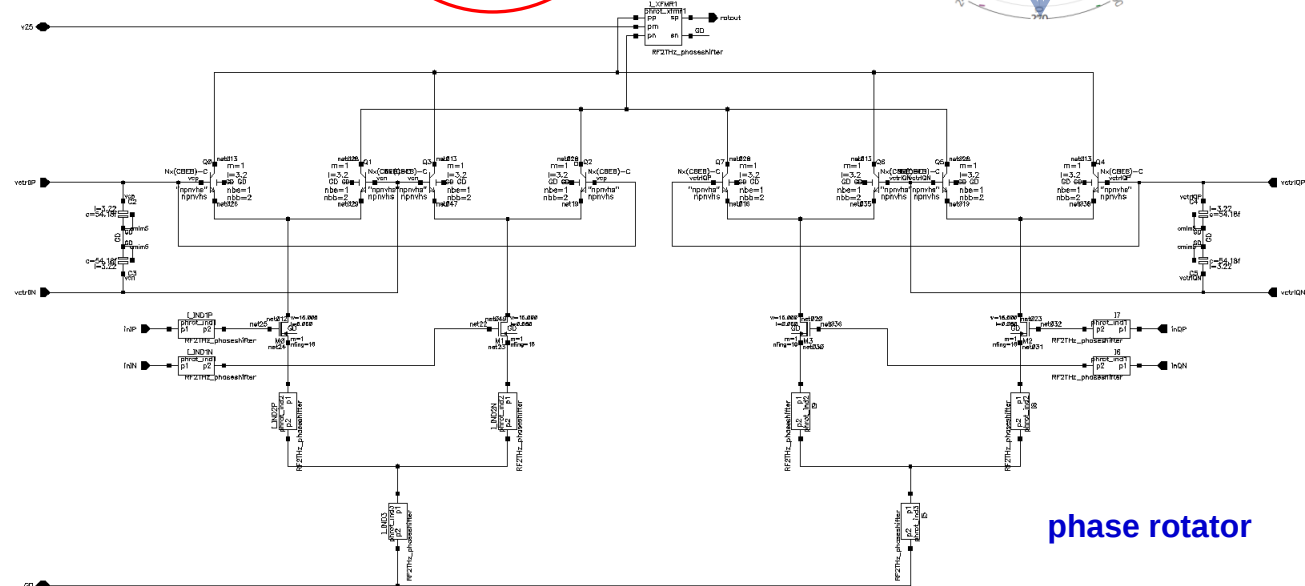


Phase shifter:

Phase 0 .. 360 degree

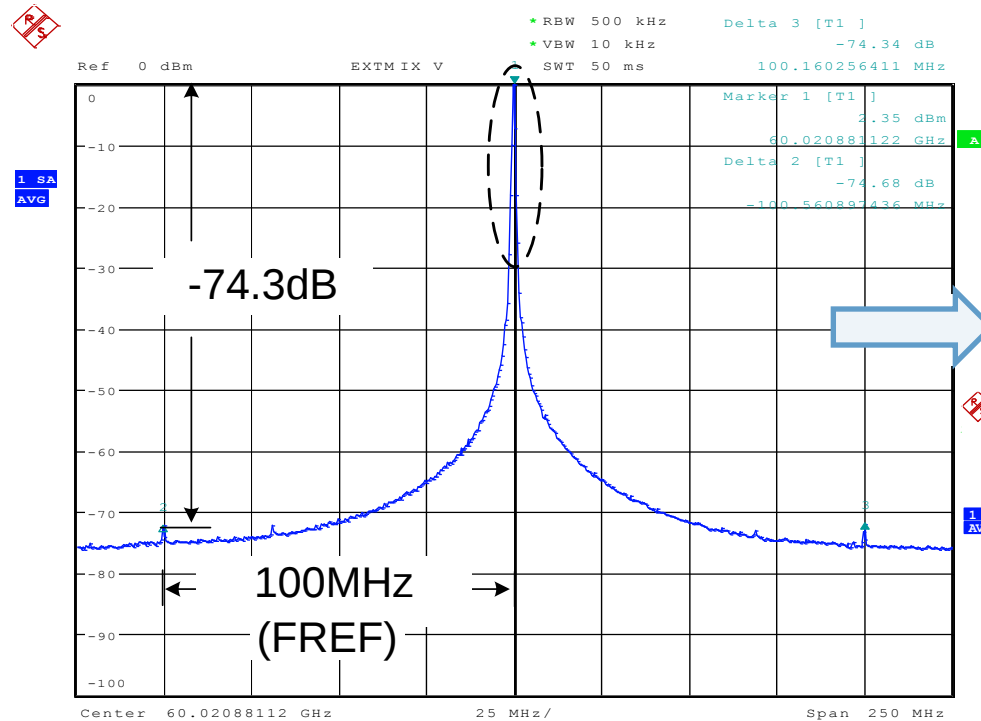
Freq. 77 .. 81 GHz

Pout 0 dBm



phase rotator

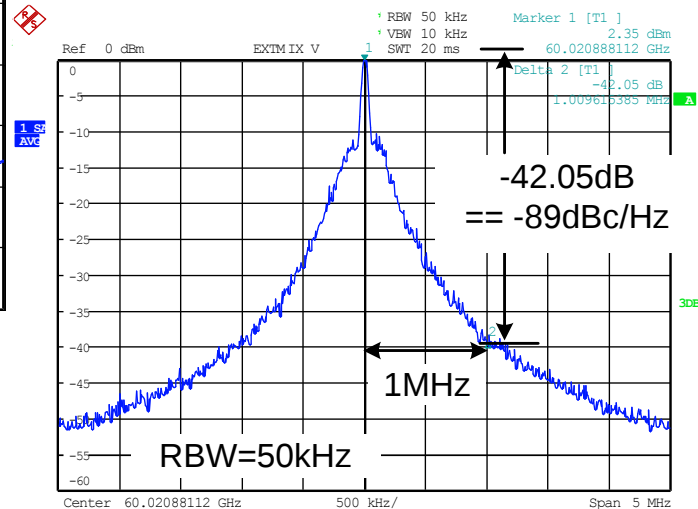
Demo 5c: All-digital FMCW synthesizer measured spectrum



- FREF = 100MHz
- Reference spur = -74.3dBc

- $f_{\text{out}} = 60.0209\text{GHz}$
- PN = -89 dBc/Hz @1MHz offset

Zoom in



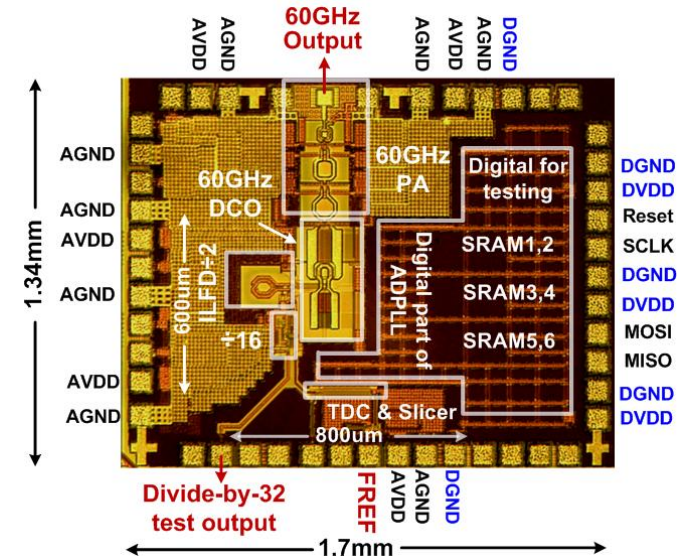
Demo 5c: First 60GHz all-digital phase-locked loop (Prototype)

- Fabricated in 65nm CMOS and characterised
- Performance surpasses conventional designs reported in literature

	This Work	ISSCC'09	JSSCC'11	ISSCC'09	TCAS-II'11
CMOS	65nm	45nm	65nm	65nm	90nm
Center frequency	60GHz	61.5GHz	60.5GHz	20GHz	40GHz
Architecture	TDC-ADPLL	Charge pump analog PLL	20GHz analog PLL x 3	BB-ADPLL	BB-ADPLL
Type	Fractional-N	Integer-N	Integer-N	Integer-N	Integer-N
Reference freq.	10...100MHz	100MHz	36MHz	275MHz	156.25MHz
Phase noise (raw)	$\Delta f=100\text{kHz}$	-72dBc/Hz	-71.5dBc/Hz	-63.6dBc/Hz	NA
	$\Delta f=1\text{MHz}$	-90dBc/Hz	-75dBc/Hz	-95dBc/Hz	NA
FREF spur	-74dBc	-42dB	-67~ -58dBc @20GHz	NA	-48dB
Frequency range	7GHz (11.6%)	9GHz (hi/lo, 2 VCOs) (14.6%) [†]	5GHz (8.3%)	6GHz (30%)	3GHz (7.5%)
Power consumption	48mW(1.2V)	78mW (1.1V) *	80mW (1.2V) *	64mW(1.6/1.1V)	46mW(1.2V)
Core area	0.48mm ²	0.82mm ² (with pad)	1.68+0.8mm ² (2 dice, with pad)	NA	0.3mm ²

* Provide quadrature outputs at 60GHz. [†] PLL locking range is 2.4GHz, limited by injection locking divider's locking range.

Table Comparison with State of Art PLLs



65nm ADPLL Prototype
(IEEE-ISSCC 2013)

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