CATRENE – CT209 – RF2THZ SiSOC

Title: Electro-thermal characterization and modelling

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Outline

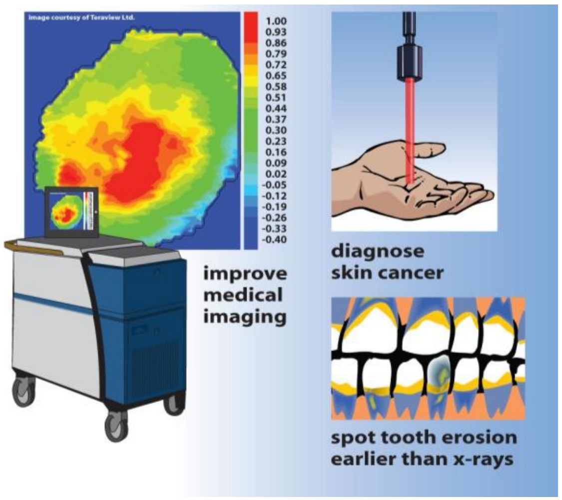
- 1- Introduction
- 2 – Self-Heating Characterization
  - Low frequency S parameters
  - Pulsed DC and S parameters
- 3 – TCAD and compact modeling
  - Scalable compact model
    - Recursive
    - Thermal dependant
  - TCAD: Impact of back end
- 4 - Application circuit
  - Ring oscillator
- 5 – Parameter extraction using test structures
  - Mullti-finger coupling
- 6 - Summary

Motivation

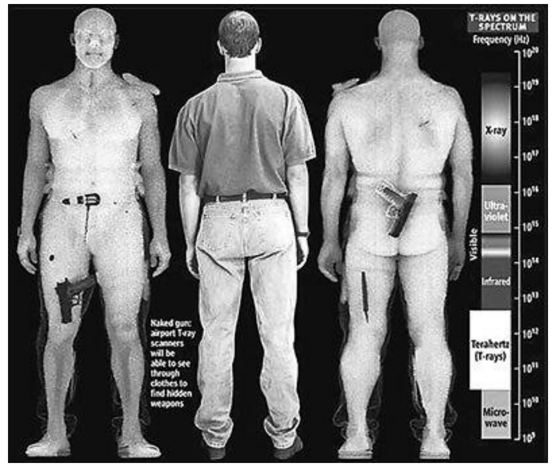
- Improved SiGe HBT performance (f_{max} of 500GHz)

$\Rightarrow$ new spectrum of sub-millimeter-wave applications [1]

Medical applications



Security



High Speed Communication

- In FP7 DOT7, the new target is f_{max} of 700GHz while CATRENE RF2THz plan to have a large scale integration

[1] E. Ojefors, J. Grzyb, Y. Zhao, B. Heinemann, B. Tillack, and U. R. Pfeiffer, "A 820GHz SiGe chipset for terahertz active imaging applications," in Solid-State Circuits Conference 2011

Motivation

❑ Improvement of technology => impact on self-heating ?

Advanced technology		Drawbacks
Vertical down scaling	➢	Increase of power density in devices
Trench isolation	➢	Heat confinement by insulated wall
Large scale integration	➢	Mutual heating – heat flow from neighboring device

⇨

- ❑ Performance and reliability limitation
- ❑ Compact model accuracy needs some improvements
- ❑ Characterization and parameter extraction method needs to be revisited.

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2 – Self-heating characterisation

- **Many methods have been developed to extract R_{TH}**
  - DC measurement, many authors have proposed some methods

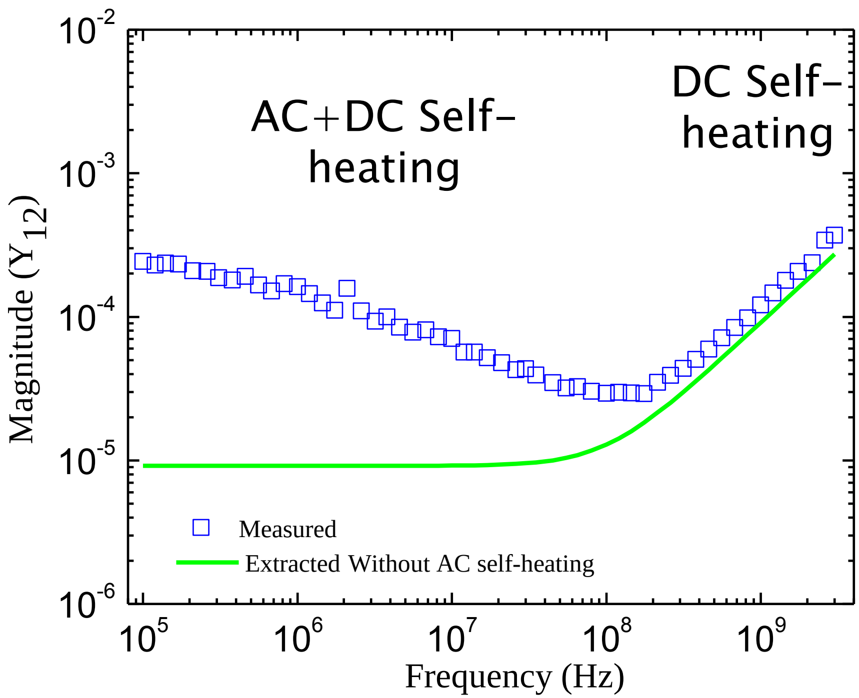
“Evaluating the Self-Heating Thermal Resistance of Bipolar Transistors by DC Measurements: A Critical Review and Update “, S. Russo et al. BCTM 2009

- **What about C_{TH} ?**
  - Transient measurement
    - Pulse generator and scope (Limitation: calibration of test set)
    - Pulse DC measurement
  - <u>Low frequency S parameter</u>

- **Getting quasi-isothermal data to simplify parameter extraction ?**
  - <u>Pulse DC and RF measurement</u>

2 – Self-Heating characterization: Low frequency S parameters

❑ Thermal impedance extraction



❑ Low frequency S-parameter measurements :

- 100 kHz – 3 GHz,
- V_{CE} = 1.5 V
- V_{BE} = 0.95 V

❑ DUT : L_E*W_E = 9.88*0.15 µm^2

Normalized Thermal Impedance →

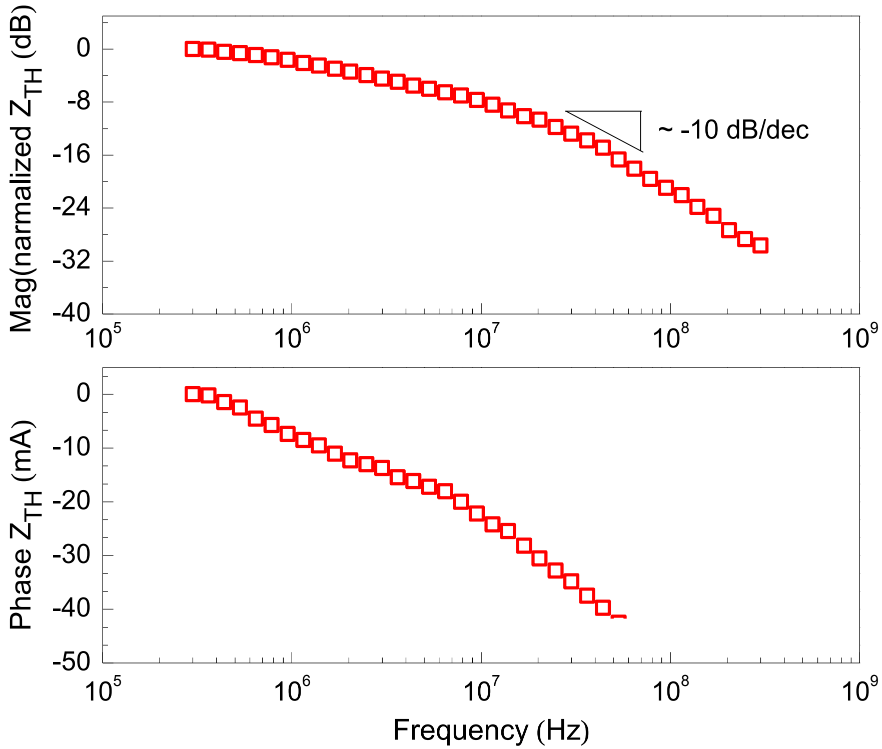
$$Z_{TH}(\omega) = \frac{\left(y_{12}(\omega) - y_{12}^{AC}\right)}{\left(y_{12}^{DC} - y_{12}^{AC}\right)} \cdot \frac{\left(I_C + V_{BE} y_{12}^{DC} + V_{CE} y_{22}^{DC}\right)}{\left(I_C + V_{BE} y_{12}(\omega) + V_{CE} y_{22}(\omega)\right)}$$

N. Rinaldi, *IEEE TED*, vol. 48, 2001, pp. 323-331.

A. K. Sahoo, et al., *IEEE EDL*, vol. 32, no. 2, pp. 119-121, 2011.

2 – Self-Heating characterization: Low frequency S parameters

❑ Thermal impedance extraction (ST Microelectronics)

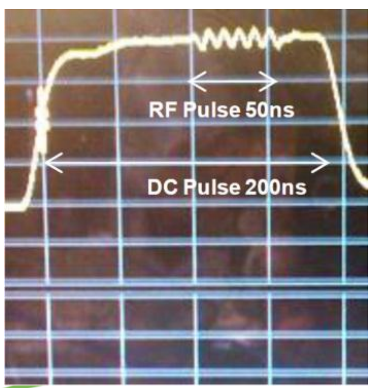


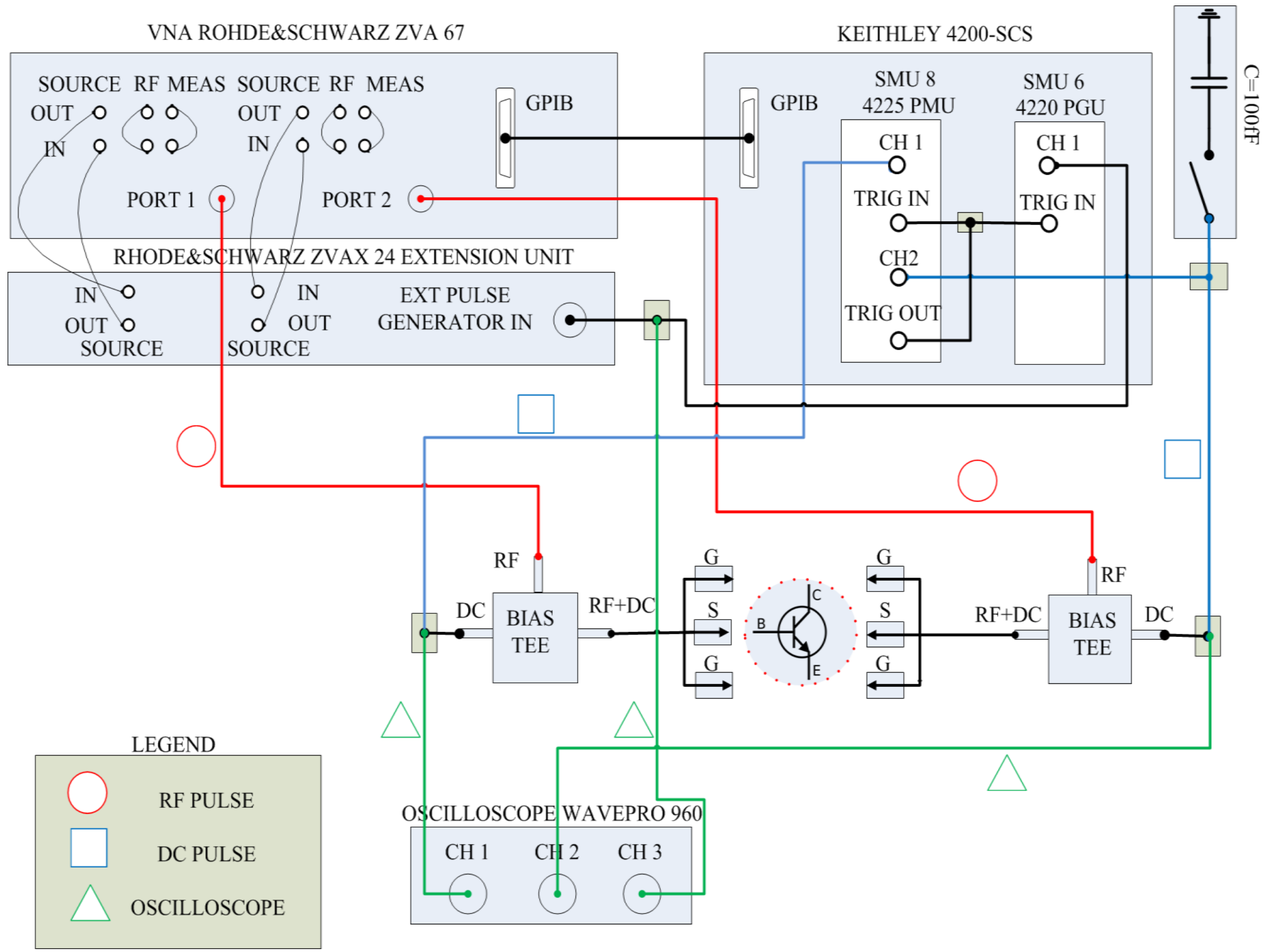
2 – Self-Heating characterization: pulsed measurements

Experimental Setup

Pulsed measurement system characteristics:

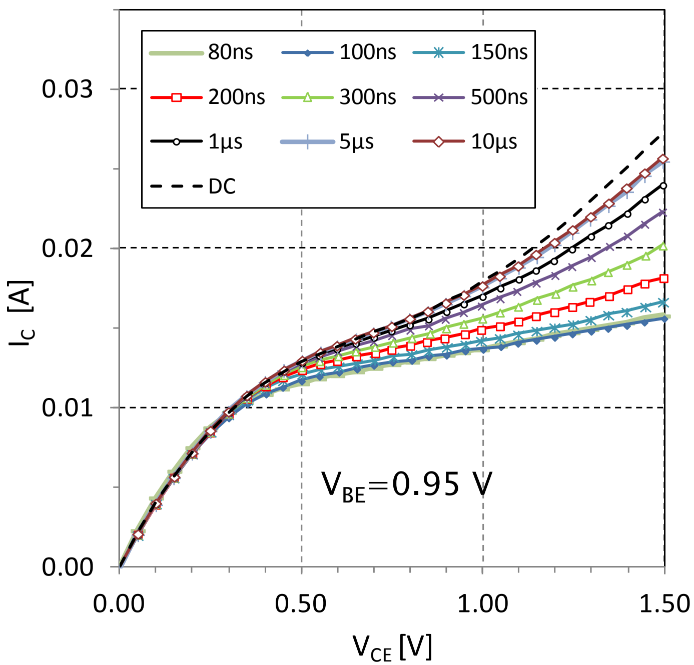
- Pulse width
  $Tw_{min} \geq 70ns$ DC
  $Tw_{min} \geq 100ns$ RF
- T_{rise} and $T_{fall} \geq 20ns$
- Frequency
  f [500MHz – 50 GHz]
- Duty-Cycle
  D [0.01% - 50%]
- Current resolution [µA]



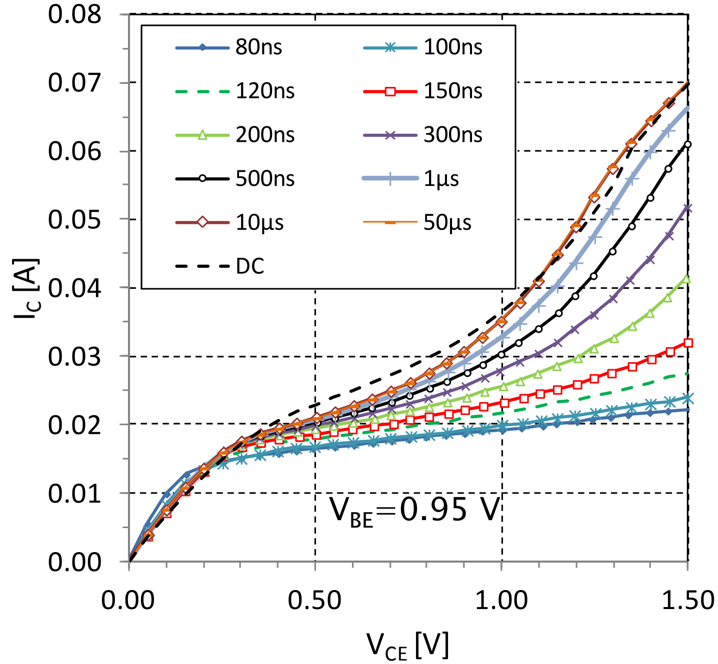


2 – Self-Heating characterization: pulsed measurements

❑ Pulsed I(V) for SiGe HBT (B3T ST Microelectronics)



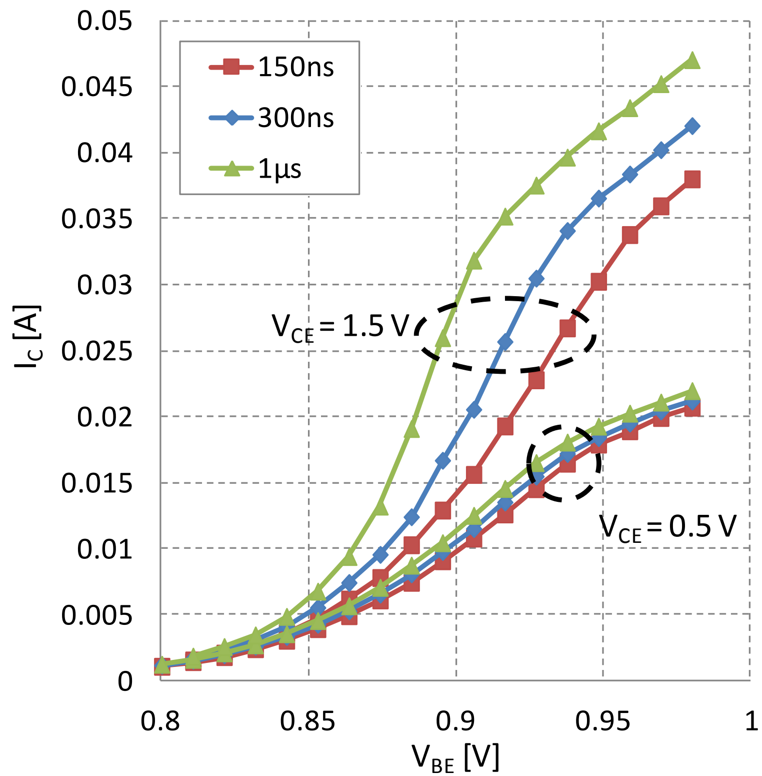
with W_E= 0.27 µm L_E = 5.0 µm



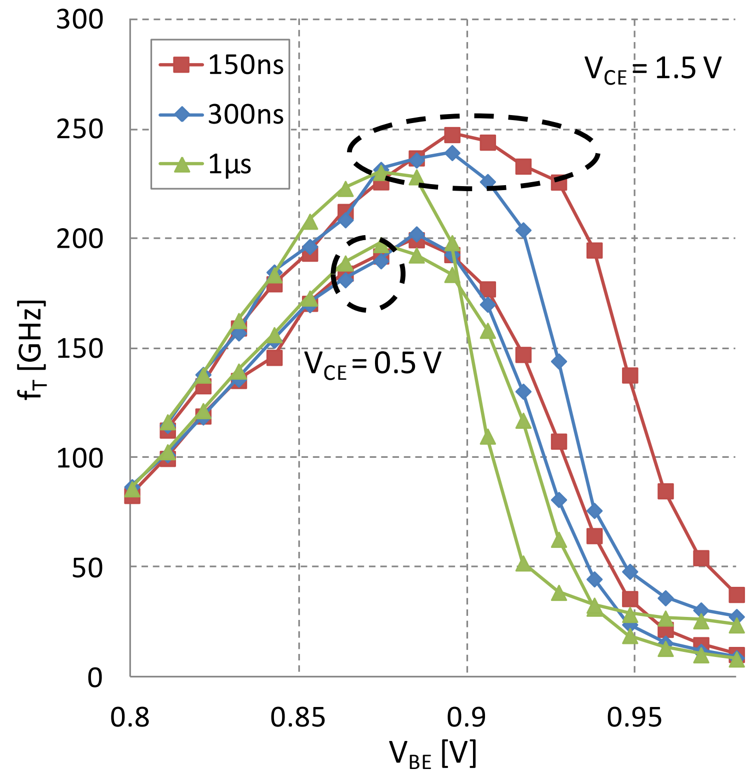
with W_E= 0.84 µm L_E = 5.0 µm

2 – Self-Heating characterization: pulsed measurements

❑ Pulsed I(V) and pulsed RF for SiGe HBT with W_E= 0.84 µm L_E = 5.0 µm (B3T ST Microelectronics)



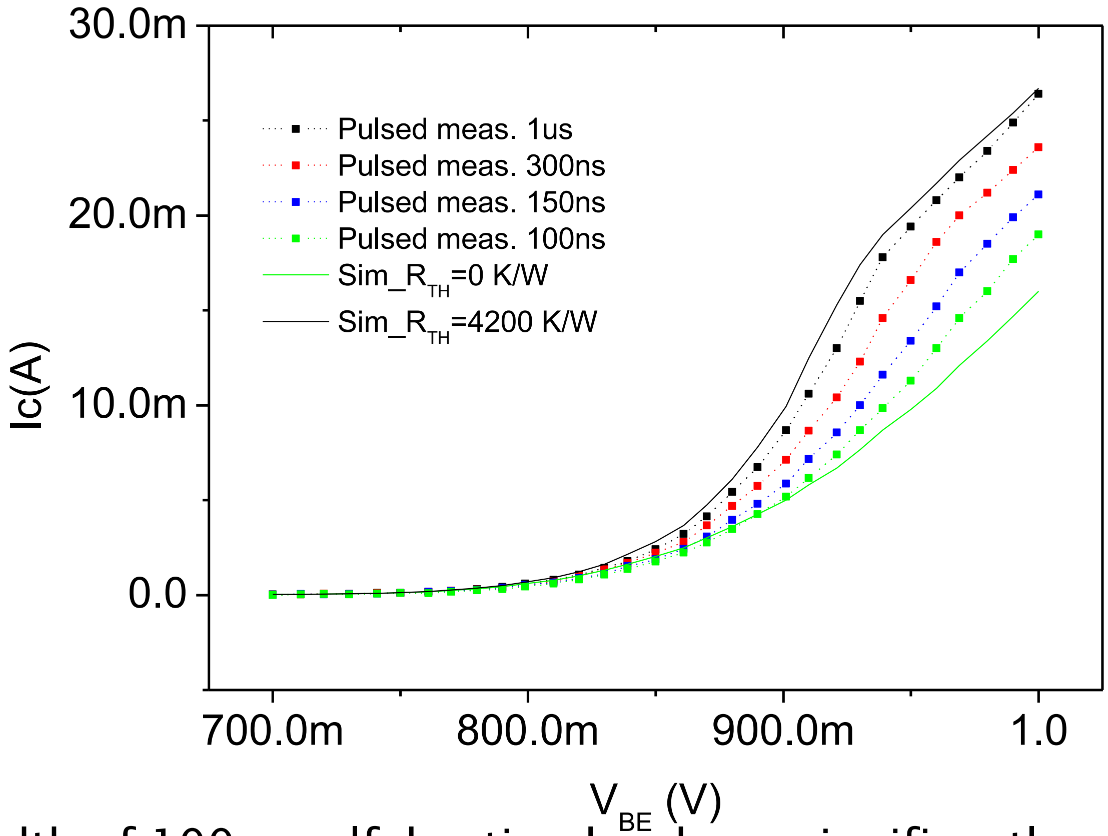
Collector current I_C vs. base emitter voltage V_{BE}



Transit frequency f_T vs. base emitter voltage V_{BE}

2 – Self-Heating characterization: pulsed measurements

❑ Isothermal measurement?



For a pulse width of 100ns self-heating has been significantly reduced

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3 – TCAD and compact modelling

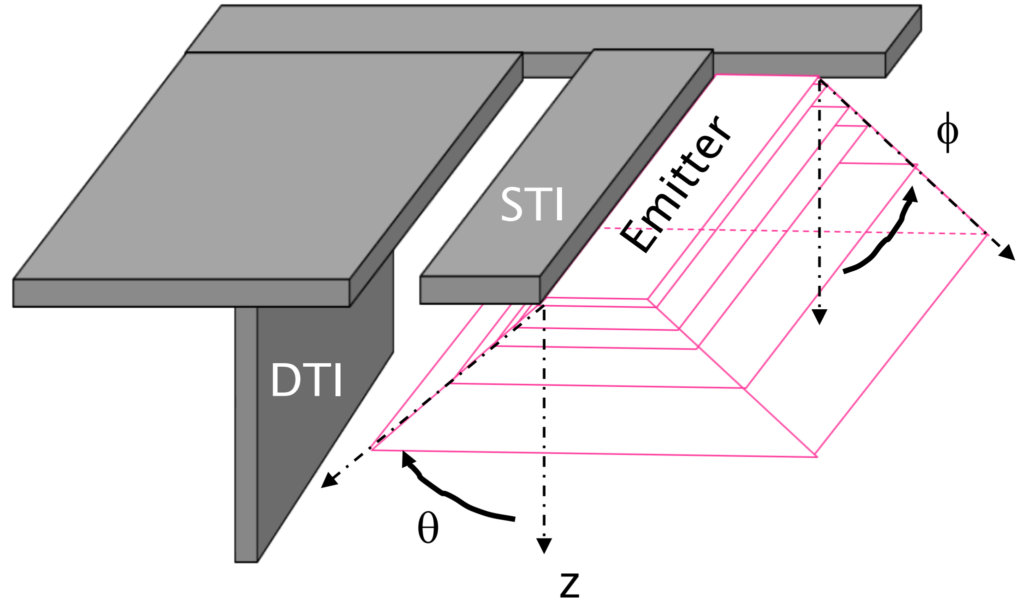
Main challenges

- Improvement of accuracy in TCAD simulation
  - Implement full structure including backend
  - Use accurate and thermal dependent model

- Compact model
  - Scalable and thermal dependent compact model
  - Improvement of network for frequency dependent model
  - Multifinger and mutual modelling
  - Backend dependent model

3 – TCAD and Compact model: recursive scalable compact model

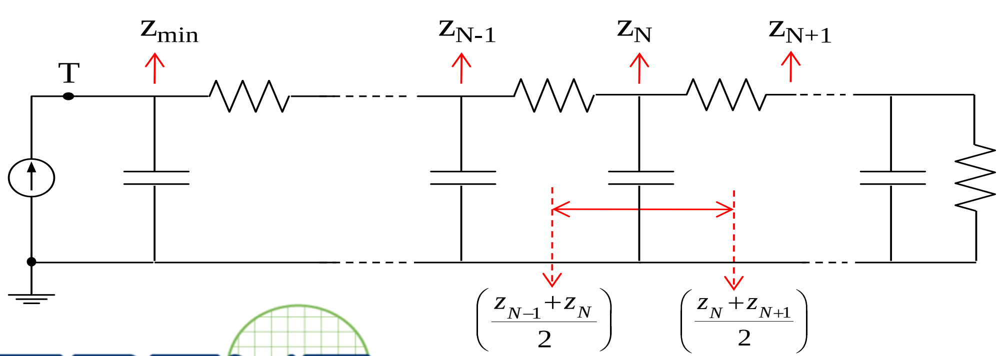
$$\int_{z_N}^{z_{N+1}} R(z)dz = \int \frac{dz}{\kappa A(z)} = \frac{1}{\kappa(aW_E - bL_E)} \cdot \ln\left(\frac{az+L_E}{bz+W_E}\right)\Bigg|_{z_N}^{z_{N+1}}$$



$$\int C(z)dz = \int C_p \rho A(z)dz$$

$$= \frac{C_p \rho}{6}\left(2abz^3 + 3\left(aW_E + bL_E\right)z^2 + 6L_E W_E z\right)\Bigg|_{\frac{(z_{N-1}+z_N)}{2}}^{\frac{(z_N+z_{N+1})}{2}}$$

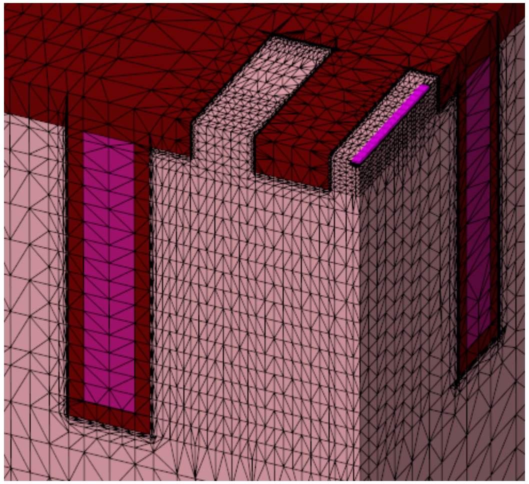
2 fitting parameters for the whole set of devices

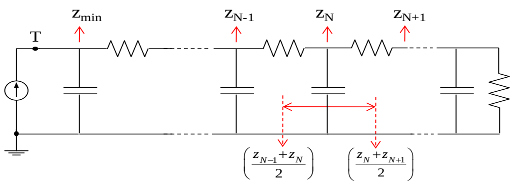


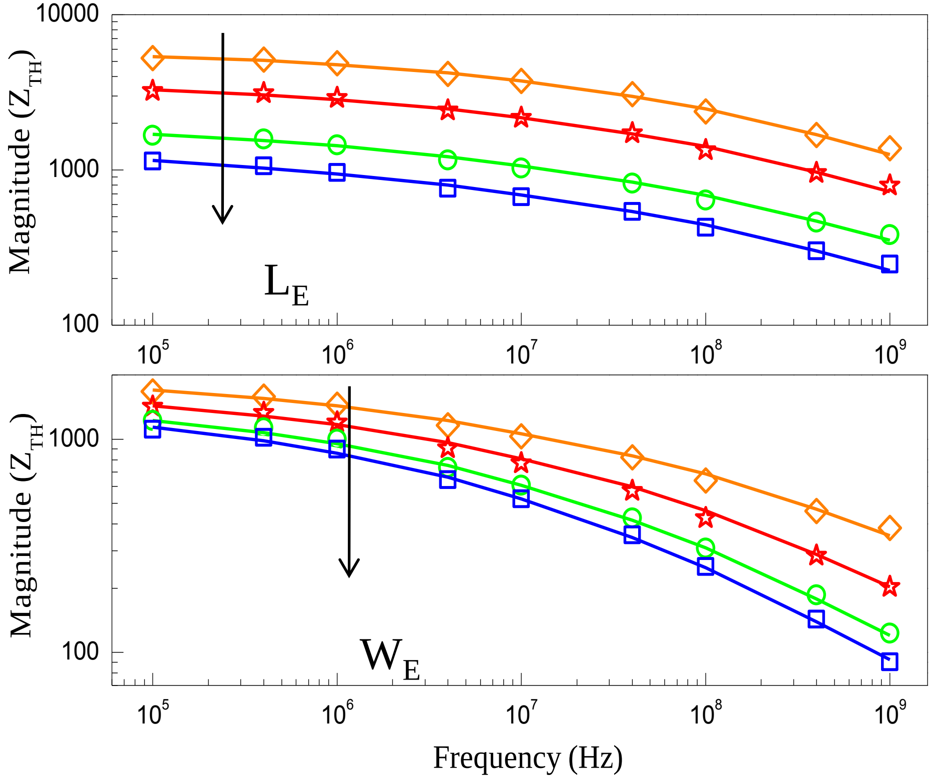
$$Z = Z_{min} \exp(\beta N)$$

3 – TCAD and Compact model: recursive scalable compact model

TCAD vs model : Thermal Impedance







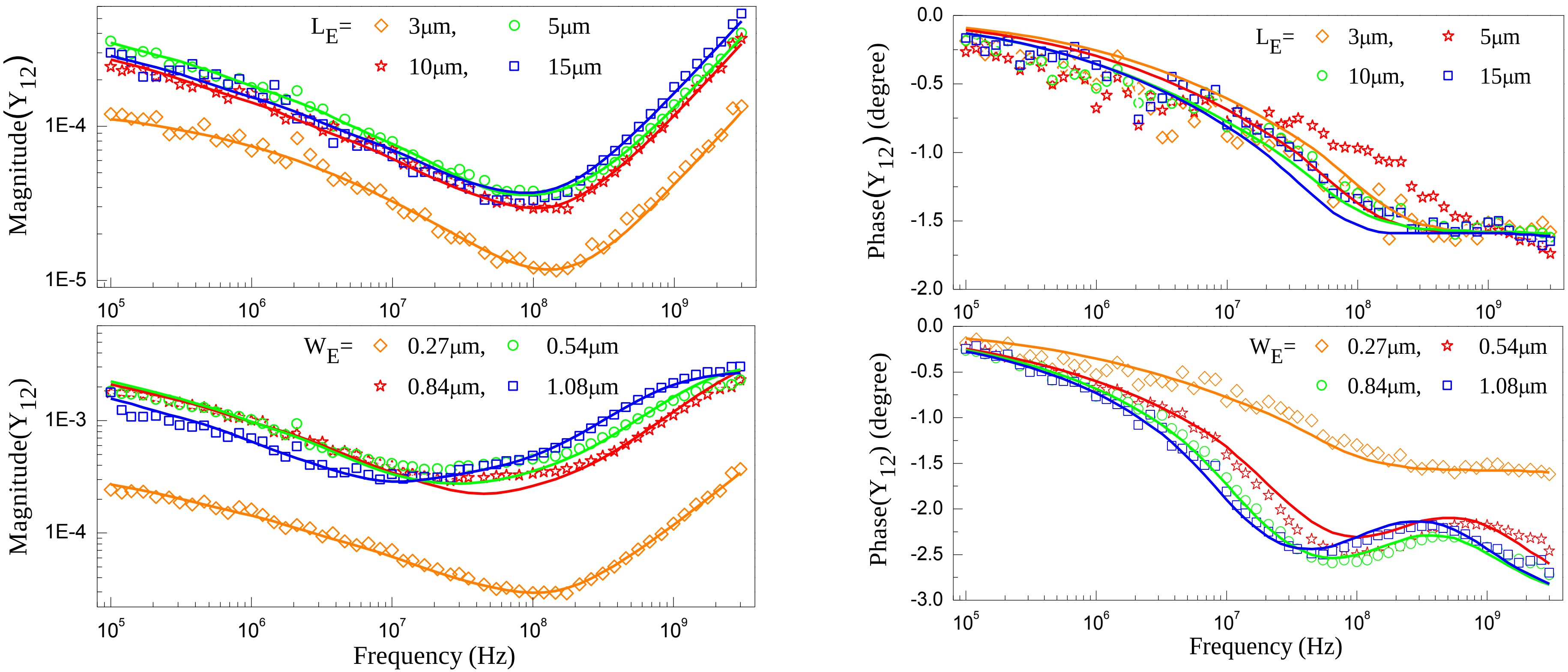
Symbols → TCAD simulation

Lines → Extracted with scalable electro-thermal network

3 – TCAD and Compact model: recursive scalable compact model

Measurement vs model : Y parameters

DUT Technology → STMicroelectronics BiCMOS9MW (CBEBC)



Symbols → Measurements

Lines → Compact model simulation

➢ Fast to use and good agreement with measurement but :

- Two fitting parameters needed (not predictive)
- Power dependence is not taken into account

3 – TCAD and Compact model: thermal dependent simulation

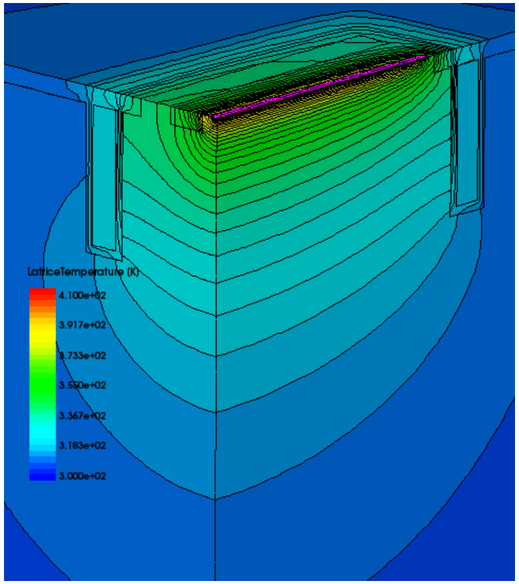
❑ Temperature dependent thermal conductivity (κ) of silicon

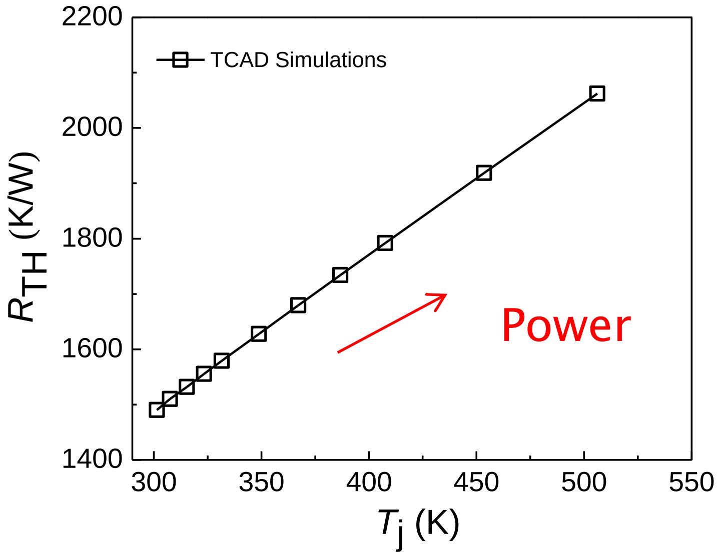
$$\kappa(T) = \frac{1}{\kappa_a + \kappa_b T + \kappa_c T^2}$$

$\kappa_a = 0.03$ cmKW^{-1},

$\kappa_b = 1.56 \times 10^{-3}$ cmW^{-1}

$\kappa_c = 1.65 \times 10^{-6}$ cmK^{-1}W^{-1}

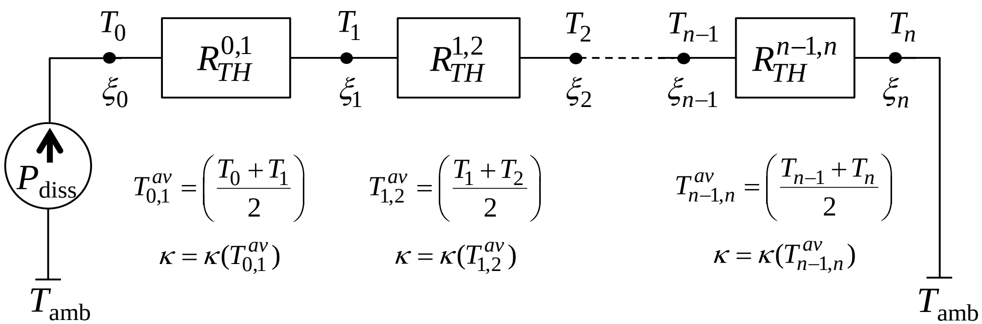


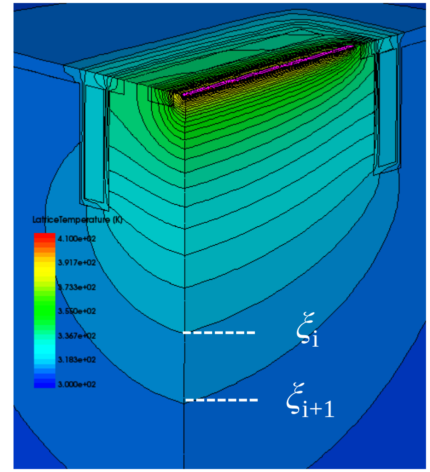


⇒ Temperature dependency is not negligible

3 – TCAD and Compact model: scalable and thermal dependant approach

Electro-thermal network :





Temperature T_i at ξ_i :

$$T_0 = T_{amb} + P_{diss} \cdot \left[R_{TH}^{0,1}\left(T_{0,1}^{av}\right) + R_{TH}^{1,2}\left(T_{1,2}^{av}\right) + \cdots + R_{TH}^{n-1,n}\left(T_{n-1,n}^{av}\right) \right]$$

$$T_1 = T_{amb} + P_{diss} \cdot \left[R_{TH}^{1,2}\left(T_{1,2}^{av}\right) + R_{TH}^{2,3}\left(T_{2,3}^{av}\right) + \cdots + R_{TH}^{n-1,n}\left(T_{n-1,n}^{av}\right) \right]$$

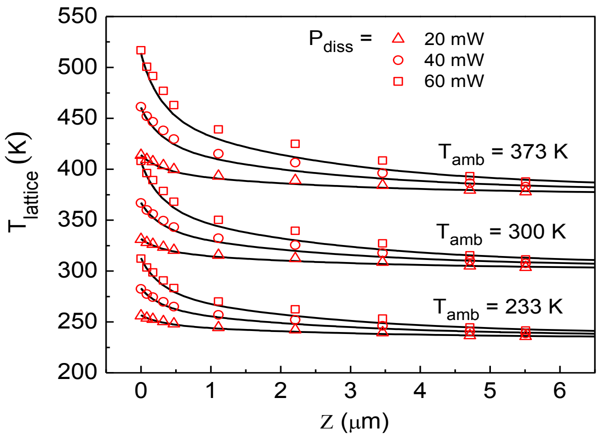
$$\vdots$$

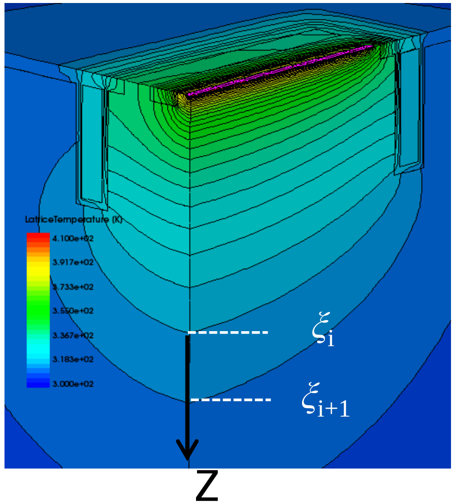
$$T_{n-1} = T_{amb} + P_{diss} \cdot \left[R_{TH}^{n-1,n}\left(T_{n-1,n}^{av}\right) \right]$$

$$T_n = T_{amb}$$

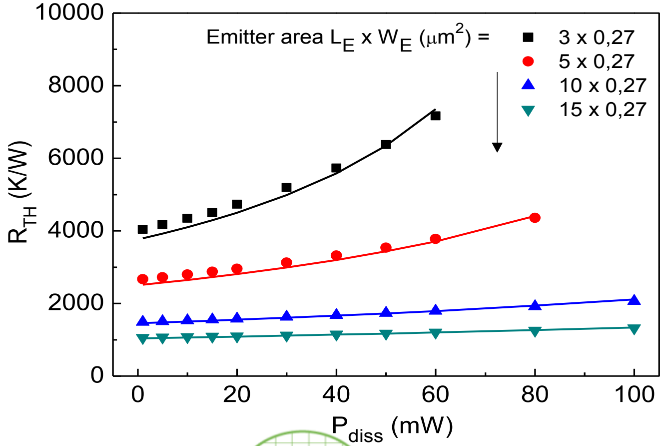
3 – TCAD and Compact model: scalable and thermal dependant approach

- Lattice temperature along z at different P_{diss} and T_{amb} :



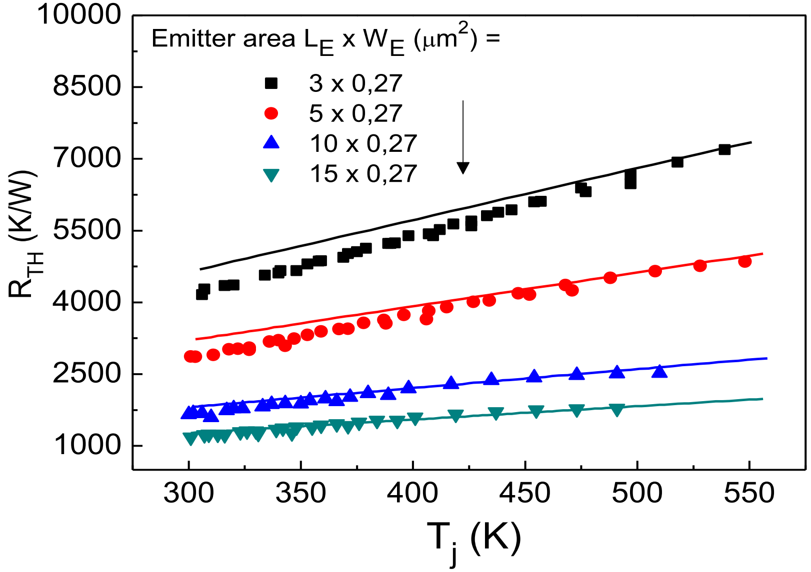


- Thermal resistance



3 – TCAD and Compact model: scalable and thermal dependant approach

Comparison with measurements

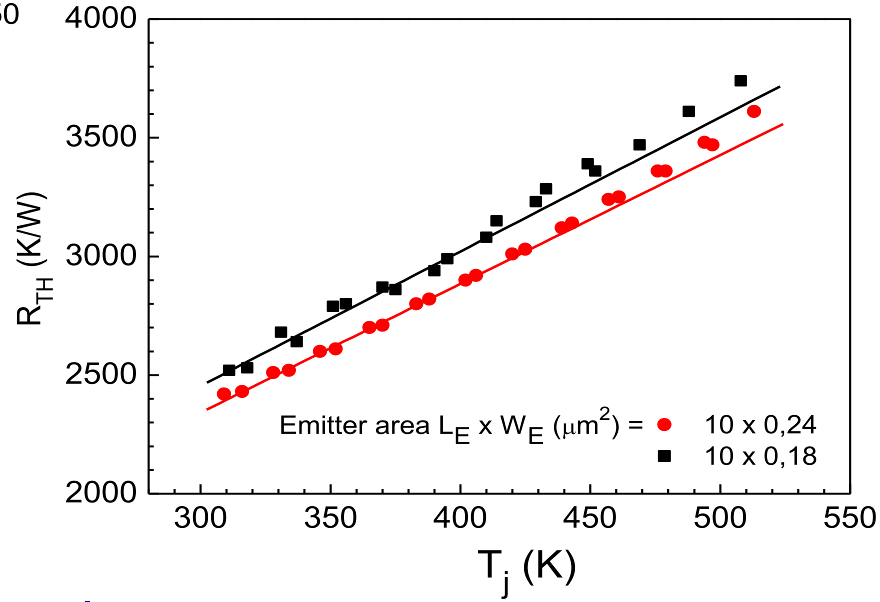


STMicroelectronics HBT

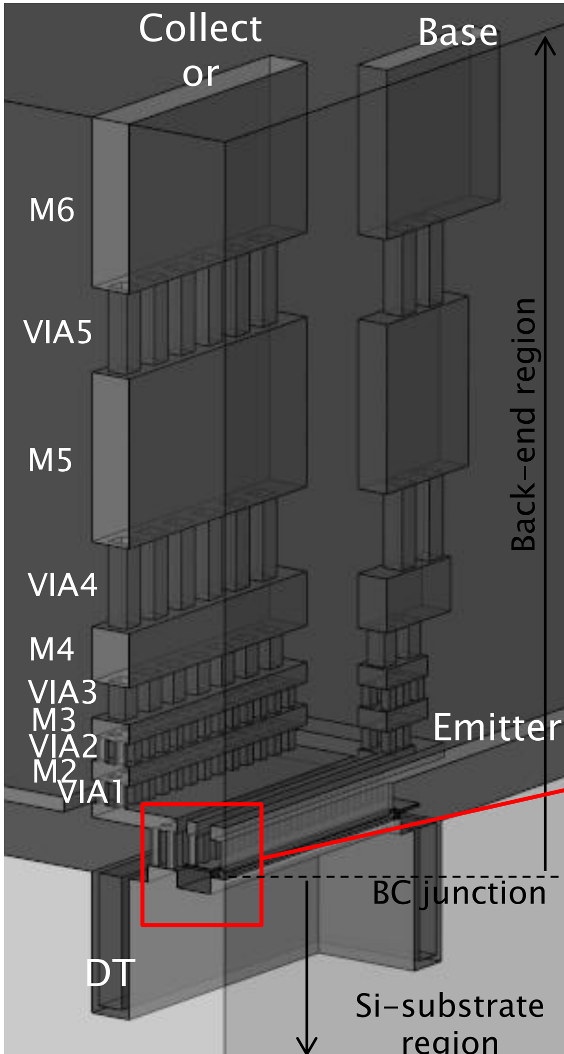
[Ref] A. Chantre, et al. “Pushing conventional SiGe HBT technology towards ‘Dotfive’ terahertz,” in *Microwave Integrated Circuits Conference (EuMIC), 2010 European*, 2010, pp. 21-24.

Infineon HBT

[Ref] M. Schwerd, et al. “A manufacturable 0.35 /spl mu/m 150 GHz f/sub T/ SiGe:C bipolar RF technology,” in *2003 Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, 2003. Digest of Papers*, 2003, pp. 10-13.

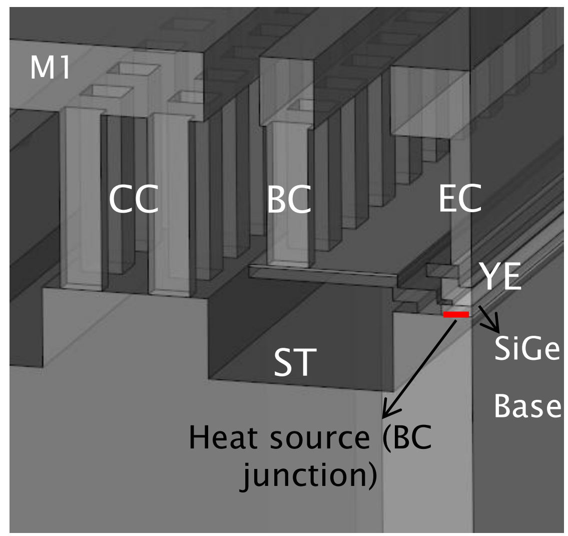


3 – TCAD and Compact model: Impact of the back-end layers on junction temperature rise



- Trench isolated SiGe HBT
- Configuration – CBEBC
- Heat source:

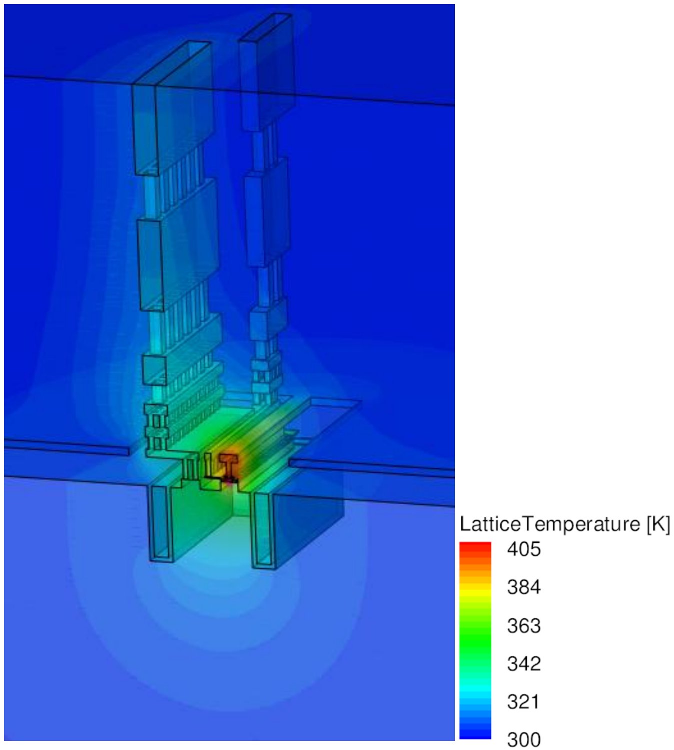
$L_E \times W_E = 9.88 \times 0.15\ \mu m^2$

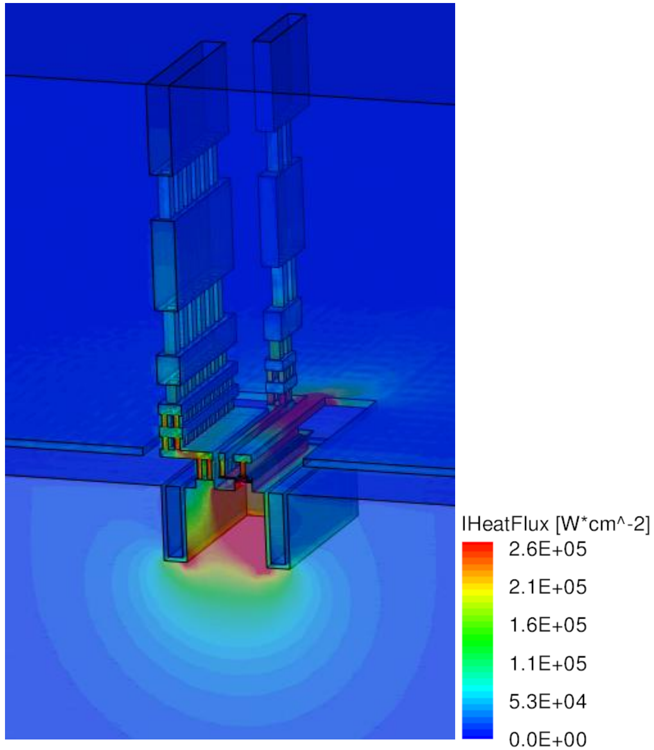


3 – TCAD and Compact model: Impact of the back-end layers on junction temperature rise

❑ Heat flux and lattice temperature distribution at steady state condition

- Power density at BC junction: 40 mW/µm^2



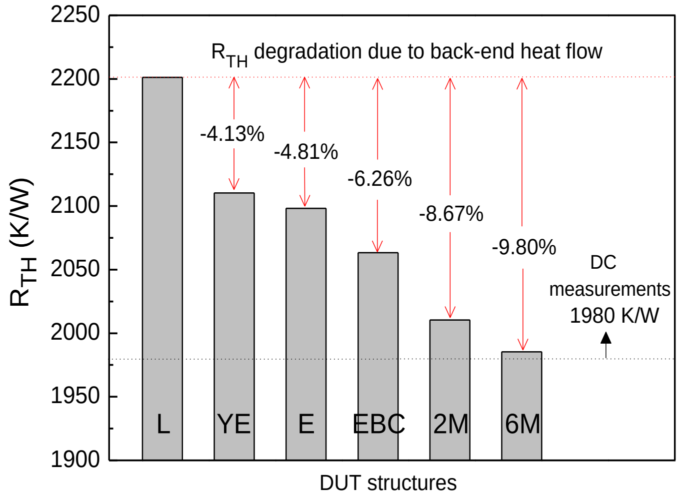


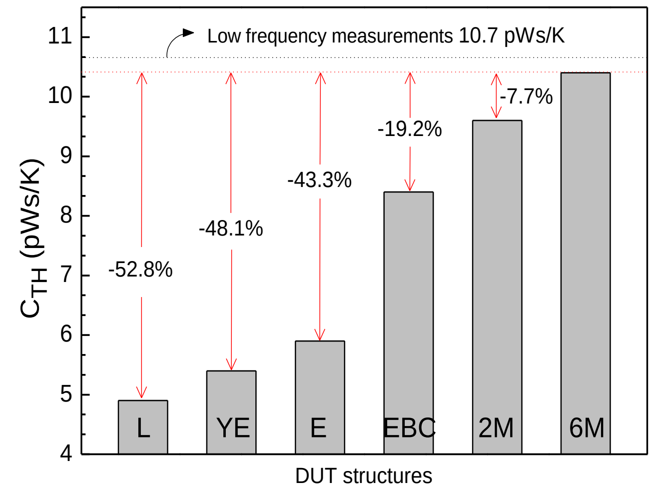
- Configuration – CBE , L_E x W_E = 9.88 x 0.15 µm^2

3 – TCAD and Compact model: Impact of the back-end layers on junction temperature rise

❑ R_{TH} and C_{TH} extraction from TCAD

Symbol	Device structure
L	Lower part
YE	+ upto Y-shape Emitter
E	+ Emitter contact
EBC	+ Base and Collector contacts
M1	+ First metal layer
M2	+ Up to second metal layer
M6	+ Up to six metal layer

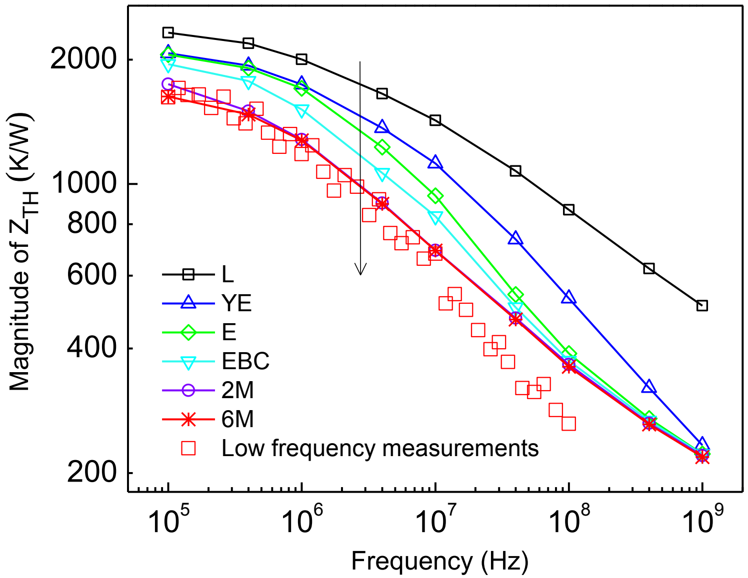


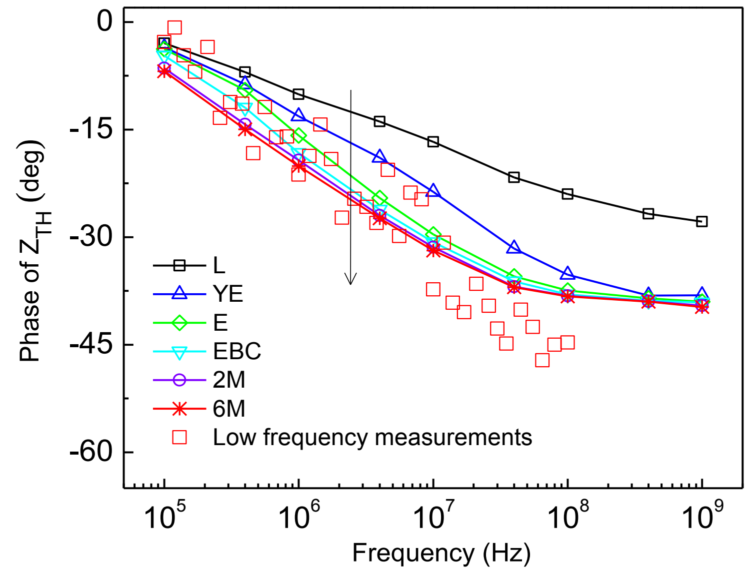


- Configuration – CBEBC ($\frac{1}{4}$ DUT) , L_E x W_E = 9.88 x 0.15 μm^2

3 – TCAD and Compact model: Impact of the back-end layers on junction temperature rise

❑ Z_{TH}: Comparison between TCAD simulations and measurements





- Configuration – CBEBC ($\frac{1}{4}$ DUT) , L_E x W_E = 9.88 x 0.15 μm^2

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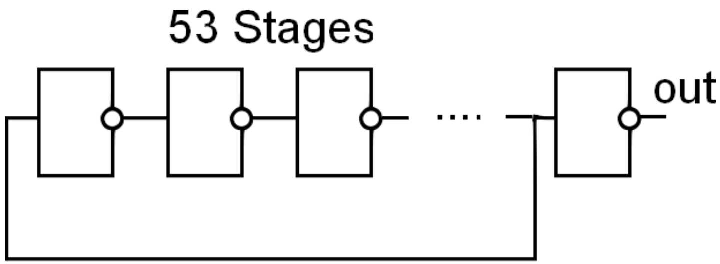
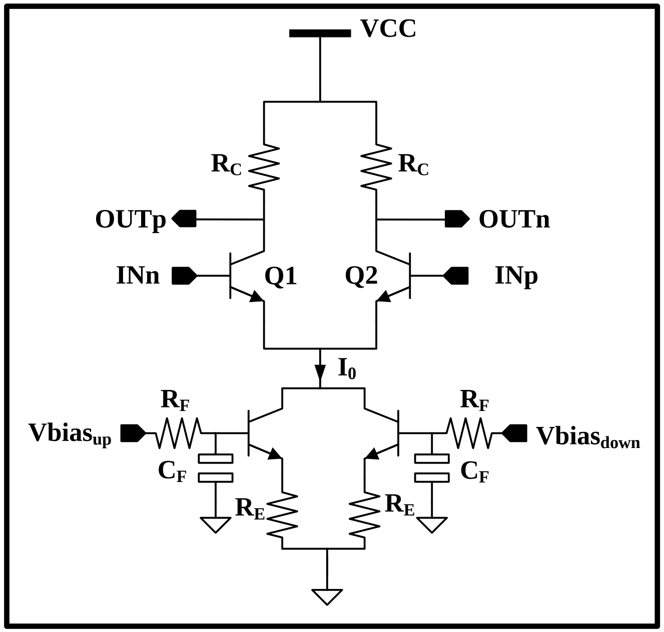
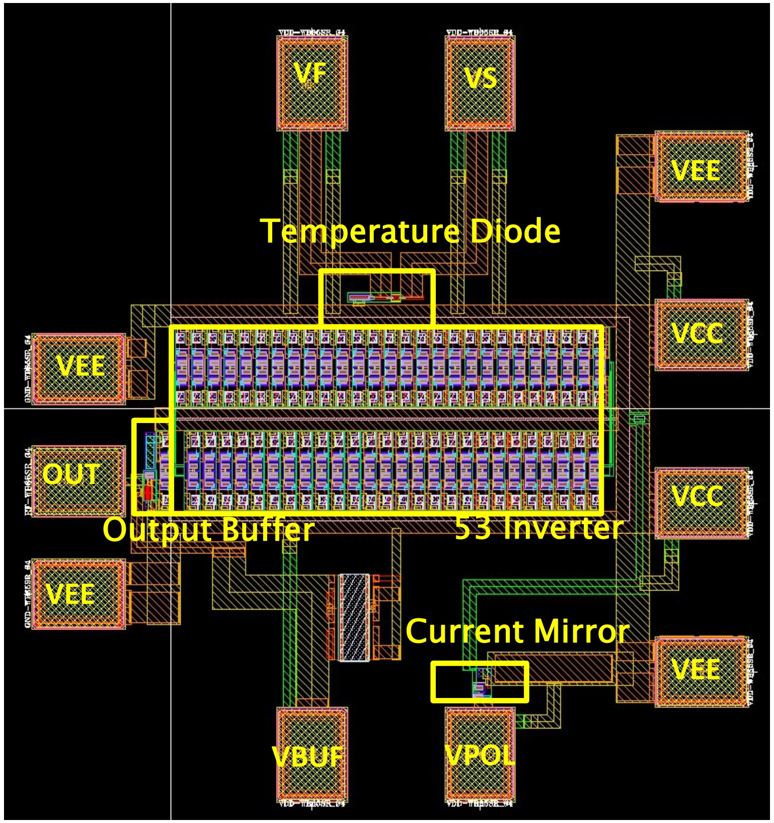
4 - Application circuit

Benchmarking Circuit for B5T (STMicroelectronics)



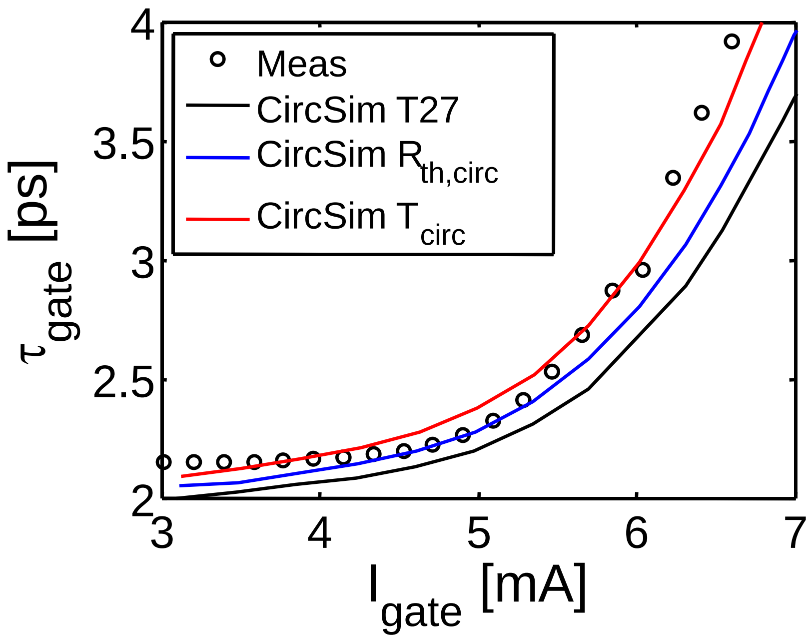




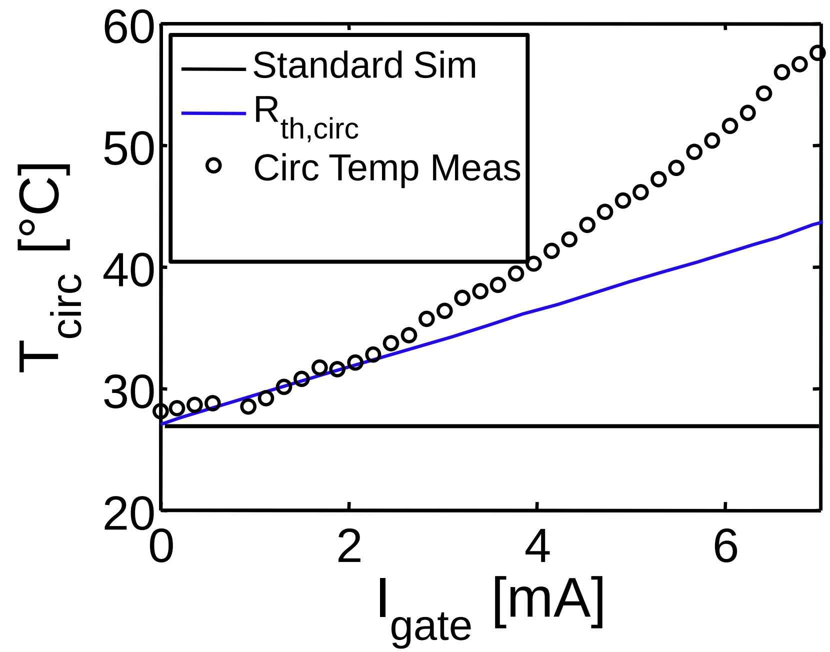
4 - Application circuit

Propagation Gate Delay: $$t_{gate} = \frac{1}{2 \cdot 53 \cdot f_{osc}}$$

$$T_{circ} = T_a + R_{th,circ} \frac{P_{diss}}{A_{circ}}$$



Propagation gate delay vs. current per inverter gate



Circuit temperature vs. current per inverter gate

Transistor Coupling modelling is needed

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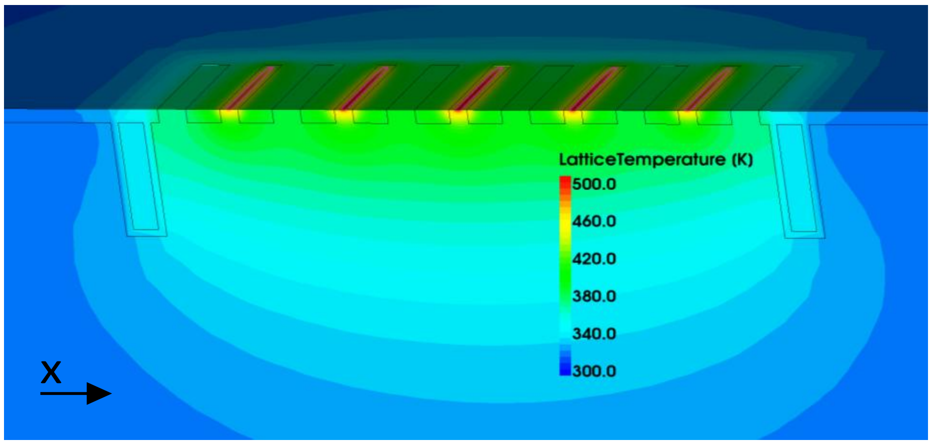
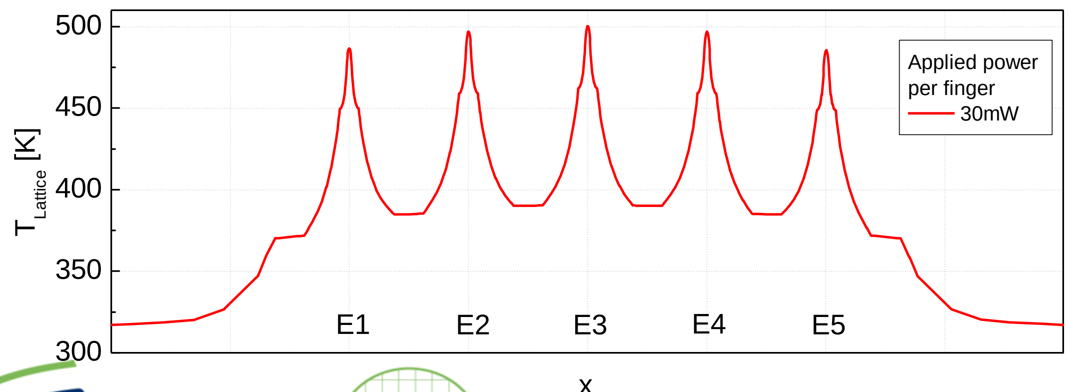
5 – Test structures for multifinger devices

- Heat sources are equal to effective emitter area and have been placed with exact technological (B5T) distances
- Heat sources surrounded by SiO2 (STI) and the whole structure is surrounded by SiO2 filled with Poly Silicon (DTI)



Lattice temperature distribution inside the device for an applied power of 30mW

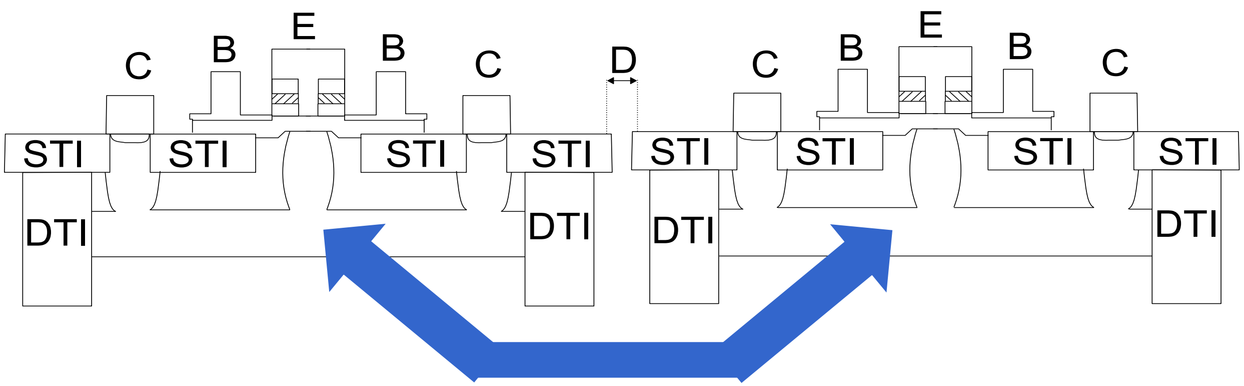


temperature difference between center and side fingers of ΔT≈17K

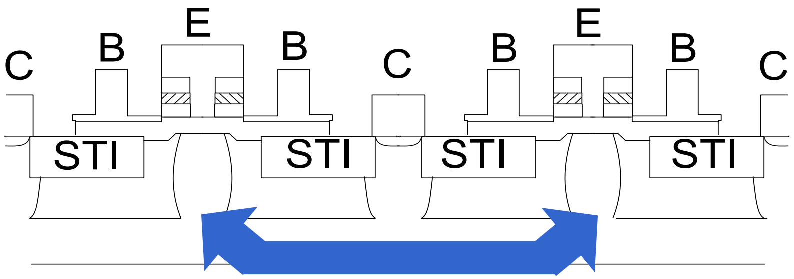
5 – Test structures for multi-finger devices

- Multi transistors have shallow trench isolation (STI) between emitter and collector contact and are separated with a deep trench isolation (DTI)
  - Multi-finger transistors share collector contact of the neigboring transistor → emitters (heat sources) are much closer + missing DTI → increased thermal coupling

Inter Device Coupling:

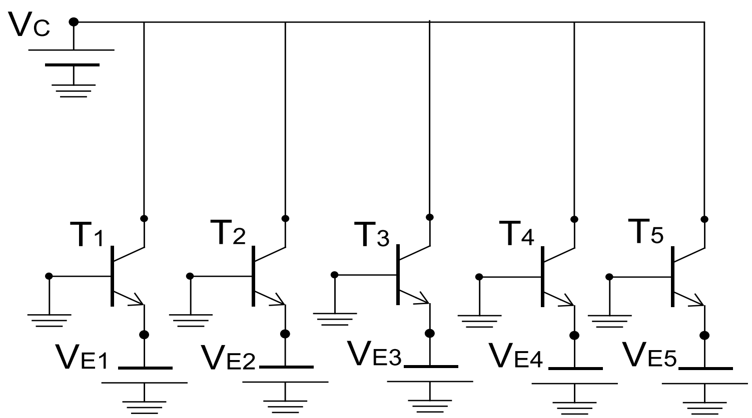


Intra Device Coupling:

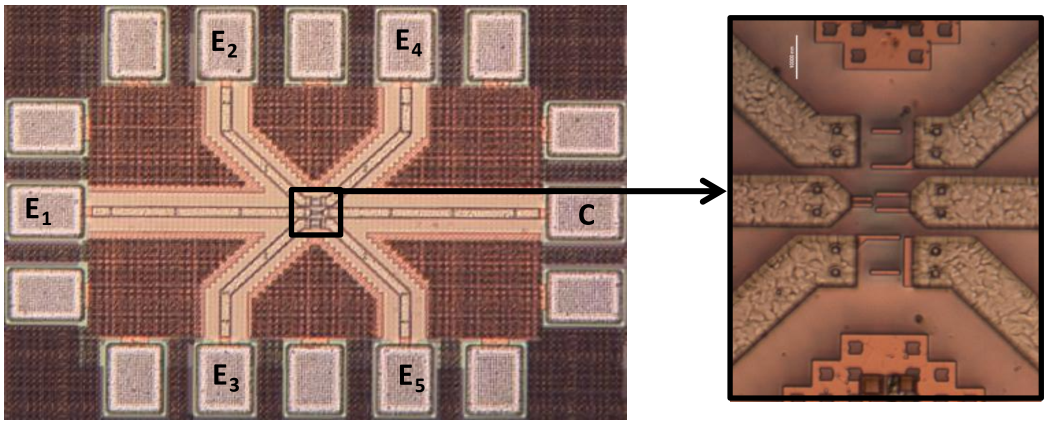


5 – Test structures for multi-finger devices

- Each finger can be used either for heating or sensing
- $I_E(V_{BE})$ characteristic to sense the temperature at low current densities
- Various heat/sense combinations are possible
- Embedded with GSG pads to allow RF measurements and avoid oscillations



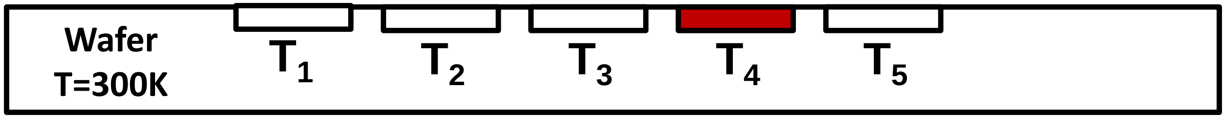
Schematic diagram of test structure

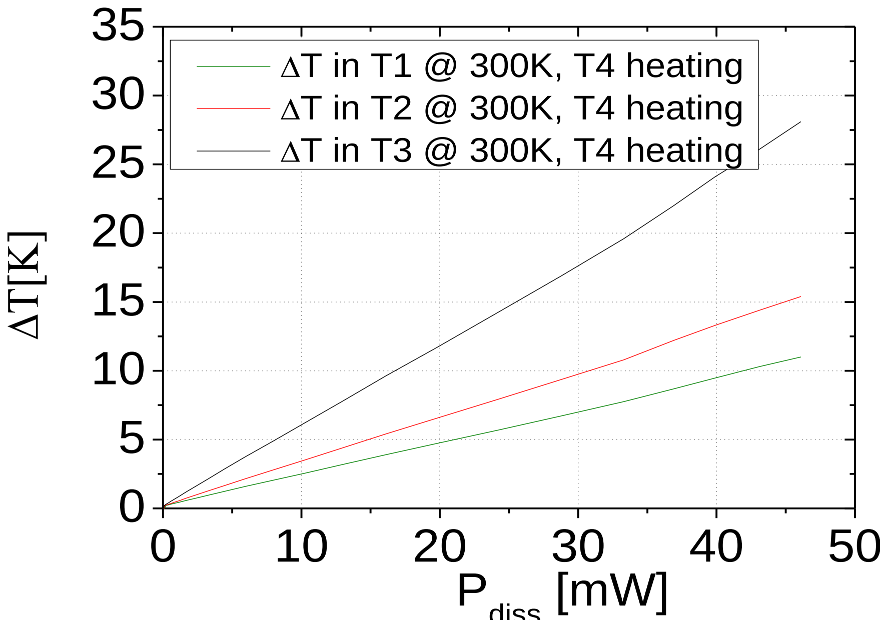


Micrograph of test structure

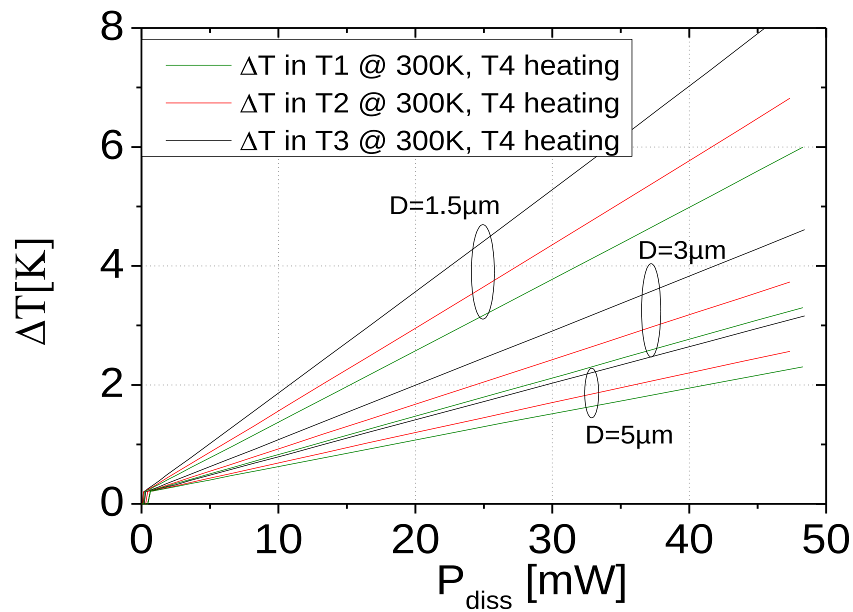
5 – Test structures for multi-finger devices

- T4 is heating, sensing transistors were forced with an emitter current I_E of 1µA in order to measure the temperature (sensitivity of around -1.55mV/K)





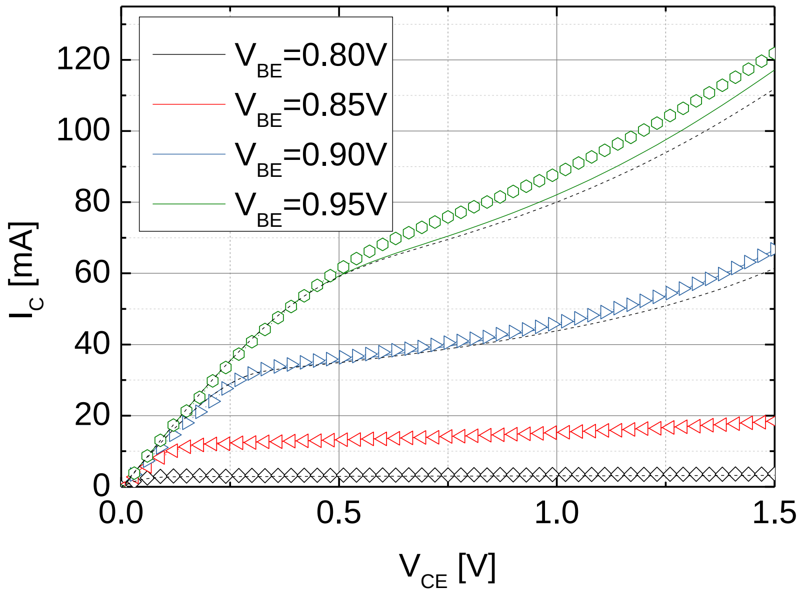
Intra device coupling in multi-finger transistor



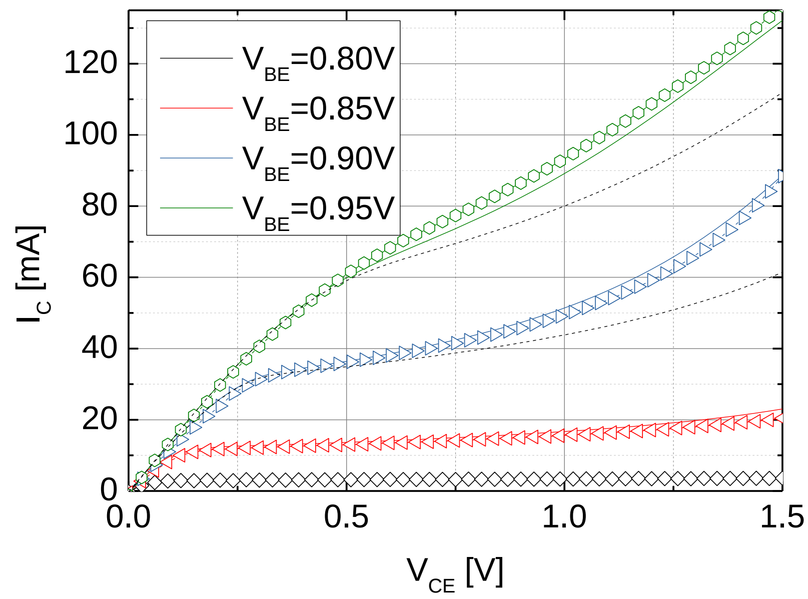
Inter device coupling in multi-transistor array

5 – Test structures for multi-finger devices

Inter device coupling



Intra device coupling



Measured (symbols) and simulated (lines) output characteristics for V_{BE}=[0.80, 0.85, 0.9, 0.95]V for five fingers working in parallel (Simulations without thermal coupling effect (dashed lines)).

6 - Summary

- 80ns pulsed DC and RF bench has been used for SiGe HBT characterisation => measurement is not isothermal but self-heating is reduced
- TCAD have highlighted that R_{TH}/C_{TH} depends of back-end
- Two compact models have been developed
  - recursive and scalable
  - predictive, scalable and power dependant
- Multi-finger devices have been characterised and modelled using specific test structure.
- Self-heating has been evaluated at circuit level and used to correct simulation

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