Title: Electro-thermal characterization and modelling

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Open Bipolar Workshop
3 October 2013, Bordeaux
1- Introduction

2 – Self-Heating Characterization
   - Low frequency S parameters
   - Pulsed DC and S parameters

3 – TCAD and compact modeling
   - Scalable compact model
     - Recursive
     - Thermal dependant
   - TCAD: Impact of back end

4 - Application circuit
   - Ring oscillator

5 – Parameter extraction using test structures
   - Multi-finger coupling

6 - Summary
Motivation

- Improved SiGe HBT performance ($f_{\text{max}}$ of 500GHz)
  \[ \Rightarrow \text{new spectrum of sub-millimeter-wave applications} \] [1]

Medical applications

Security

High Speed Communication

- In FP7 DOT7, the new target is $f_{\text{max}}$ of 700GHz while CATRENE RF2THz plan to have a large scale integration

Motivation

- **Improvement of technology => impact on self-heating?**

<table>
<thead>
<tr>
<th>Advanced technology</th>
<th>Drawbacks</th>
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<tbody>
<tr>
<td>Vertical down scaling</td>
<td>Increase of power density in devices</td>
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<tr>
<td>Trench isolation</td>
<td>Heat confinement by insulated wall</td>
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<tr>
<td>Large scale integration</td>
<td>Mutual heating – heat flow from neighboring device</td>
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- Performance and reliability limitation

- Compact model accuracy needs some improvements

- Characterization and parameter extraction method needs to be revisited.
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6 - Summary
Many methods have been developed to extract $R_{TH}$
- DC measurement, many authors have proposed some methods

What about $C_{TH}$?
- Transient measurement
  - Pulse generator and scope (Limitation: calibration of test set)
  - Pulse DC measurement
- Low frequency S parameter

Getting quasi-isothermal data to simplify parameter extraction?
- Pulse DC and RF measurement
2 – Self-Heating characterization: Low frequency S parameters

Thermal impedance extraction

Low frequency S-parameter measurements:
- 100 kHz – 3 GHz,
- $V_{CE} = 1.5$ V
- $V_{BE} = 0.95$ V

DUT: $L_E \times W_E = 9.88 \times 0.15 \, \mu m^2$

Normalized Thermal Impedance $\rightarrow$

$$Z_{TH}(\omega) = \frac{\left( y_{12}(\omega) - y_{12}^{AC} \right)}{\left( y_{12}^{DC} - y_{12}^{AC} \right)} \cdot \frac{\left( I_C + V_{BE} y_{12}^{DC} + V_{CE} y_{22}^{DC} \right)}{\left( I_C + V_{BE} y_{12}(\omega) + V_{CE} y_{22}(\omega) \right)}$$


2 – Self-Heating characterization: Low frequency S parameters

Thermal impedance extraction (ST Microelectronics)

- Phase $Z_{TH}$ (mA)
- Frequency (Hz)
- Maximum phase shift

- Magnitude $\text{Mag}(n_{\text{normalized }}Z_{TH} (\text{dB})$ ~ -10 dB/dec
Experimental Setup

Pulsed measurement system characteristics:

- Pulse width
  \( T_{\text{w\_min}} \geq 70\text{ns} \) DC
  \( T_{\text{w\_min}} \geq 100\text{ns} \) RF
- \( T_{\text{rise}} \) and \( T_{\text{fall}} \) \( \geq 20\text{ns} \)
- Frequency
  \( f \ [500\text{MHz} \text{ – } 50 \text{ GHz}] \)
- Duty-Cycle
  \( D \ [0.01\% \text{ – } 50\%] \)
- Current resolution [\( \mu \text{A} \)]

**Diagram:**

- RF Pulse 50ns
- DC Pulse 200ns

**Legend:**

- RF PULSE
- DC PULSE
- OSCILLOSCOPE
2 – Self-Heating characterization: pulsed measurements

- Pulsed I(V) for SiGe HBT (B3T ST Microelectronics)

with $W_E = 0.27 \ \mu m$ $L_E = 5.0 \ \mu m$

with $W_E = 0.84 \ \mu m$ $L_E = 5.0 \ \mu m$
2 – Self-Heating characterization: pulsed measurements

- Pulsed I(V) and pulsed RF for SiGe HBT with $W_E = 0.84 \, \mu m$ $L_E = 5.0 \, \mu m$
  (B3T ST Microelectronics)

Collector current $I_C$ vs. base emitter voltage $V_{BE}$

Transit frequency $f_T$ vs. base emitter voltage $V_{BE}$
For a pulse width of 100ns self-heating has been significantly reduced.
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3 – TCAD and compact modelling

Main challenges

- Improvement of accuracy in TCAD simulation
  - Implement full structure including backend
  - Use accurate and thermal dependent model

- Compact model
  - Scalable and thermal dependent compact model
  - Improvement of network for frequency dependent model
  - Multifinger and mutual modelling
  - Backend dependent model
3 – TCAD and Compact model: recursive scalable compact model

\[
\int_{z_N}^{z_{N+1}} R(z) \, dz = \int \frac{dz}{\kappa A(z)} = \frac{1}{\kappa(aW_E - bL_E)} \cdot \ln \left( \frac{a z + L_E}{b z + W_E} \right)_{z_N}^{z_{N+1}}
\]

\[
\int C(z) \, dz = \int C_p \rho A(z) \, dz
\]

\[
= \frac{C_p \rho}{6} \left( 2abz^3 + 3(aW_E + bL_E)z^2 + 6L_E W_E z \right)_{z_{N-1}}^{z_{N+1}}
\]

2 fitting parameters for the whole set of devices

\[
Z = Z_{\text{min}} \exp(\beta N)
\]
3 – TCAD and Compact model: recursive scalable compact model

TCAD vs model: Thermal Impedance

Symbols → TCAD simulation

Lines → Extracted with scalable electro-thermal network
3 – TCAD and Compact model: recursive scalable compact model

Measurement vs model: Y parameters

DUT Technology → STMicroelectronics BiCMOS9MW (CBEBC)

Symbols → Measurements

Lines → Compact model simulation

- Fast to use and good agreement with measurement but:
  - Two fitting parameters needed (not predictive)
  - Power dependence is not taken into account
3 – TCAD and Compact model: thermal dependent simulation

- Temperature dependent thermal conductivity ($\kappa$) of silicon

\[
\kappa(T) = \frac{1}{\kappa_a + \kappa_b T + \kappa_c T^2}
\]

\[
\kappa_a = 0.03 \text{ cmKW}^{-1}, \\
\kappa_b = 1.56 \times 10^{-3} \text{ cmW}^{-1}, \\
\kappa_c = 1.65 \times 10^{-6} \text{ cmK}^{-1}\text{W}^{-1}
\]

Temperature dependency is not negligible
3 – TCAD and Compact model: scalable and thermal dependant approach

Electro–thermal network:

\[ P_{\text{diss}} \]

\[ T_0 = T_{\text{amb}} + P_{\text{diss}} \cdot \left[ R_{TH}^{0,1} \left( T_{0,1}^{\text{av}} \right) + R_{TH}^{1,2} \left( T_{1,2}^{\text{av}} \right) + \cdots + R_{TH}^{n-1,n} \left( T_{n-1,n}^{\text{av}} \right) \right] \]

\[ T_1 = T_{\text{amb}} + P_{\text{diss}} \cdot \left[ R_{TH}^{1,2} \left( T_{1,2}^{\text{av}} \right) + R_{TH}^{2,3} \left( T_{2,3}^{\text{av}} \right) + \cdots + R_{TH}^{n-1,n} \left( T_{n-1,n}^{\text{av}} \right) \right] \]

\[ \vdots \]

\[ T_{n-1} = T_{\text{amb}} + P_{\text{diss}} \cdot \left[ R_{TH}^{n-1,n} \left( T_{n-1,n}^{\text{av}} \right) \right] \]

\[ T_n = T_{\text{amb}} \]

Temperature \( T_i \) at \( \xi_i \):

\[ T_i^{\text{av}} = \frac{T_i + T_{i+1}}{2} \]

\[ \kappa = \kappa(T^{\text{av}}) \]
3 – TCAD and Compact model: scalable and thermal dependant approach

- Lattice temperature along z at different $P_{\text{diss}}$ and $T_{\text{amb}}$:

![Graph showing lattice temperature along z at different $P_{\text{diss}}$ and $T_{\text{amb}}$.]

- Thermal resistance

![Graph showing thermal resistance vs. $P_{\text{diss}}$.]

Emitter area $L_E \times W_E \, (\mu m^2) = 3 \times 0.27$, $5 \times 0.27$, $10 \times 0.27$, $15 \times 0.27$
Comparison with measurements

**R_{TH} (K/W) vs. T_j (K)**

- Emitter area \( L_E \times W_E \) (\( \mu m^2 \)) =
  - 3 x 0.27
  - 5 x 0.27
  - 10 x 0.27
  - 15 x 0.27

**STMicroelectronics HBT**


**Infineon HBT**

3 – TCAD and Compact model: Impact of the back-end layers on junction temperature rise

- Trench isolated SiGe HBT
- Configuration – CBEBC
  - Heat source:
  \[ L_E \times W_E = 9.88 \times 0.15 \, \mu m^2 \]
3 – TCAD and Compact model: Impact of the back-end layers on junction temperature rise

- Heat flux and lattice temperature distribution at steady state condition
  - Power density at BC junction: 40 mW/μm²

- Configuration – CBE, \( L_E \times W_E = 9.88 \times 0.15 \mu m^2 \)
3 – TCAD and Compact model: Impact of the back-end layers on junction temperature rise

- $R_{TH}$ and $C_{TH}$ extraction from TCAD

<table>
<thead>
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<th>Symbol</th>
<th>Device structure</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>Lower part</td>
</tr>
<tr>
<td>YE</td>
<td>+ upto Y-shape Emitter</td>
</tr>
<tr>
<td>E</td>
<td>+ Emitter contact</td>
</tr>
<tr>
<td>EBC</td>
<td>+ Base and Collector contacts</td>
</tr>
<tr>
<td>M1</td>
<td>+ First metal layer</td>
</tr>
<tr>
<td>M2</td>
<td>+ Up to second metal layer</td>
</tr>
<tr>
<td>M6</td>
<td>+ Up to six metal layer</td>
</tr>
</tbody>
</table>

- Configuration – CBEBC ($\frac{1}{4}$ DUT), $L_E \times W_E = 9.88 \times 0.15 \, \mu m^2$
3 – TCAD and Compact model: Impact of the back-end layers on junction temperature rise

- $Z_{TH}$: Comparison between TCAD simulations and measurements

- Configuration – CBEBC ($\frac{1}{4}$ DUT), $L_E \times W_E = 9.88 \times 0.15 \ \mu m^2$
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Benchmarking Circuit for B5T (STMicroelectronics)

53 Stages

![Diagrams and schematic of the benchmarking circuit](image_url)
4 - Application circuit

Propagation gate delay vs. current per inverter gate

Gate Delay:

\[ t_{gate} = \frac{1}{2 \cdot 53 \cdot f_{osc}} \]

Circuit temperature vs. current per inverter gate

\[ T_{circ} = T_a + R_{th,circ} \frac{P_{diss}}{A_{circ}} \]

Transistor Coupling modelling is needed
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5 – Test structures for multifinger devices

- Heat sources are equal to effective emitter area and have been placed with exact technological (B5T) distances
- Heat sources surrounded by SiO2 (STI) and the whole structure is surrounded by SiO2 filled with Poly Silicon (DTI)

Lattice temperature distribution inside the device for an applied power of 30mW

Temperature difference between center and side fingers of $\Delta T \approx 17 \text{K}$
5 – Test structures for multi-finger devices

- Multi transistors have shallow trench isolation (STI) between emitter and collector contact and are separated with a deep trench isolation (DTI).
- Multi-finger transistors share collector contact of the neighboring transistor → emitters (heat sources) are much closer + missing DTI → increased thermal coupling.

Inter Device Coupling:

Intra Device Coupling:
5 – Test structures for multi-finger devices

- Each finger can be used either for heating or sensing
- $I_E(V_{BE})$ characteristic to sense the temperature at low current densities
  - Various heat/sense combinations are possible
- Embedded with GSG pads to allow RF measurements and avoid oscillations

Schematic diagram of test structure  
Micrograph of test structure
5 – Test structures for multi-finger devices

- T4 is heating, sensing transistors were forced with an emitter current $I_E$ of 1µA in order to measure the temperature (sensitivity of around -1.55mV/K)

\[ \Delta T \text{ in } T_i @ 300K, T4 \text{ heating} \]

Intra device coupling in multi-finger transistor

Inter device coupling in multi-transistor array
5 – Test structures for multi-finger devices

Measured (symbols) and simulated (lines) output characteristics for $V_{BE}=[0.80, 0.85, 0.9, 0.95]V$ for five fingers working in parallel (Simulations without thermal coupling effect (dashed lines)).
6 - Summary

- 80ns pulsed DC and RF bench has been used for SiGe HBT characterisation => measurement is not isothermal but self-heating is reduced
- TCAD have highlighted that $R_{TH}/C_{TH}$ depends of back-end
- Two compact models have been developed
  - recursive and scalable
  - predictive, scalable and power dependant
- Multi-finger devices have been characterised and modelled using specific test structure.
- Self-heating has been evaluated at circuit level and used to correct simulation
Acknowledgement

This work is part of the:

- **RF2THz** is a CATRENE project (Cluster for Application and Technology Research in Europe on NanoElectronics).

- **DOTFIVE** and **DOTSEVEN project** supported by the European Commission through the Seventh Framework Program for Research and Technological Development.

- We would like to thank **ST Microelectronics, Infineon Technologies and XMOD Technologies**.