

# CATRENE – CT209 – RF2THZ SiSOC

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**Title: Passive Integration and Packaging for mm-wave applications**

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**Open Bipolar Workshop  
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# Motivations - challenge

- ❑ Breakthrough in terms of passive quality factor can be shown to improve phase noise performances, as required by the communication standards
- ❑ Recent achievements done on active devices in order to compete with III-V devices -> effort to be put on passive devices
- ❑ At mm-wave, packaging will play a significant role and must be considered as a block of the design -> co-design approach
- ❑ Unfortunately Si substrate is lossy vs. GaAs substrate
- ❑ How can we provide in fast way accurate modelling
- ❑ Two ways to improve passive:
  - Improve the technology process
  - Consider different device architecture

**RF2THz**

# Contents

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- ❑ Introduction – Perceived state of the art
- ❑ Going to elite passive devices
  - Considering process update
  - Considering new layout architecture for passive devices
- ❑ Improve performances with customized package solution
- ❑ Conclusion – Look ahead

# Introduction

## □ HF, real need to pay careful attention to the electrical characteristics of everything along the signal path!

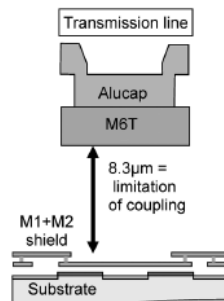
- Metal **type** (Cu/Al/Ag/Au) and **thickness** -> electrical resistance, inductance
- Dielectric material:
  - **Relative permittivity** : parasitic capacitance value (the lower the better)
  - **Dielectric losses** ( $\tan \delta$ ) : signal attenuation (behaviour @ HF?)
  - **Thickness** : parasitic capacitance value/Line quality factor
- Metal **roughness**:
  - Impact on resistive part of the attenuation
- Substrate **resistivity**:
  - Passive devices quality factor
  - With or without **DTI/shield** and which pattern to be used
  - **Homogeneity** within the bulk
  - **Via** between top copper (if any!) and Al:

## □ Electrical resistance must be as low as possible (!) with acceptable dimensions

# Perceived state of the art

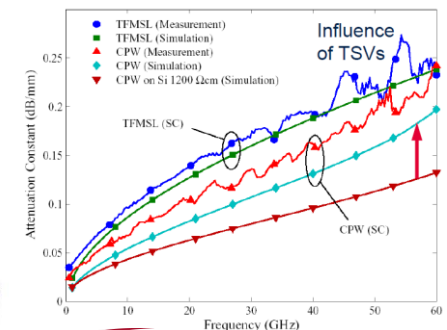
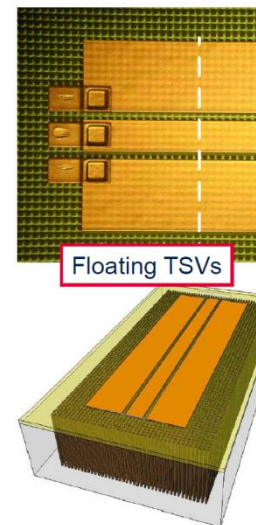
- ❑ Already Tlines measured in 7<sup>th</sup> generation of NXP BiCMOS (coplanar with poly and/or metal1 shield)
  - Al BEOL – Slow Wave architecture
  - $0,49 < \alpha < 0,78$  dB/mm @ 40 GHz
  - $0,56 < \alpha < 0,94$  dB/mm @ 50 GHz
  - Currently implemented with patterned metal1 shield in the DK
- ❑ 0,096 dB/mm @ 110 GHz !! already measured on Cu Lines deposited on LCP material (source )
- ❑ In the litterature:

*G Avenier et al.,  
JSSC 2009*



BACK-END DEVICES CHARACTERISTICS SUMMARY

| Device    | Charact. Value | Parameter                           | Comment  |
|-----------|----------------|-------------------------------------|----------|
| Line      | 50Ω            | 0.40dB/mm                           | at 40GHz |
|           |                | 0.50dB/mm                           | at 60GHz |
|           |                | 0.58dB/mm                           | at 77GHz |
| Induct. 1 | 74pH           | Q = 25.2                            | at 60GHz |
| Induct. 2 | 107pH          | Q = 24.0                            | at 77GHz |
| MIM       | 39pF           | $C_0 = 1.96\text{fF}/\mu\text{m}^2$ | at 25°C  |
|           |                | Leak. < 1nA/cm <sup>2</sup>         | at -5V   |
|           |                | BV > 28V                            | at 25°C  |



**infineon**

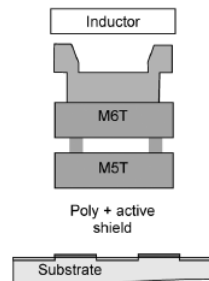
*M. Wojnowski, EuMW  
2008*

# Perceived state of the art

## ❑ Q4X coils generally made with M6 or M6+M5 (both Al)

- From NXP RF manual,  $Q > 17$  @ 2 GHz for a 1.5 nH device

## ❑ In the litterature



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| BV > 28V at 25°C                            |                |                            |          |

*G Avenier et al.,  
JSSC 2009*

## ❑ Differential varactors for LO designs

- Find a trade-off between losses and tuning range
- Provide accurate modeling and/or extraction

|                          | Multi-Finger varactor <sup>+</sup> | Multi-Finger varactor (with interconnect) <sup>+</sup> | IGV MOS varactor <sup>*</sup> |
|--------------------------|------------------------------------|--------------------------------------------------------|-------------------------------|
| TR                       | 36.9%                              | 31.9%                                                  | 29.5%                         |
| Q <sub>min</sub> (5GHz)  | 33                                 | 34                                                     | 50                            |
| Q <sub>min</sub> (10GHz) | 17                                 | 18                                                     | 40                            |
| Q <sub>min</sub> (40GHz) | 5                                  | 5                                                      | 7                             |
| Q <sub>max</sub> (5GHz)  | 84                                 | 95                                                     | 91                            |
| Q <sub>max</sub> (10GHz) | 42                                 | 47                                                     | 73                            |
| Q <sub>max</sub> (40GHz) | 10                                 | 12                                                     | 13                            |
| FOM (5GHz)               | 113 <sup>e9</sup>                  | 109 <sup>e9</sup>                                      | 111 <sup>e9</sup>             |
| FOM (10GHz)              | 107 <sup>e9</sup>                  | 103 <sup>e9</sup>                                      | 167 <sup>e9</sup>             |
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# Contents

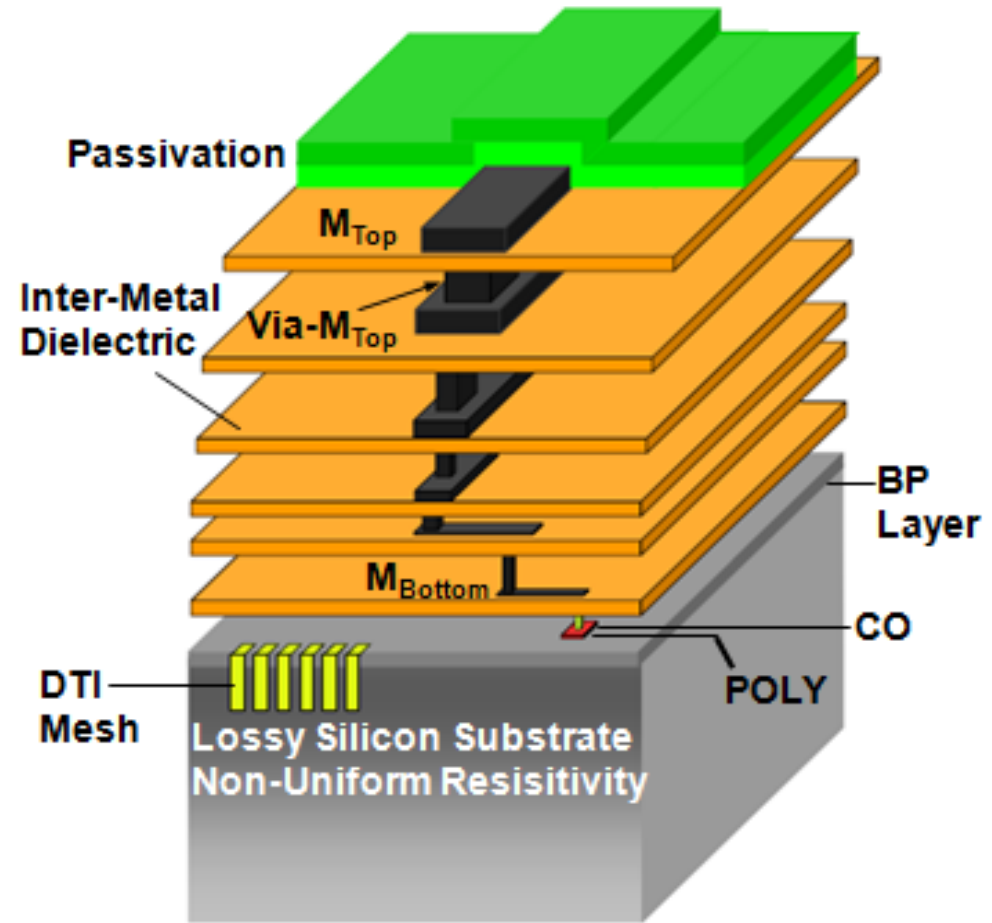
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- ❑ Introduction – Perceived state of the art
- ❑ **Going to elite passive devices**
  - Considering process update
  - Considering new layout architecture for passive devices
- ❑ **Improve performances with customized package solution**
- ❑ **Conclusion – Look ahead**

# Considering process update

## ❑ Elite passive devices will result from

- ILD/IMD thickness increase (distance between Back-End passive devices and substrate increased)
- Higher Substrate Resistivity (up to 750  $\Omega\cdot\text{cm}$ )
- Deep Trench Isolation implementation with/without new design
- Use a thick Copper IC layer on top of current BiCMOS process
- In combination with enhancement of devices architecture update (will be addressed later on)

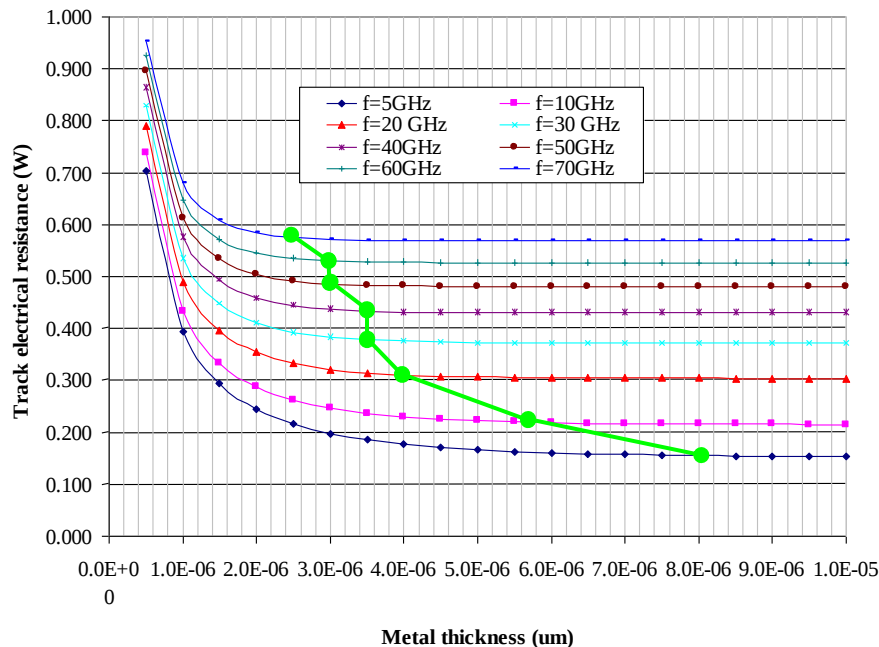


*Current NXP BiCMOS BEOL*

# Add top Copper on top of current process

## □ What is the right thickness of top copper?

- Applications (i.e., frequency driven)
- Trade-off between parasitic capacitances and resistive losses



C-band:  $t_{\text{opt}} = 8.0 \text{ um}$

X-band:  $t_{\text{opt}} = 5.5 \text{ um}$

Ku-band:  $t_{\text{opt}} = 4.0 \text{ um}$

K-band:  $t_{\text{opt}} = 3.5 \text{ um}$

Ka-band:  $t_{\text{opt}} = 3-3.5 \text{ um}$

V-band:  $t_{\text{opt}} = 2.5-3 \text{ um}$

$$R = \frac{\rho \cdot l}{S} = \frac{l}{2 \cdot w \cdot \delta \cdot \sigma_o \cdot \left(1 - e^{-t/2\delta}\right)}$$

$$\delta = \sqrt{\frac{1}{\sigma_o \cdot \mu_o \cdot \pi \cdot \text{freq}}}$$

$\delta$  is the skin depth

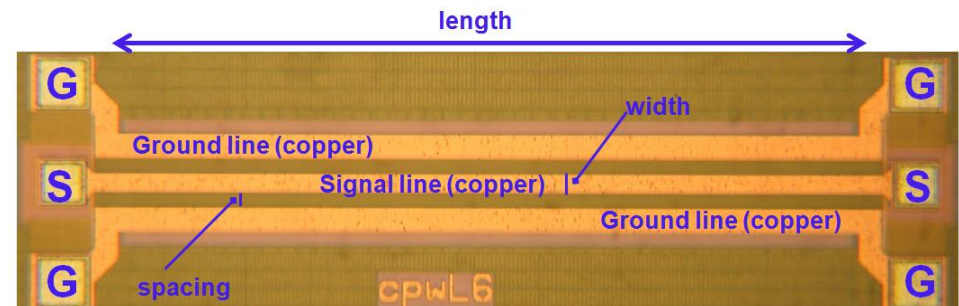
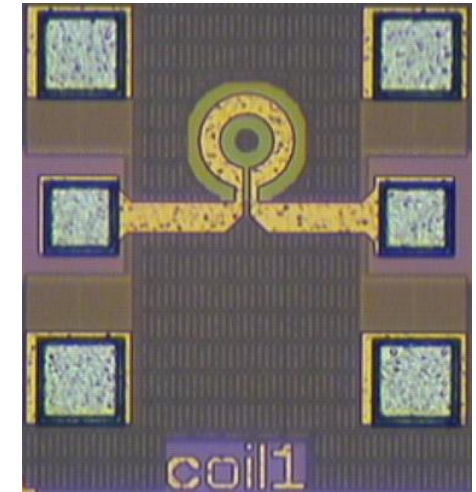
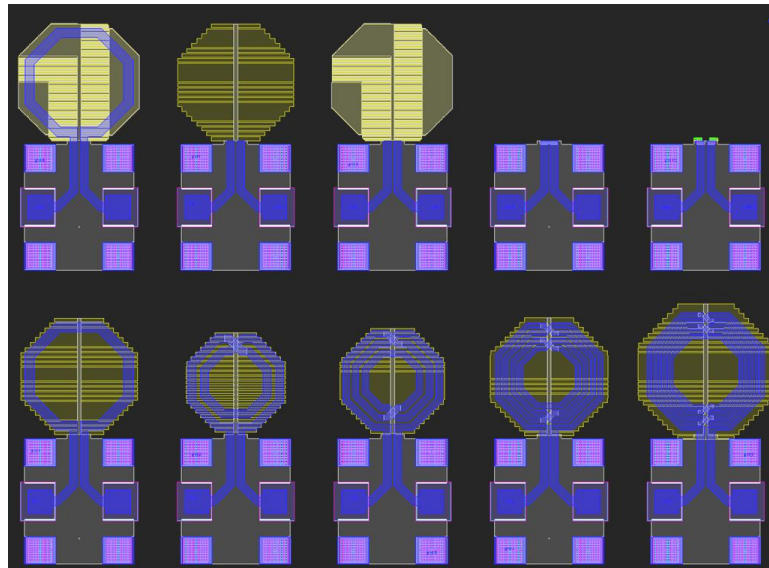
$\sigma_o$  the intrinsic conductivity of the metal

$\mu_o$  the vacuum permittivity

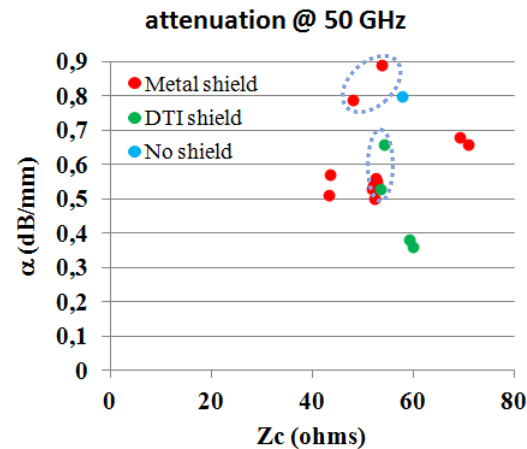
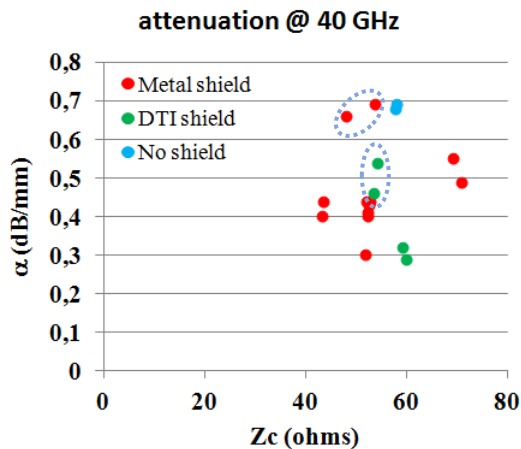
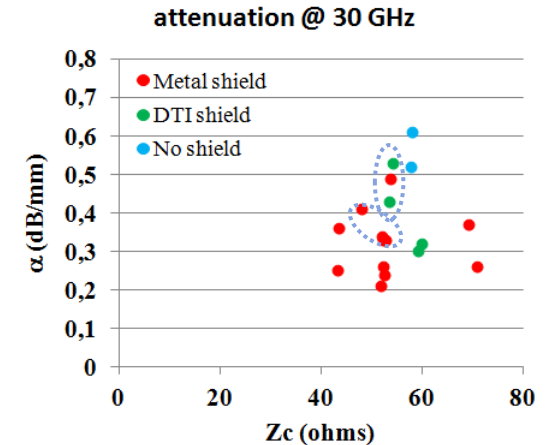
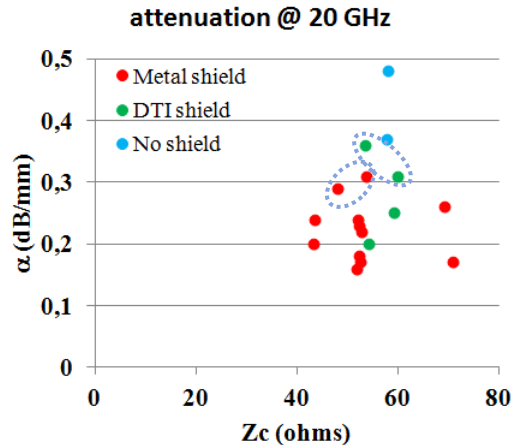
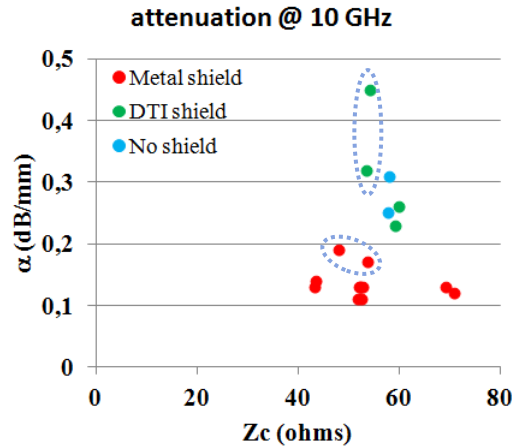
# Test structures description and results

## □ Full set of geometries designed on silicon

- Tlines (Coplanar & Micro Strip + different shield option)
- Small Cu Inductors (different shield option)
  - 70 to 120 pH devices
- Multi Turns Inductors (different shield option)
  - 0,5 to 8 nH devices

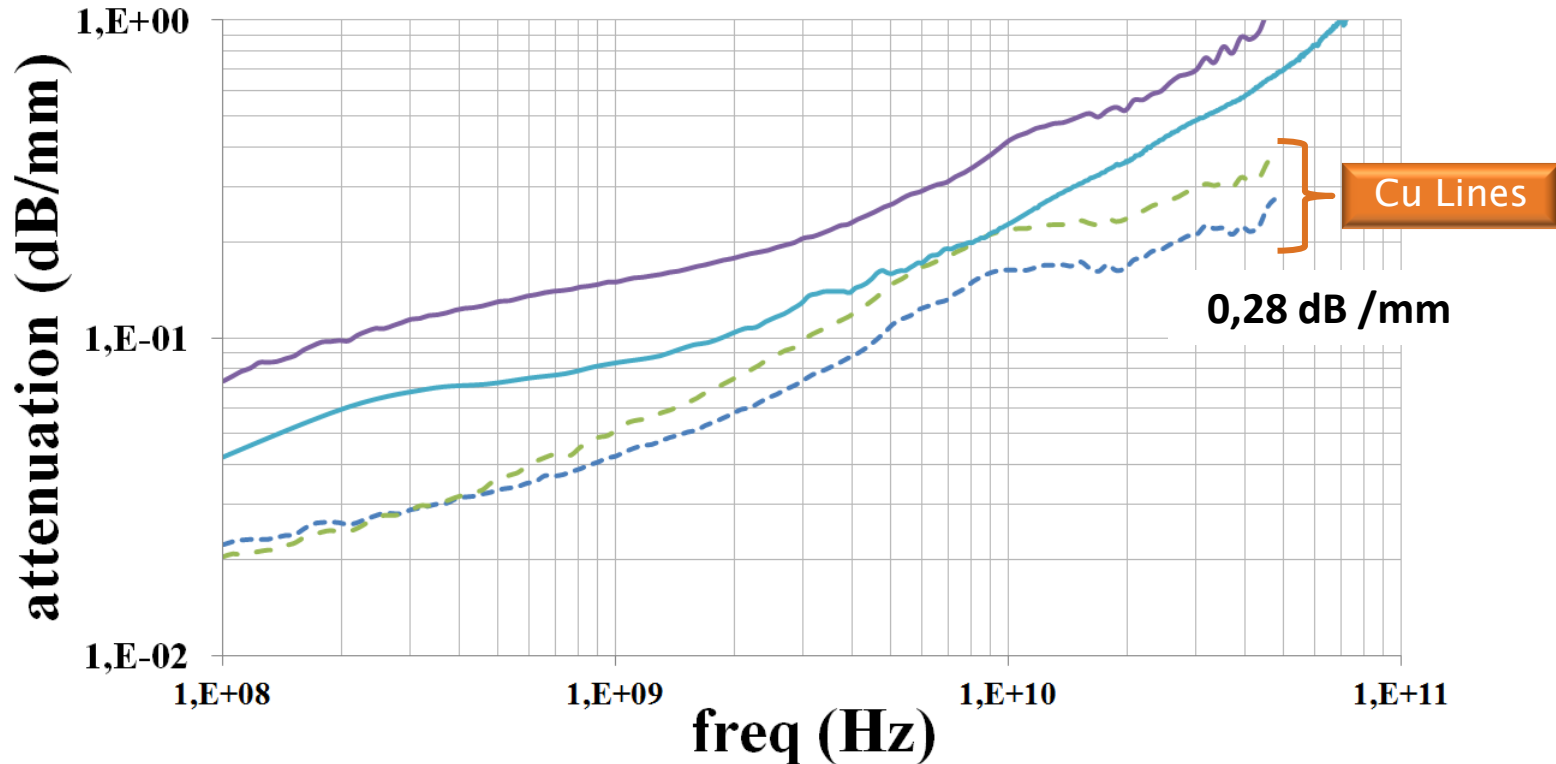


# Results



- Best  $\alpha = 0.36$  dB/mm @ 50 GHz
- Metal1 shield is better up to 30 GHz while DTI gives the best results after
- 2 metals signal lines do not help to decrease  $\alpha$
- Q-factor of 30** achieved (really great on Si)

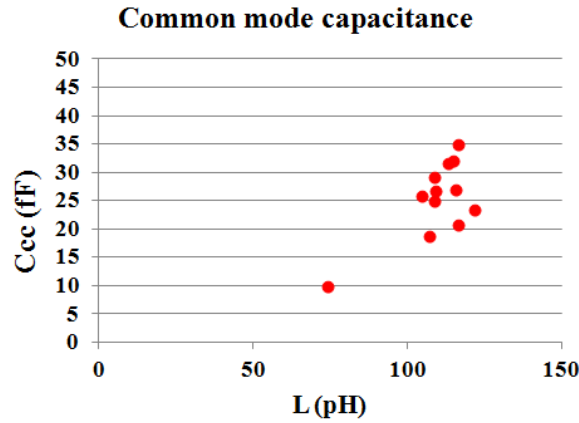
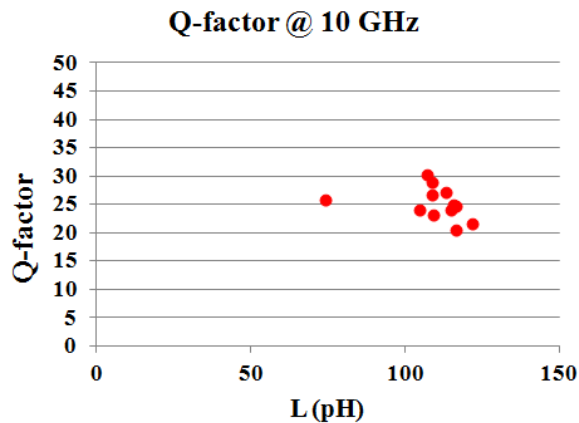
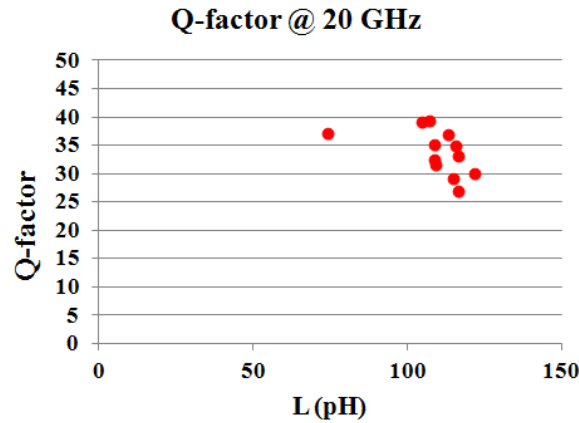
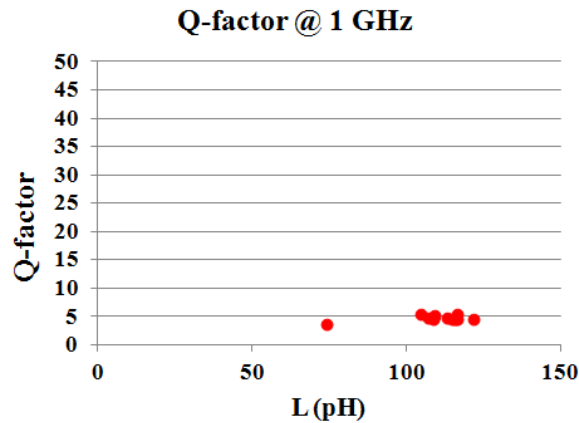
# Going further with DTI and substrate



- Combination of DTI pattern pattern and HRS can really help to decrease attenuation
- Further improvement can also be obtained by increasing distance to substrate (i.e., thicker dielectric)

# Coil characterization

## ☐ Devices from 70 to 120 pH



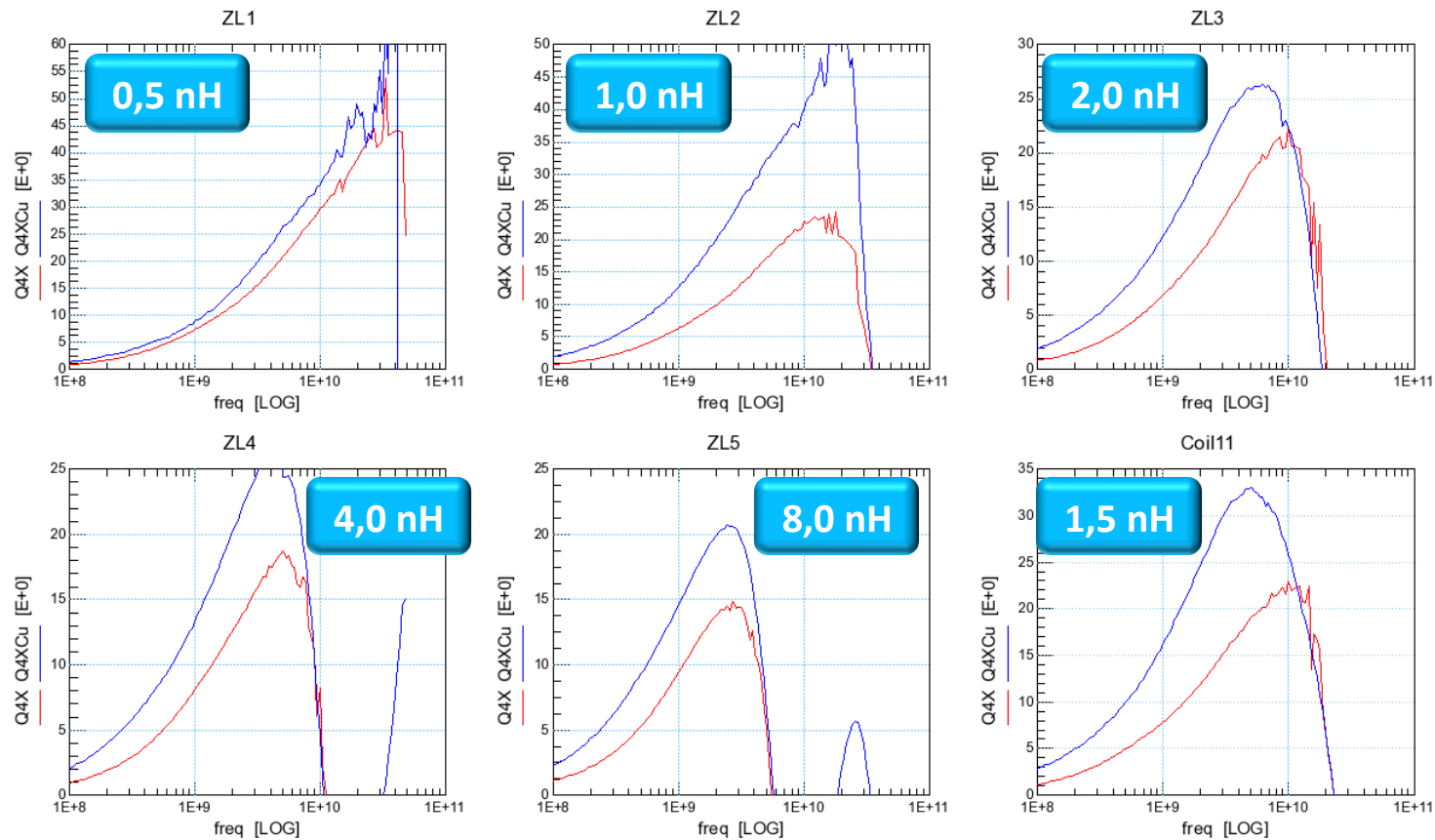
☐ As expected, spiral shapes gives the best Q-factor (not really new! 😊)

☐ DTI shield gives the best Q (like for Tlines)

☐ Thicker metals (M7+M6 or M7+M6+M5) has no real interest @ HF

☐ Q-factor of 40 can be obtained @ 20 GHz

# Cu BEOL vs. Al BEOL



- Q-factor improvement results from Cu and increased distance to substrate
- Will help reducing Phase Noise (PN) of VCO's

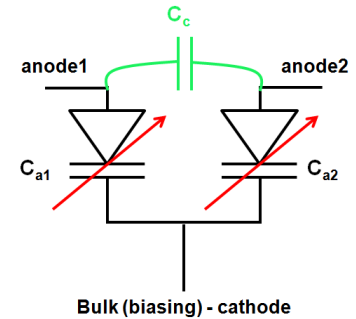
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# Device architecture update

- ❑ A typical example: Variable capacitors
- ❑ Varactors often used in VCO's as tuning elements
- ❑ Varactor performances are characterized by:
  - Its tuning range (TR) – can be limited by the fixed parasitic capacitances
  - Its quality factor: In the low GHz freq. Range, varactors show Q-factor considerably higher than inductors and hence they have a light influence on the oscillator Phase Noise (PN). However, for frequencies of 10 GHz and above, the varactor Q-factor can seriously limit the resonator performances and consequently the oscillator PN
- ❑ A good compromise between TR and Q-factor needs to be found



$$C_{diff} = \frac{C_{a1} + C_{a2} + 4C_c}{4}$$

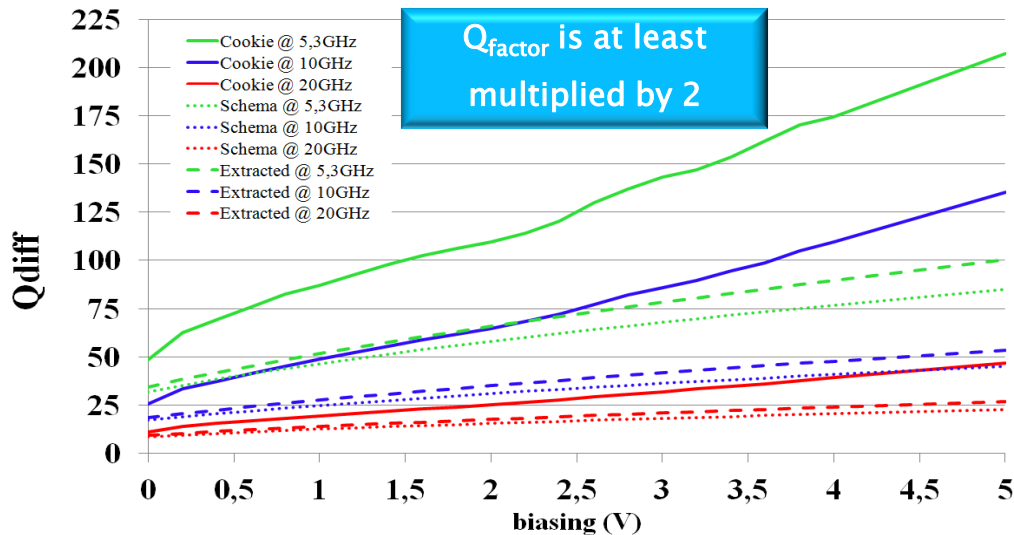
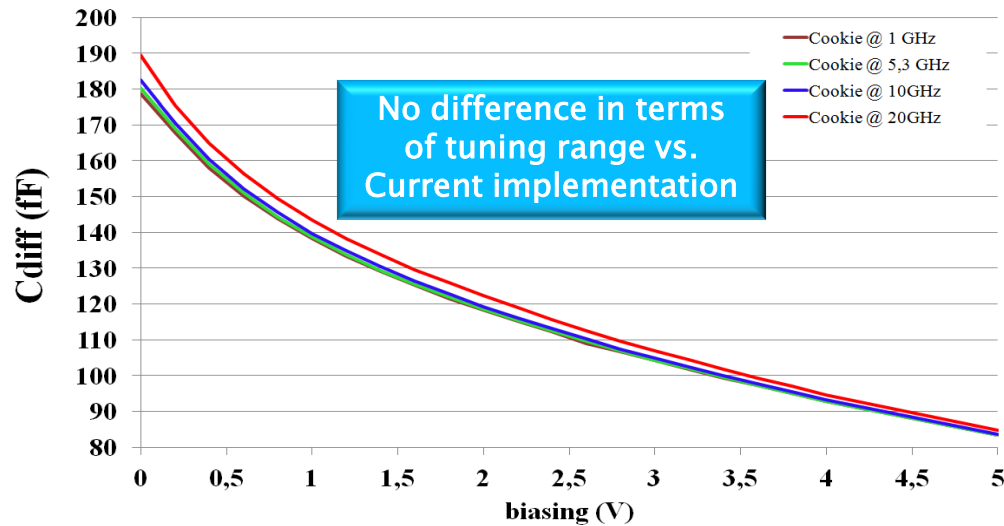
Differential capacitance

# Varactor layout topology improvement

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- ❑ Re-arrange the fingers into 4 several clusters
- ❑ Each cluster is orthogonal to the previous one
- ❑ Donut connection applied to the bulk
- ❑ Symmetrical distributed anode connection (with vertical plugs) and donut with different metals to allow cell abutment
  - No extra connection required
  - No parasitic extraction required
  - Device and model sent as « a black box »

# Results (Measurements)



|                   | Multi-Finger varactor <sup>+</sup> | Multi-Finger varactor (with interconnect) <sup>+</sup> | IGV MOS varactor <sup>*</sup> | Our Proposal <sup>+</sup> |
|-------------------|------------------------------------|--------------------------------------------------------|-------------------------------|---------------------------|
| TR                | 36.9%                              | 31.9%                                                  | 29.5%                         | 31.6%                     |
| $Q_{min}$ (5GHz)  | 33                                 | 34                                                     | 50                            | 49                        |
| $Q_{min}$ (10GHz) | 17                                 | 18                                                     | 40                            | 26                        |
| $Q_{min}$ (40GHz) | 5                                  | 5                                                      | 7                             | 4                         |
| $Q_{max}$ (5GHz)  | 84                                 | 95                                                     | 91                            | 174                       |
| $Q_{max}$ (10GHz) | 42                                 | 47                                                     | 73                            | 110                       |
| $Q_{max}$ (40GHz) | 10                                 | 12                                                     | 13                            | 21                        |
| FOM (5GHz)        | 113 <sup>e9</sup>                  | 109 <sup>e9</sup>                                      | 111 <sup>e9</sup>             | 188 <sup>e9</sup>         |
| FOM (10GHz)       | 107 <sup>e9</sup>                  | 103 <sup>e9</sup>                                      | 167 <sup>e9</sup>             | 215 <sup>e9</sup>         |
| FOM (40GHz)       | 109 <sup>e9</sup>                  | 108 <sup>e9</sup>                                      | 118 <sup>e9</sup>             | 158 <sup>e9</sup>         |

\*50 fF device (must lead to higher Q-factor!)

+140 fF device

- ☐ FOM = freq.TR.Qdiff
- ☐ Improvement up to 110% of the Q-factor vs. state of art
- ☐ Improvement up to 80% of the FOM (includes tuning range)

# Modelling?

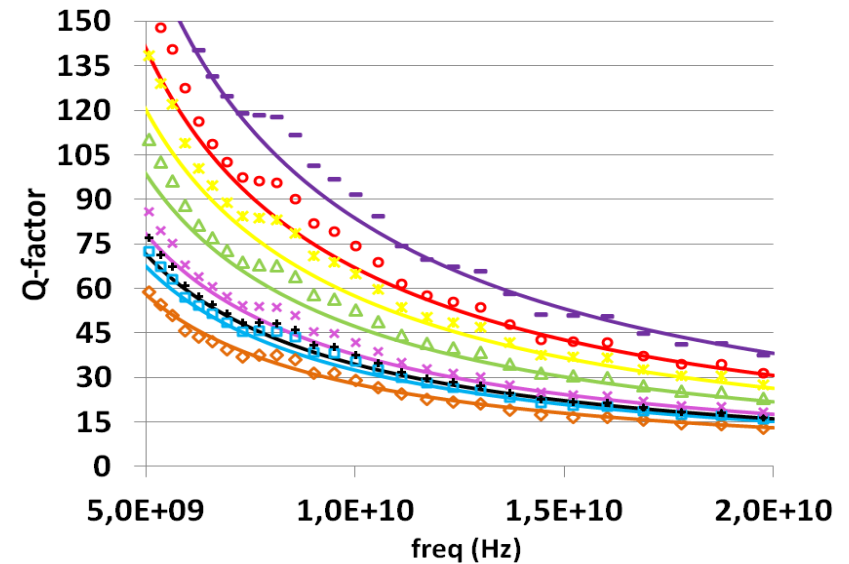
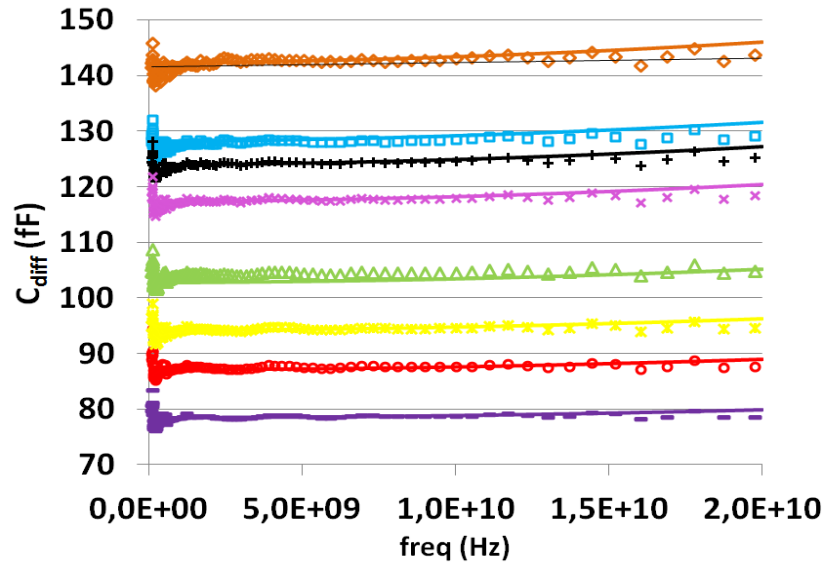
- ❑ Not enough data to have accurate modelling up to now
- ❑ R,L,C,k extraction does not give satisfying results (vs. Measurements)
- ❑ Turn to Electromagnetic modelling?
  - Maxwell Equations: OK 😊
  - Boltzman Equations: 😞 Capacitance variation (i.e., depletion layer thickness) is driven by solid state physics and not by electromagnetism!
  - Implement different depletion layer thicknesses
- ❑ Choice has been done to go to EMPro (i.e., FEM method)
  - Can resolve small details in larger problem space (thin dielectric layer with thicker oxide/Semiconductor)
  - Easy to define arbitrary geometries
  - Mesh refinement!

# EM modelling

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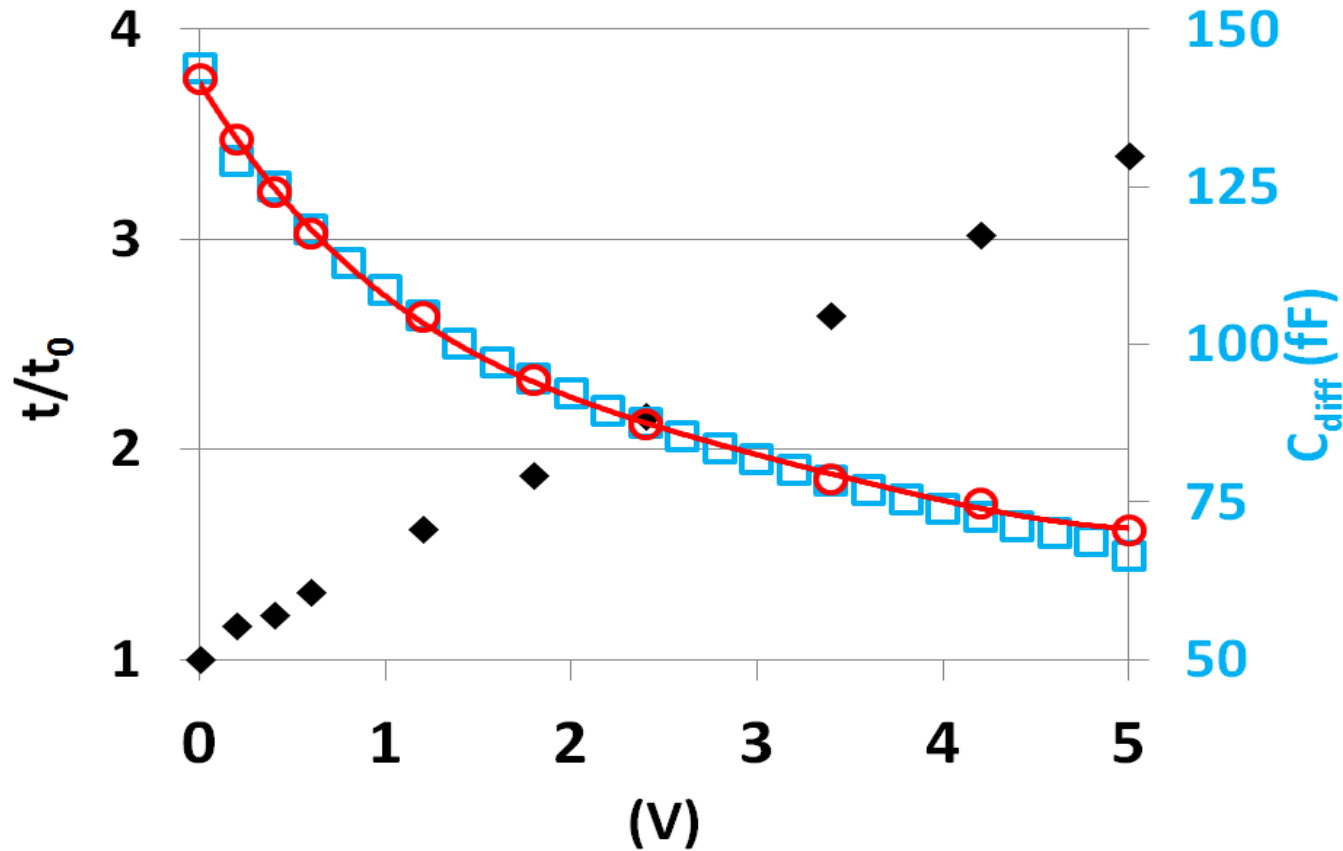
- ❑ Closed box formulation with current definition of dielectric
- ❑ Cathode defined as a metal with a low conductivity
- ❑ Substrate considered as a sheet of 10  $\mu\text{m}$  thickness (to avoid really thick material in combination with very thin ones)
- ❑ Comparison done with two-ports S-params measurements
  - Based on  $C_{\text{diff}}$  and  $Q_{\text{diff}}$  + tuning range

# EM modelling results



- ☐ Really nice agreement between EM model and measurements
- ☐ 90 sec simulation time for a device (16 core + 4 graphical cards)

# EM modelling results



□ Relative variations of depletion layer thickness in good agreement with theory and measurements

# Summary

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## ❑ Clear breakthrough obtained on passive devices considering:

- Process update (metal, stack and substrate patterns)
- Layout topology update
  - Black box EM model proposed (compact modeling can also be achieved) to decrease iterations during design (no extra connection nor parasitic extraction required)
  - 2 to 3 dB reduction on Phase Noise has been measured on L,C based VCO including the new varactor
  - Same exercise done on MOS varactor with terrific quality factor (x4 current state of the art)
- Several devices also implemented to support theoretical investigations
  - On Si Lange Coupler with 0,3 dB IL @ 25 GHz
  - On Si Hairpin filter with 0,7 dB IL @ 42 GHz

## ❑ Brings the SiGe process in competition with GaAs at a lower cost on particular applications

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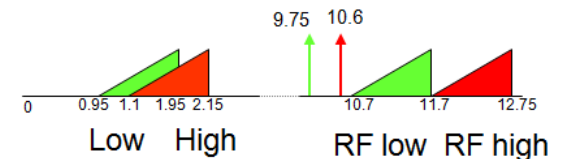
# Motivations-challenges

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- ☐ Look for high volume packaging solutions for Ku, K and Ka band applications
- ☐ Evaluate the **Fan-Out solution** (eWLB: embedded Wafer Level Ball grid array)
- ☐ Demonstrate a breakthrough in terms of electrical performances vs. HVQFN type (wire based solution)
- ☐ Have accurate 3D EM model available for both packaging and carrier substrate (How can i improve confidence of the FEM solver!)
- ☐ Provide efficient characterization techniques for packaging model validation

# Test vehicle description

- ❑ TFF1014 IC (QUBiC4X) is used within a LNB (Low-Noise Block) which converts Ku-band input signal down to L-band output signal.
- ❑ It's a PLL based LO frequency generator.
- ❑ A switchable LO frequency generator (9,75 and 10,6 GHz) is implemented within the IC.
- ❑ RFin signal varies between 10,7 and 12,75 GHz depending on the band (low or high) leading to IF output comprised between 0,95 and 1,9 GHz or 1,1 and 2,15 GHz after combination with the LO signal.
- ❑ IC is embedded within a DHVQFN16 package. Package is then soldered on a 2 layers RO4233C substrate

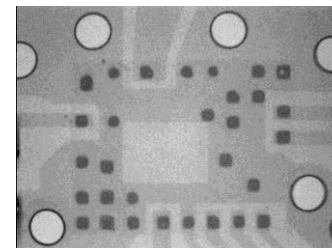
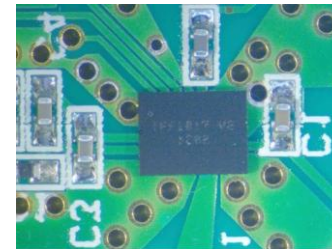
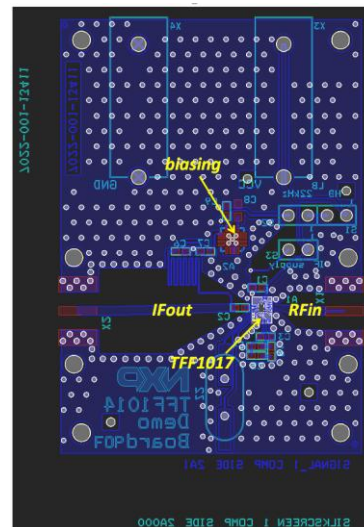
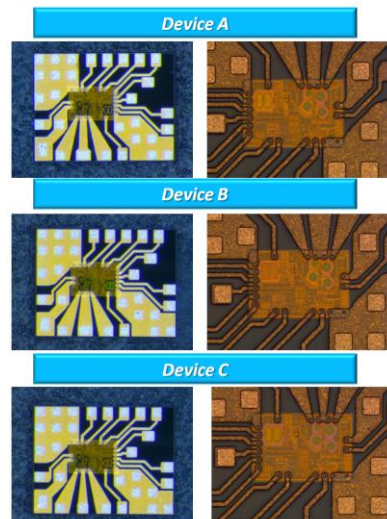
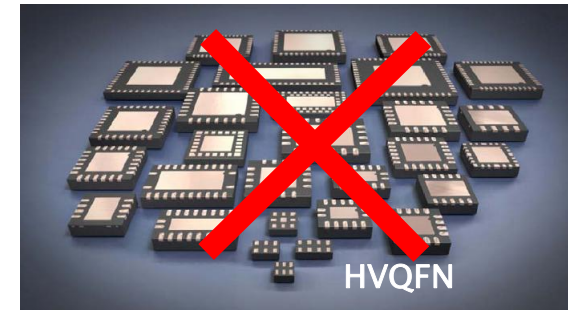


*Courtesy of P. Philippe*

# Turn to High Performance Packaging

## Package choice done and full characterization performed

- Choice have been done to turn to a flip-chip technology
  - Customized design of the package → co-design approach
  - Matched accesses up to V-band
  - Reduced ground impedance
  - Ku to L band down converter used as test vehicle
- Full EM and compact modelling issued to allow RF analog simulations
- Full characterization performed and compared with existing solution (QFN type)

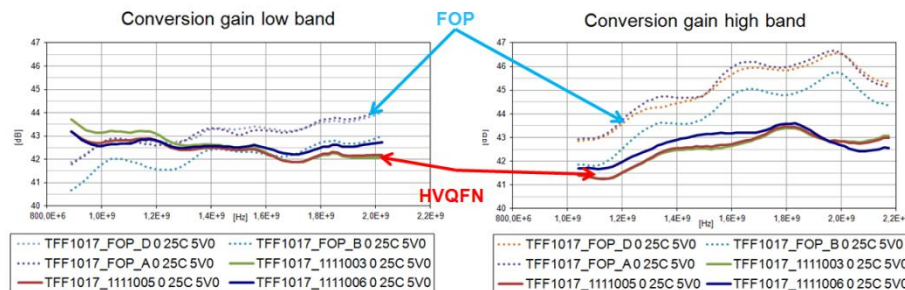


*P. Gamand, O.  
Tesson, EuMW  
2013*

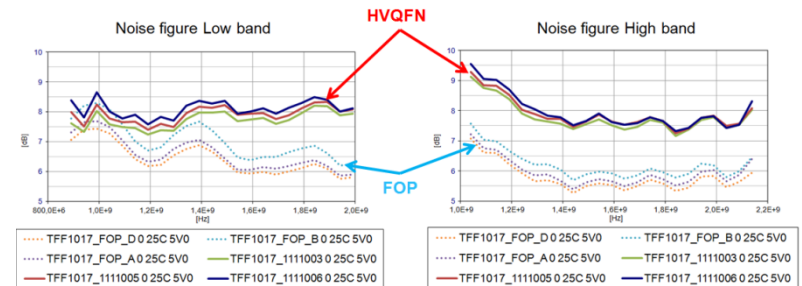
# Measurement results

## Characterization results on the Tx chain

- Strong improvements of the conversion Gain (3 dB)
- Strong reduction of the NF (up to 2,5 dB) especially in the highest band



Conversion gain



Noise Figure

- Package is clearly differentiator at mmWave frequencies despite of his cost
- Can be a way to integrate antenna and/or passive devices as well

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# Conclusion – Look ahead

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## ❑ Packaging technologies can be a key differentiator for forthcoming mm-wave applications

- Co-design approach is mandatory
- Passive integration and/or antenna implementation can be also performed on package
- Need further investigations on material characterization ( $\epsilon_r$ ,  $\tan \delta$  in wide frequency range)

## ❑ Presentation put in obviousness the impact of layout topology update on device performances

- Up to 300 % improvement on quality factor achieved
- In combination with process update, allow BiCMOS to compete with III-V (FEM IC)
- Black-Box modelling to decrease time to market and to provide better accuracy

# Dissemination

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- ☐ 1 regular paper
- ☐ 5 papers @ conference
- ☐ 6 patents
- ☐ 1 PhD defense

# Acknowledgments

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- ❑ Pieter Weijs, Peter Magnee, Ivo Powel, Patrick Sebel, Andrea Scarpa from NXP Nijmegen (ICN8)
- ❑ Laure Rolland du Roscoat, Dominique Lesénéchal, Patrice Gamand, Stéphane Charlot from NXP Caen
- ❑ Erik de Hoog, Paul Disjkstra, Roelf Groenhuis, Niels Kramer<sup>+</sup> from Back-end Innovation

*<sup>+</sup> moved to Philips*