CATRENE – CT209 – RF2THZ SiSOC

Title: BiCMOS Integration of Photonic Components

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innovations
for high
performance
microelectronics

Leibniz-Institut für
innovative Mikroelektronik

Open Bipolar Workshop
3 October 2013, Bordeaux

Cluster for Application and Technology Research in Europe on NanoElectronics

Outline

- **Introduction**
  - RF2THZ motivation for an **EPIC** (=> **E**lectronic **P**hotonic **IC**) technology
  - Motivation beyond RF2THZ-demo application
- **Choice of EPIC technology**
  - Photonic devices that are to be integrated
  - FEOL integration vs. other approaches of photonic device integration
  - Baseline for photonic device integration: BiCMOS vs. CMOS
- **Substrate issue: SOI (Photonics) vs. Bulk (BiCMOS)**

  → local-SOI approach
- **Ge photo-detector integration**

Outline (cont'd)

- **Photonic BiCMOS**
  - Process flow
  - Design features
  - BiCMOS yield and parameter behavior
  - Photonic device performance
  - What next?
- **First EPIC demonstrators in Photonic BiCMOS**
  - 10Gbit/sec Silicon modulator with driver (SG25H3)
  - 20Gbps receiver: Ge-PD + TIA (SG25H1)
- **Summary and conclusions**

Introduction

- **European (CATRENE) project**
  - **More than 30 companies, institutes, universities**
  - **For German partners, like <u>IHP</u> & <u>TU Berlin</u>: January 2012 -- December 2014**
  - **IHP and TUB funding by <u>BMBF</u>** (Federal Ministry of Education and Research)

- **3 big work packages dealing with technology development**
  - ST: WP1.1 "55 nm SiGe BiCMOS process integration" → *Development of 300mm SiGe BiCMOS technology with 300/400GHz f_T/f_{MAX} SiGe HBT and 55nm CMOS (B55)* → ***Previous talk***
  - NXP: WP1.2 "Elite passive devices integration" → *Development of elite passive devices (inductors, TL's, …) and integration in 0.25µm SiGe BiCMOS technology*
  - **IHP: WP1.3 "Photonic devices integration"** → *Development of photonic SiGe BiCMOS technology with front-end (FEOL) integration of photonic components (including Ge photodetector)* → ***<u>This talk</u>***

RF2THZ motivation for EPIC technology

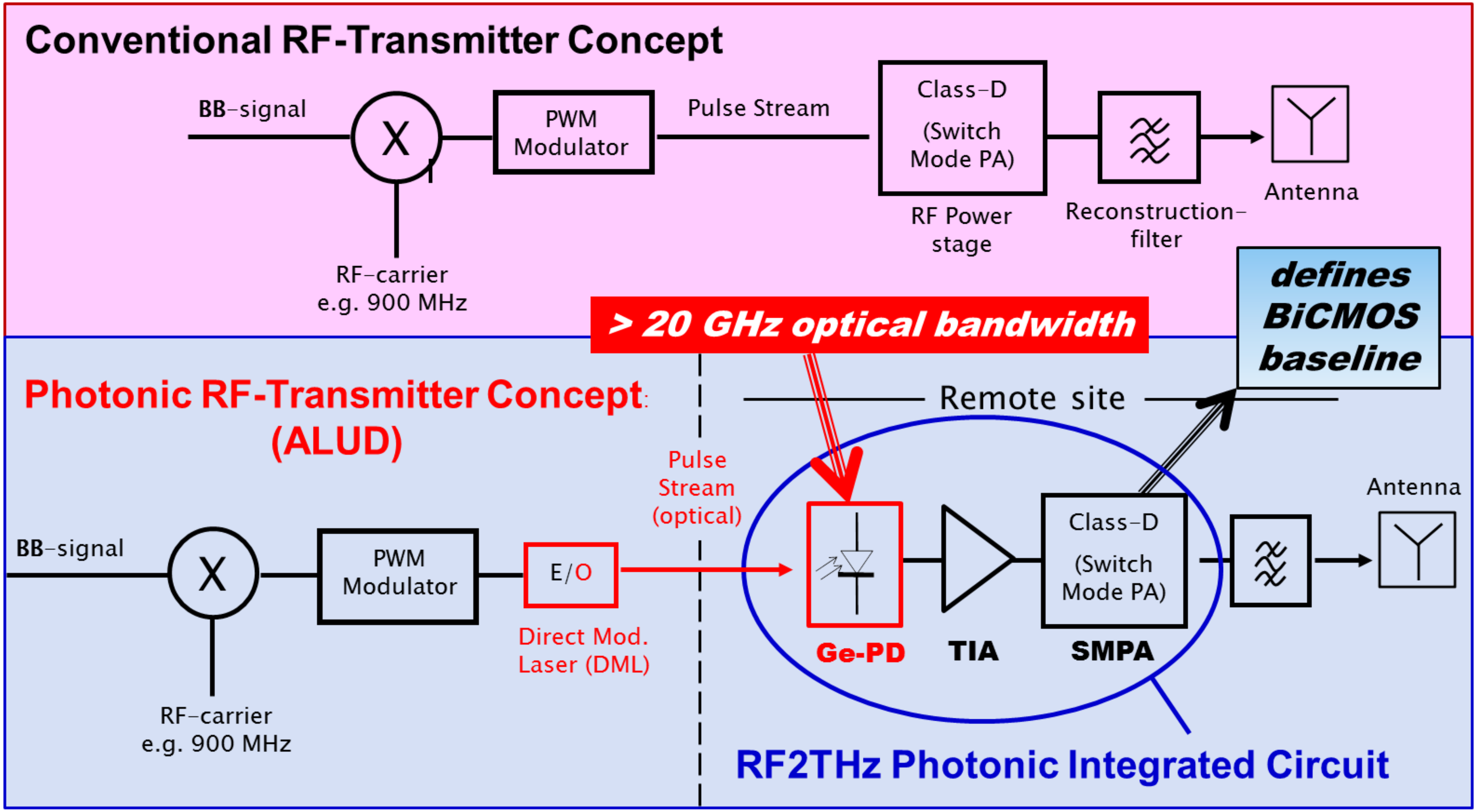
Demo2:

Photonic RF-Transceiver for 3G/4G Base Transceiver Station (BTS)

- **Low-cost remote RF-antenna unit for femto cell BTS***
  - Reducing hardware effort by EPIC integration combining Ge-PD with SiGe BiCMOS TIA and switch mode PA (TX: 15dBm @ 900GHz)
  - Status:
    - System level requirements defined
    - SiGe BiCMOS technology identified
    - Electrical test structures realized
    - First EPIC fabrication will start November this year

** More details in the afternoon talk (3:20 pm): **"Application Scenarios from RF2THZ" (W. Templ)***

Photonic RF-transceiver for 3G/4G BTS



IHP SiGe BiCMOS baseline choice: SG25H1 vs. SG25H3

- Investigated components from IHP technologies SG25H1 and SG25H3 under ideal driving signal conditions ($\tau_{rise,fall}$ = 0) using PWM modulated rf signal (f_c = 920 MHz):

BiCMOS	Transistor	f_T (GHz)	BV_{CEO} (V)	Vcc (V)	Pch (dBm)	ηch (%)	Rl (Ω)
SG25H1	50 x npn200_1	200	2.4	1.5	4.4	38.2	50
SG25H3	100 x npnh3_shp1	120	2.4	1.5	4.9	40.3	50
SG25H3	**20 x npnh3_MV**	50	4.5	3.5	5.7	**55.5**	580
SG25H3	140 x npnh3_MV	50	4.5	3.5	8.4	38.3	110
SG25H3	**100 x npnH3_HV**	**30**	**7**	5	**9.9**	41.2	200

- **npnH3_HV device (BV_{CEO} = 7 V) provides highest output power → chosen**
- Switches total efficiency was >70%, but for channel efficiency (ηch=Pch/Pdc), best value (55 %) has been achieved by combining npnH3_MV devices
  - Reduction of efficiency caused by Vdd not returning to zero between short pulses
- Re-characterized npnH3_HV with 2 GHz PWM modulated signal:

BiCMOS	Transistor	Vcc (V)	Pch (dBM)	ηch (%)	Rl (Ω)
SG25H3	80 x npnH3_HV	5.4	6.3	28.9	180

Motivation for EPIC technology beyond this project

General objectives to bring optical functionalities to electronics integrated circuits

J.-M. Fedeli, "Integration of silicon photonics with electronics"; Photonics –PhD course prepared within FP7-224312 Helios project

- Increase the performance of photonics with embedded electronics
- Increase the data transmission speed between cores with photonics

→ Enables new or improved applications in fields such as:

- Communication
- Measurement instrumentation
- …

Much more "motivation" details can be found in the ST and Analog Devices papers in this year's BCTM "Emerging technologies" session

→ IHP will extend MPW offers (incl. small volume production) over PIC to EPIC fabrication ASAP

IHP MPW technology roadmap: BiCMOS baselines

- **Development** (no access for external customer)
- **Early access** (MPW access, electrical parameters stable, not complete fixed)
- **Qualified**
- **Space evaluated**

BiCMOS Process	Features	2013				2014				2015		'16
	f_T/f_{max} (GHz)//BV_{CEO} (V)	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	H1	H2	→
SGB25V	75/95//2.4; 45/90//4; 25/70//7											
SGB25RH												
SG25H3	120/140//2.4; 110/180//2.3; 45/140//5; 30/80/7											
SG25H1	190/190//1.9; 180/220//1.9											
SG13S	250/300//1.7; 50/120//3.7											
SG13RH												
SG13G2	300/500//1.6; no digital libs											

by September 2013

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IHP MPW technology roadmap: Modules

Development　Early access　Qualified

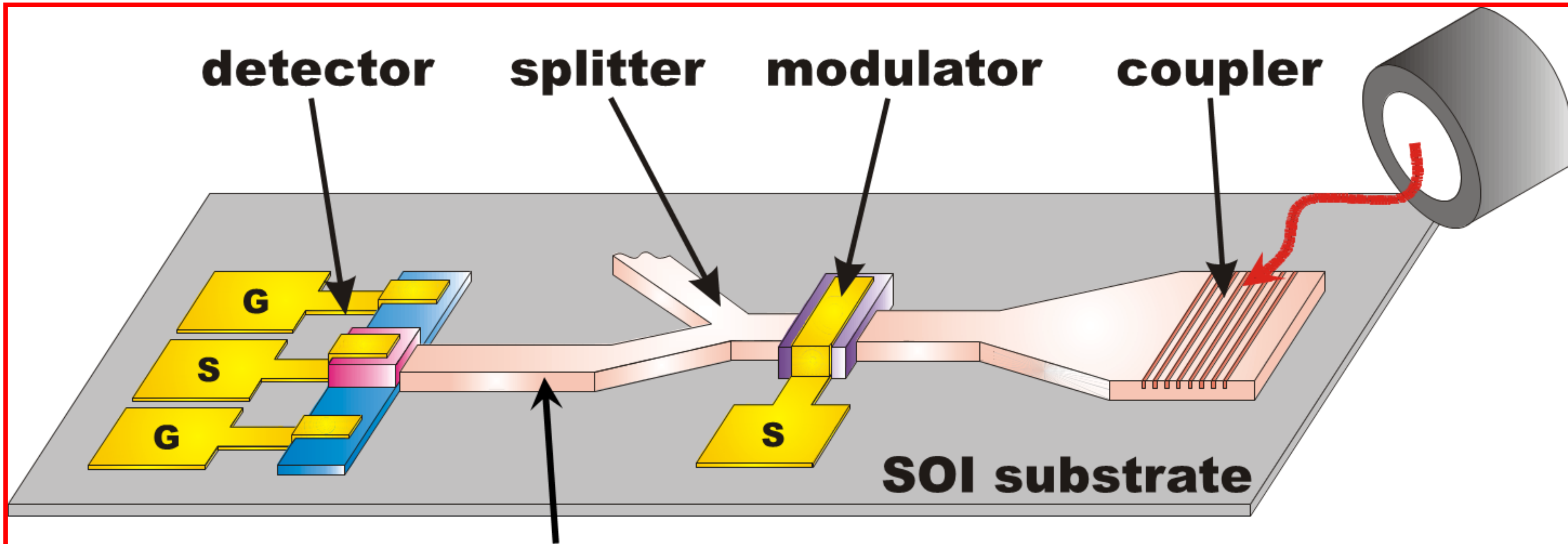
[1)] Qualification on customer request　*LBE: Local backside etching

Module (baseline)	Features	2013				2014				2015		16
	f_T/f_{max} (GHz)//BV (V)	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	H1	H2	→
GD (SG25V)	NLDMOS: 18/48//22 PLDMOS: 8/28//-17											
PNP (SG25H3)	pnp90: 90/120//-2.5											
RF MEMS (SG25H1, H3)	Switch: 30-110 GHz								1)			
RF MEMS (SG13S)	Switch: 40-140 GHz											
LBE* (all)									1)			
SG25_(E)PIC (SG25H1, H3)	Photonic devices (w/ SG25-BEOL)						PIC		→ EPIC			
TSV (H1, H3)	for grounding											

by September 2013

Choice of EPIC technology: Photonic components

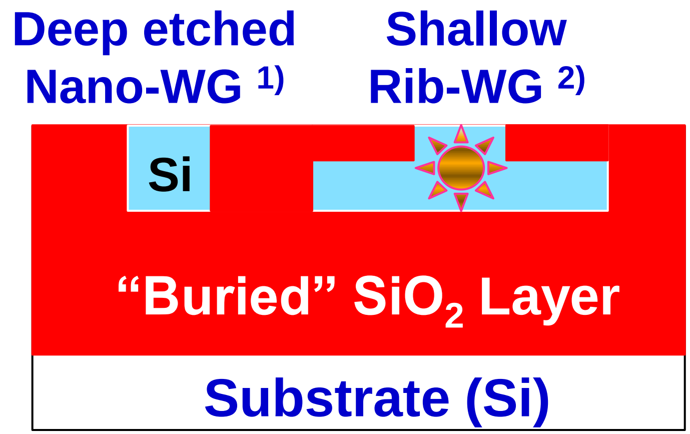
Photonic Integrated Circuit → **How to get EPIC??**



Source: IHT Stuttgart

Photonic components (cont'd)

Waveguides



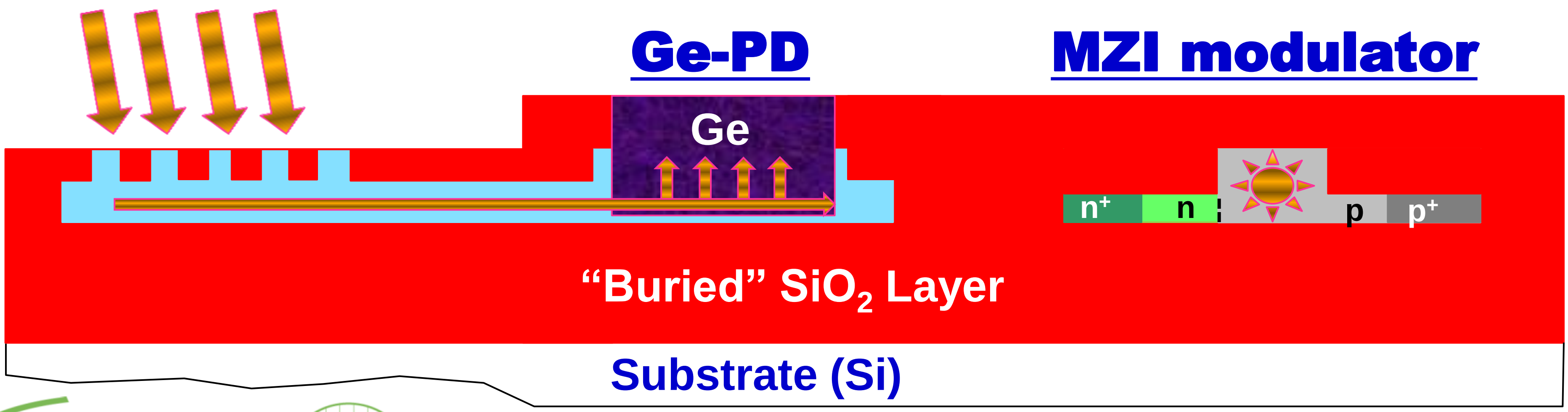
1) **Nano-WG:**

- dense optical routing
- basic structure for most compact integrated optics (splitters, combiners, λ-selective filters)

2) **Shallow Rib-WG:**

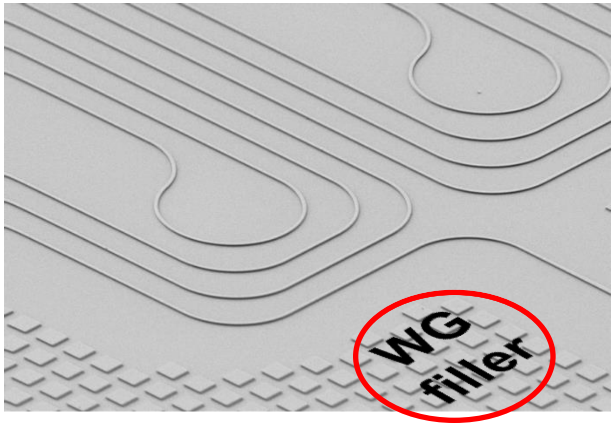
- low-loss waveguides

Coupling structures

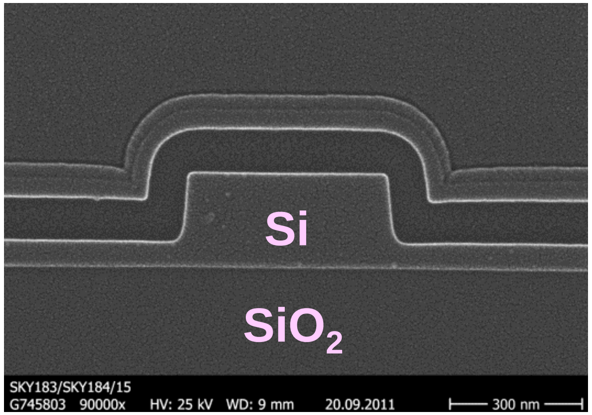


Photonic components (cont'd)

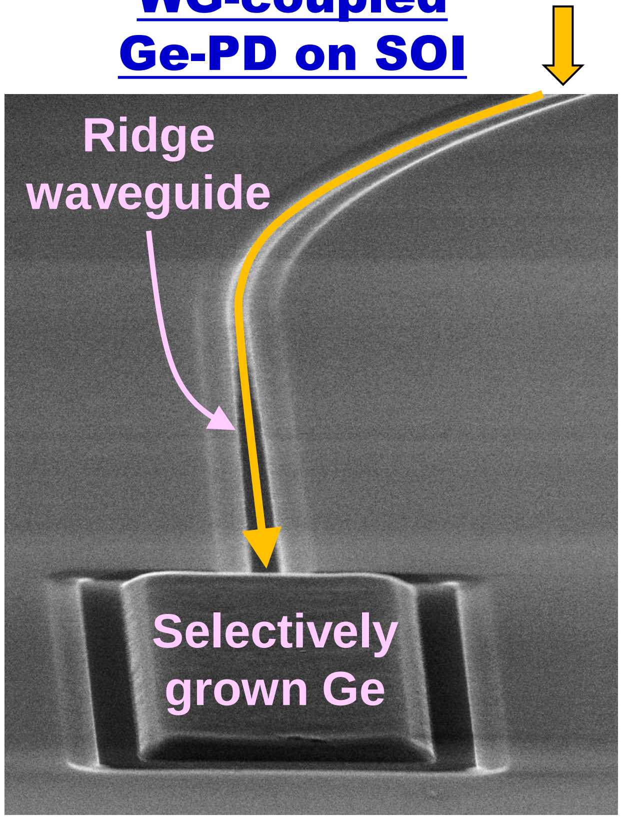
WG pattern



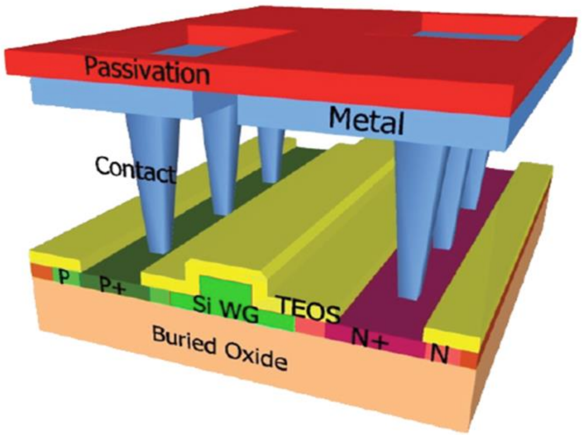
Rib-WG

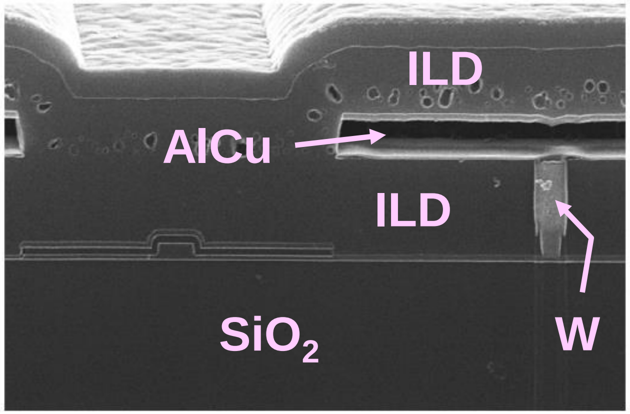


WG-coupled Ge-PD on SOI



MZI depletion modulator





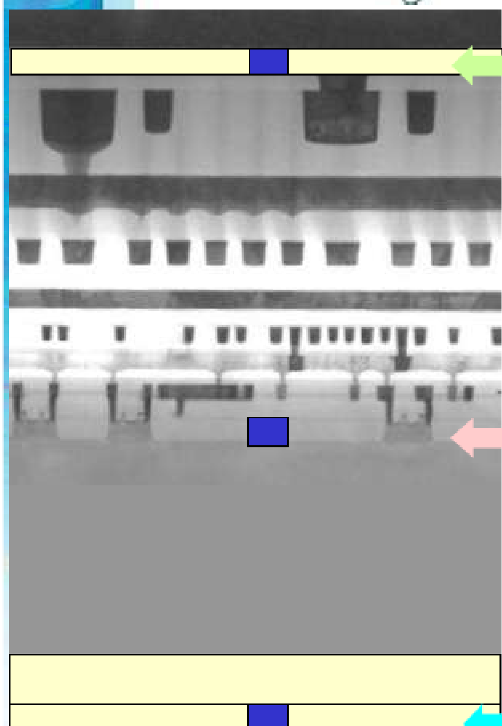
Choice of EPIC technology: FEOL-integration vs. others

Integration of complex photonic functions with EIC

by J. M. Fedeli

heliOs

cea leti · ihp · austriamicrosystems · TU Berlin · imec



Photonic layer at the last levels of metallizations with back-end fabrication

1) Wafer bonding of PIC (high T℃)

2) BE fab(<400℃)

- Use of standard FE CMOS technologies
- Heterogeneous integration of III-V on Si
- High integration density (AboveIC)
- Multilevel process capability

Combined front-end fabrication

- Specific FE CMOS technology and library
- Flip-Chip hybridization of InP components
- Moderate integration density
- Efficient connections of EIC and PIC

IHP approach

Backside fabrication

- BE fab(<400℃) or FE fab with wafer bonding
- Through substrate connections
- High integration density
- Heterogeneous integration of III-V on Si

BE: Back end FE:Front end

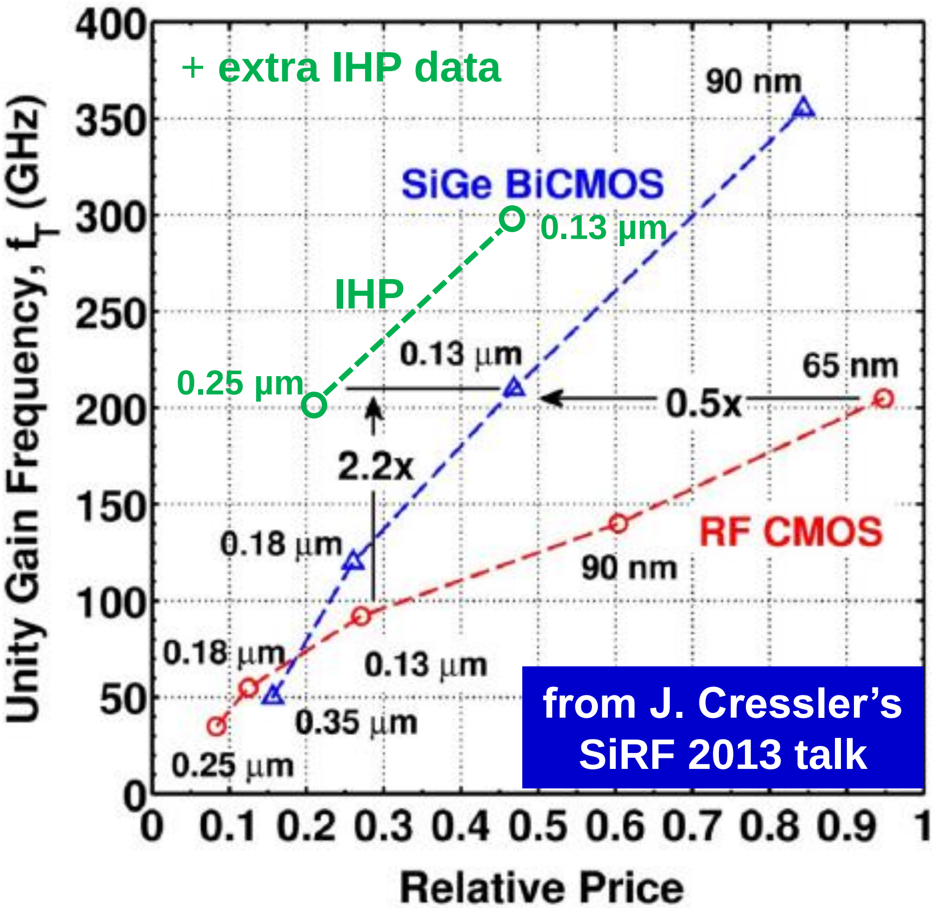
Choice of EPIC technology: BiCMOS vs. CMOS baseline

- **Photonic integration with advanced (≤ 45 nm) CMOS is highly desirable in modern communication systems where DSP is deployed** (for example to compensate for signal distortions caused by fiber optical transmission effects)

- **However: CMOS scaling lowers operating voltage and current driving capabilities → BiCMOS better suited for developing silicon photonic devices integrated with driving or read-out electronics plus a built-in electronic interface matching advanced CMOS** → RF2THZ demo

- **Present networks operate with per-channel data rates between 10Gbit/sec – 100Gbit/sec, necessitating high speed broadband drive and receive electronics → Can be got much cheaper in BiCMOS: same speed @ relaxed litho node → lower mask & development cost**

BiCMOS vs. CMOS baseline (cont'd)



Courtesy of D. Harame, A. Joseph

SiGe BiCMOS has a performance advantage of 2-3 generations over CMOS

- **Saving lots of € or $ for same performance!! <u>or</u>**
- **Much higher performance (> 2x) @ same price**

<u>For example:</u> need 65/45 nm CMOS to equal 130 nm SiGe BiCMOS!!

Photonic BiCMOS: Components

- **"Normal" BiCMOS devices:**
  - **SiGe HBTs**
  - **MOS transistors**
  - **Resistors, etc**

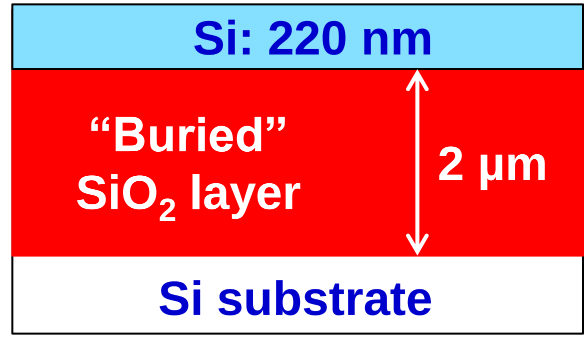
"Unchanged" (or better) parameters & yield, compared to the parent BiCMOS process !!

??

- **New, photonic components** (examples)**:**
  - **Several sorts waveguides, coupling structures**
  - Modulator (MZI type) → "beyond RF2THz requirements"
  - **Ge-PD, coupled to waveguide**

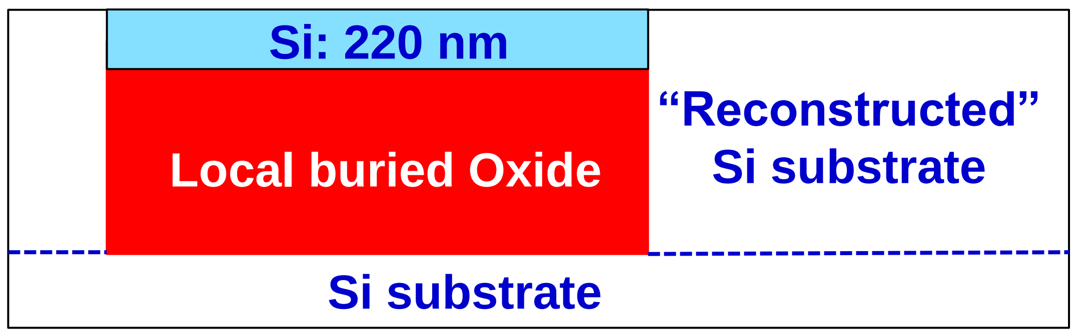
Substrate issue: SOI (Photonics) vs. Bulk (BiCMOS)

Photonic components:



- Need SOI substrate for low loss, but "optimum for photonic" dimensions are by far not optimal or even unfit for CMOS and, fortiori, BiCMOS!!
- CMOS: both Si (220 nm) and SiO_2 layers (2 µm) much too thick
- HBT: Si layer much too thin for a low-R_C HBT collector fabrication; bad HBT head dissipation because of higher R_{TH} of SiO_2, comp. to Si

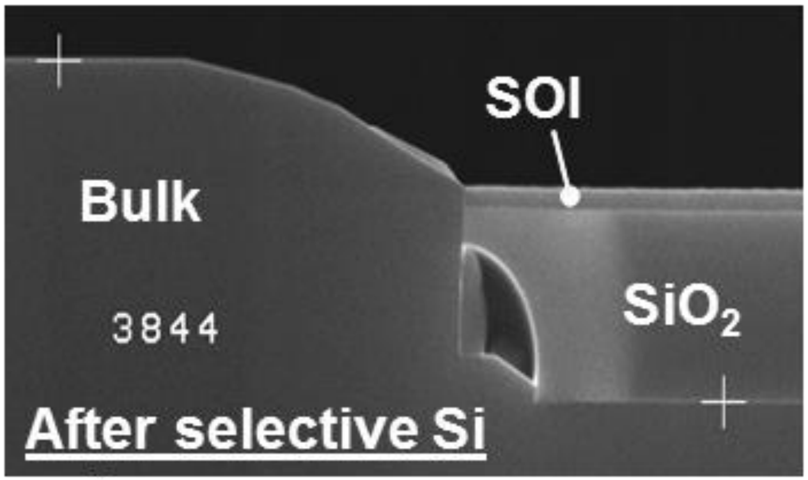
Solution: "Local-SOI"

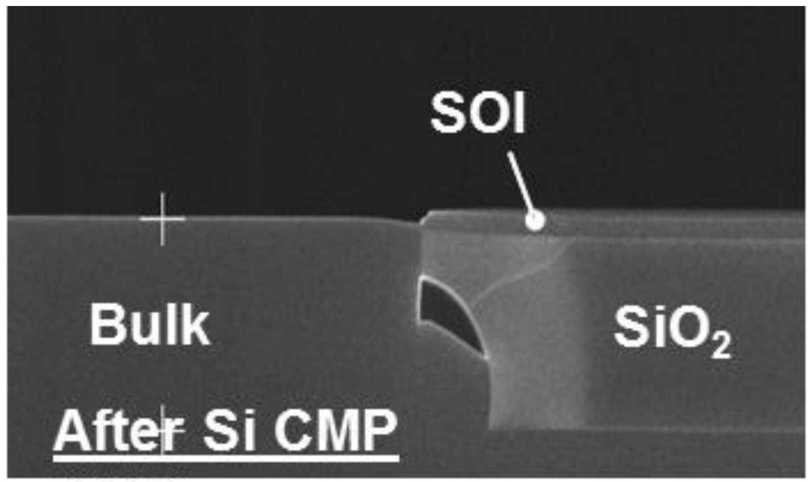


Local-SOI fabrication

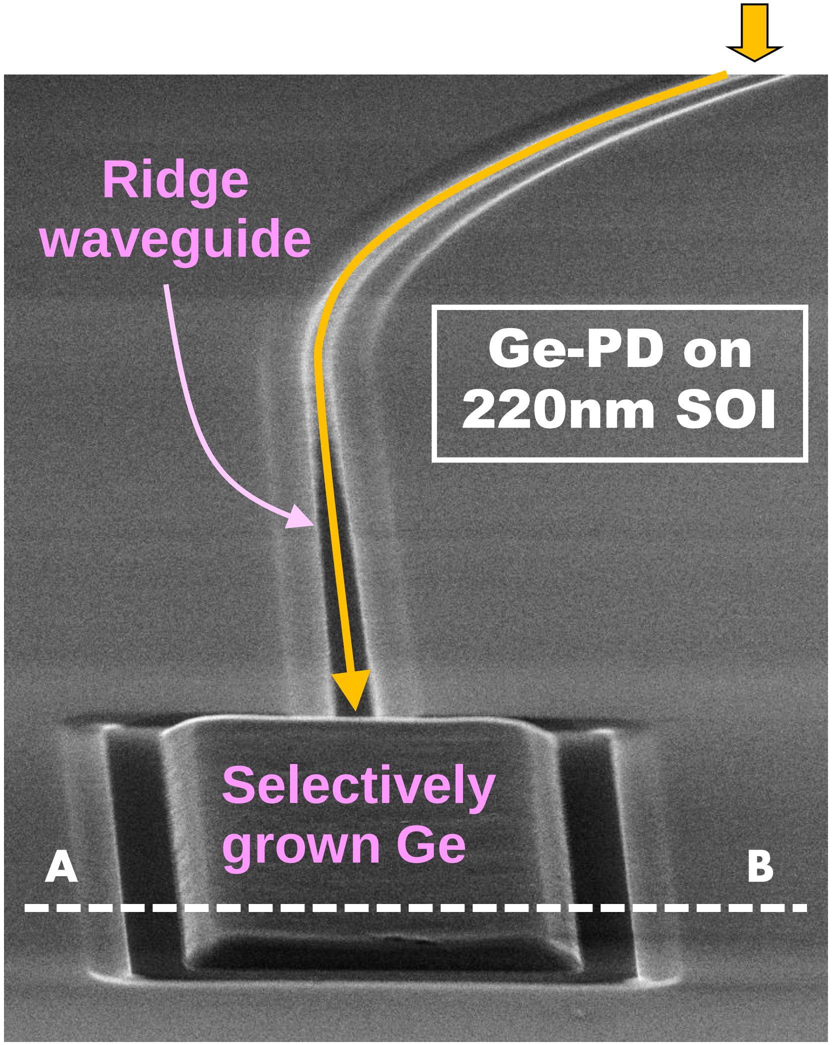
- Locally removing SOI structure by RIE/wet etch sequence
- Selective Si epitaxy
- Planarization by Si-CMP

BiCMOS yield??

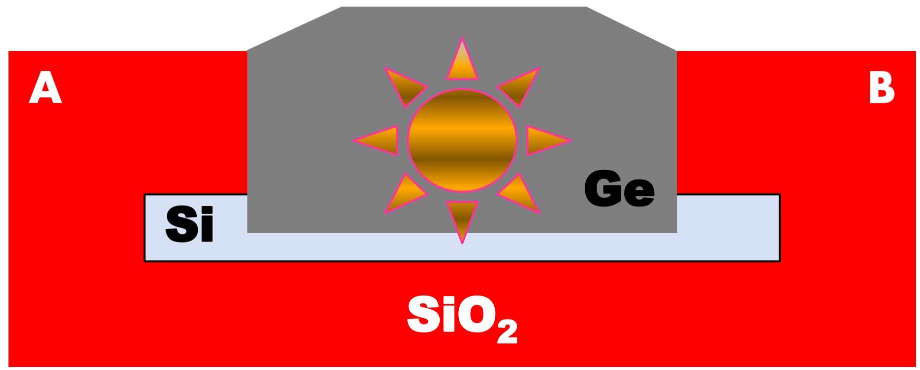




Ge photo detector integration

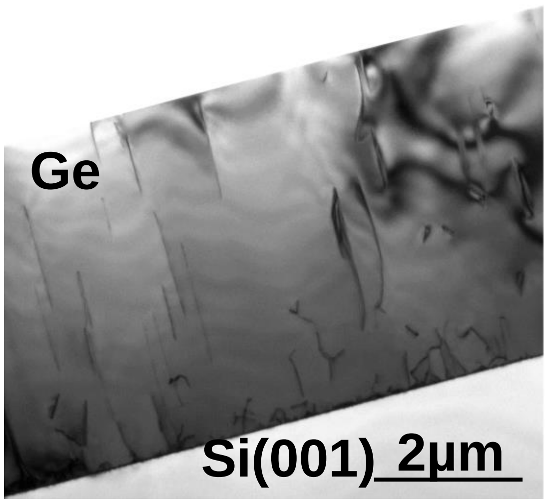


- <u>WG-coupled photo detectors</u>
- selective Ge epitaxy in a window within an isolator layer stack (mainly SiO_2), protecting the BiCMOS devices during detector fabrication
- Ge epitaxy directly on a silicon waveguide (w/ or w/o recess)

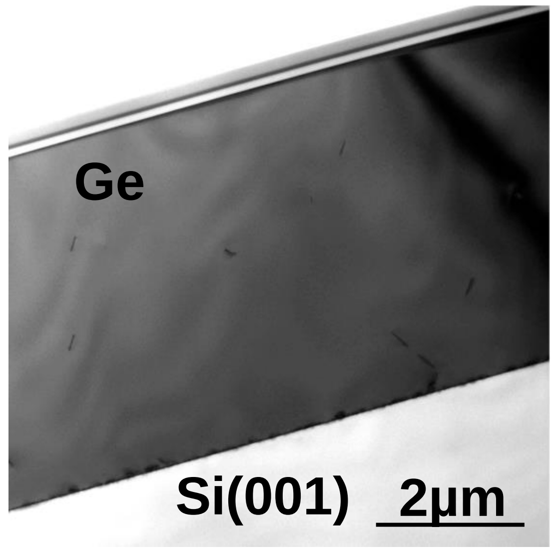


Ge on Si hetero-epitaxy

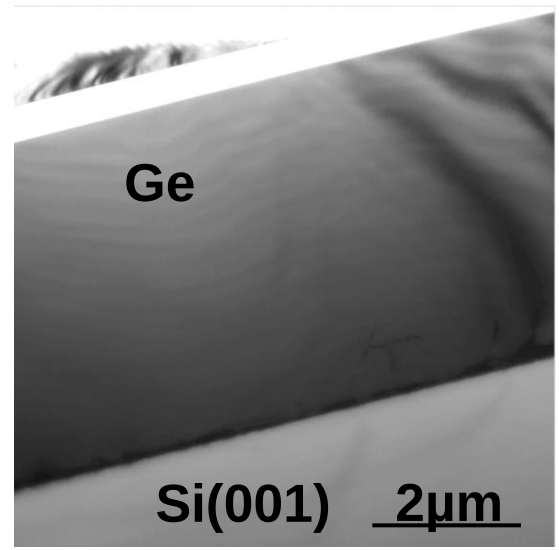
Need some thermal budget for acceptable layer quality!!



As grown



Post annealing



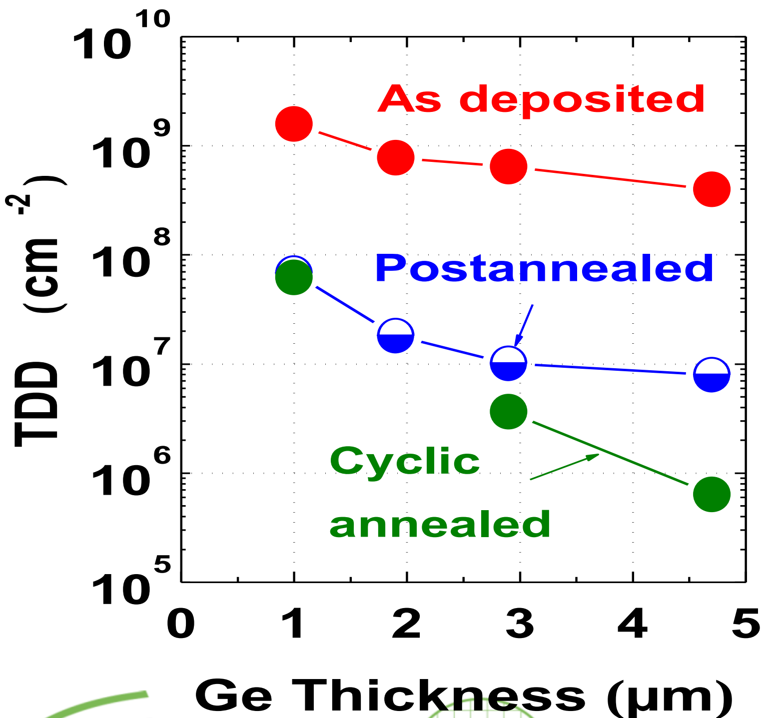
Cyclic annealing

Integration problems: Ge-PD thermal budget

Problem: Acceptable Ge layer defect densities, i.e. PD-I_{dark}, need a certain thermal budget which is applied after BiCMOS S/D anneal

($T_{Ge,\ melting} = 938°C < T_{S/D\ anneal}$)

Strong impact on BiCMOS device parameters



Cyclic anneal:

@ 800 °C, some minutes in total (incl. epi pre-bake)

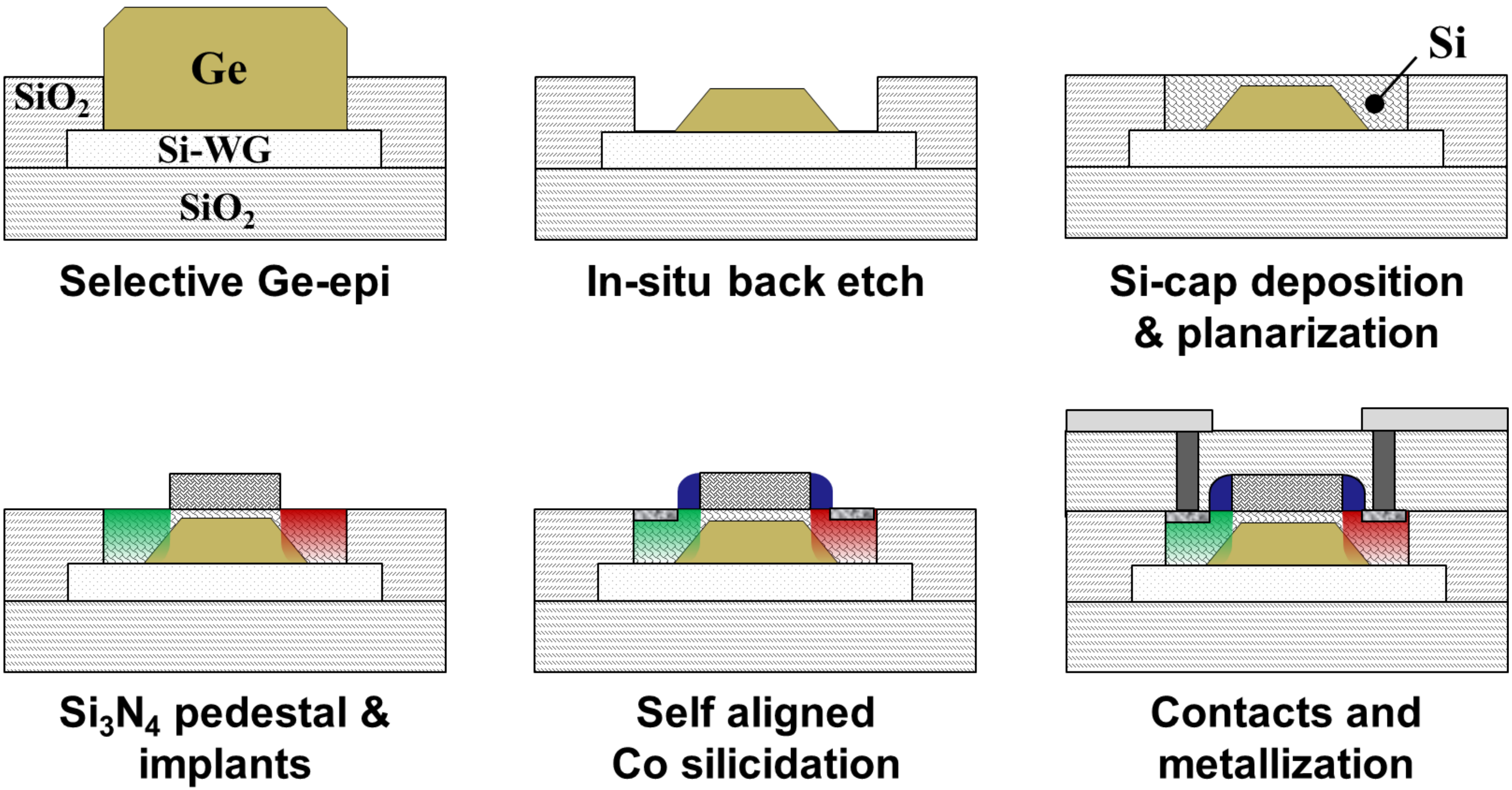
Threading dislocation density (TDD) vs. thickness for Ge layers epitaxially grown on Si under different anneal conditions

Y. Yamamoto et al; SSE, 60, 1, 2011, pp. 2 - 6)

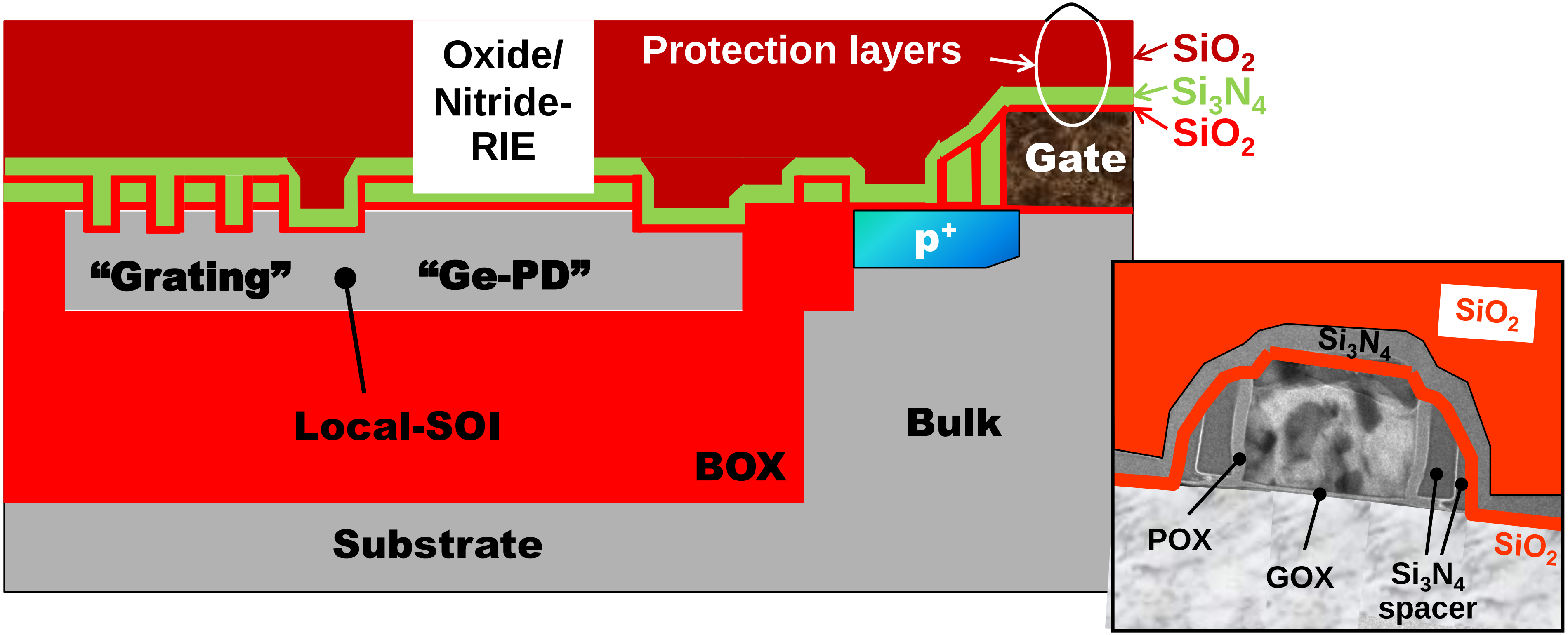
Before or after CoSi ??
after ➢*saving a mask*
before!! ➢***can co-use BiCMOS CoSi***

Electrical data → no choice!!

Ge photo-detector: PIN diode fabrication



Ge photo-detector: Protection layers



- Additional thermal budget → BiCMOS parameter compatibility?
- Have to be removed before CoSi formation → BiCMOS yield problems?
- Covering couplers → changed behavior?

Photonic BiCMOS: Process overview

SOI Substrate

- STI, DEEP N ISO IMP
- NWELL IMPs, PWELL IMPs
- 5nm GATE OXIDE + GATE POLY
- GATE STRUCTURING + SPACER
- **SG25H1 or H3 HBT MODULE**
- PSD IMPs, NSD IMPs
- SALBLOCK NITRIDE
- SALBLOCK RIE, SD RTA
- CoSi, BEOL: LI, CNT, MET1 to PAD

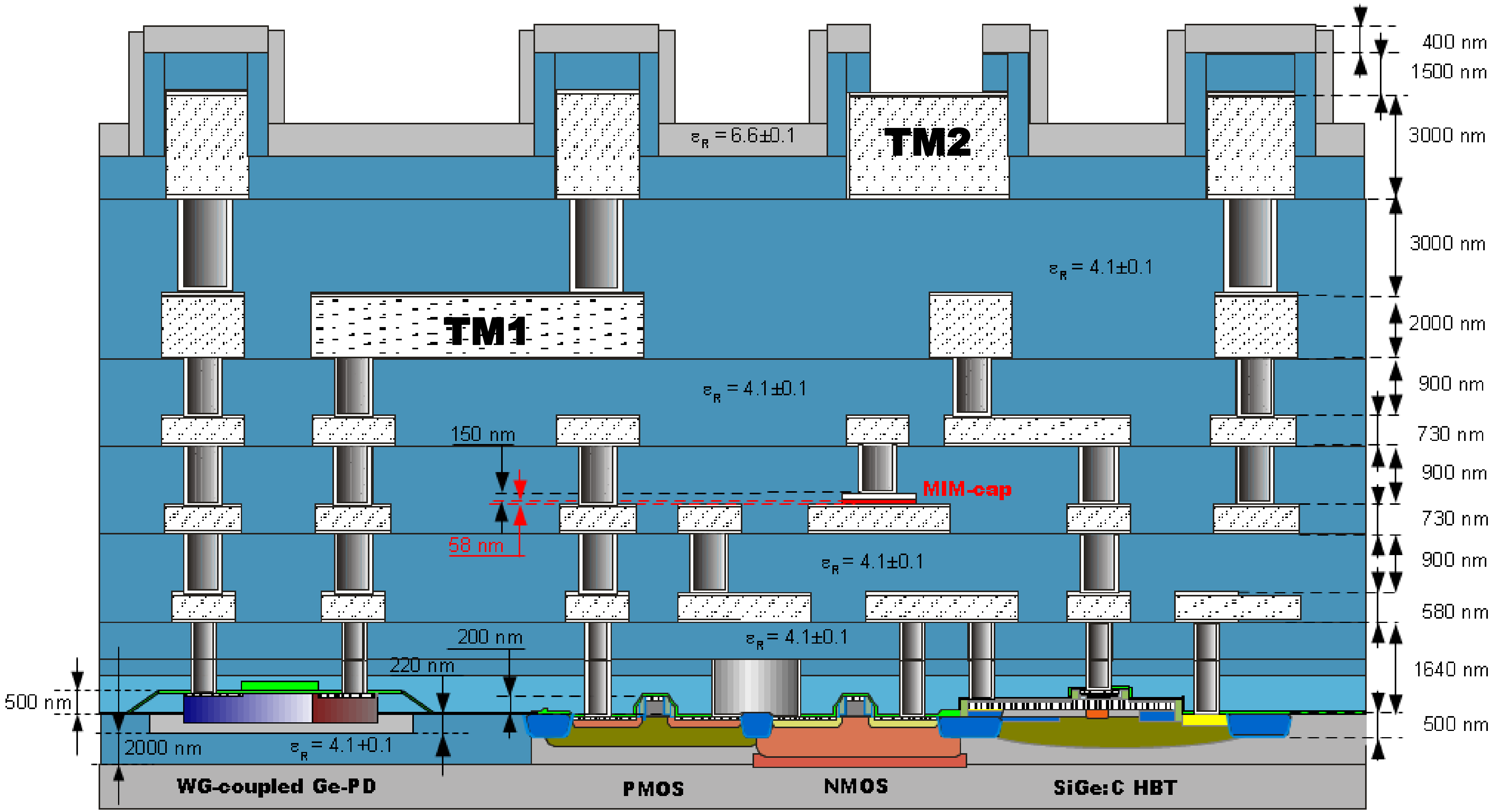
(26 Masks)

		# of additional mask steps
1st PHOT. MODULE	"LOCAL SOI / WG"	(+2)
2nd PHOT. MODULE	"MODULATOR"	(+5)
3rd PH. MODULE	"RIB WG/ COUPLER"	(+1)
4rd PH. MODULE	"PHOTO DETECTOR"	(+5)
5th PH. MODULE:	"GRATING OPEN"	(+1)??

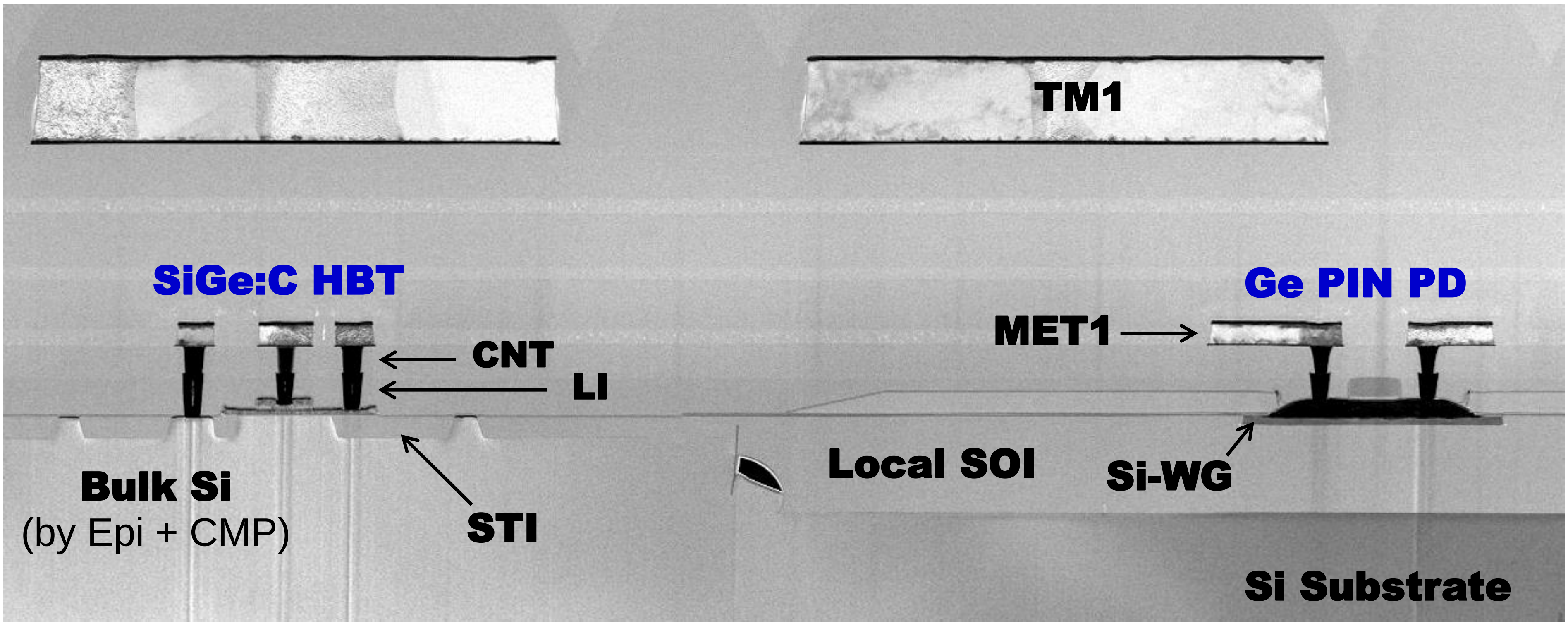
BiCMOS baselines for photonic device integration:

SG25H1 and SG25H3

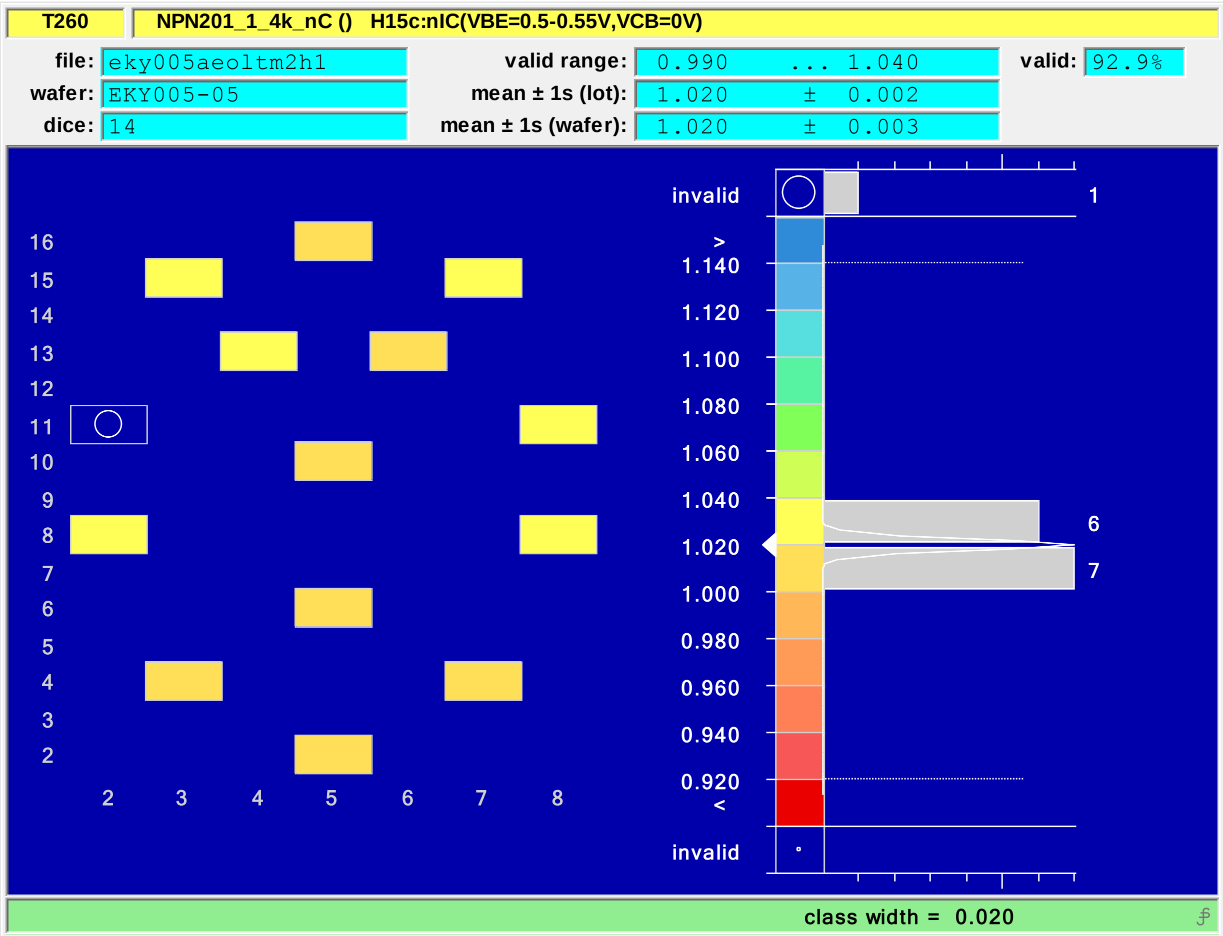
Photonic BiCMOS: Schematic process X-section



Photonic BiCMOS: Real process X-section



Photonic BiCMOS: BiCMOS yield behavior

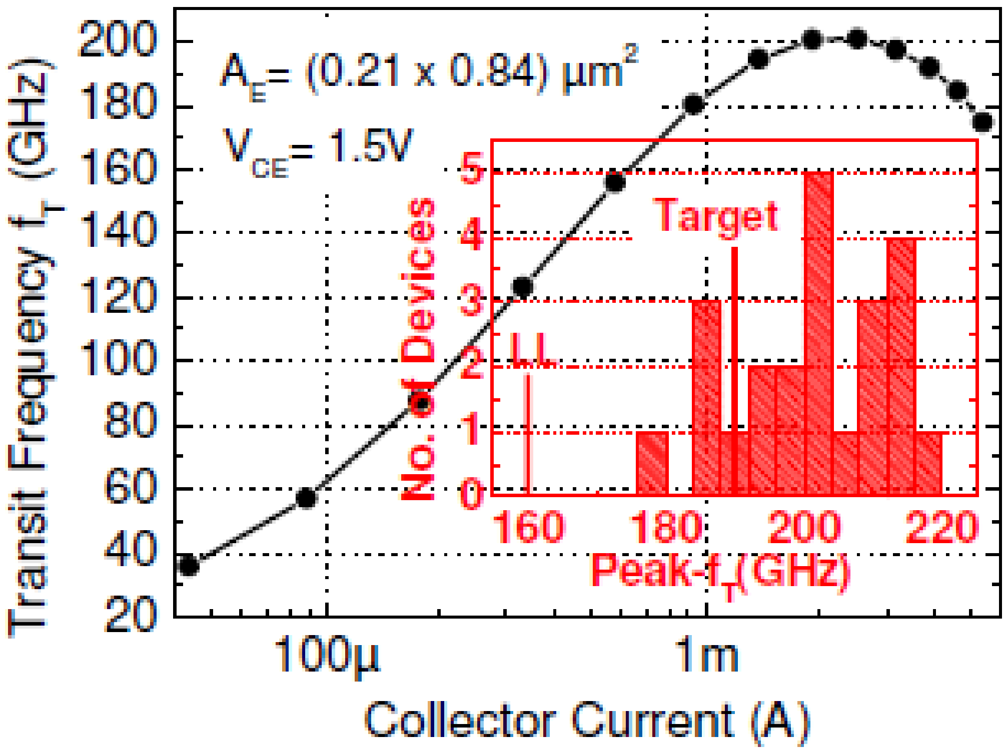


- I_C ideality factor (nC) wafer map for 4k HBT arrays (@ ~ 0.5 V V_{BE})
- nC < 1.05 indicates a pipe-free array, i.e. defect free HBT epi on local-bulk regions formed between local-SOI regions by selective Si-epi + Si-CMP

Local-SOI is not a "Bipolar-yield-limiter" (also confirmed for CMOS-yield-monitors)

Photonic BiCMOS: BiCMOS parameter behavior

f_T vs. I_C for SiGe:C HBTs fabricated in the photonic BiCMOS process + wafer histogram of peak-f_T vs. the baseline SG25H1 BiCMOS process limits



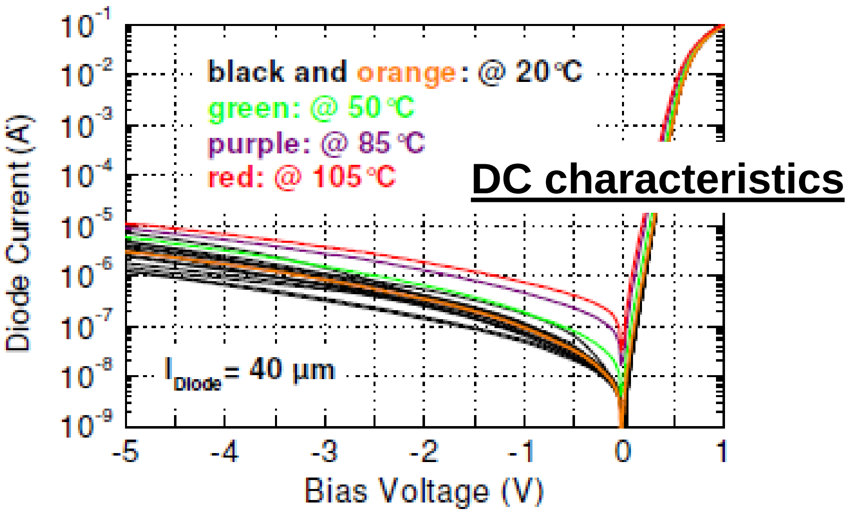
Despite the additional thermal budget of Ge-PD fabrication:

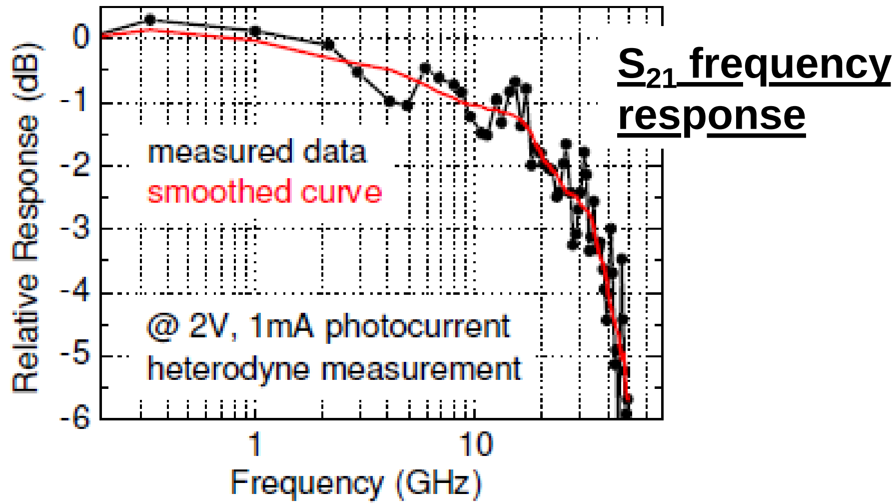
- **HBTs**
- **NMOS**
- **Poly-Si-Resistors**

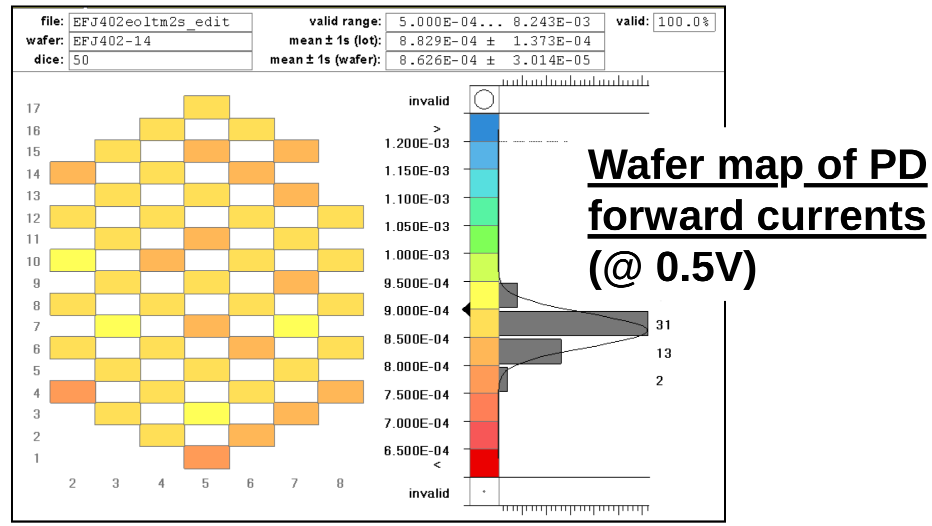
meet the parent BiCMOS process specs

- Not yet in the specs is PMOS

Photonic BiCMOS: Photonic performance (Ge-PD)







- Nice dark current behavior
- 30(+) GHz (-3dB) bandwidth with > 0.6A/W responsivity @ λ= 1.55µm
- Good Ge-PD manufacturability

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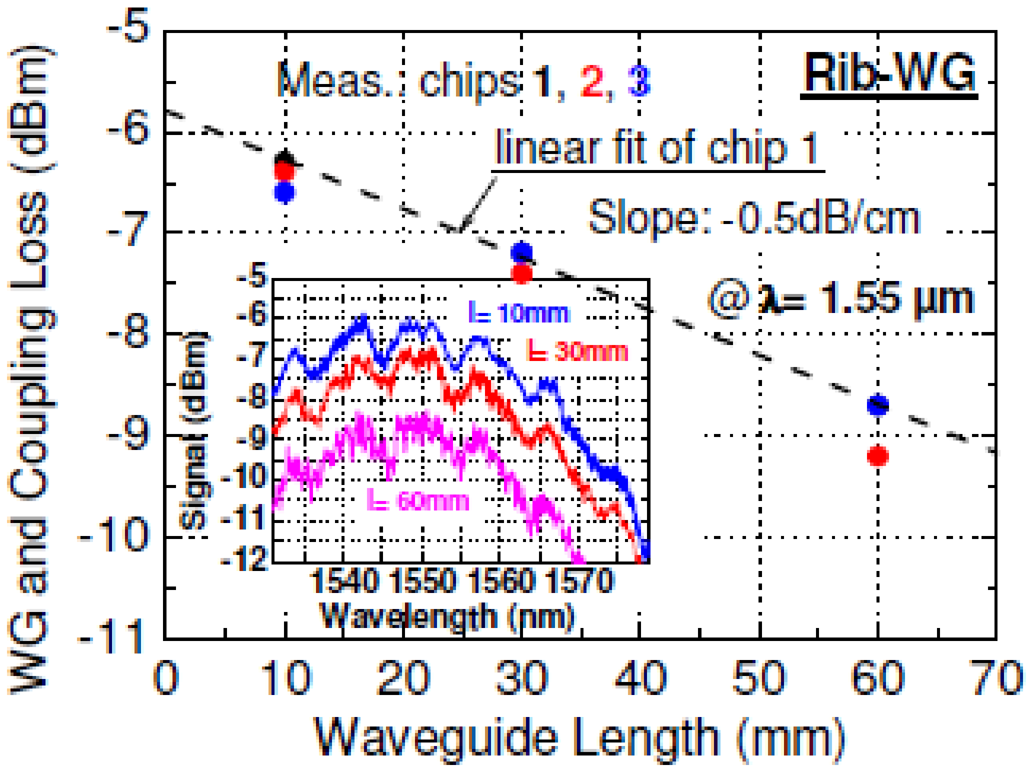
Photonic BiCMOS: WG and coupler performance



- Total loss vs. WG length of grating couplers w/ shallow-etched WG
- Coupling behavior was measured with BiCMOS protection and ILD layers over the coupler
- Note that we obtain the loss of coupling twice: in and out of the WG
- The inset shows the signal vs. wavelength curves

State-of-the-art PIC performance also in photonic BiCMOS:

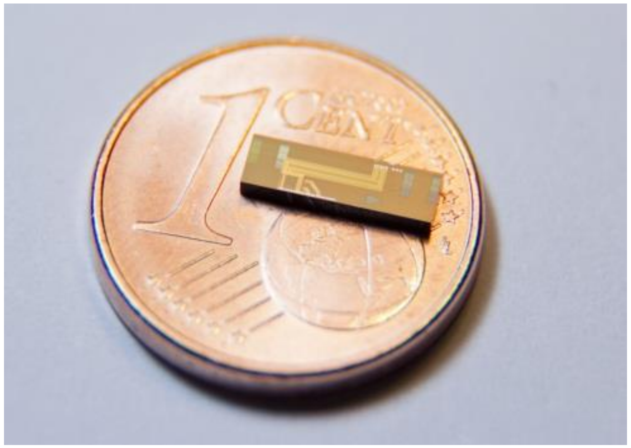
- ➢ **3dB coupling loss** (reduction to 1.5dB w/ advanced version → + 1 mask)
- ➢ **< 0.7 dB/cm linear loss for Rib-WG** (2.4 dB/cm for Nano-WG)

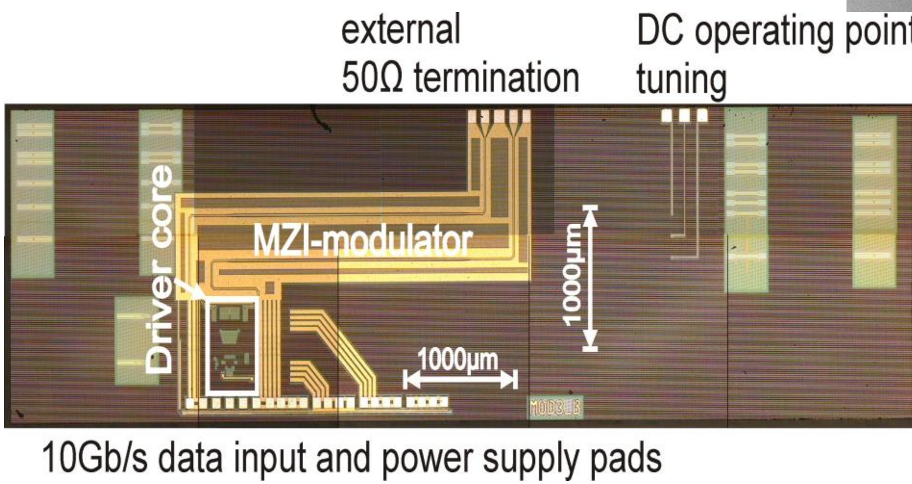
Photonic BiCMOS: What next?

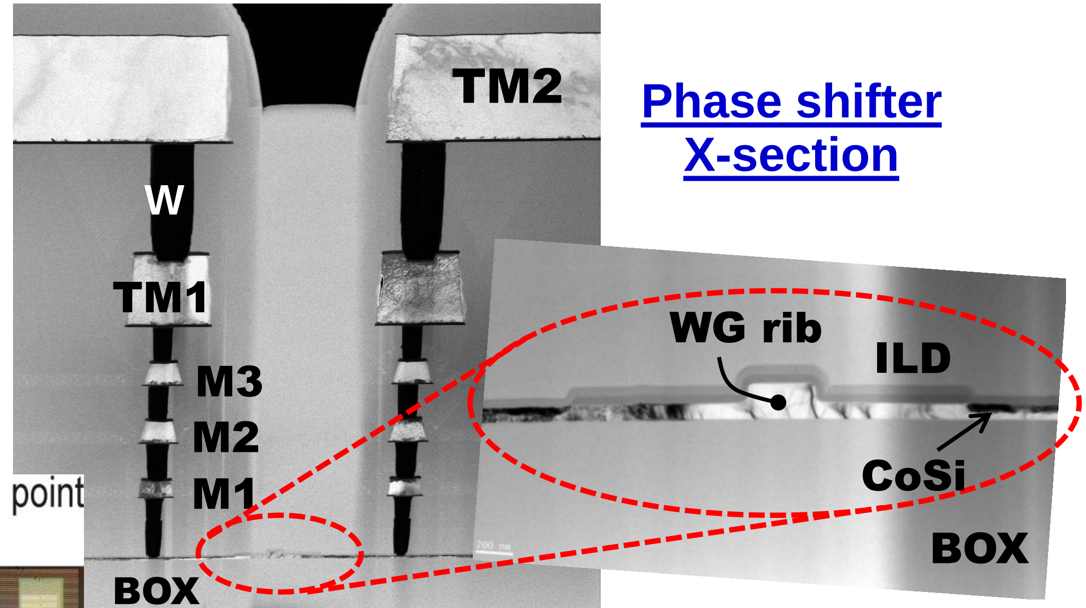
- **Bring PMOS in the specs:**
  - **Key is a Ge epitaxy with much lower thermal budget than applied so far** (promising layer defectivity results already exist; maybe to compromise w/ dark current behavior)
  - "Colder" BiCMOS protection layers for Ge-PD-fabrication??
- **Improve photo-detector bandwidth** (for applications beyond the RF2THZ demo)**:**
  - **Reduce thermal budget of detector post-processing** (by the BiCMOS CoSi module; ILD reflow)**, but without negative impact on BiCMOS device yield and parameters**

First EPIC demonstrators in "Photonic BiCMOS"

Photonic BiCMOS (SG25H3): Driver + Mach-Zehnder modulator

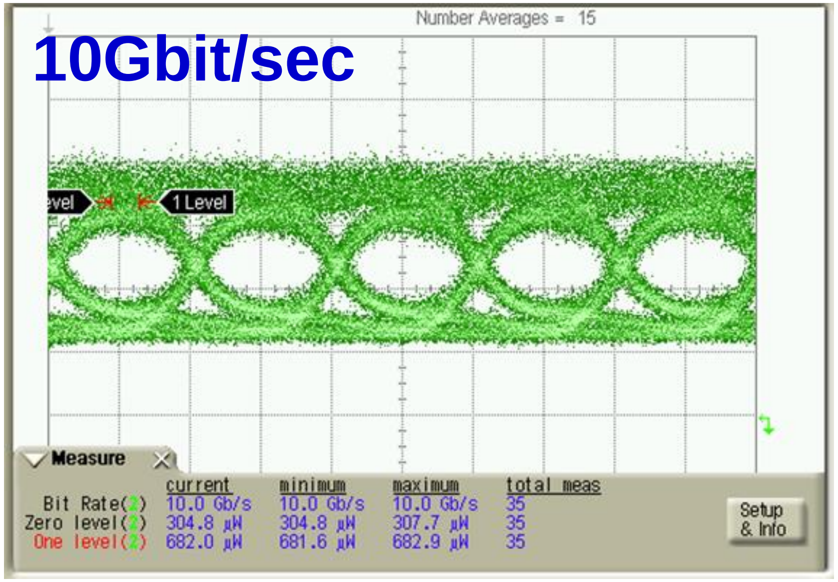






L. Zimmermann et al.: "Monolithically Integrated 10Gbit/sec Silicon Modulator with Driver in 0.25µm SiGe:C BiCMOS"; 39th European Conference on Optical Communication (ECOC), London, 2013

First EPIC demonstrators in "Photonic BiCMOS" (cont'd)



Dominant loss:
RF phase shifter 7.5dB
DC phase shifter 4.0dB

Co-work of Vienna Uni (EMCE), Uni Southampton (Optoel. Res. Centre), PHOTLINE Technologies, TU Berlin (Joint Lab Silicon Photonics), and IHP in the HELIOS project:

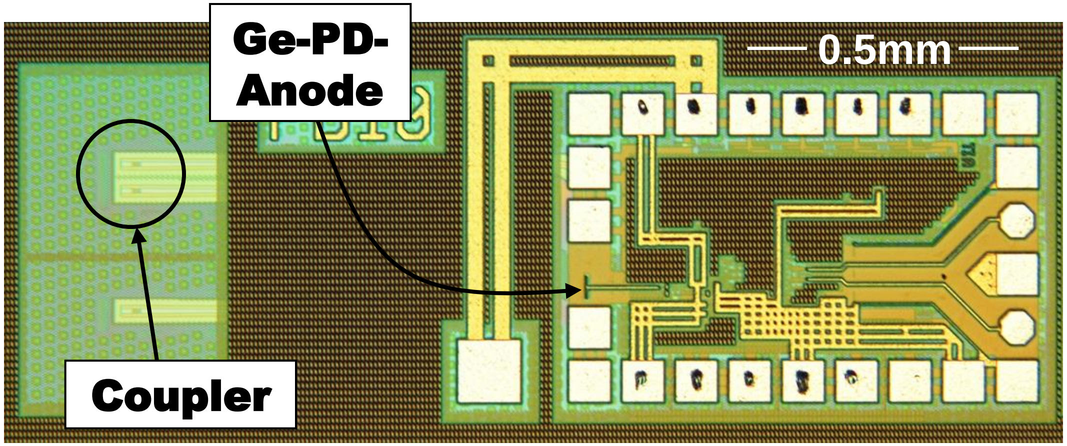
Driving test conditions:
240mV PRBS (digital)
1540nm
TE
8.5dB extinction ratio

Total on chip loss: 13dB

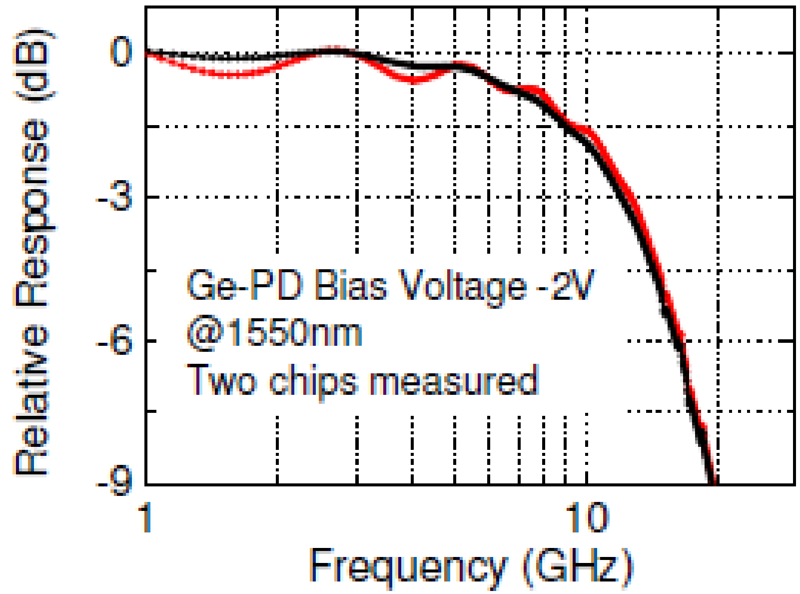
- **Photonic BiCMOS 1st driver + MZM**
- **Target speed demonstrated**
- Much too high insertion loss due to doping issues → expect improvements with next design + process)
- **Higher speed by design**
- **Low loss due to process tuning**

First EPIC demonstrators in “Photonic BiCMOS” (cont’d)

Photonic BiCMOS (SG25H1): Receiver (Ge-PD + TIA)



SG25H1-TIA designed for 20Gbps data rate



Measured receiver characteristics demonstrate successful implemen-tation of our photonics integration approach

Summary and conclusions

- The development status of a new "Photonic BiCMOS" process in the RF2THZSiSoC project was presented and discussed
- State-of-the-art photonic devices, including a high-speed Ge-PD, were integrated in a high-performance SiGe BiCMOS process for the first time
- First fabricated demonstrators but also the reached performance of most photonic and BiCMOS devices demonstrate the successful implementation of our photonics integration approach
- A weak point in the current status of process development, un-sufficient PMOS compatibility with Ge-PD integration, must be "repaired" next

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Federal Ministry of Education and Research

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