DE LA RECHERCHE À L'INDUSTRIE

cea

ATRENE

Cluster for Application and Technology Research in Europe on NanoElectronics

RF2THZ SISOC Project

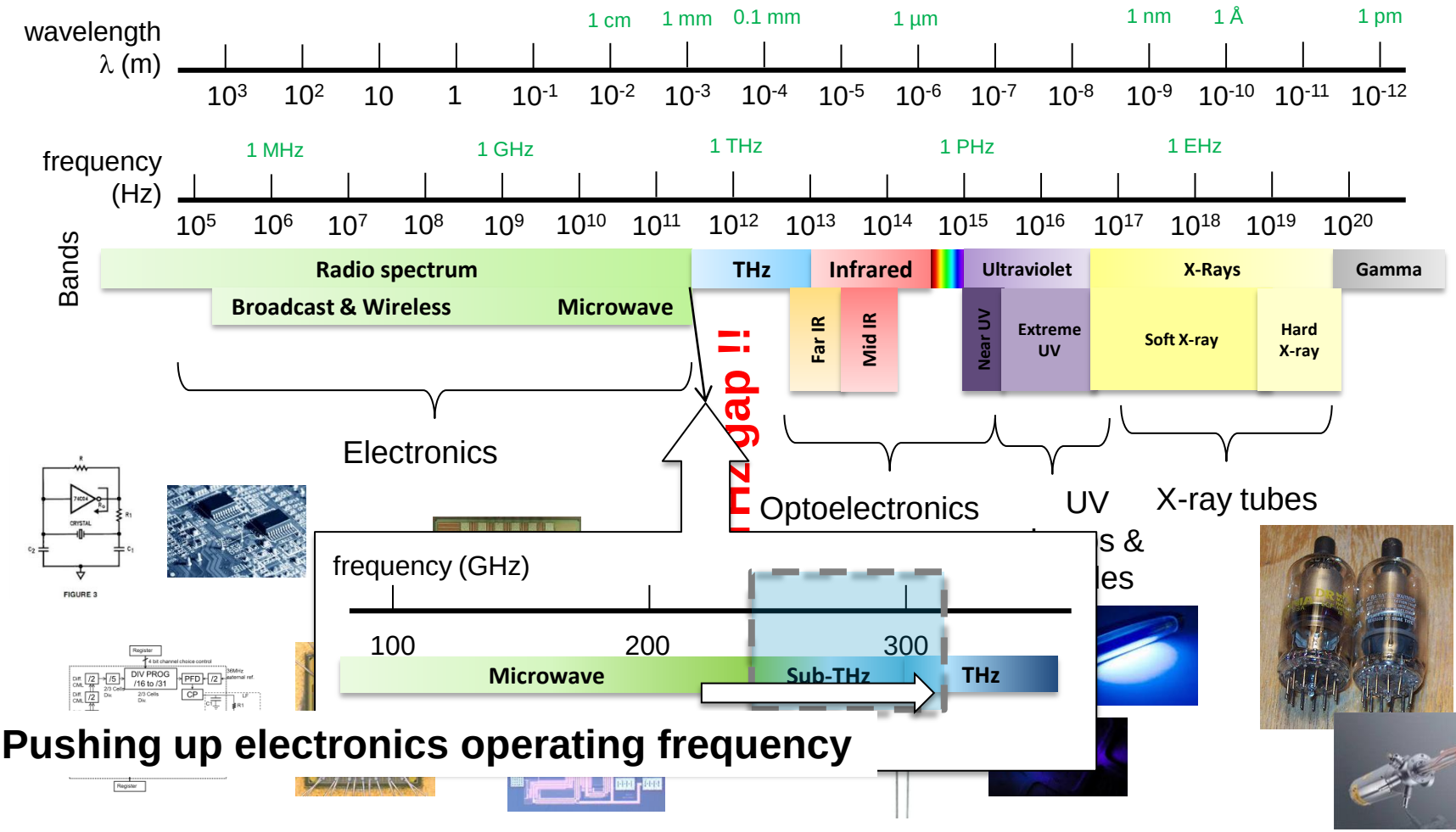
Coherent sub-THz transmission systems in Silicon technologies: design challenges for frequency synthesis

Alexandre Siligaris

Outline

- Introduction-context for sub-THz
- Some ideas for low PhN
- Architecture and design choices
- Examples on fabricated circuits
  - CMOS 65nm
- Application to THz imagers : impact of PhN

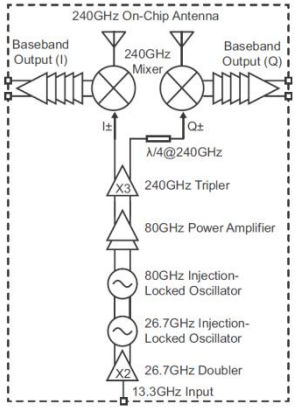
Spectrum : available sources



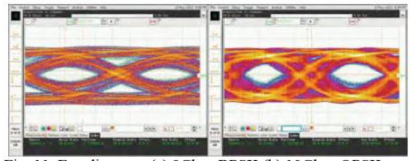
Introduction-Context

- THz gap: increasing electronics frequency
  - Application to

Communication systems



>10 Gbps QPSK RX at 240 GHz



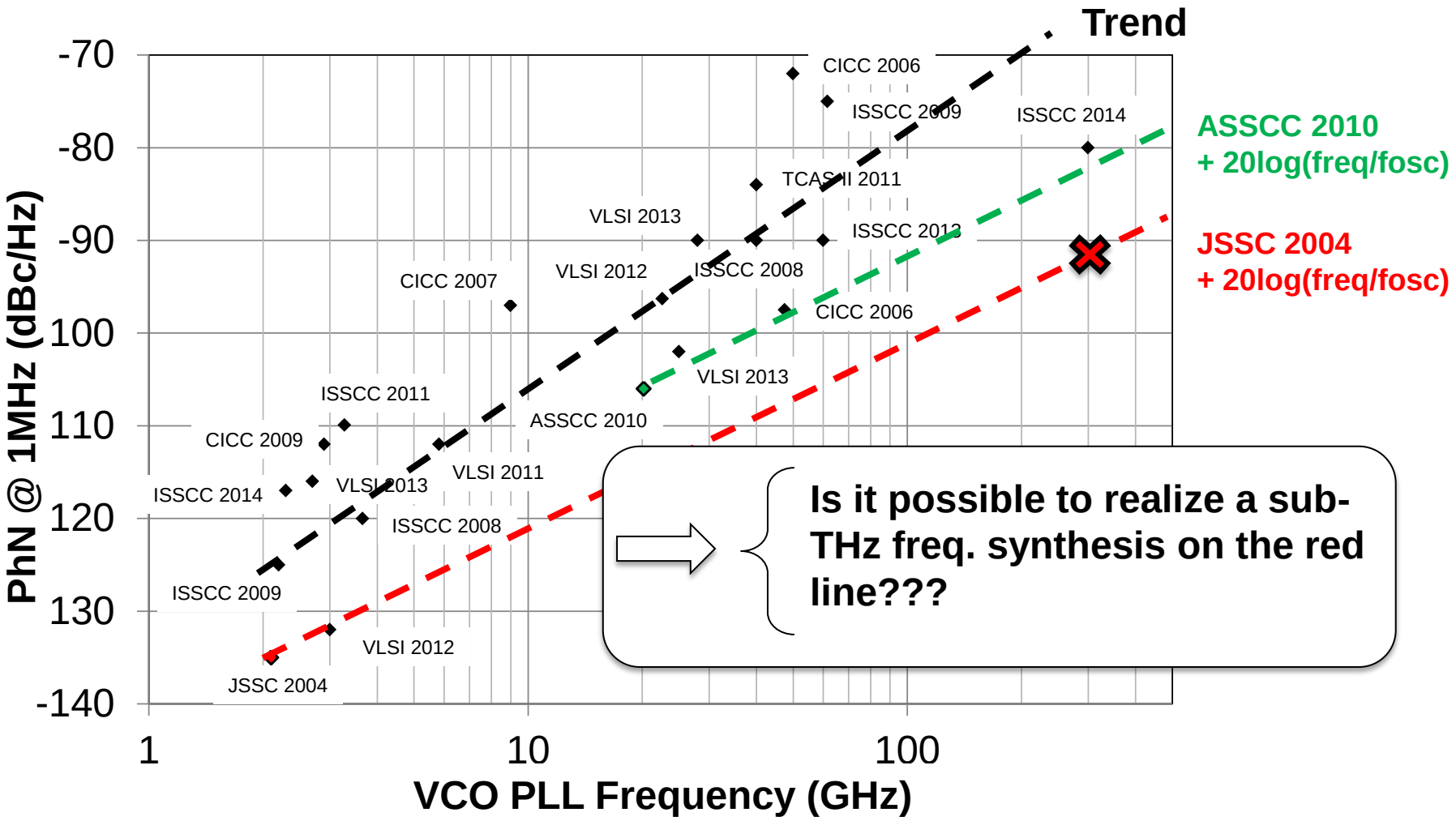
Thyagarajan et al. RFIC 2014

Need of coherent (locked) frequency sources

THz imaging :

* F. Schuster et al, ISSCC 2011

- RF & mmW PLL state of the art. PhN vs Osc. frequency



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  - BiCMOS 55nm
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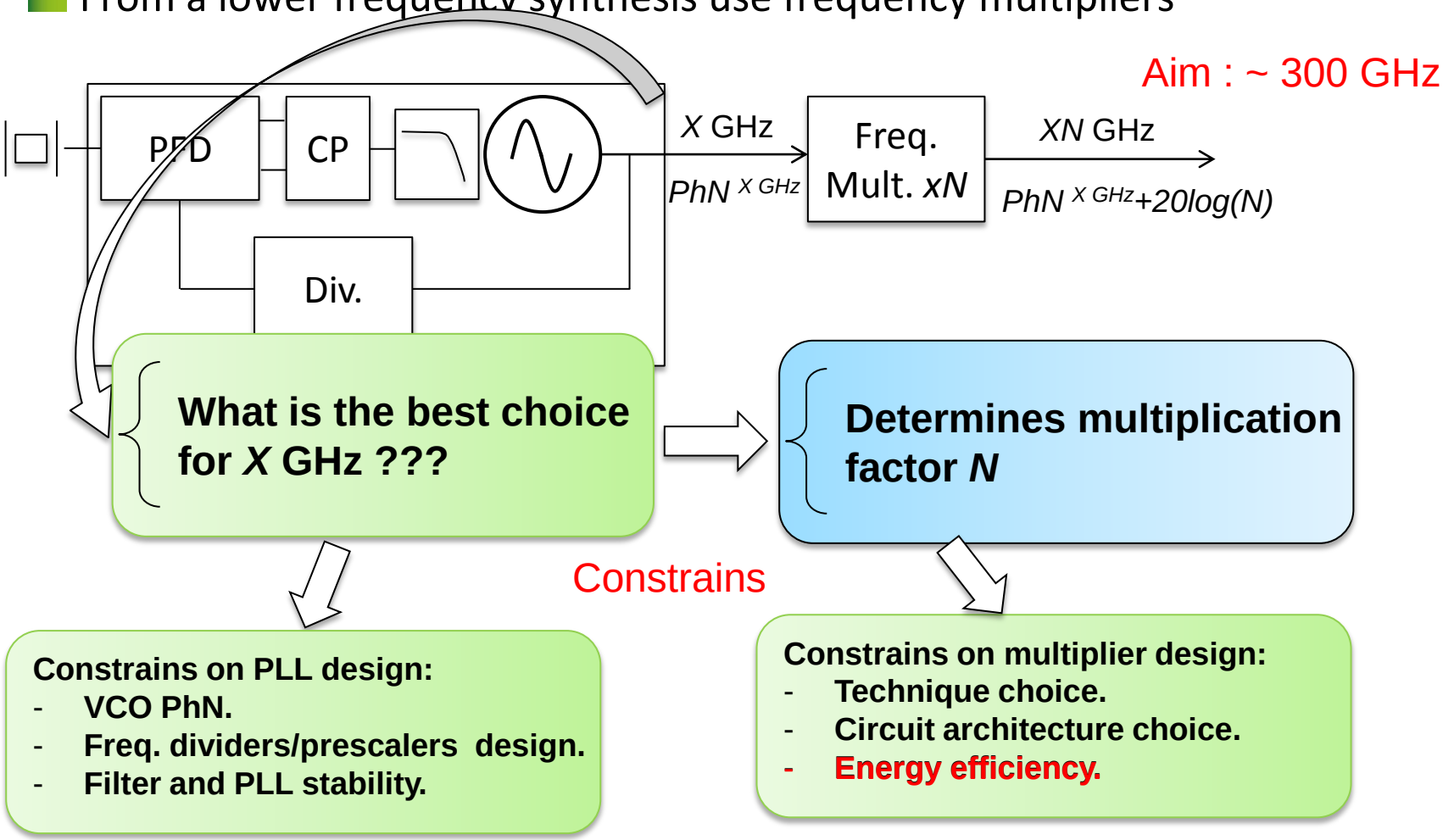
Some ideas for low PhN

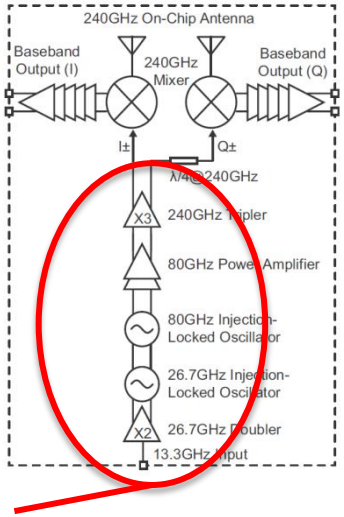
- Main idea:
  - From a lower frequency synthesis use frequency multipliers



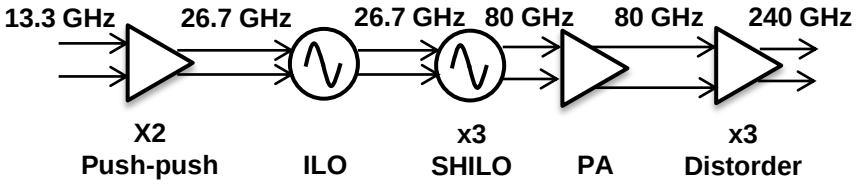
Some ideas for low PhN

- State of the art high order freq. mult. for THz

Berkeley (RFIC 2014): 240 GHz QPSK Rx

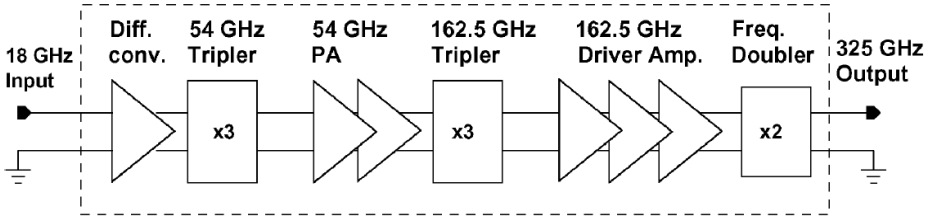


LO generator @ 240 GHz



X18 Multiplier in CMOS 65nm
P_{DC}~ 180 mW

University of Wuppertal (TMTT 2011): 325 GHz LO generator

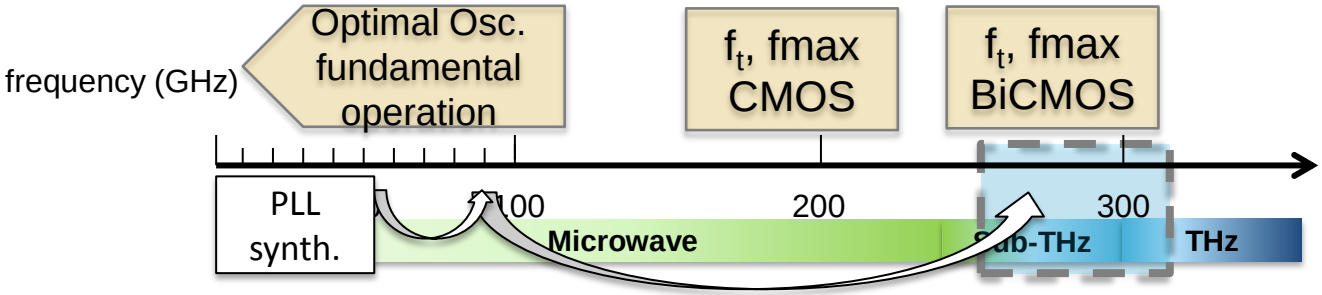


x3 Distorder **x3 Distorder** **x2 Distorder**

X18 Multiplier in CMOS 65nm
P_{DC}~ 1500 mW

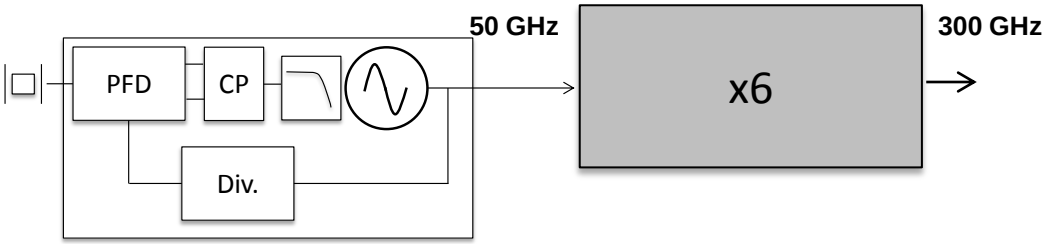
Some ideas for low PhN

- Frequency Multiplication steps: example 1



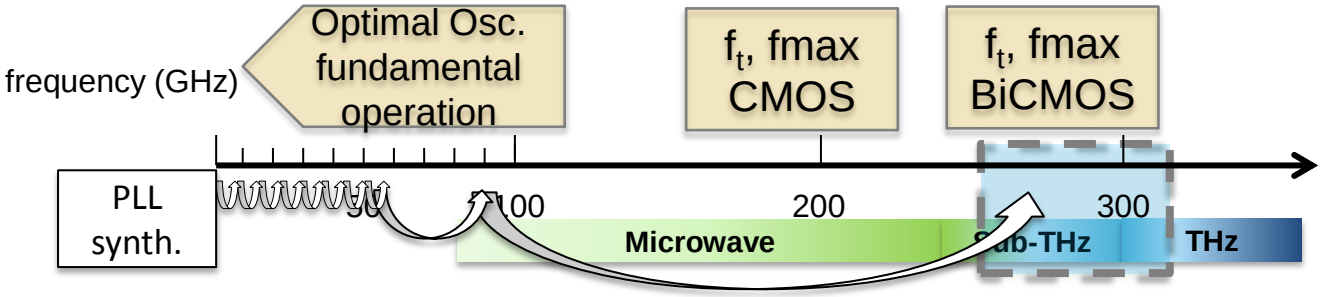
Example : PLL_{freq}=50 GHz, F_{out}=300 GHz => N=6

x6 the oscillator fundamental frequency



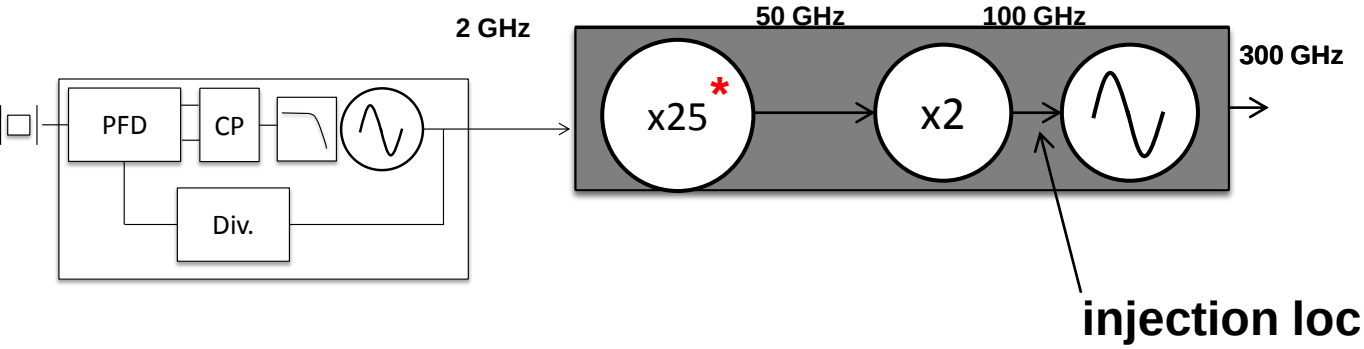
Some ideas for low PhN

Frequency Multiplication steps: example 2



Example : PLL_{freq}=2 GHz, F_{out}=300 GHz => N=150

x150 the oscillator fundamental frequency



* C. Jany et al. "A novel ultra-low phase noise, programmable frequency multiplier-by-30 architecture. Application to 60-GHz frequency generation," ESSCIRC 2014.

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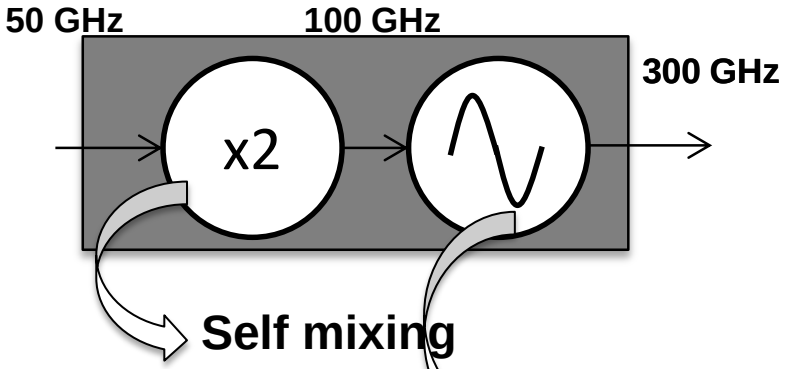
Architecture and design choices

- Frequency Multiplication steps: design choices

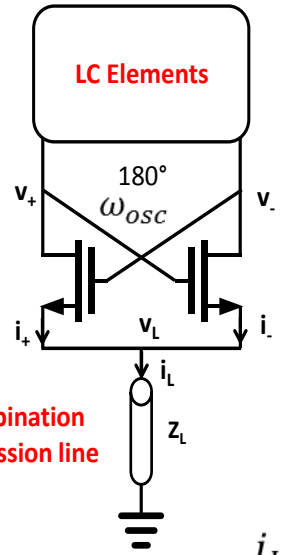


High order oscillator :

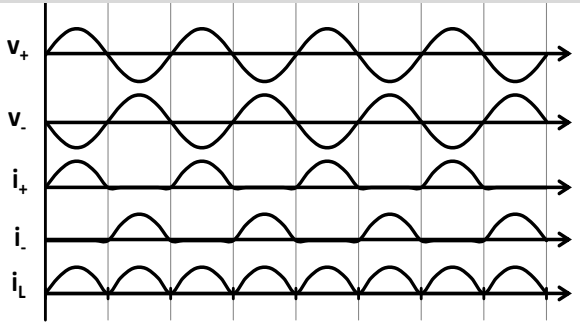
- **Push-Push** → 2nd harmonic
- **Push-Push-Push (Triple Push)** → 3rd harmonic
- **Push-Push-Push-Push (Q-Push)** → 4th harmonic
- **…**

- N-Push principle:

Example Push-Push:



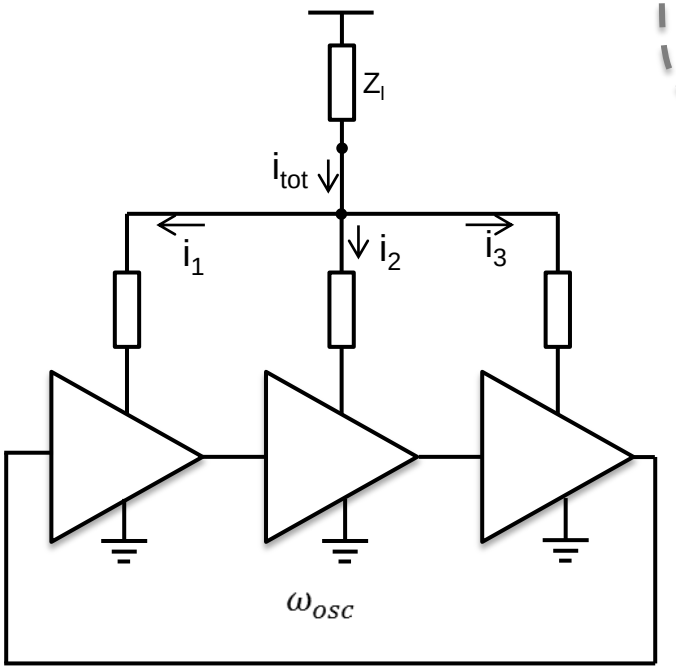
On common mode node:
- **Even Harmonics combined**
- **Odd harmonics out of phase**

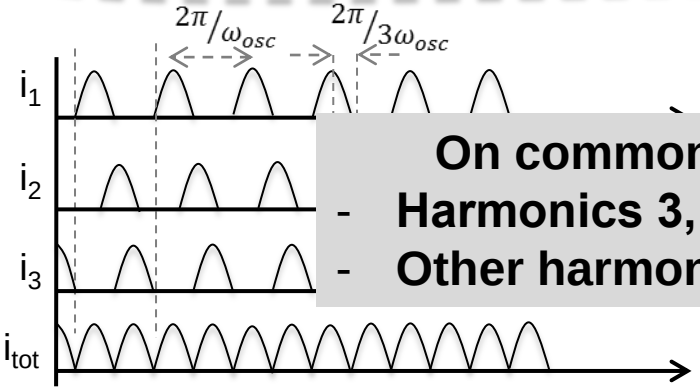


$v_L = i_L * Z_L$

$$i_L \approx I_{osctot_2} e^{j(2\omega_{osc}t)} + I_{osctot_4} e^{j(4\omega_{osc}t)} + \cdots$$

Example Triple-Push:





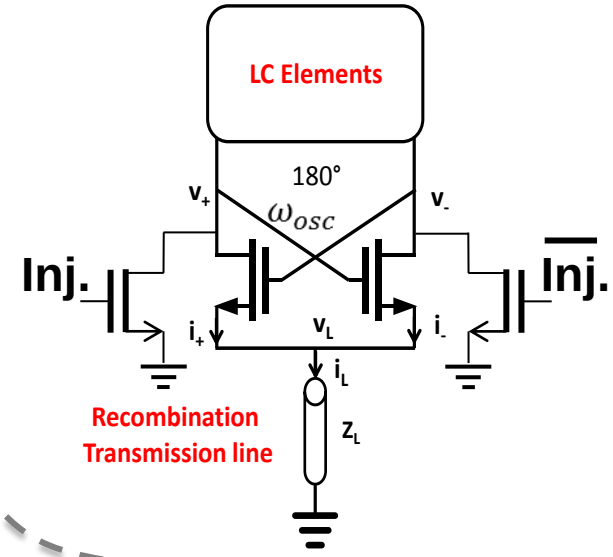
On common mode node:
- **Harmonics 3, 6, 9 … combined**
- **Other harmonics out of phase**

$$i_{tot} \approx I_{osctot_3} e^{j(3\omega_{osc}t)} + I_{osctot_6} e^{j(6\omega_{osc}t)} + \cdots$$

Architecture and design choices

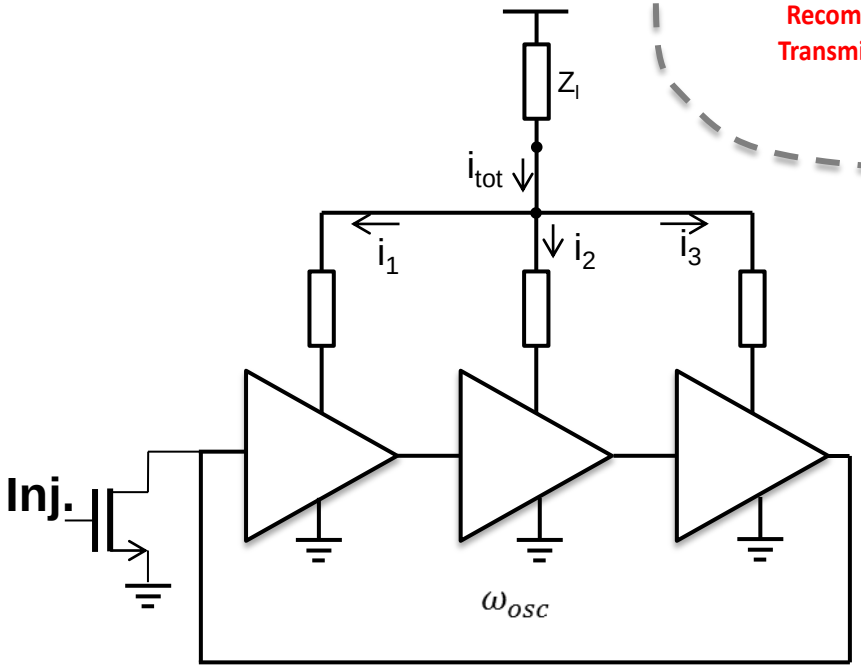
- N-Push sub-harmonic locking principle:

Example Push-Push:



$$\omega_{inj} \approx \omega_{osc}$$

Example Triple-Push:



$$\omega_{inj} \approx \omega_{osc}$$

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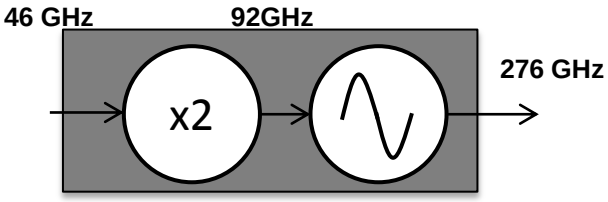
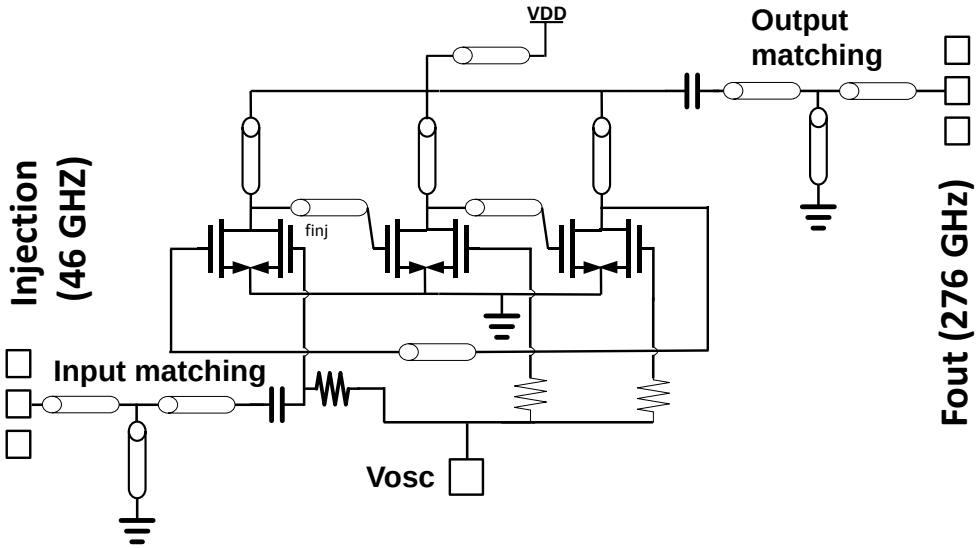
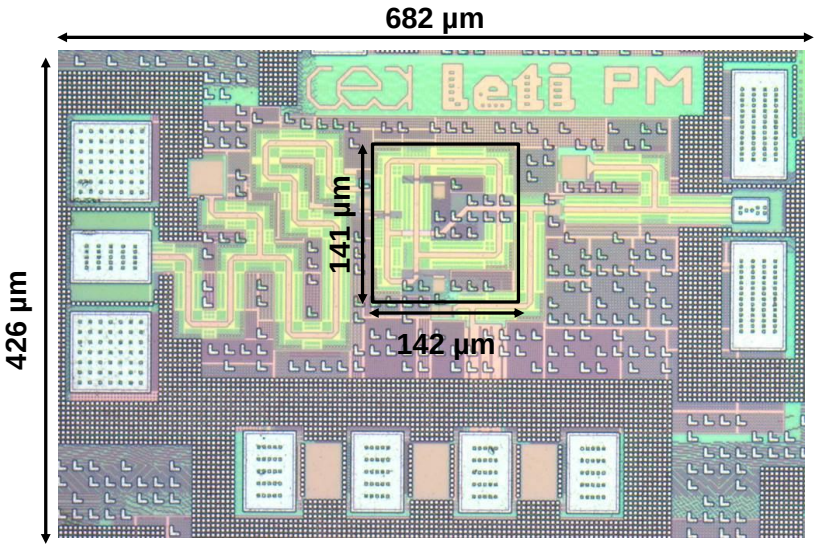
Examples on fabricated circuits

- Fabricated circuits in CMOS 65nm

Triple-Push oscillator in CMOS 65nm:

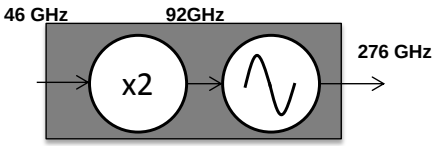




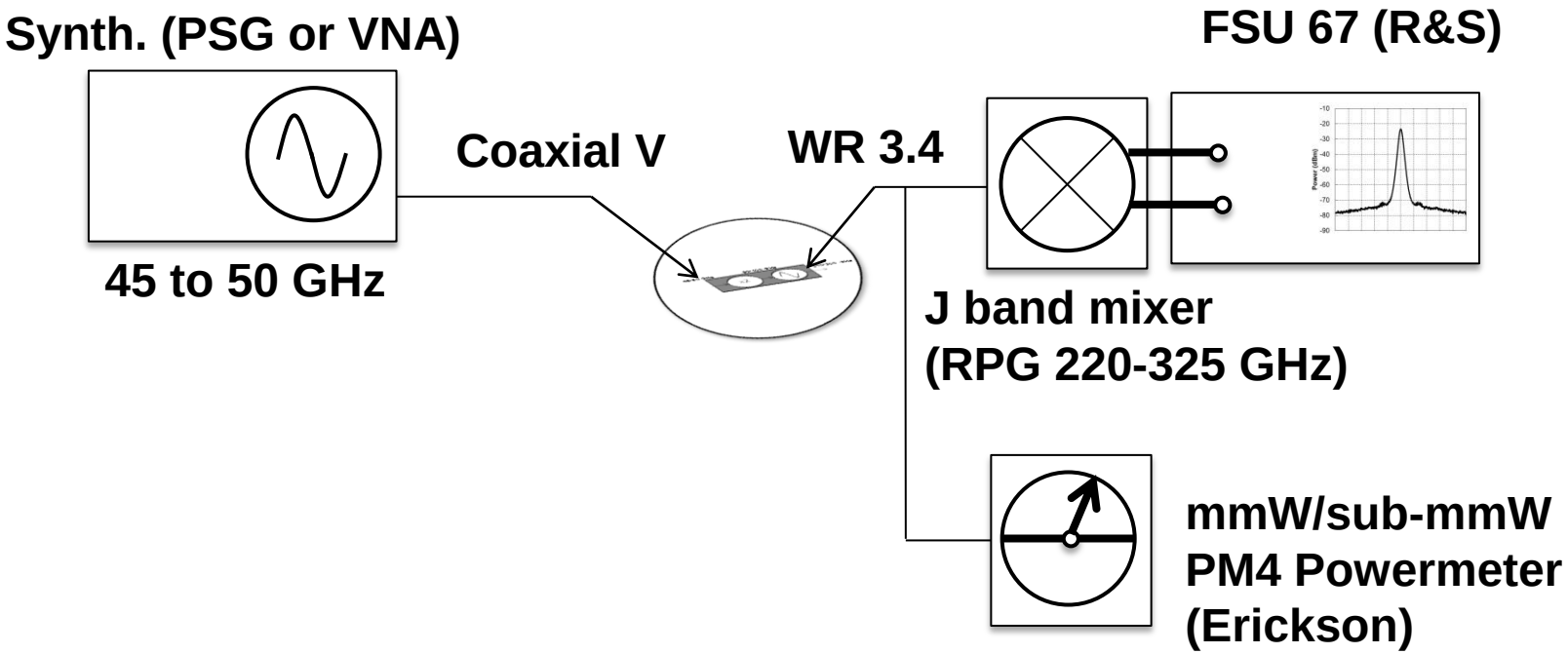


Examples on fabricated circuits

- Fabricated circuits in CMOS 65nm

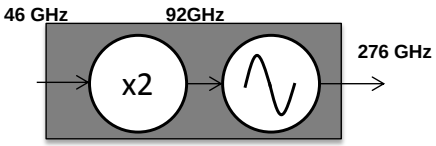


Triple-Push oscillator measurement setup:

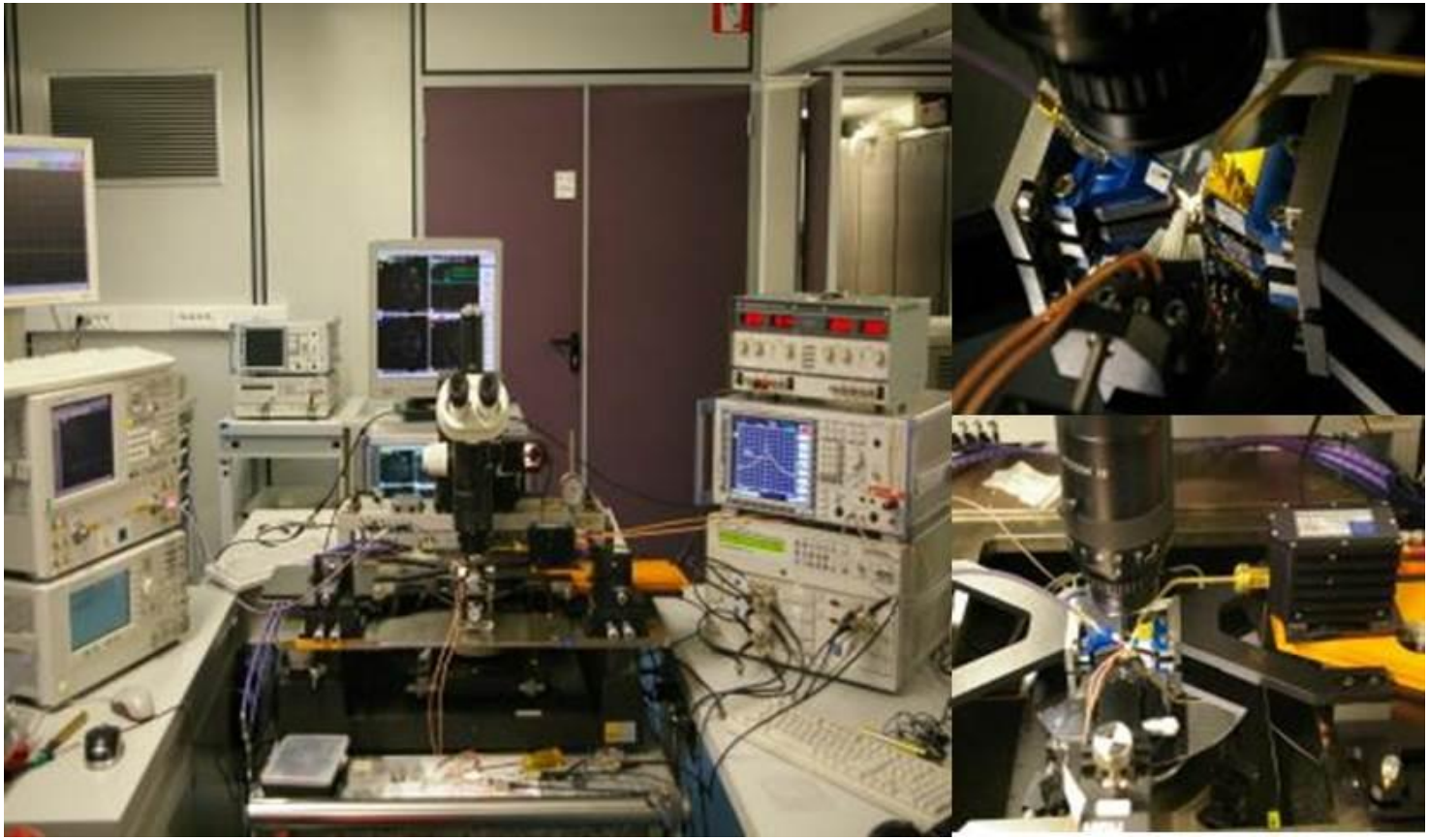


Examples on fabricated circuits

- Fabricated circuits in CMOS 65nm

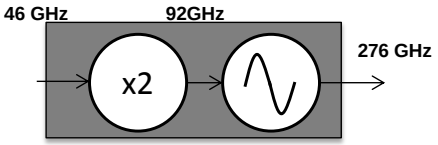


Triple-Push oscillator measurement setup:

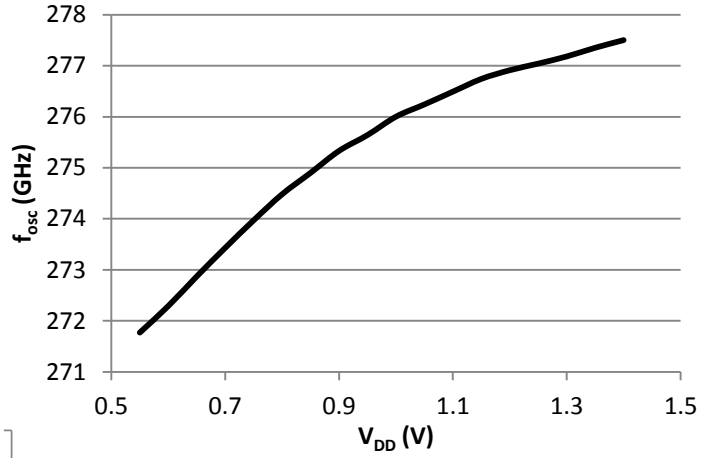


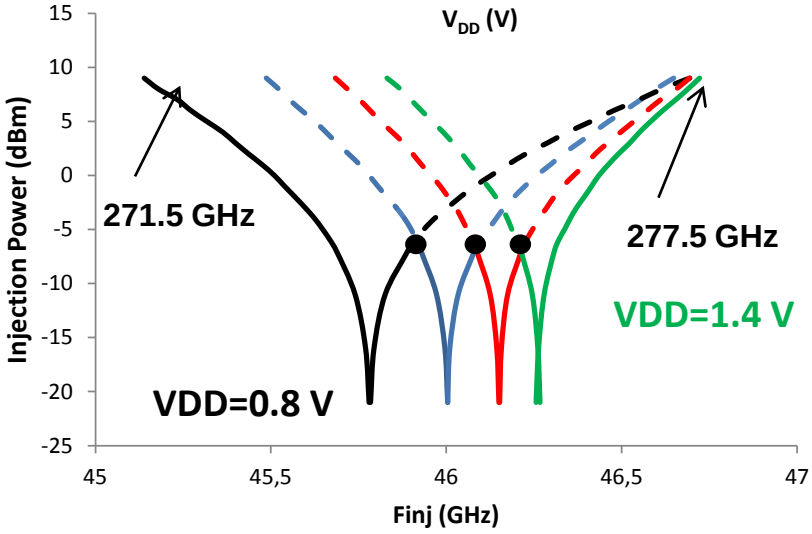
Examples on fabricated circuits

- Fabricated circuits in CMOS 65nm

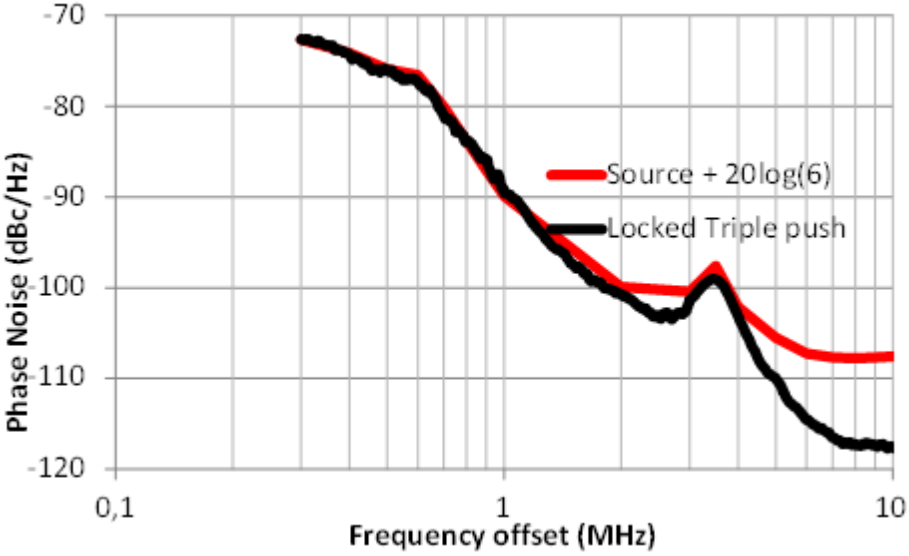


Triple-Push oscillator measurement results:



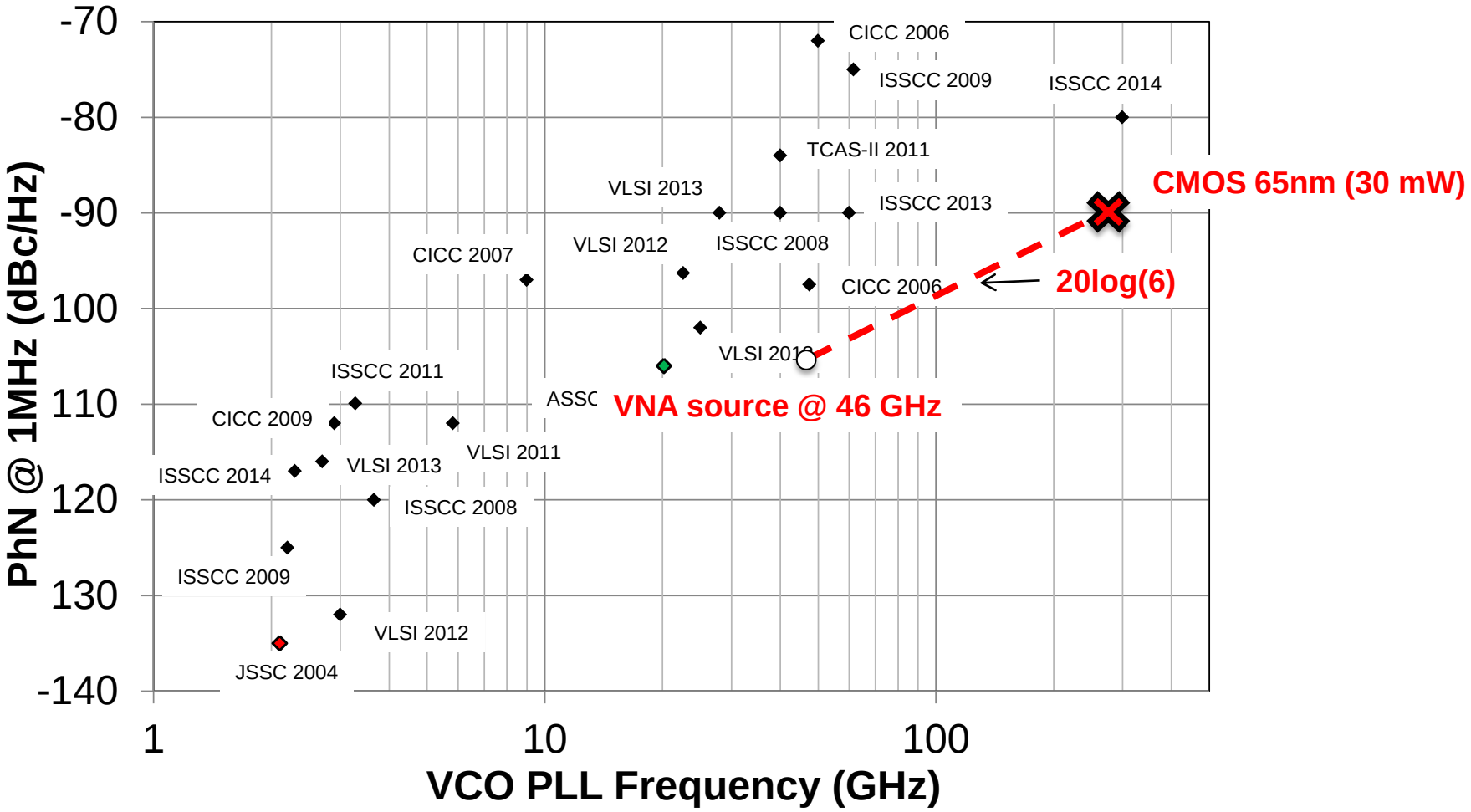


Pdc: 15 – 90 mW
Nominal at 276 GHz : 30 mW



Examples on fabricated circuits

- RF & mmW PLL state of the art. PhN vs Osc. frequency



Examples on fabricated circuits

- THz oscillators-sources state of the art

TABLE I
Comparison of recently published Silicon Oscillators near 300 GHz

Ref.	Tech.	Fosc. (GHz)	Tunning Range (%)	Pout (dBm)	Pdc (mW)	PhN(1MHz) (dBc/Hz)	FOM(1MHz)* (dBc/Hz)
[3]	BiCMOS 90nm	280-303	8	-14	105	-80	-169.1
[4]	CMOS 65nm	338	2	-1	82	-93	-184.4
[5]	CMOS 65nm	288	-	-1.5	275	-87	-171,8
[6]	CMOS 65nm	285-290	1.7	-19	70	-80.5	-171,2
[7]	CMOS 65nm	283-296	4.5	-1.5	325	-78	-162,1
This Work	**BiCMOS 55nm**	**272-303**	**10.8**	**-9**	**52**	**-105**	**-197**

$$*FOM(\Delta f) = PhN(\Delta f) - 20log\left(\frac{f_{osc}}{\Delta f}\right) + 10log\left(\frac{P_{DC}}{1mW}\right)$$

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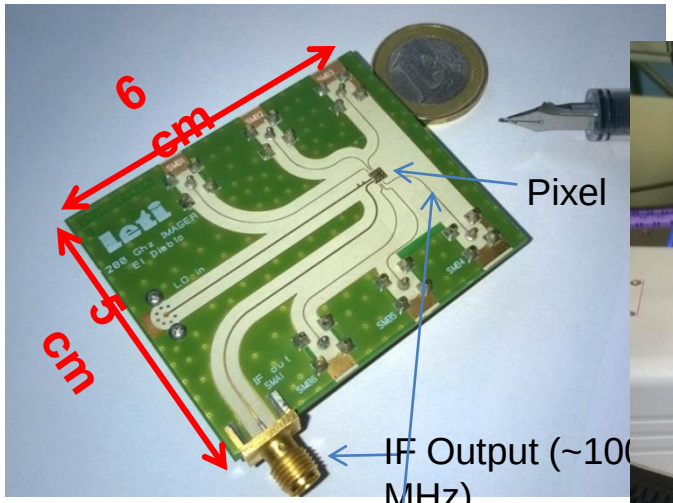
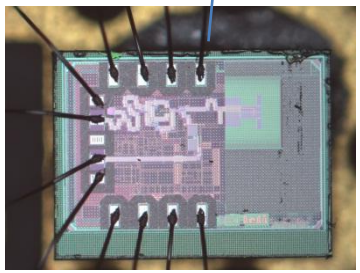
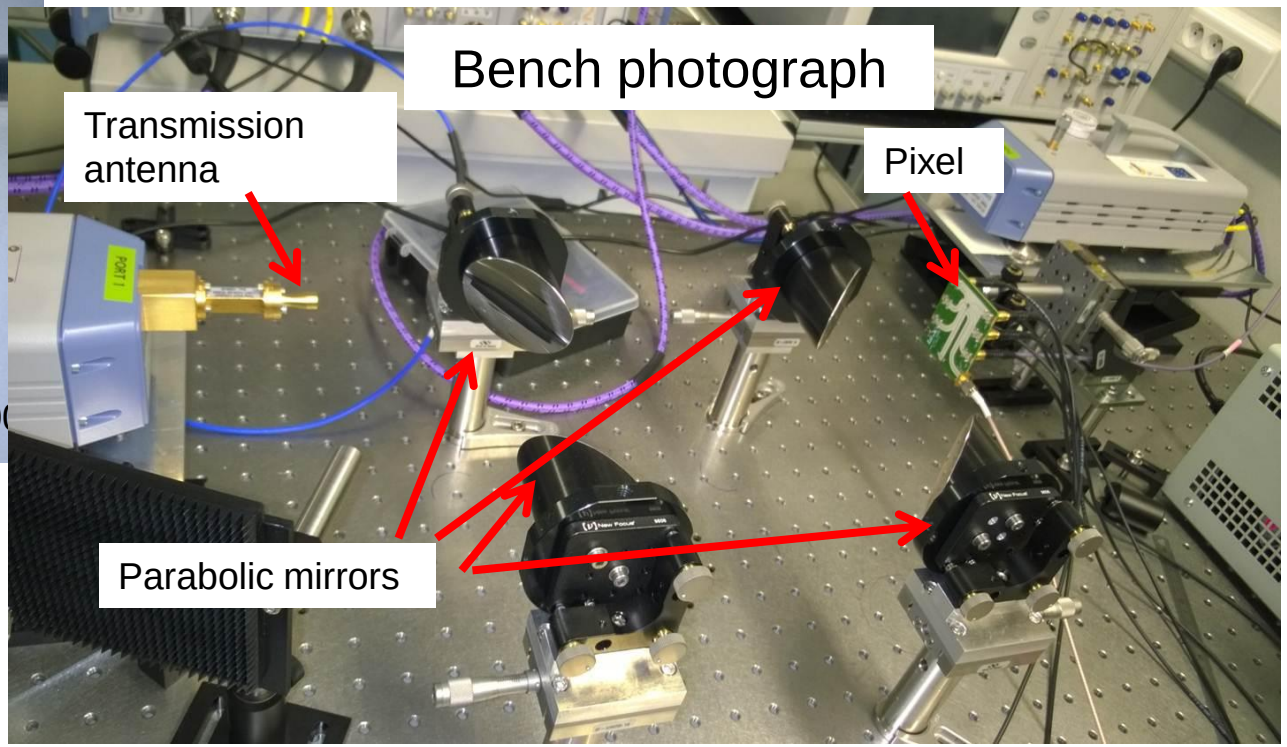
Application to THz imagers : impact of PhN

- Sub-THz heterodyne pixel in CMOS 65nm



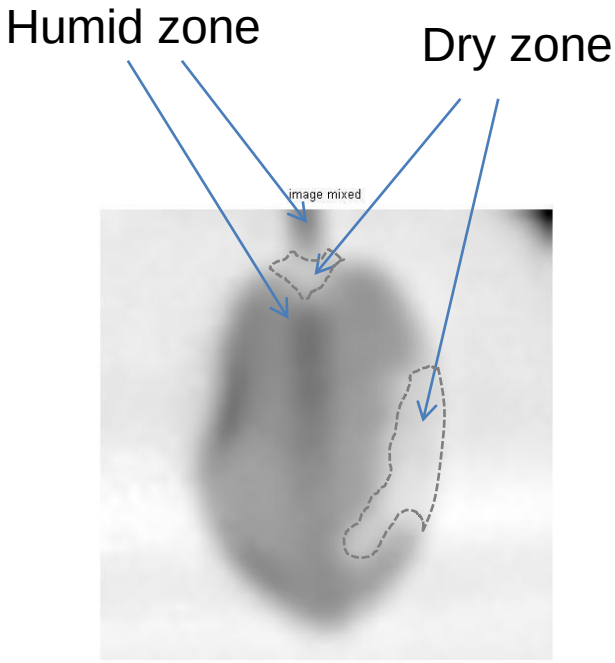




First LETI's 280 GHz heterodyne receiver with integrated antenna
(CMOS 65nm using the presented sub-harmonic injection locked oscillator)

Application to THz imagers : impact of PhN

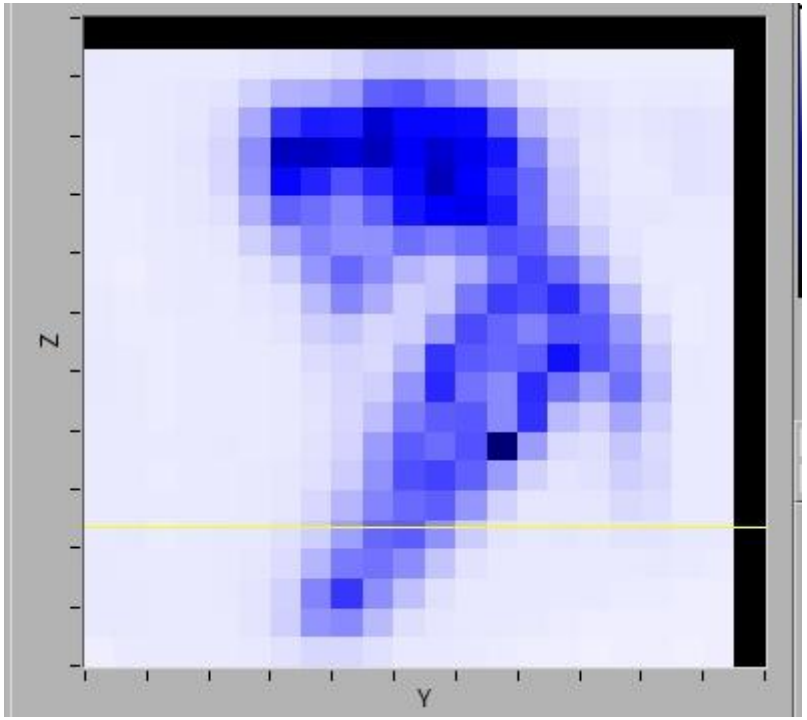
- Sub-THz heterodyne pixel in CMOS 65nm: Raster scan image (step 0.75 mm)



Rx with locked oscillator at 278 GHz
Image Dynamic (max SNR) : 20 dB

Application to THz imagers : impact of PhN

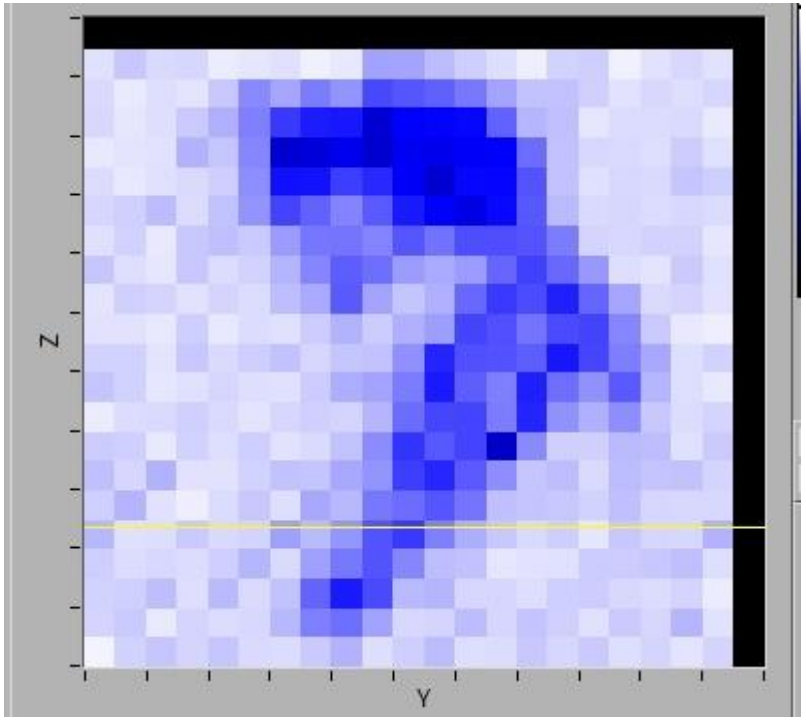
- Sub-THz heterodyne pixel in CMOS 65nm: raster scan image (step : 1.5 mm)



Rx with locked oscillator at 278 GHz
Image Dynamic (max SNR) : 45 dB

Application to THz imagers : impact of PhN

- Sub-THz heterodyne pixel in CMOS 65nm: raster scan image (step : 1.5 mm)



Rx with **free run** oscillator at 278 GHz
Image Dynamic (max SNR) : 35 dB
(10 dB loss on SNR !!!)

Application to THz imagers : impact of PhN

- Sub-THz heterodyne pixel in CMOS 65nm: raster scan image (step : 0.75 mm)

Rx with locked oscillator at 278 GHz
Image Dynamic (max SNR) : 50 dB

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- **CONCLUSION**

Conclusion

- Need of coherent (locked) frequency synthesis in the THz band.
- Low phase noise implies low frequency PLLs and high multiplication factors.
- Multiply, multiply, mutiply…

leti

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