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Advances in SiGe BiCMOS Technology for mm-Wave Applications in the DOTSEVEN Project

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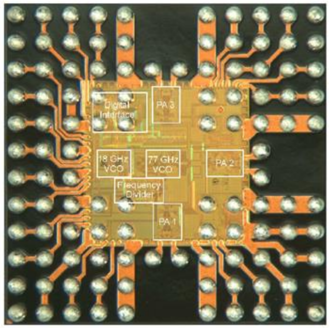
WS12: EuMIC - *SiGe for mm-Wave and THz*

Outline

- Introduction
  - Motivation – market pull and technology push
- DOTSEVEN results:
  - Exploitation of „evolutionary“ DOTFIVE results: Scaled conventional **D**ouble-**P**olysilicon **S**elf-**A**ligned (DPSA) HBT with **S**electively **E**pitaxially **G**rown (SEG) base to BiCMOS – B11HFC
  - Exploitation of „revolutionary“ DOTFIVE results: DPSA-SEG HBT with Epitaxial Base Link – Joint IHP/Infineon Flow
  - SiGe HBT Performance Status
- Summary
- Acknowledgement
- References

Motivation – Market Pull

- High-speed SiGe HBT bipolar processes are used today for leading edge RF applications like
  - Automotive radar @ 77 GHz
  - Front-ends for high-speed data links
  - Microwave radio links
  - …



Example:
IFX SiGe 3-Ch TX

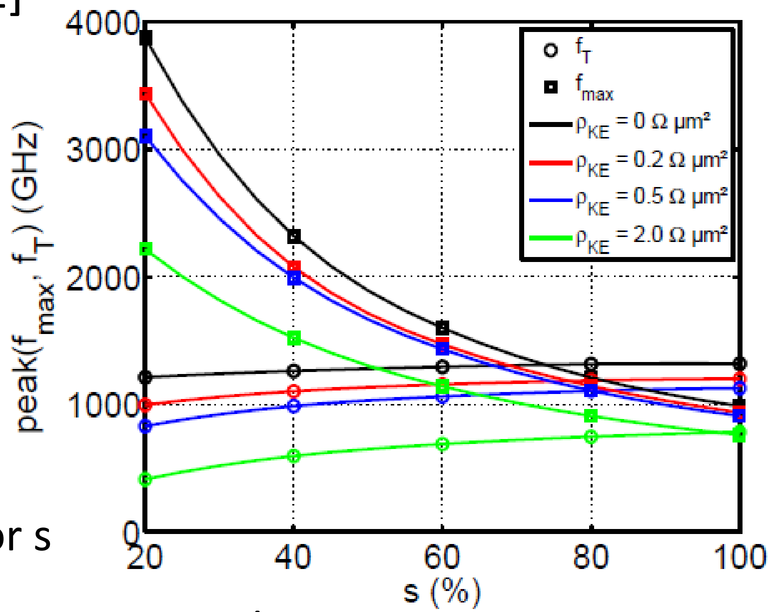
- Cut-off frequencies (f_T, f_{max}) of process should be 5-10 x larger than operating frequency
  - For radar: f_{op}~80 GHz ➔ f_{max} > 400 GHz (today: f_{max}/f_{op}~250/80~3)
- Improvement of today's applications
  - Larger design margins / lower noise / higher gain / better linearity
  - Lower power consumption / enables low cost packaging

Motivation – Technology Push

Results from Dotfive:

- Experimental proven HBT performance [Chevalier et al. 2011]
  - Evolution of industrial transistor concepts (DPSA): f_{max} ~ 400 GHz
  - New transistor concepts (“revolution”): f_{max} ~ 500 GHz and potential
- TCAD simulations [Schroeter et al. 2011]
  - Ultimate doping profile proposal for simulation of f_T and f_{max} roadmap

➔ No physical blocking point for THz SiGe HBT



Example of scaling analysis for f_T, f_{max} vs. a lateral scaling factor s

➔ Additionally new application fields, e.g. imaging/radar above 100 GHz, are enabled.

DOTSEVEN in a Nutshell

- Continuation of successful DOTFIVE
- Main objectives:
  - The realization of SiGeC Heterojunction Bipolar Transistors (HBTs) operating at a maximum oscillation frequency up to 0.7 THz at room temperature
  - The design and demonstration of integrated mm- and sub-mm-wave circuits using such HBTs for specific applications
  - The evaluation, understanding, and modeling of the relevant physical effects occurring in such high-speed devices and circuits
- Duration: 10/2012 – 3/2016
- 14 Partners from 6 EU countries: Infineon (IFX), IHP, Dice, Sivers IMA (SIMA), Trebax AB (TRE), XMOD, Alma, Universities: Aachen (RWTH), Bordeaux (UB1), Delft (TUDelft), Dresden (TUD), Linz (JKU), Napoli (UN), Wuppertal (BUW)
- Website: www.dotseven.eu

DOTSEVEN – Work Packages

- WP5 : Training & Dissemination
  (UB1, all partners)
  - Education of talented researchers and engineers
  - Website, publications
  - Workshops, tutorials,

- WP1 : SiGe HBT technology platform
  (IHP, IFX)
  - f_{max} / τ_D enhancement: 500GHz/2ps => 600GHz/1.7ps => 700GHz/1.4ps
  - Balanced f_t enhancement (350/350GHz…400/400GHz)
  - CMOS integratability, passives, interconnects

- WP2 : TCAD and physics-based modelling
  (UN, RWTH, TUD)
  - Advanced device simulation
  - Development of simulation tools (3D, nano-scale, thermal effects)
  - Reliability modelling (SOA, mixed-mode, high current degradation)

- WP3 : Device characterization & compact modelling
  (XMOD, TUD, UB1, UN, DICE, IFX)
  - Parameter extraction & methodology
  - Accurate compact models incl. electro-thermal & substrate effects
  - Predictive & statistical modelling

- WP4 : Applications & demonstrators
  (BUW, TUD, IFX, UB1, XMOD, JKU, SIMA, TRE, DICE, TUDelft)
  - Benchmark MMICs (PA, LNA, Mux, Demux, VCO, Mixer, Multiplier)
  - Demo: Radar @ 240GHz; 100Gb/s comm.; THz imaging > 300GHz

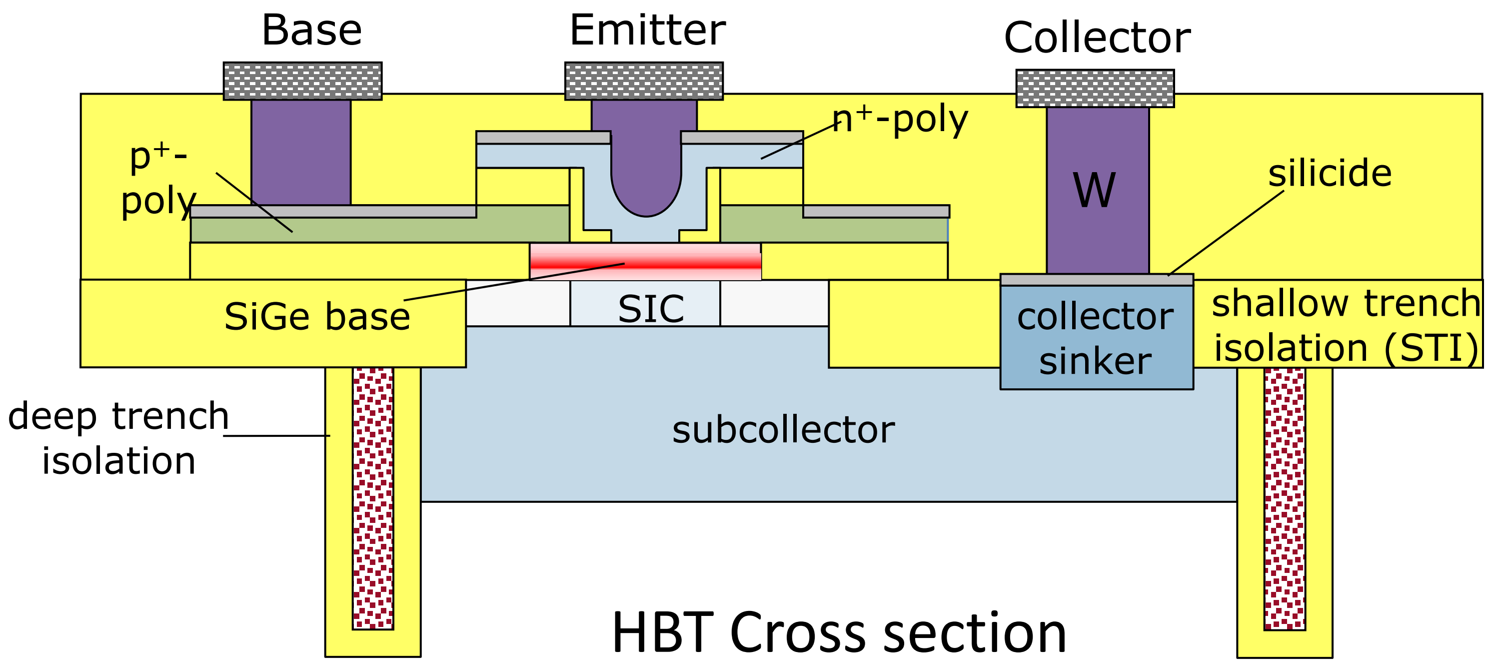
- WP6 : Project coordination & management
  (IFX, ALMA)
  - Overall control of deliverables, milestones, schedule
  - Organization of meetings, reporting
  - Financial distribution

WP1, SiGe Technology Platform Task Overview

- WP1: Two technology partners/providers:
  Innovations for High Performance Microelectronics (IHP) , Leibniz Institute
  Infineon
- WP1 - Task 1: Advanced Device Architectures (IHP, Infineon)
  - ➔Stage 1: f_{max} = 600GHz / τ_D = 1.7ps
  - ➔Stage 2: f_{max} = 700GHz / τ_D = 1.4ps
- WP1 - Task 2: f_T Enhancement (IHP)
- WP1 - Task 3: CMOS Compatibility (Infineon)
- WP1 - Task 4: Circuit Runs (IHP, Infineon)

In this talk focus on task 3 and task 1

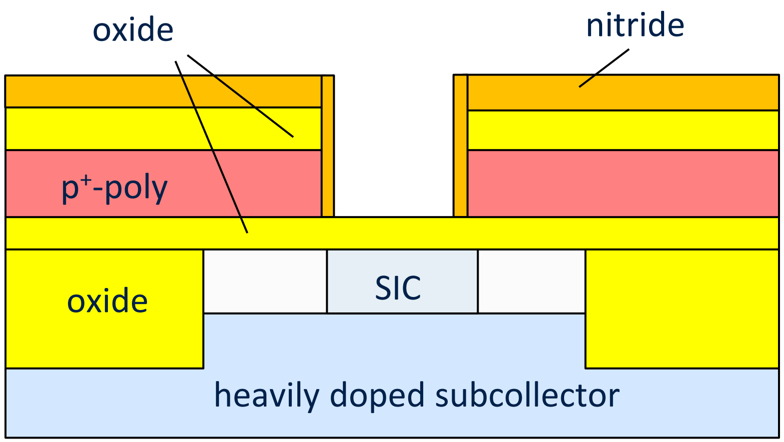
Standard DPSA-SEG Approach



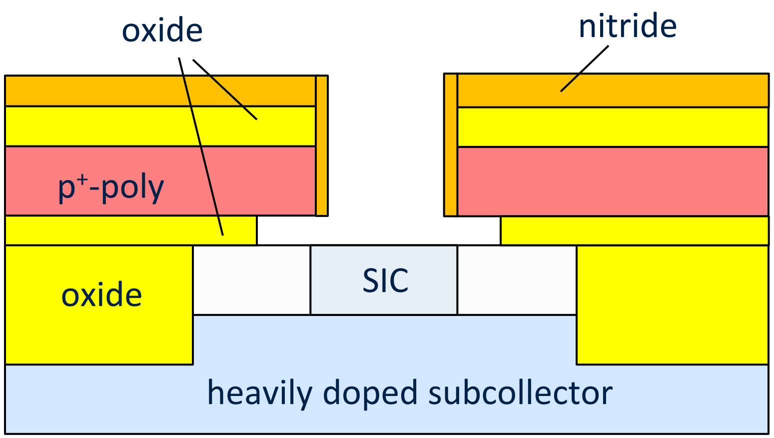
HBT Cross section

- E/B configuration: Double Polysilicon Self-Aligned with Selectively Epitaxially Grown base (DPSA-SEG)
- Transistor isolation: Deep trench (DT) and shallow trench isolation (STI)

Fabrication Process of DPSA-SEG HBT - I

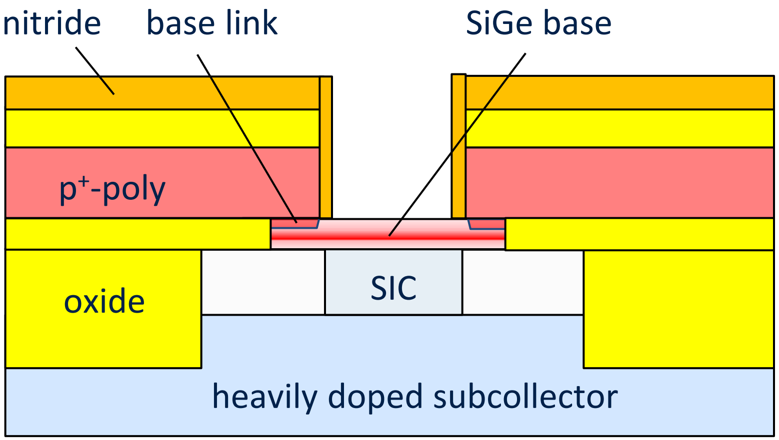


- Deposition of pedestal oxide/p⁺-poly/oxide/nitride stack on transistor isolation
- Patterning of emitter window
- Formation of nitride spacers
- Self-aligned collector implantation (SIC)

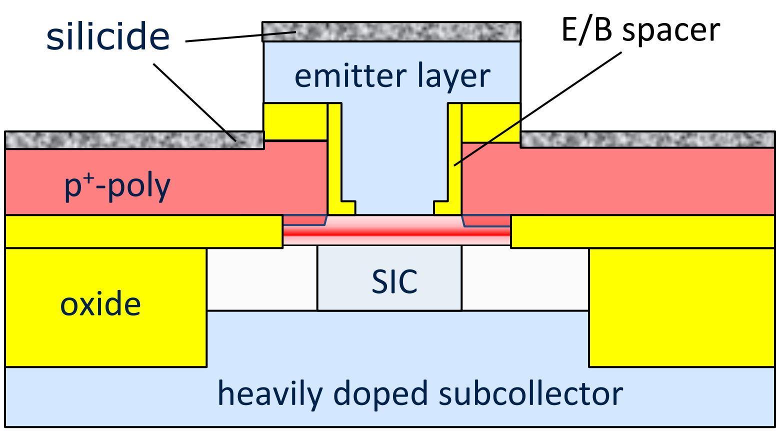


- Wet etch of pedestal oxide → creates self-aligned adjusted p⁺-poly overhangs

Fabrication Process of DPSA-SEG HBT - II



- Selective epitaxial growth of SiGe base
  - Growth only occurs on Si or poly-Si regions not covered by oxide or nitride
  - During SEG the base link is formed which connects the SiGe base with the p^+-poly base electrodes

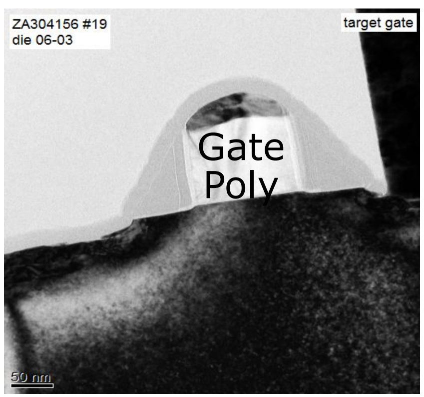


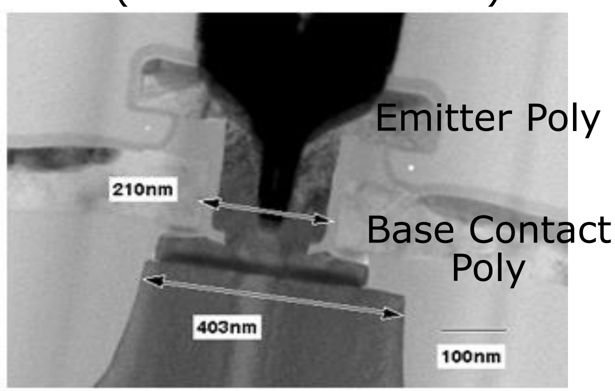
- Nitride layer removal
- Formation of emitter/base spacer
- Emitter deposition
- Emitter patterning
- Silicidation

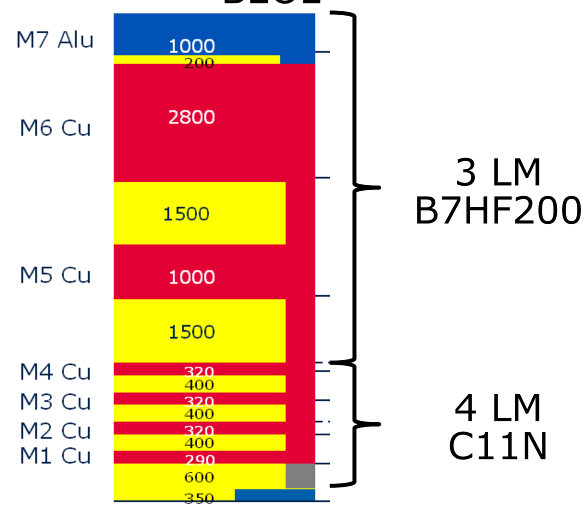
BiCMOS – B11HFC

- DOTFIVE: pure bipolar technology developed
- Future product generations require more digital functionality
- DOTSEVEN (one task):
  - Integration of the conventional (DPSA-) SiGe HBT developed in DOTFIVE into a 130nm CMOS platform at Infineon

130nm MOSFETs (C11) + Scaled SiGe HBTs (DOTFIVE SiGe HBT) + mmWave BEOL







BiCMOS Integration Topics

- HBT is integrated into an established CMOS technology
  ➔ CMOS devices should not be changed (reuse CMOS IP, ROM, SRAM, …)
- MOS thermal steps (LDD-& SD-anneals, poly oxidation) deteriorate HBT performance
- Specifically for integration of DOTFIVE HBT into Infineon's 130nm CMOS technology:
  - Substrate orient. for best HBT performance & yield different from standard CMOS
    - ➔ Adjust CMOS: Re-center MOS parameters by modification of implant and anneal steps
  - Different optimal thermal budgets for HBT and CMOS fabrication, find compromise:
    - ➔ Reduce S/D & LDD anneals so that MOS parameters can still be re-centered
    - ➔ Adjust base- and emitter-modules of the HBT to the reduced S/D anneal (which is still higher than in the DOTFIVE HBT process), e.g. reduce emitter doping
  - Structural problems during process integration

    E. g. removal of layers of bipolar fabrication from MOS gates ➔ introduction of a nitride protection layer that acts as etch-stop-layer during layer removal
  - …

Simplified Process Flow and Device List

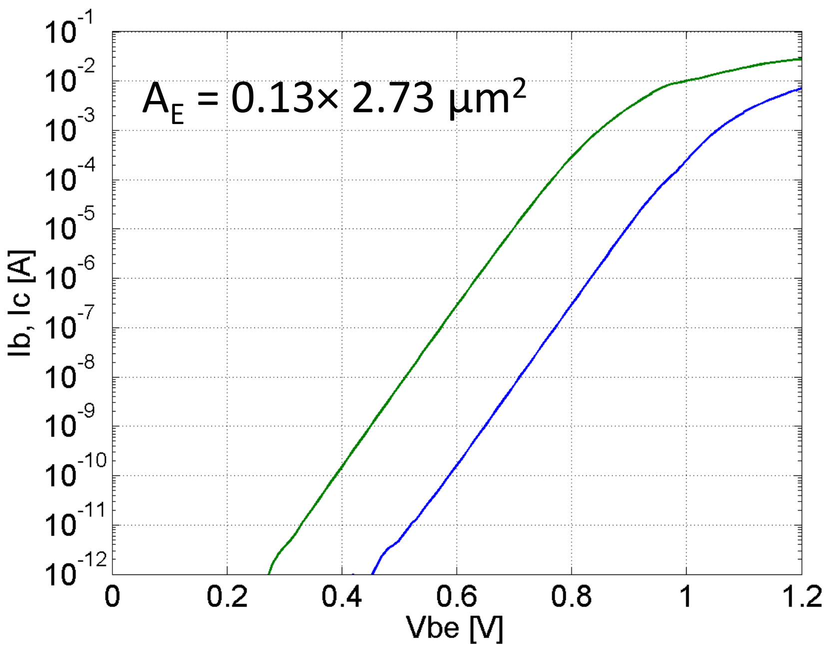
1. Substrate
2. Buried Layers Collector Epitaxy
3. Deep Trench Isolation
4. Shallow Trench Isolation
5. Collector Sinker
6. MOS Wells
7. Gate and Sidewall oxidation
8. CMOS Protection
9. SiGe HBT Module
10. Protection Removal
11. MOS Implants
12. S/D/E Anneal
13. Spacer Removal
14. Salicide
15. Metal 1-4
16. mmW Metal 5-6 MIM-Capacitor TaN resistor
17. Al Pad

Main devices:

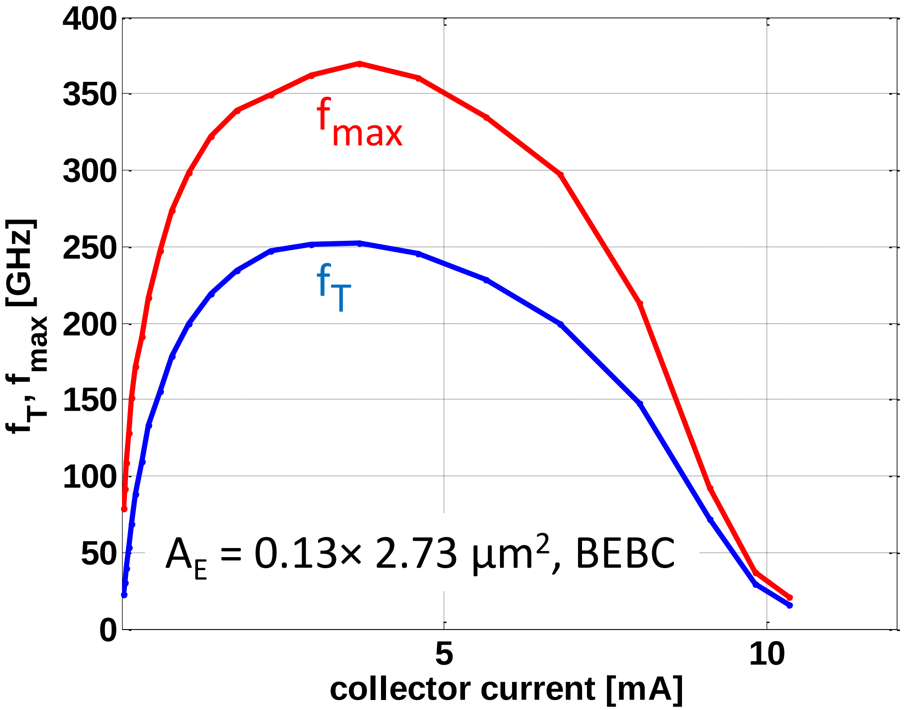
- High speed NPN
- Medium speed NPN
- High voltage NPN
- 2.2nm NMOS & PMOS
- 5.2nm NMOS & PMOS
- Bipolar varactor
- TaN resistor
- ppoly resistor
- MIM capacitor
- 2 thick upper metal layers

BiCMOS integration – Electrical Results

Gummel characteristics



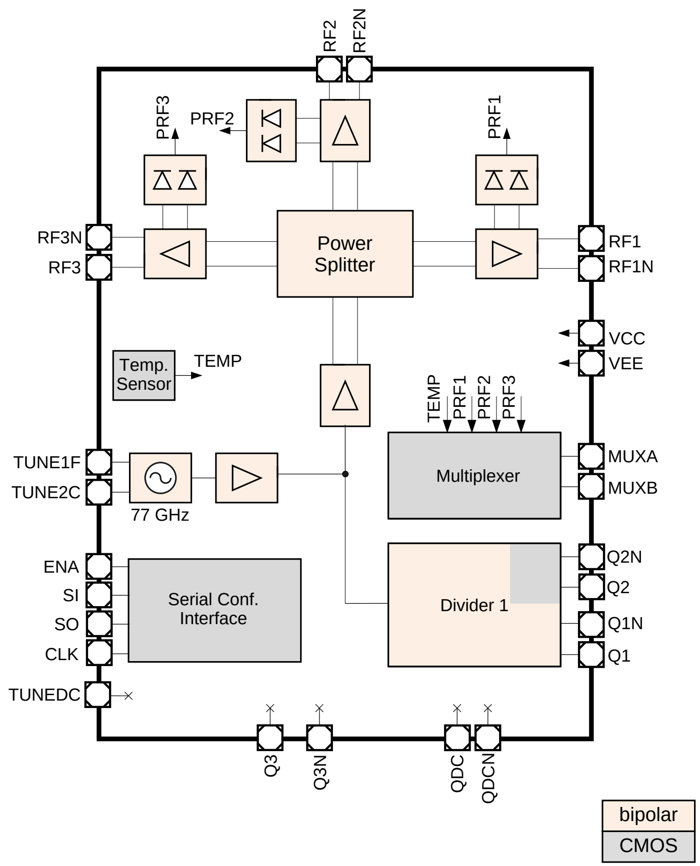
f_T, f_{max} vs. collector current characteristics



- 250 GHz f_T, 370 GHz f_{max}, CML gate delay: 2.5 ps
- Similar performance in BiCMOS flow as in pure bipolar (DOTFIVE)

Circuit Example - B11HFC vs. B7HF200

Block Diagram of 3 Channel 77 GHz Transmitter



Comparsion new process with current production process

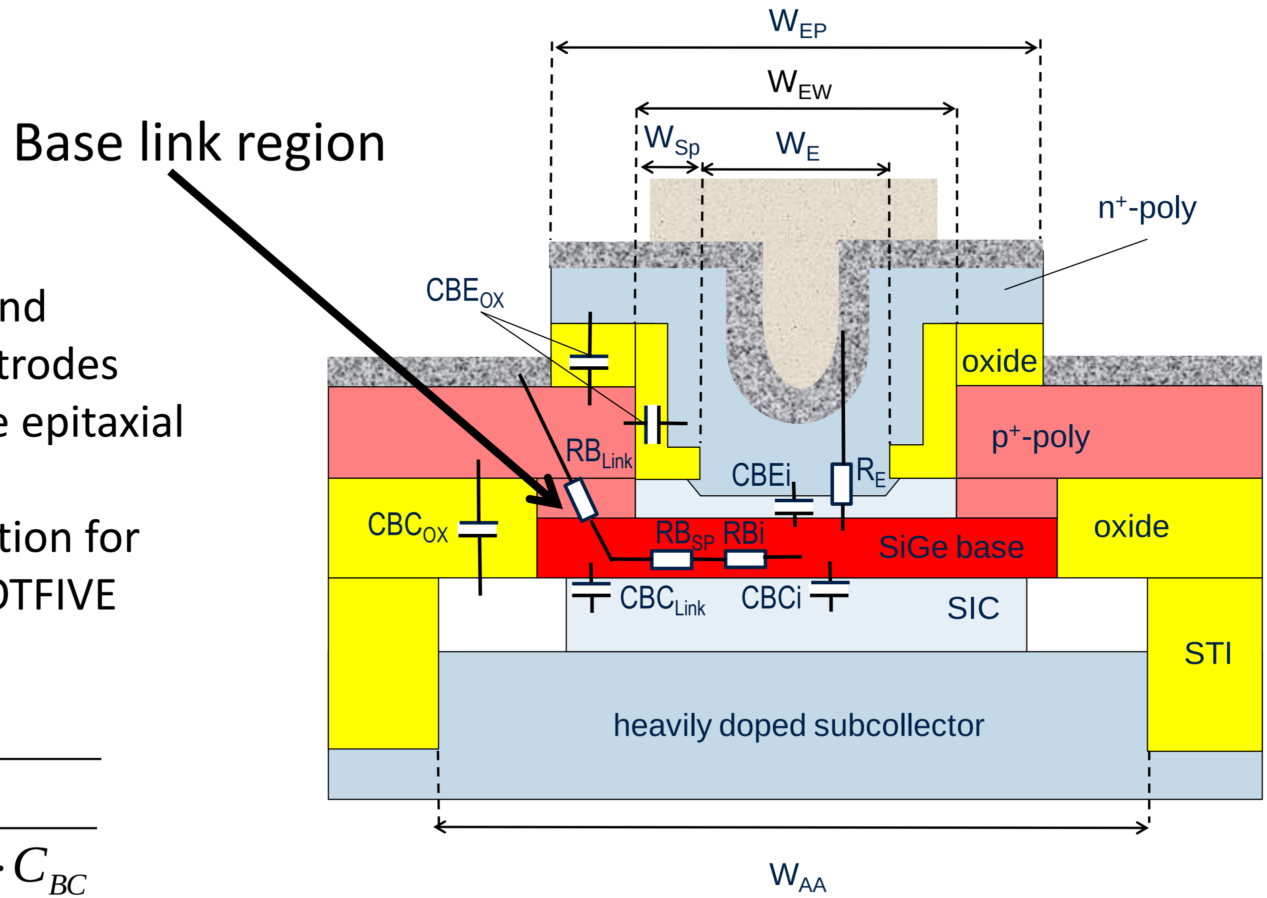
	B7HF200	B11HFC
Output power @ 25°C	12.5 dBm	14.9 dBm
Output power @ 125°C	10.5 dBm	14.3 dBm
Phase noise @ 1 MHz offset	-96.5 dBc/Hz	-99 dBc/Hz
Power consumption	1.82 W	0.94 W

- Higher output power
- Lower temperature dependence
- Better phase noise
- Half of the power consumption

Base Link Region

- Links active NPN base and p⁺-polysilicon base electrodes
- Formed during selective epitaxial growth
- Found as a major limitation for NPN performance in DOTFIVE (high R_B)

$$f_{\max} \approx \sqrt{\frac{f_T}{8\pi \cdot R_B \cdot C_{BC}}}$$

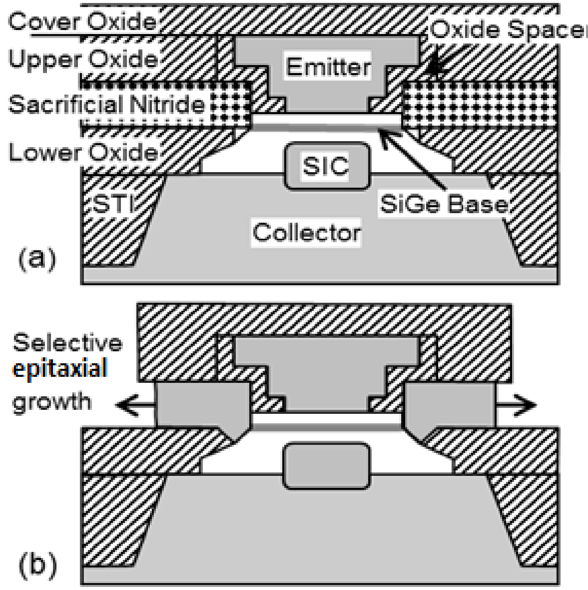


Schematic cross section of EB region and electrical parasitic elements

DPSA-SEG HBT with Epitaxial Base Link (EBL)

Main performance limitation of standard DPSA-SEG: Base link region and related parameter trade-offs

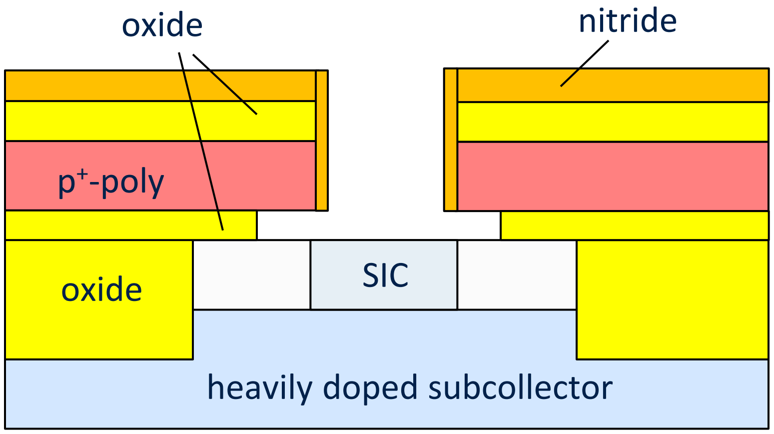
➔ Adapt IHP's HBT with epitaxially grown base link [Fox et al. 2011] to Infineon's 130nm BiCMOS platform: Joint Infineon/IHP mask set and process flow with EBL module established [Fox et al. 2015]



- Sacrificial nitride as a placeholder for external base during SiGe HBT fabrication
- SEG growth of base link after SiGe base and after emitter formation

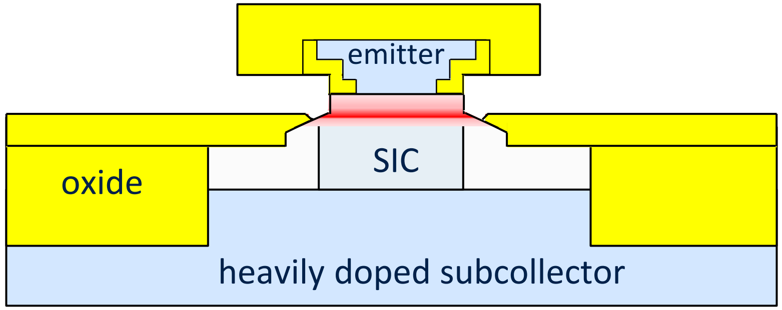
Comparison DPSA-SEG with and without EBL

Standard DPSA-SEG HBT



DPSA-SEG HBT with epitaxial base link (EBL)

[Fox et al. 2011]



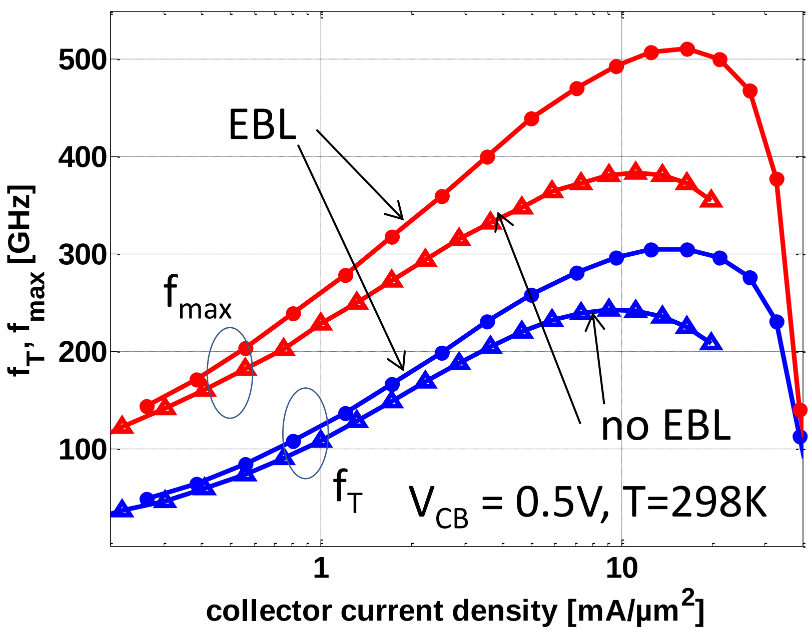
- Base link is formed during SEG simultaneously with active base
- Low doping in link region
- Link anneal needed (broadens base profile, f_T ↓)

- In-situ doped lateral base link growth after SiGe Epi & emitter formation
- SiGe base & base link formation decoupled
- No separate link anneal

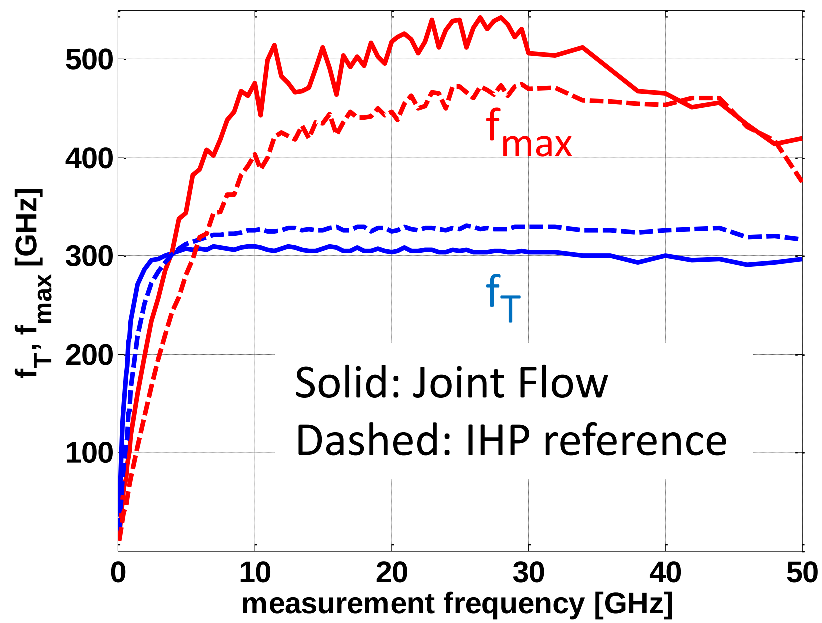
DPSA-SEG with EBL – Experimental Results for Joint EBL Flow

[Fox et al. 2015]

Comparison of RF characteristics with and without EBL



f_T, f_{max} vs. measurement frequency and comparison with IHP reference

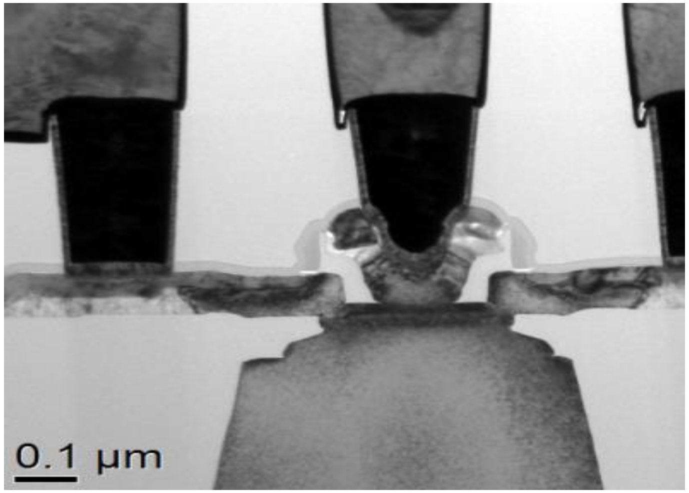


- f_{max} = 500 GHz, f_T = 300 GHz
- RF performance of original IHP process [Fox et al. 2011] reproduced

DPSA-SEG with EBL – Experimental Results for Joint EBL Flow

Parameter	Unit	Infineon/IHP joint flow		IHP ref.*)	Infineon ref. **)
Process		DPSA-SEG with EBL			DPSA-SEG without EBL
Layout		BEBC	BEC	BEC	BEC
$W_E \times L_E$	µm²	0.13×2.7		0.155×1.0	0.13×2.69
f_T	GHz	300	305	320	240
f_{max}	GHz	**500**	**465**	**445**	**380**
j_C (peak f_T)	mA/µm²	17		16	10
BV_{CE0}	V	1.5		1.75	1.5
BV_{CB0}	V	4.8		4.1	5.5
BV_{EB0}	V	1.5		1.35	2.3
$(R_B + R_E) \times L_E$	Ω ×µm	**46**	**51**	**52**	**86**
C_{CB}/L_E	fF/µm	**1.45**	**1.4**	**2.2**	**1.3**
C_{BE}/L_E	fF/µm	2.1	1.9	2.4	2.1
R_{SBi}	KΩ	3.0		2.6	2.6

Measured transistor parameters with and without EBL [Fox et al. 2015] (*) [Fox et al. 2011] , **) [Chevalier et al. 2011]).

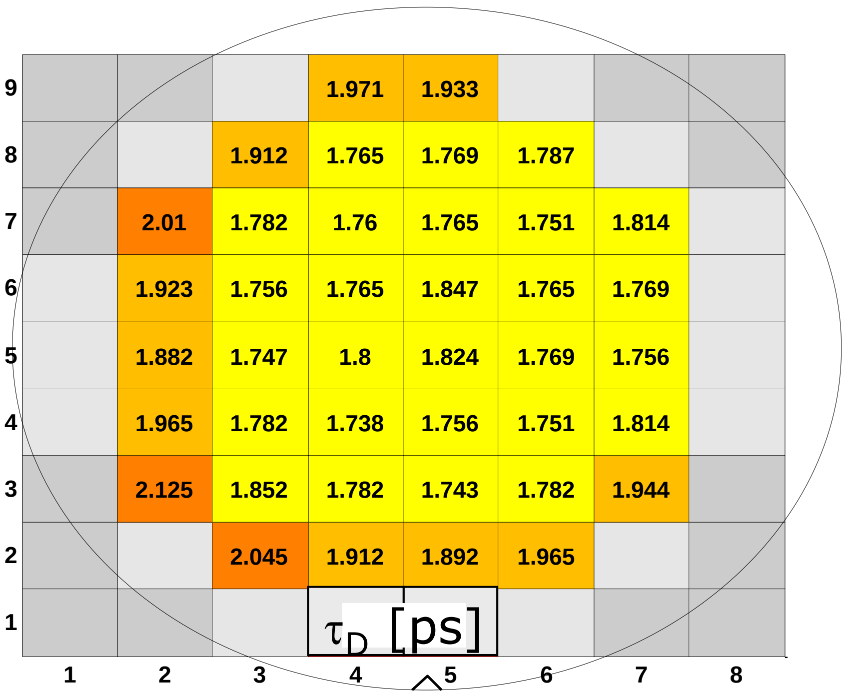


TEM image of the HBT [Fox et al. 2015]

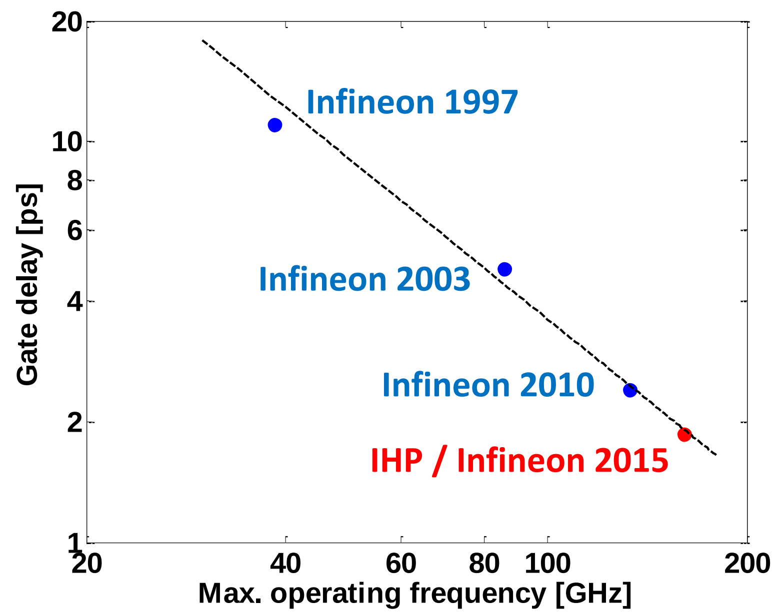
- R_B reduced by 40 % for EBL module
- f_{max} improvement vs. IHP reference due to reduced C_{CB}

Benchmark Circuit Results

- Record gate delay performance (without inductive peaking)
- Record static frequency divider operation: 161 GHz



Wafer map of CML gate delay [Lachner 2014]



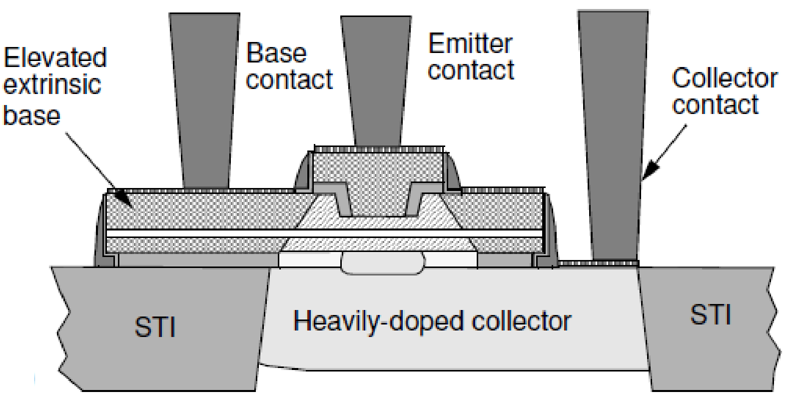
Evolution of maximum static divider operating frequency with decreasing gate delay τ_D

SiGe HBT performance improvements

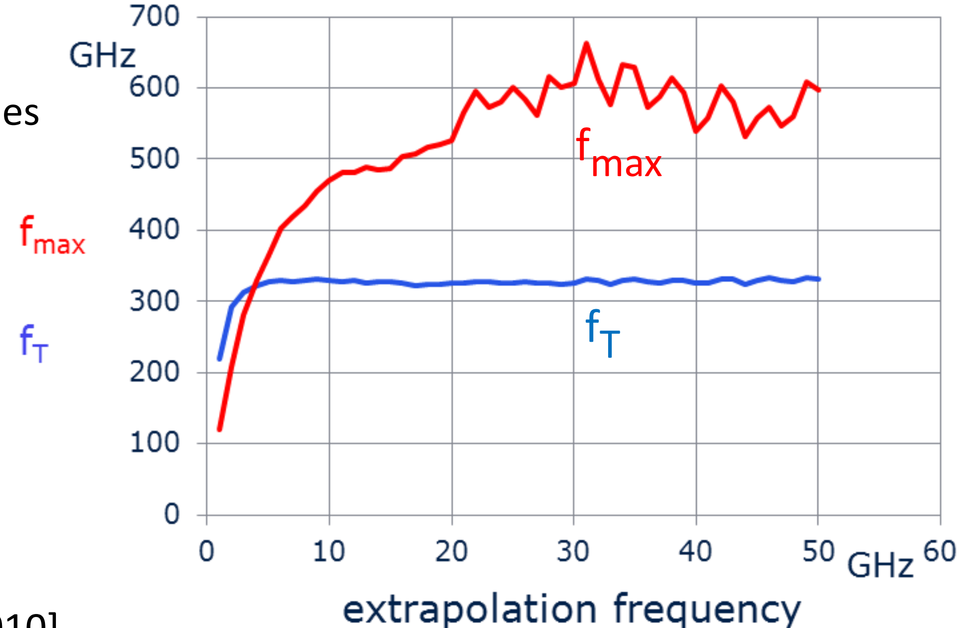
For further optimization IHP also uses their HBT with **N**on-**S**elective **E**pitaxial **G**rowth (N-SEG) of the base and **E**levated **E**xtrinsic **B**ase (EEB) [Heinemann et al. 2010]

- Other method to achieve low base link resistance
- Similar RF performance as EBL
- N-SEG control is simpler than SEG

➔ easier realization of aggressively scaled profiles



Schematic cross section [Heinemann et al. 2010]



f_T, f_{max} vs. extrapolation frequency for an N-SEG EEB example

- Lateral scaling & further optimized base profile

➔ f_{max} close to 600 GHz demonstrated

Summary

- Laterally and vertically scaled conventional DPSA-SEG HBT from DOTFIVE has been integrated into 130nm BiCMOS with only marginal influence on high speed performance
  τ_D: 2.5ps, f_{max}: 370GHz

  ➔ Design platform for next generation SiGe MMICs, e.g. for automotive radar
- This conventional architecture is limited by the base link region (base resistance)
- Novel device architectures overcome this limitation, offer low base link resistance and provide key performance metrics like $\tau_D \sim 1.7$ps or $f_{max} \sim 600$ GHz
- The achieved results are a base for further lateral and vertical scaling

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- Many thanks to our DOTSEVEN partners for the extremely fruitful cooperations, and to the numerous colleagues at Infineon and IHP who have achieved these technology results.

References

[Chevalier et al. 2011] P. Chevalier, T. F. Meister, B. Heinemann, S. Van Huylenbroeck, W. Liebl, A. Fox, A. Sibaja-Hernandez, A. Chantre, "Towards THz SiGe HBTs," Proc. of the IEEE *BCTM*, 2011, pp. 57-65, DOI: 10.1109/BCTM.2011.6082749.

[Fox et al. 2011] A. Fox, B. Heinemann, R. Barth, S. Marschmeyer, C. Wipf, Y. Yamamoto, "SiGe:C HBT architecture with epitaxial external base", Proc. of the IEEE *BCTM*, 2011, pp. 70-73, DOI: 10.1109/BCTM.2011.6082751

[Fox et al. 2015] A. Fox, B. Heinemann, H. Ruecker, R. Barth, G. Fischer, S. Marschmeyer, C. Wipf, K. Aufinger, J. Boeck, S. Boguth, H. Knapp, R. Lachner, W. Liebl, D. Manger, T. F. Meister, A. Pribil, J. Wursthorn, "Advanced Heterojunction Bipolar Transistor for Half-THz SiGe BiCMOS Technology", IEEE Electron Device Letters, 2015, DOI: 10.1109/LED.2015.2432130

[Heinemann et al. 2010] B. Heinemann, R. Barth, D. Bolze, J. Drews, G. G. Fischer, A. Fox, O. Fursenko, T. Grabolla, U. Haak, D. Knoll, R. Kurps, M. Lisker, S. Marschmeyer, H. Rücker, D. Schmidt, J. Schmidt, M. A. Schubert, B. Tillack, C. Wipf, D. Wolansky, Y. Yamamoto, "SiGe HBT technology with f_T/f_{max} of 300GHz/500GHz and 2.0 ps CML gate delay," IEEE IEDM Tech. Dig., 2010, pp. 688-691, DOI: 10.1109/IEDM.2010.5703452.

[Lachner 2014] R. Lachner, "Towards 0.7 terahertz Silicon Germanium heterojunction bipolar technology – The DOTSEVEN project," *ECS Trans*., vol. 64, issue 6, pp. 21-37, Oct. 2014, DOI: 10.1149/06406.0021ecst

[Schroeter et al. 2011] M. Schroeter, G. Wedel, B. Heinemann, C. Jungemann, J. Krause, P. Chevalier, and A. Chantre, "Physical and Electrical Performance Limits of High-Speed SiGeC HBTs—Part I: Vertical Scaling", IEEE TED, 2011, pp. 3687-3696

M. Schroeter, J. Krause, N. Rinaldi, G. Wedel, B. Heinemann, P. Chevalier, and A. Chantre, "Physical and Electrical Performance Limits of High-Speed SiGeC HBTs—Part II: Lateral Scaling", IEEE TED, 2011, pp. 3697-3706