Advances in SiGe BiCMOS Technology for mm-Wave Applications in the DOTSEVEN Project

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WS12: EuMIC - SiGe for mm-Wave and THz
Outline

• Introduction
  – Motivation – market pull and technology push
• DOTSEVEN results:
  – Exploitation of „evolutionary“ DOTFIVE results: Scaled conventional Double-Polysilicon Self-Aligned (DPSA) HBT with Selectively Epitaxially Grown (SEG) base to BiCMOS – B11HFC
  – SiGe HBT Performance Status
• Summary
• Acknowledgement
• References
Motivation – Market Pull

• High-speed SiGe HBT bipolar processes are used today for leading edge RF applications like
  – Automotive radar @ 77 GHz
  – Front-ends for high-speed data links
  – Microwave radio links
  – ...

• Cut-off frequencies ($f_T$, $f_{\text{max}}$) of process should be 5-10 x larger than operating frequency
  – For radar: $f_{\text{op}} \sim 80$ GHz $\Rightarrow f_{\text{max}} > 400$ GHz (today: $f_{\text{max}}/f_{\text{op}} \sim 250/80\sim 3$)

• Improvement of today’s applications
  – Larger design margins / lower noise / higher gain / better linearity
  – Lower power consumption / enables low cost packaging

Example:
IFX SiGe 3-Ch TX

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Motivation – Technology Push

Results from Dotfive:

- Experimental proven HBT performance [Chevalier et al. 2011]
  - Evolution of industrial transistor concepts (DPSA): $f_{\text{max}} \sim 400$ GHz
  - New transistor concepts (“revolution”): $f_{\text{max}} \sim 500$ GHz and potential

- TCAD simulations [Schroeter et al. 2011]
  - Ultimate doping profile proposal for simulation of $f_T$ and $f_{\text{max}}$ roadmap

$\Rightarrow$ No physical blocking point for THz SiGe HBT

Example of scaling analysis for $f_T$, $f_{\text{max}}$ vs. a lateral scaling factor $s$

$\Rightarrow$ Additionally new application fields, e.g. imaging/radar above 100 GHz, are enabled.

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DOTSEVEN in a Nutshell

- Continuation of successful DOTFIVE

- Main objectives:
  - The realization of SiGeC Heterojunction Bipolar Transistors (HBTs) operating at a maximum oscillation frequency up to 0.7 THz at room temperature
  - The design and demonstration of integrated mm- and sub-mm-wave circuits using such HBTs for specific applications
  - The evaluation, understanding, and modeling of the relevant physical effects occurring in such high-speed devices and circuits

- Duration: 10/2012 – 3/2016

- 14 Partners from 6 EU countries: Infineon (IFX), IHP, Dice, Sivers IMA (SIMA), Trebax AB (TRE), XMOD, Alma, Universities: Aachen (RWTH), Bordeaux (UB1), Delft (TUDelft), Dresden (TUD), Linz (JKU), Napoli (UN), Wuppertal (BUW)

- Website: www.dotseven.eu
DOTSEVEN – Work Packages

WP1: SiGe HBT technology platform (IHP, IFX)
- $f_{\text{max}}/\tau_D$ enhancement: $500\text{GHz}/2\text{ps} \Rightarrow 600\text{GHz}/1.7\text{ps} \Rightarrow 700\text{GHz}/1.4\text{ps}$
- Balanced $f_t$ enhancement ($350/350\text{GHz} \ldots 400/400\text{GHz}$)
- CMOS integratability, passives, interconnects

WP2: TCAD and physics-based modelling (UN, RWTH, TUD)
- Advanced device simulation
- Development of simulation tools (3D, nano-scale, thermal effects)
- Reliability modelling (SOA, mixed-mode, high current degradation)

WP3: Device characterization & compact modelling (XMOD, TUD, UB1, UN, DICE, IFX)
- Parameter extraction & methodology
- Accurate compact models incl. electro-thermal & substrate effects
- Predictive & statistical modelling

WP4: Applications & demonstrators (BUW, TUD, IFX, UB1, XMOD, JKU, SIMA, TRE, DICE, TUDelft)
- Benchmark MMICs (PA, LNA, Mux, Demux, VCO, Mixer, Multiplier)
- Demo: Radar @ 240GHz; 100Gb/s comm.; THz imaging > 300GHz

WP5: Training & Dissemination (UB1, all partners)
- Education of talented researchers and engineers
- Website, publications, workshops, tutorials

WP6: Project coordination & management (IFX, ALMA)
- Overall control of deliverables, milestones, schedule
- Organization of meetings, reporting
- Financial distribution
WP1, SiGe Technology Platform
Task Overview

• WP1: Two technology partners/providers: Innovations for High Performance Microelectronics (IHP), Leibniz Institute Infineon

• WP1 - Task 1: Advanced Device Architectures (IHP, Infineon)
  ➔ Stage 1: $f_{\text{max}} = 600\text{GHz} / \tau_D = 1.7\text{ps}$
  ➔ Stage 2: $f_{\text{max}} = 700\text{GHz} / \tau_D = 1.4\text{ps}$

• WP1 - Task 2: $f_T$ Enhancement (IHP)

• WP1 - Task 3: CMOS Compatibility (Infineon)

• WP1 - Task 4: Circuit Runs (IHP, Infineon)

In this talk focus on task 3 and task 1
Standard DPSA-SEG Approach

- E/B configuration: Double Polysilicon Self-Aligned with Selectively Epitaxially Grown base (DPSA-SEG)
- Transistor isolation: Deep trench (DT) and shallow trench isolation (STI)

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Fabrication Process of DPSA-SEG HBT - I

- Deposition of pedestal oxide/p⁺-poly/oxide/nitride stack on transistor isolation
- Patterning of emitter window
- Formation of nitride spacers
- Self-aligned collector implantation (SIC)

- Wet etch of pedestal oxide \(\Rightarrow\) creates self-aligned adjusted p⁺-poly overhangs
Selective epitaxial growth of SiGe base
- Growth only occurs on Si or poly-Si regions not covered by oxide or nitride
- During SEG the base link is formed which connects the SiGe base with the p⁺-poly base electrodes

Nitride layer removal
- Formation of emitter/base spacer
- Emitter deposition
- Emitter patterning
- Silicidation
• DOTFIVE: pure bipolar technology developed
• Future product generations require more digital functionality
• DOTSEVEN (one task):
  • Integration of the conventional (DPSA-) SiGe HBT developed in DOTFIVE into a 130nm CMOS platform at Infineon

130nm MOSFETs (C11) + Scaled SiGe HBTs (DOTFIVE SiGe HBT) + mmWave BEOL

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BiCMOS Integration Topics

• HBT is integrated into an established CMOS technology
  ➔ CMOS devices should not be changed (reuse CMOS IP, ROM, SRAM, ...)
• MOS thermal steps (LDD- & SD-anneals, poly oxidation) deteriorate HBT performance
• Specifically for integration of DOTFIVE HBT into Infineon’s 130nm CMOS technology:
  – Substrate orient. for best HBT performance & yield different from standard CMOS
    ➔ Adjust CMOS: Re-center MOS parameters by modification of implant and anneal steps
  – Different optimal thermal budgets for HBT and CMOS fabrication, find compromise:
    ➔ Reduce S/D & LDD anneals so that MOS parameters can still be re-centered
    ➔ Adjust base- and emitter-modules of the HBT to the reduced S/D anneal (which is still higher than in the DOTFIVE HBT process), e.g. reduce emitter doping
  – Structural problems during process integration
    E. g. removal of layers of bipolar fabrication from MOS gates ➔ introduction of a nitride protection layer that acts as etch-stop-layer during layer removal
  – ...

SiGe for mm-Wave and THz
### SiGe for mm-Wave and THz

#### Simplified Process Flow and Device List

<table>
<thead>
<tr>
<th>Substrate</th>
<th>Buried Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>Collector Epitaxy</td>
<td>Deep Trench Isolation</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Shallow Trench Isolation</th>
<th>Collector Sinker</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS Wells</td>
<td>Gate and Sidewall oxidation</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CMOS Protection</th>
<th>SiGe HBT Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Protection Removal</td>
<td></td>
</tr>
</tbody>
</table>

| MOS Implants | S/D/E Anneal | Spacer Removal | Salicide |

<table>
<thead>
<tr>
<th>Metal 1-4</th>
<th>mmW Metal 5-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIM-Capacitor</td>
<td>TaN resistor</td>
</tr>
</tbody>
</table>

**Al Pad**

- Main devices:
  - High speed NPN
  - Medium speed NPN
  - High voltage NPN
  - 2.2nm NMOS & PMOS
  - 5.2nm NMOS & PMOS
  - Bipolar varactor
  - TaN resistor
  - ppoly resistor
  - MIM capacitor
  - 2 thick upper metal layers
**BiCMOS integration – Electrical Results**

- 250 GHz $f_T$, 370 GHz $f_{\text{max}}$, CML gate delay: 2.5 ps
- Similar performance in BiCMOS flow as in pure bipolar (DOTFIVE)

**Gummel characteristics**

\[ A_E = 0.13 \times 2.73 \text{ } \mu \text{m}^2 \]

**$f_T$, $f_{\text{max}}$ vs. collector current characteristics**

\[ A_E = 0.13 \times 2.73 \text{ } \mu \text{m}^2, \text{ BEBC} \]
Block Diagram of 3 Channel 77 GHz Transmitter

Comparsion new process with current production process

<table>
<thead>
<tr>
<th></th>
<th>B7HF200</th>
<th>B11HFC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output power @ 25°C</td>
<td>12.5 dBm</td>
<td>14.9 dBm</td>
</tr>
<tr>
<td>Output power @ 125°C</td>
<td>10.5 dBm</td>
<td>14.3 dBm</td>
</tr>
<tr>
<td>Phase noise @ 1 MHz offset</td>
<td>-96.5 dBC/Hz</td>
<td>-99 dBC/Hz</td>
</tr>
<tr>
<td>Power consumption</td>
<td>1.82 W</td>
<td>0.94 W</td>
</tr>
</tbody>
</table>

- Higher output power
- Lower temperature dependence
- Better phase noise
- Half of the power consumption
- Links active NPN base and p⁺-polysilicon base electrodes
- Formed during selective epitaxial growth
- Found as a major limitation for NPN performance in DOTFIVE (high $R_B$)

$$f_{\text{max}} \approx \sqrt{\frac{f_T}{8\pi \cdot R_B \cdot C_{BC}}}$$

Schematic cross section of EB region and electrical parasitic elements

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Main performance limitation of standard DPSA-SEG: Base link region and related parameter trade-offs

→ Adapt IHP’s HBT with epitaxially grown base link [Fox et al. 2011] to Infineon’s 130nm BiCMOS platform: Joint Infineon/IHP mask set and process flow with EBL module established [Fox et al. 2015]

- Sacrificial nitride as a placeholder for external base during SiGe HBT fabrication
- SEG growth of base link after SiGe base and after emitter formation
Comparison DPSA-SEG with and without EBL

Standard DPSA-SEG HBT

- Base link is formed during SEG simultaneously with active base
- Low doping in link region
- Link anneal needed (broadens base profile, $f_T \downarrow$)

DPSA-SEG HBT with epitaxial base link (EBL)

- In-situ doped lateral base link growth after SiGe Epi & emitter formation
- SiGe base & base link formation decoupled
- No separate link anneal

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[Fox et al. 2011]
DPSA-SEG with EBL – Experimental Results for Joint EBL Flow

Comparison of RF characteristics with and without EBL

- $f_{\text{max}} = 500$ GHz, $f_T = 300$ GHz
- RF performance of original IHP process [Fox et al. 2011] reproduced

[Graphs showing comparison of $f_T$, $f_{\text{max}}$ vs. measurement frequency and comparison with IHP reference]
DPSA-SEG with EBL – Experimental Results for Joint EBL Flow

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Infineon/IHP joint flow</th>
<th>IHP ref. (*)</th>
<th>Infineon ref. **)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td></td>
<td>DPSA-SEG with EBL</td>
<td></td>
<td>DPSA-SEG without EBL</td>
</tr>
<tr>
<td>Layout</td>
<td></td>
<td>BEBC BEC BEC BEC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( W_E \times L_E )</td>
<td>( \mu m^2 )</td>
<td>0.13 \times 2.7</td>
<td>0.155 \times 1.0</td>
<td>0.13 \times 2.69</td>
</tr>
<tr>
<td>( f_T )</td>
<td>GHz</td>
<td>300</td>
<td>305</td>
<td>320</td>
</tr>
<tr>
<td>( f_{\text{max}} )</td>
<td>GHz</td>
<td>500</td>
<td>465</td>
<td>445</td>
</tr>
<tr>
<td>( j_C ) (peak ( f_T ))</td>
<td>mA/( \mu m^2 )</td>
<td>17</td>
<td>16</td>
<td>10</td>
</tr>
<tr>
<td>( B V_{CE0} )</td>
<td>V</td>
<td>1.5</td>
<td>1.75</td>
<td>1.5</td>
</tr>
<tr>
<td>( B V_{CB0} )</td>
<td>V</td>
<td>4.8</td>
<td>4.1</td>
<td>5.5</td>
</tr>
<tr>
<td>( B V_{EB0} )</td>
<td>V</td>
<td>1.5</td>
<td>1.35</td>
<td>2.3</td>
</tr>
<tr>
<td>( R_B + R_E ) \times L_E</td>
<td>( \Omega \times \mu m )</td>
<td>46 51 52 86</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{CB} / L_E )</td>
<td>fF/( \mu m )</td>
<td>1.45 1.4 2.2 1.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{BE} / L_E )</td>
<td>fF/( \mu m )</td>
<td>2.1 1.9 2.4 2.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( R_{SBi} )</td>
<td>K( \Omega )</td>
<td>3.0 2.6 2.6</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TEM image of the HBT [Fox et al. 2015]

- \( R_B \) reduced by 40 % for EBL module
- \( f_{\text{max}} \) improvement vs. IHP reference due to reduced \( C_{CB} \)

Measured transistor parameters with and without EBL [Fox et al. 2015] (*) [Fox et al. 2011], **) [Chevalier et al. 2011].
Benchmark Circuit Results

- Record gate delay performance (without inductive peaking)
- Record static frequency divider operation: 161 GHz

Wafer map of CML gate delay [Lachner 2014]

Evolution of maximum static divider operating frequency with decreasing gate delay $\tau_D$

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SiGe HBT performance improvements

For further optimization IHP also uses their HBT with **Non-Selective Epitaxial Growth** (N-SEG) of the base and **Elevated Extrinsic Base** (EEB) [Heinemann et al. 2010]
- Other method to achieve low base link resistance
- Similar RF performance as EBL
- N-SEG control is simpler than SEG
  ➔ easier realization of aggressively scaled profiles

![Schematic cross section](image)

- Lateral scaling & further optimized base profile
  ➔ $f_{\text{max}}$ close to 600 GHz demonstrated
Summary

- Laterally and vertically scaled conventional DPSA-SEG HBT from DOTFIVE has been integrated into 130nm BiCMOS with only marginal influence on high speed performance
  - $\tau_D$: 2.5ps, $f_{\text{max}}$: 370GHz
  - Design platform for next generation SiGe MMICs, e.g. for automotive radar
- This conventional architecture is limited by the base link region (base resistance)
- Novel device architectures overcome this limitation, offer low base link resistance and provide key performance metrics like $\tau_D \sim 1.7$ps or $f_{\text{max}} \sim 600$ GHz
- The achieved results are a base for further lateral and vertical scaling
• Dotseven has received funding from the European Union’s Seventh Programme for research, technological development and demonstration under grant agreement N°316755, which is gratefully acknowledged.

• Many thanks to our DOTSEVEN partners for the extremely fruitful cooperations, and to the numerous colleagues at Infineon and IHP who have achieved these technology results.
References


