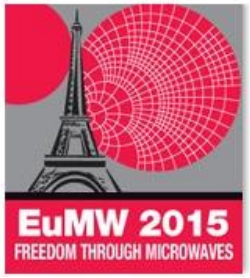

EUROPEAN MICROWAVE WEEK 2015
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PALAIS DES CONGRÈS, PARIS, FRANCE
SEPTEMBER 6 - 11, 2015

Exhibition Opening Hours:
- Tuesday 8th September: 9.30 – 18.00
- Wednesday 9th September: 9:30 – 17.30
- Thursday 10th September: 9:30 – 16.30

55nm SiGe BiCMOS for Optical, Wireless and High-Performance Analog Applications

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life.augmented

WS12: EuMIC - *SiGe for mm-Wave and THz*

Outline

- Introduction
- SiGe HBT scaling
- 55nm BiCMOS
- Summary & perspectives

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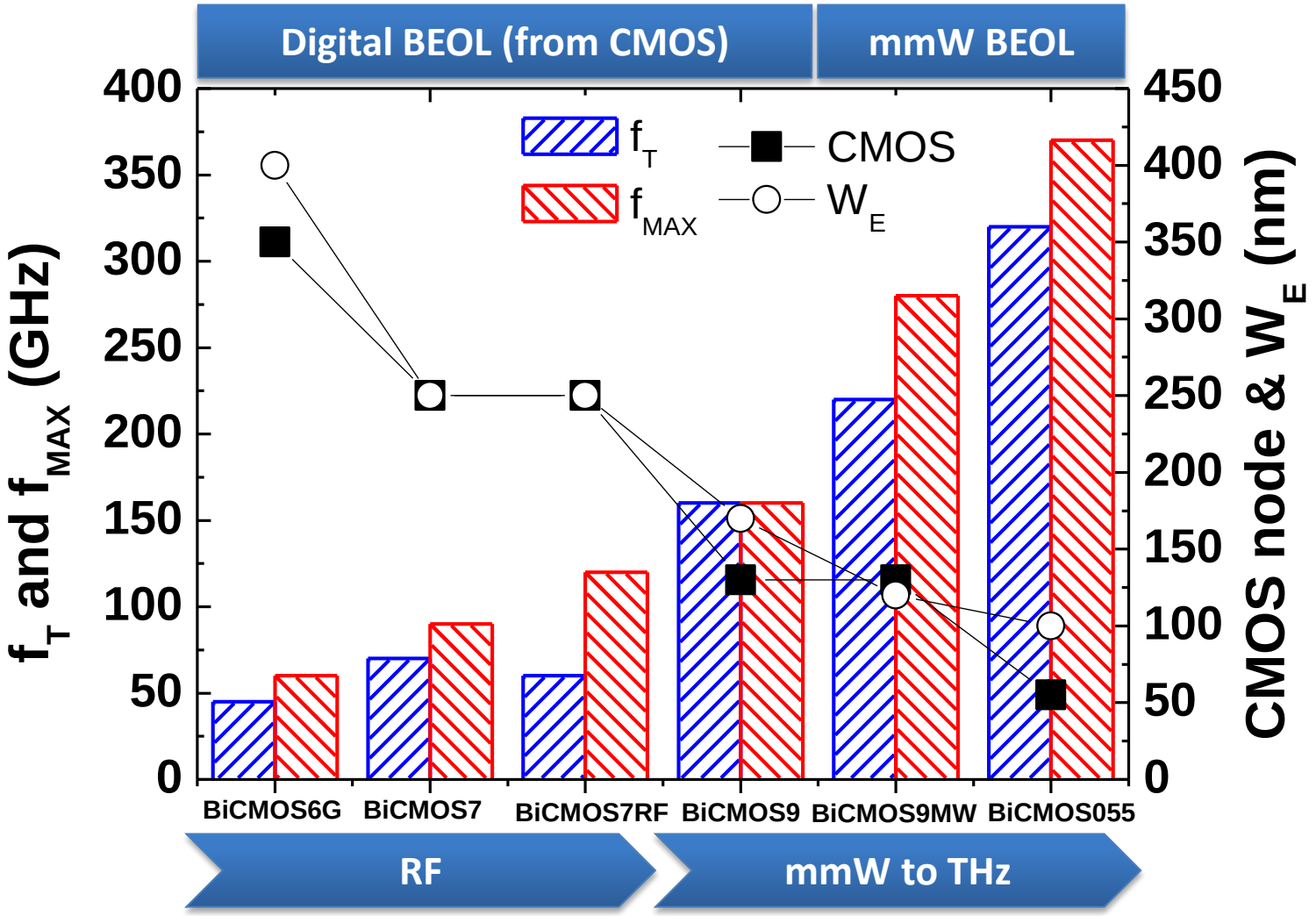
BiCMOS drivers

- Ethernet bandwidth explosion drives BiCMOS roadmap for:
  - Dense CMOS (skyrocket of digital need)
  - High-Q passives
  - High-speed SiGe HBT
- Other millimeter-wave applications benefit from this push:
  - Move up in frequency spectrum with highly integrated solutions becomes possible
  - Current applications can be improved (gain, noise, power consumption,…)

BiCMOS enablers

- CMOS node choice based on:
  - CMOS area (density × 5.5 from 120nm to 55nm)
  - CMOS speed (digital signal processing)
- High-Q passives impose:
  - Modifications to the native CMOS BEOL (thick Cu layers for T-lines, inductors,…)
- HBT architecture choice depends on:
  - Targeted performance (f_T, f_{MAX}, BV_{CEO},…), which drives the operation frequency
  - Integration constraints & manufacturability

15y BiCMOS scaling history at ST



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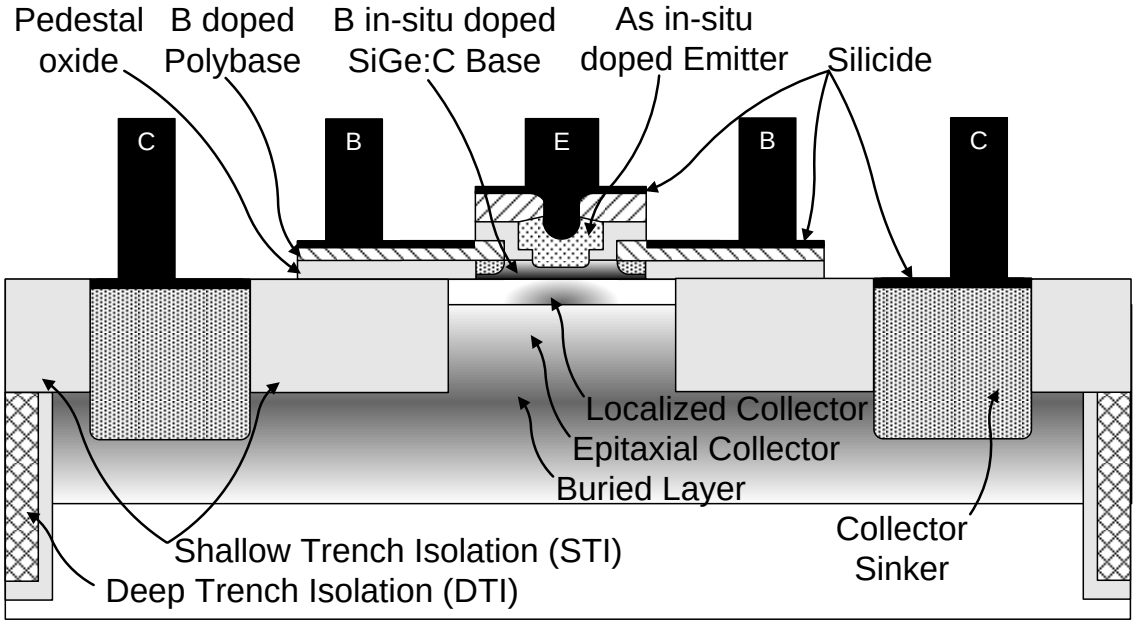
DPSA-SEG architecture

- Double Polysilicon Self-Aligned architecture with Selective Epitaxial Growth of the base

- Substrate
- …… N+ buried layer (M1)
- …… N epitaxy
- …… Deep trench isolation (M2)
- Shallow trench isolation
- …… N+ sinker (M3)
- Wells
- Gate oxides (GO1 & GO2)
- Gate polysilicon
- …… Bipolar opening (M4)
- …… SIC implant (M5)
- …… Polybase deposition
- …… Emitter window (M6)
- …… SiGe:C base epitaxy (SEG)
- …… Emitter deposition
- …… Polyemitter patterning (M7)
- …… Polybase patterning (M8)
- Gate patterning
- Extensions and source/drains
- Spike activation anneal
- Salicide
- Contacts
- Cu BEOL

- Emitter-base HBT module inserted between gate poly deposition and patterning, which minimizes impact of HBT thermal budget on CMOS devices



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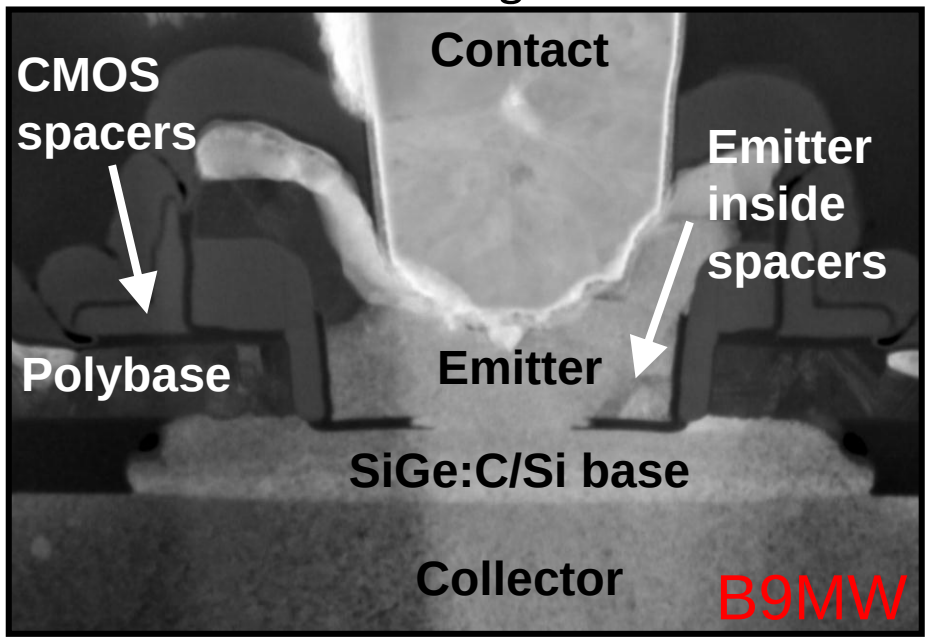
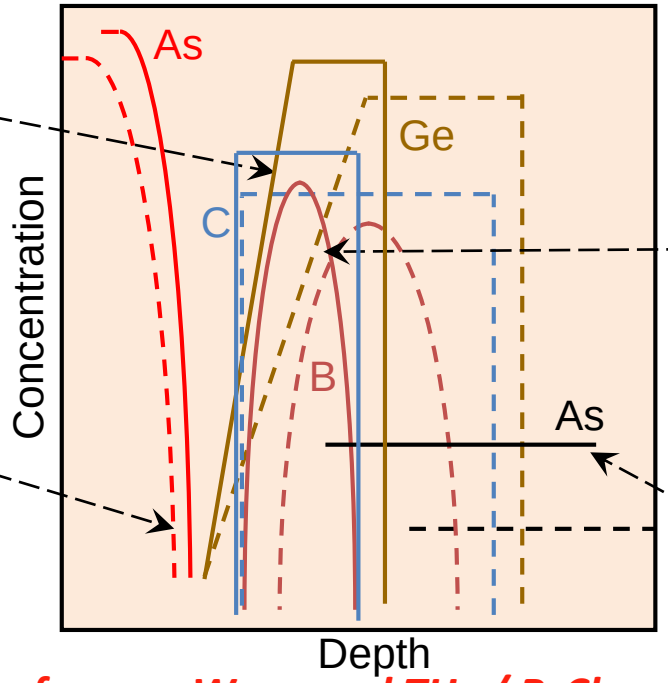


Vertical scaling principles

- Challenge of vertical scaling is to increase f_T ($\propto 1/\tau_{EC}$) without penalizing too much f_{MAX} ($\propto f_T/(R_B.C_{BC})$)
- Doping & thicknesses of the layers drive the R.C trade-offs
  ⇨ Process thermal budget is critical

Larger Ge slope to increase electric field and reduce base transit time (τ_B)

Reduced arsenic/boron spacing to reduce basewidth (W_B), emitter resistance (R_E) and transit time (τ_E)

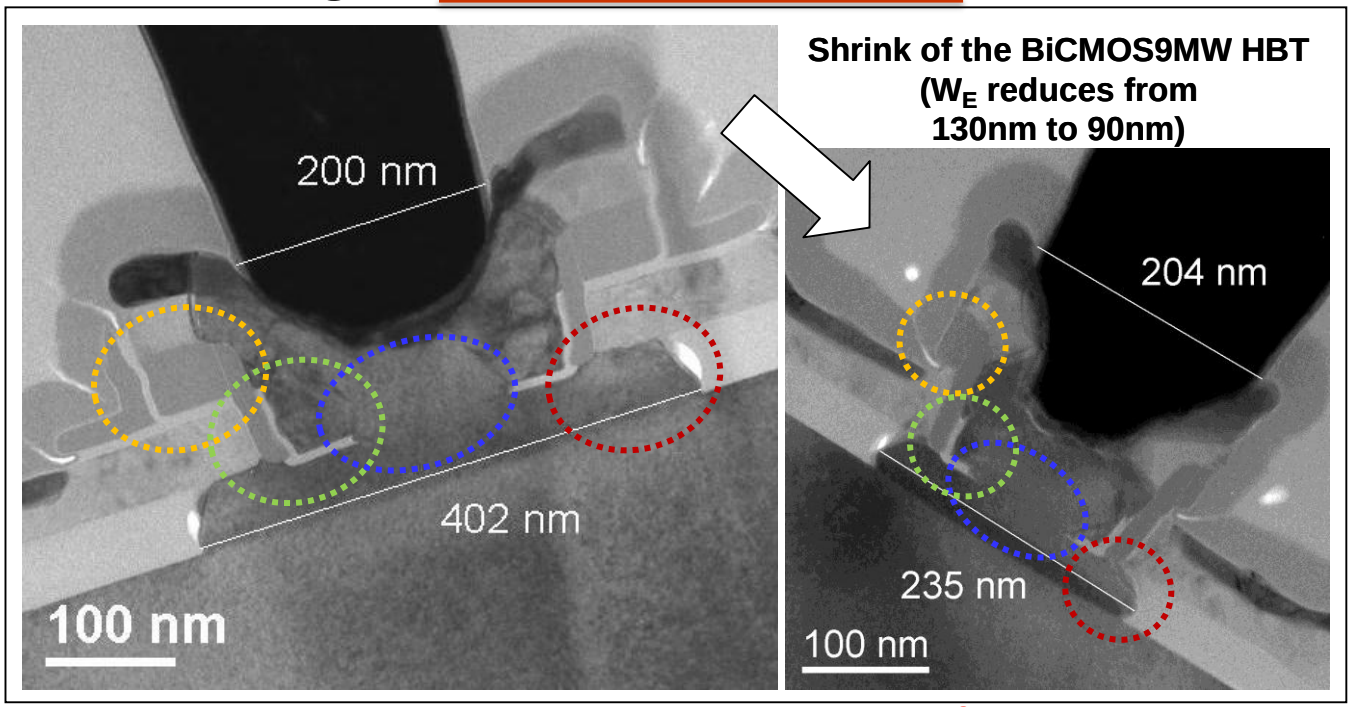


Narrower boron profile to reduce basewidth and base transit time (τ_B)

Larger collector doping to reduce collector resistance (R_C) & transit time (τ_{BC})

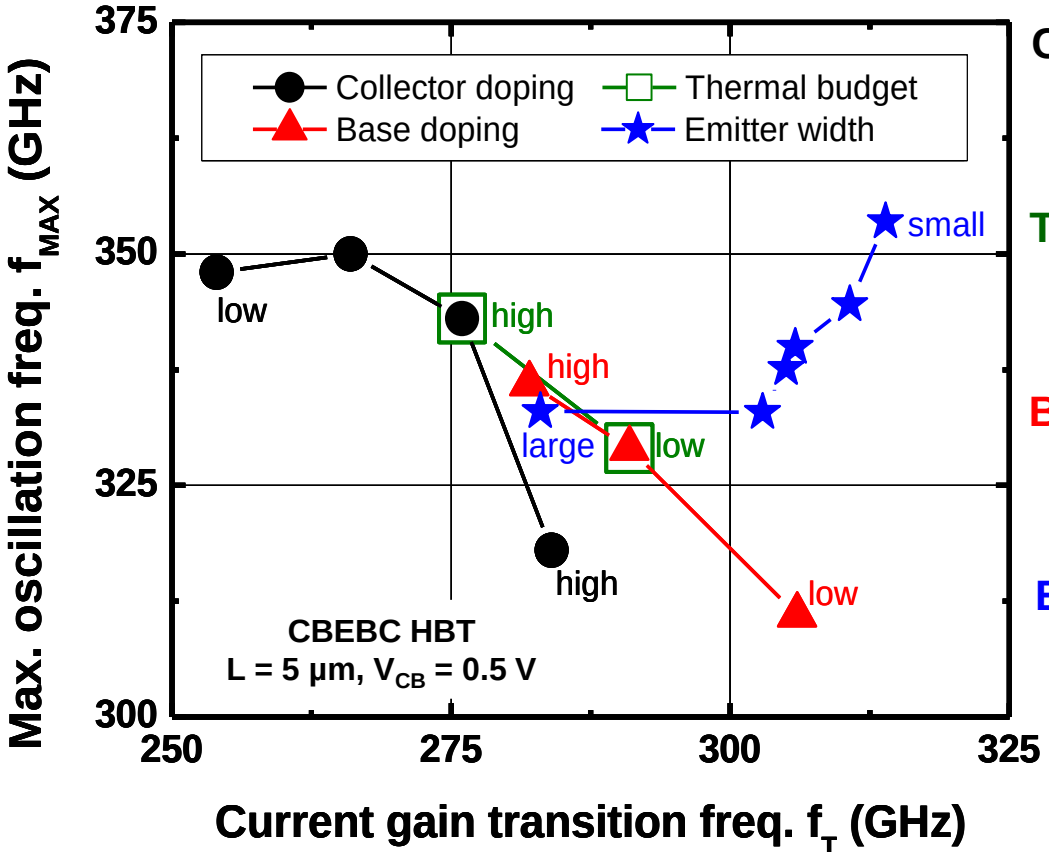
Lateral scaling principles

- Lateral scaling allows reducing all capacitances & resistances but R_E: Downscaling of emitter, polyemitter and inside spacer widths is beneficial to R_B
- Downscaling of base/collector width is beneficial to C_{BC}



Results example of scaling

- Results illustrate the impact of τ_{BC} / C_{BC} & τ_B / R_B trade-offs, R_{Bx} (extrinsic), and the benefit of lateral scaling, on f_T & f_{MAX}



Collector doping (BV_{CBO})
- **Low: 5.9 V**
- **High: 5.2 V**

Thermal budget (spike temp.)
- **High: 1080° C**
- **Low: 1050° C**

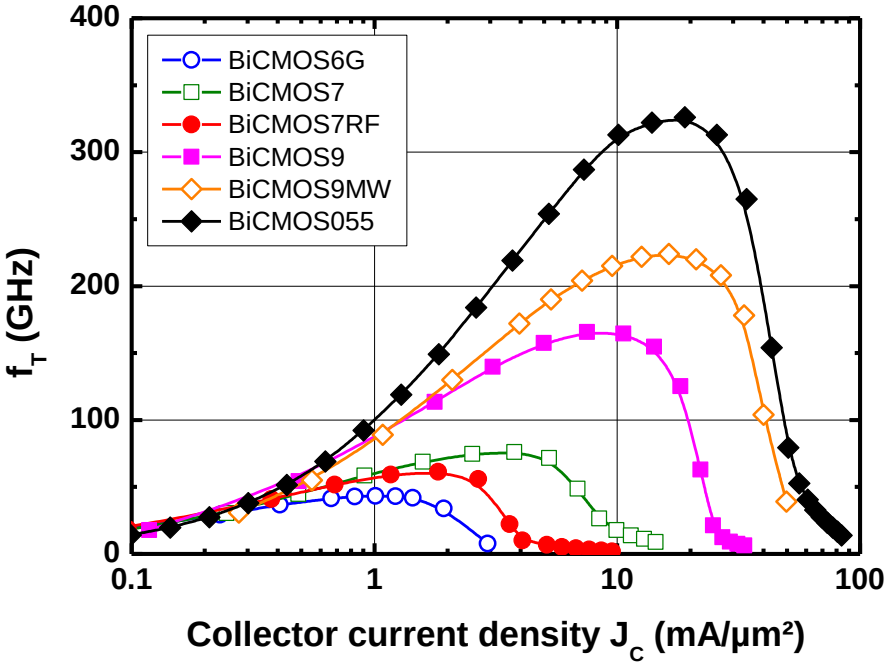
Base doping (Boron dose)
- **High: 2.5E13 at/cm²**
- **Low: 1.5E13 at/cm²**

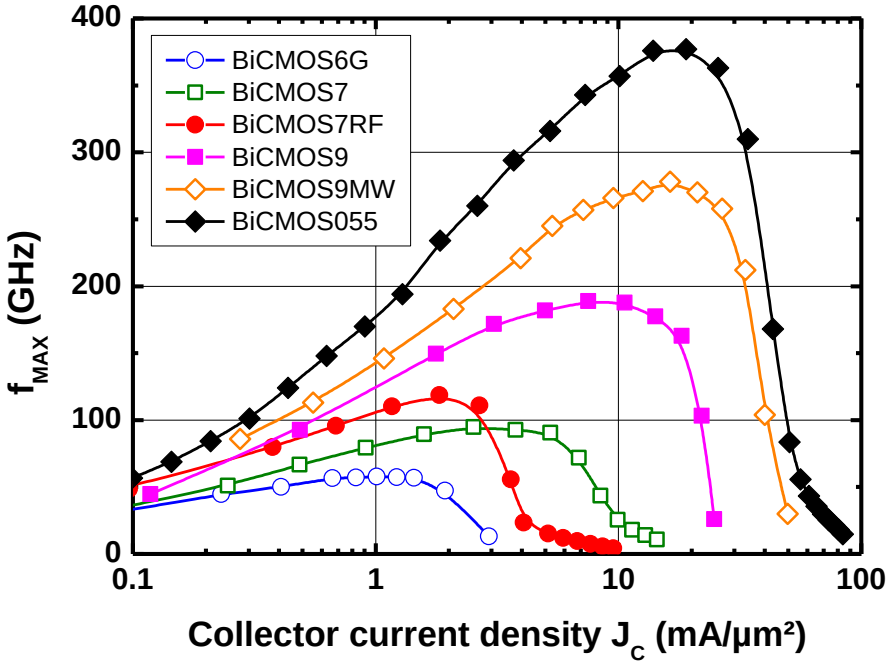
Emitter width (W_E)
- **Large: 0.17 µm**
- **Small: 0.10 µm**

[Chevalier12]

Scaling outcome

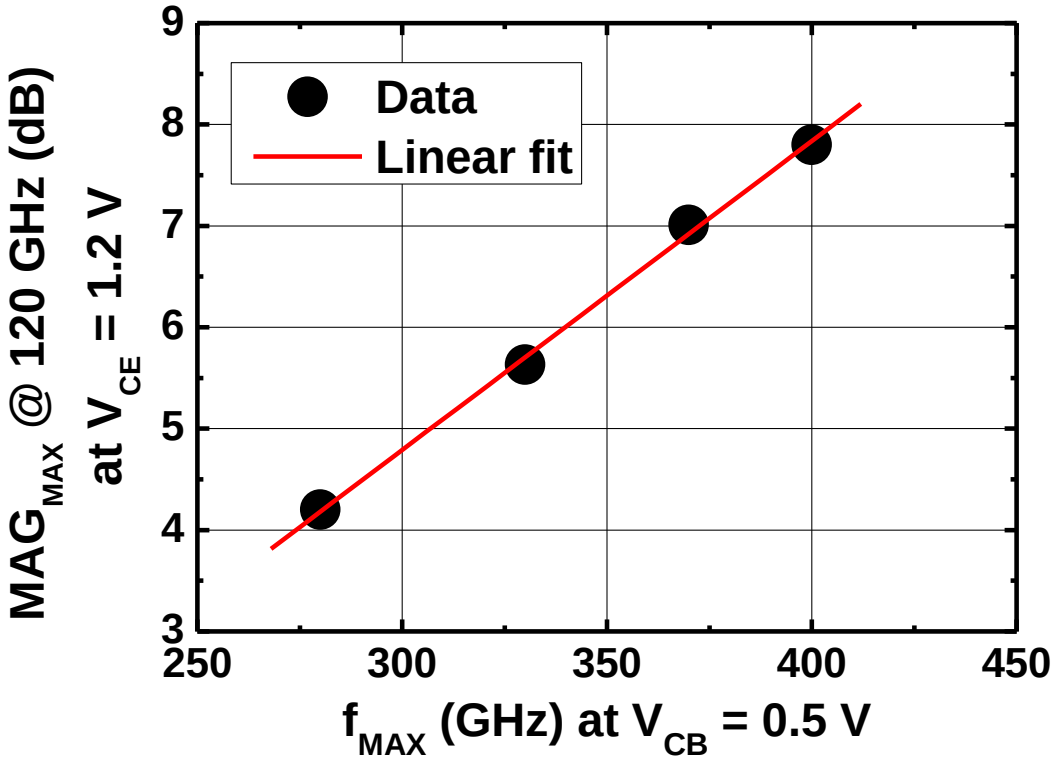
- f_T and f_{MAX} have been increased by a factor of about 6 from 0.35µm to 55nm CMOS nodes (in ~15 years)
  - Scaling strategy described previously for DPSA-SEG architecture is part of the work done to move from BiCMOS9MW to BiCMOS055





Benefits of scaling: MAG

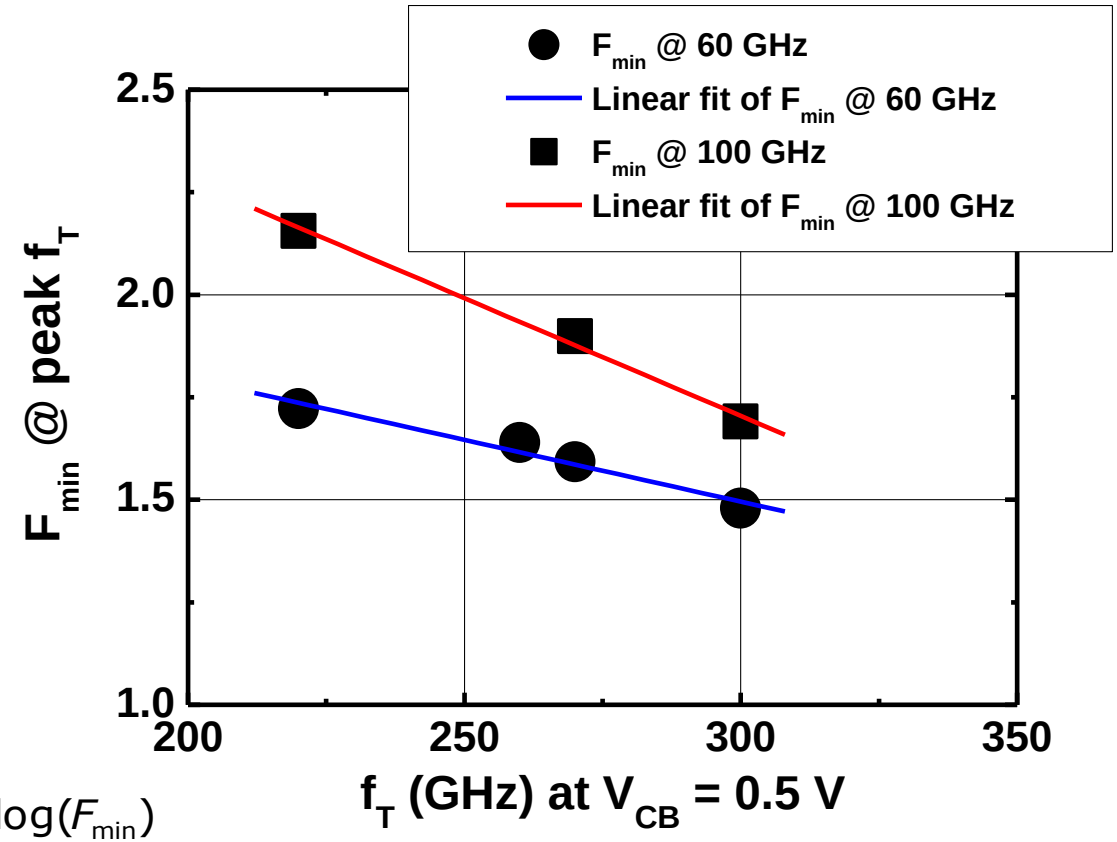
- As expected MAG (given here at 120 GHz) is well correlated to f_{MAX}



[Chevalier12]

Benefits of scaling: NF_{min}

- As expected minimum noise factor is well correlated to f_T

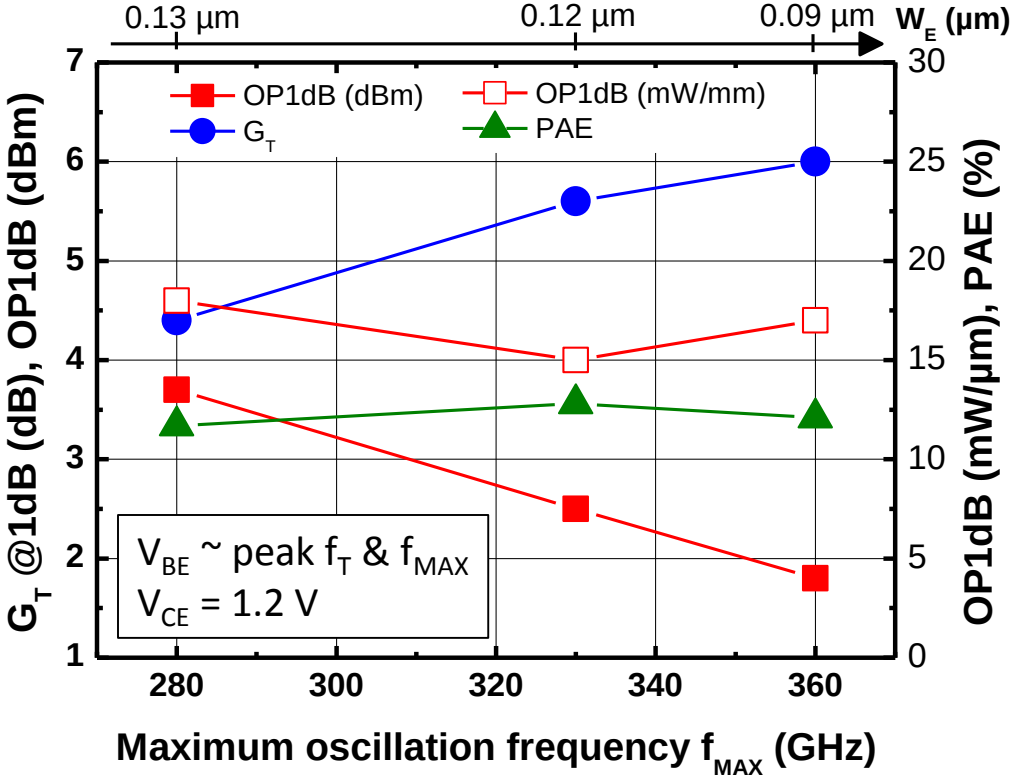


$NF_{min} = 10\log(F_{min})$

[Chevalier12]

Benefits of scaling: Power

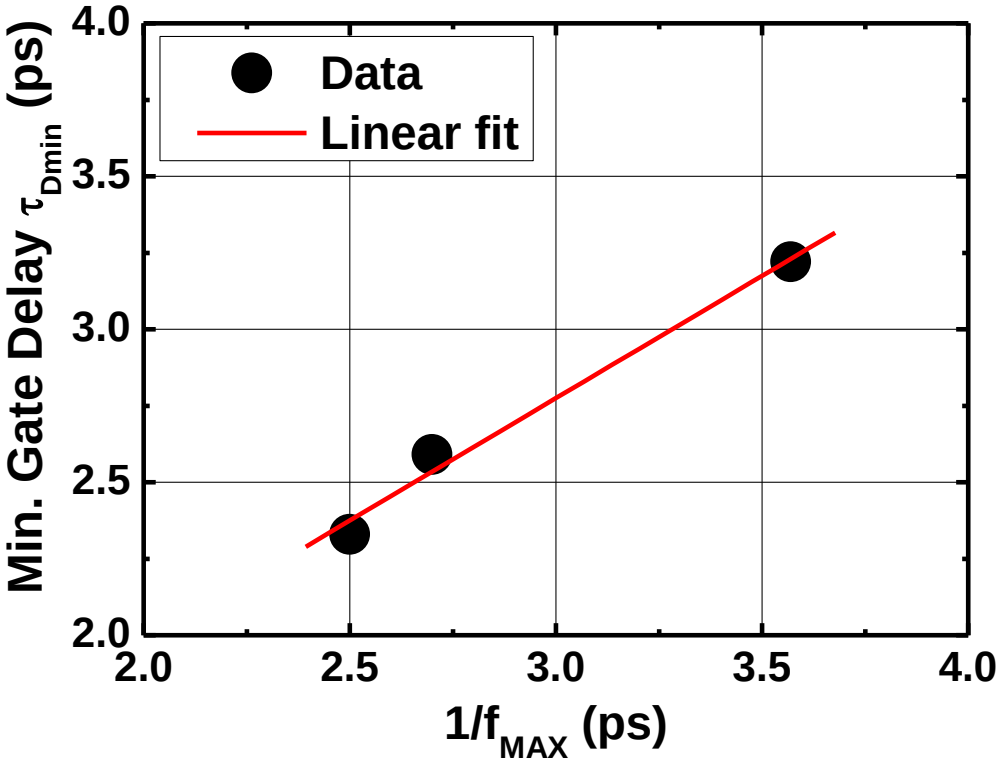
- Power performance in class A at 94 GHz
  - Transducer gain G_T improves with f_{MAX}
  - Output power (OP1dB) density remains constant



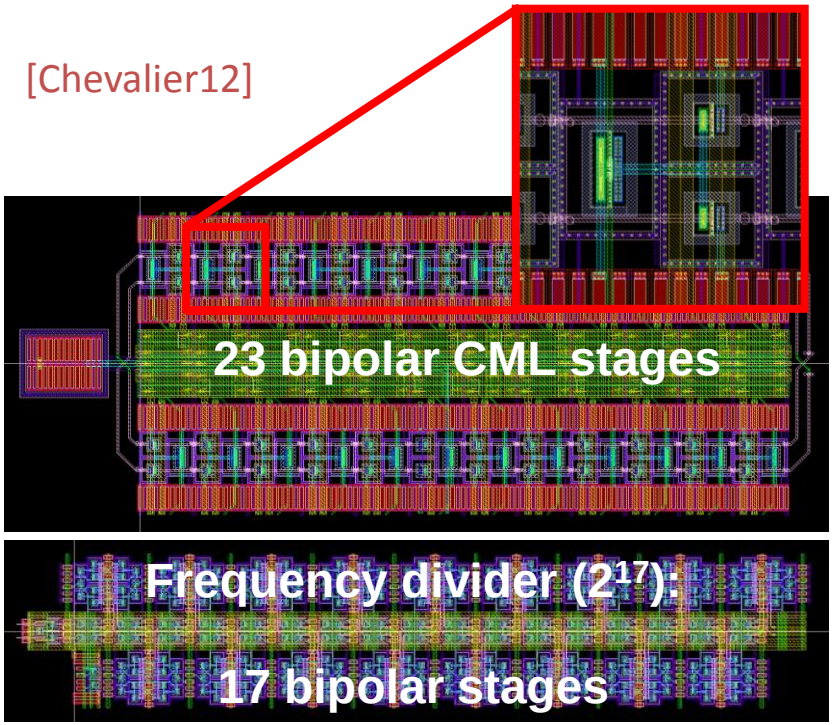
[Chevalier12]

Benefits of scaling: CML gate delay

- CML ring oscillator gate delay correlated to $1/f_{MAX}$
  - 23-stage CML ring oscillator (L_E = 1.5 µm, V_{dd} = 2.5 V, 400 mV differential voltage swing) with $1/2^{17}$ static CML frequency divider



[Chevalier12]



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Technology overview

55nm triple-gate oxide CMOS baseline

LP & GP HVT, SVT & LVT[1] CMOS w/ 2.5V IOs + LP LVT & HVT SRAM

High-Performance Analog GO1 LP LVT CMOS[1,2]

Natural bipolar transistors, resistors & capacitors + 6 kΩ/sq. HIPO resistor[1]

\+ \+ \+

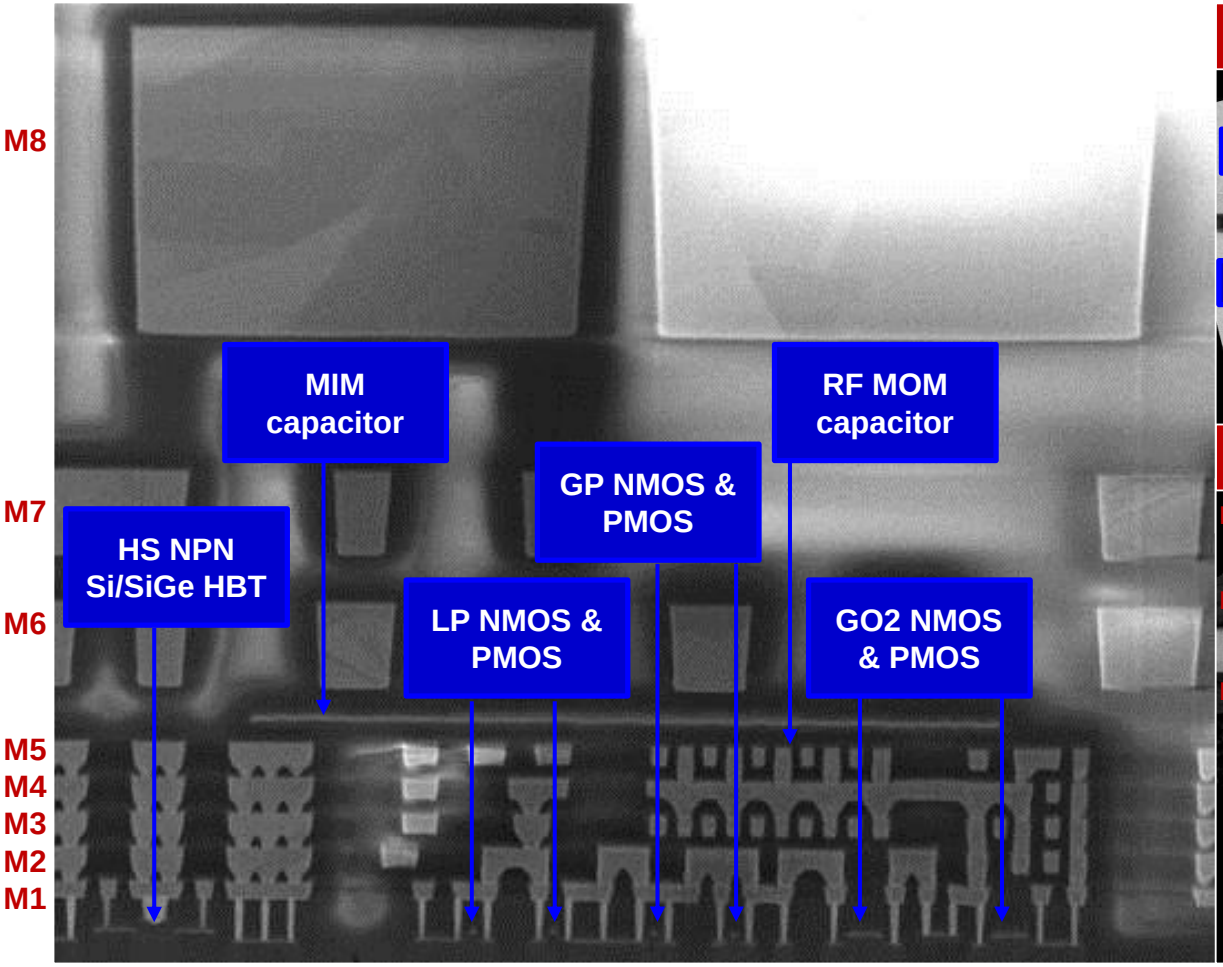
SiGe NPN HBTs	Varactors	Thick copper BEOL
(High-Speed Medium-Voltage & High-Voltage[1])	(MOS & Diode)	5 fF/µm² MIM[1]
	14V isolated GO2 MOS[2]	Thin Film Resistor[1,2]
		Transmission lines
		Inductors

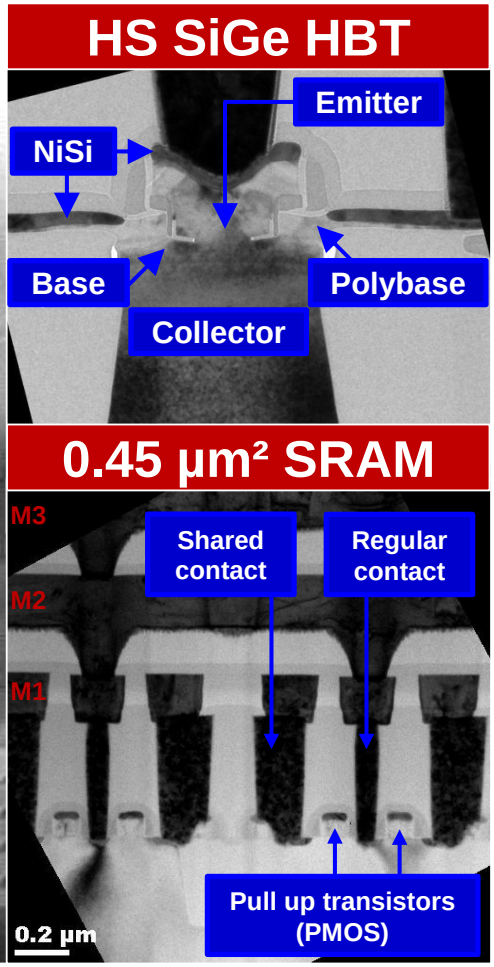
55-nm SiGe BiCMOS technology = BiCMOS055

Core process: 53 masks / Options: Up to +8 masks

(1) Option (2) Available end of 2015

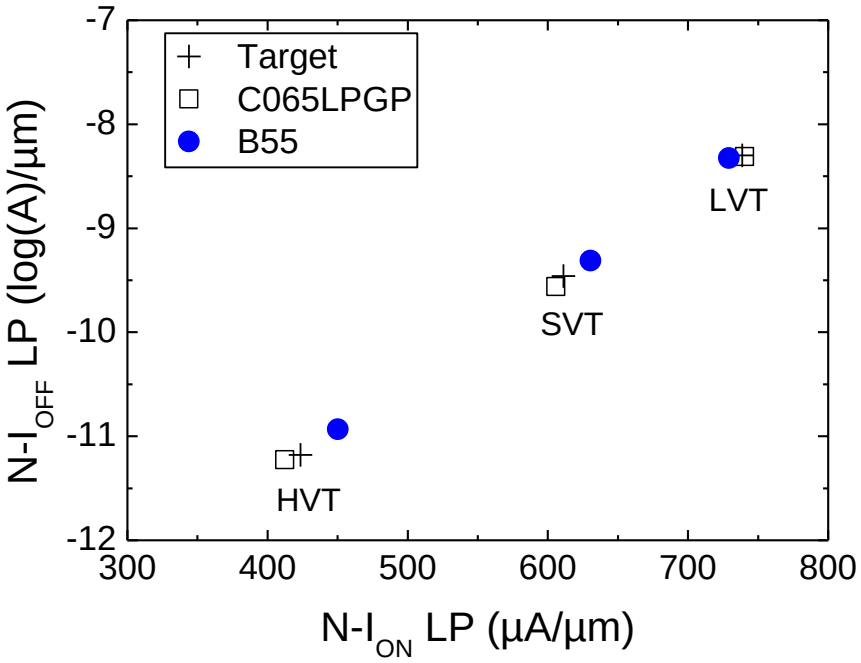
Technology cross-sections

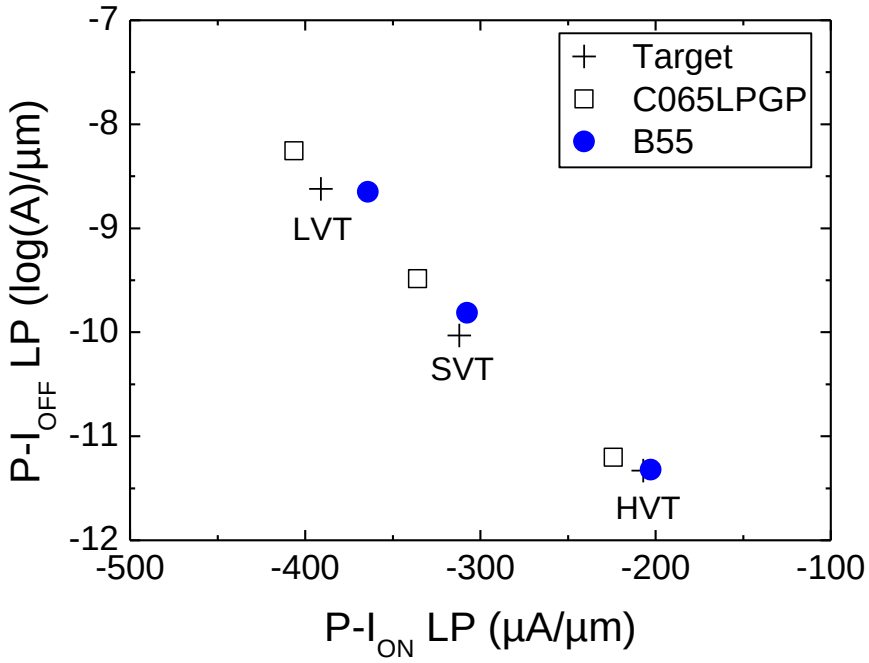




CMOS LP devices

- CMOS centering for all the families (LP/GP) & flavors (HVT/SVT/LVT) demonstrated by the I_{OFF}-I_{ON} plots

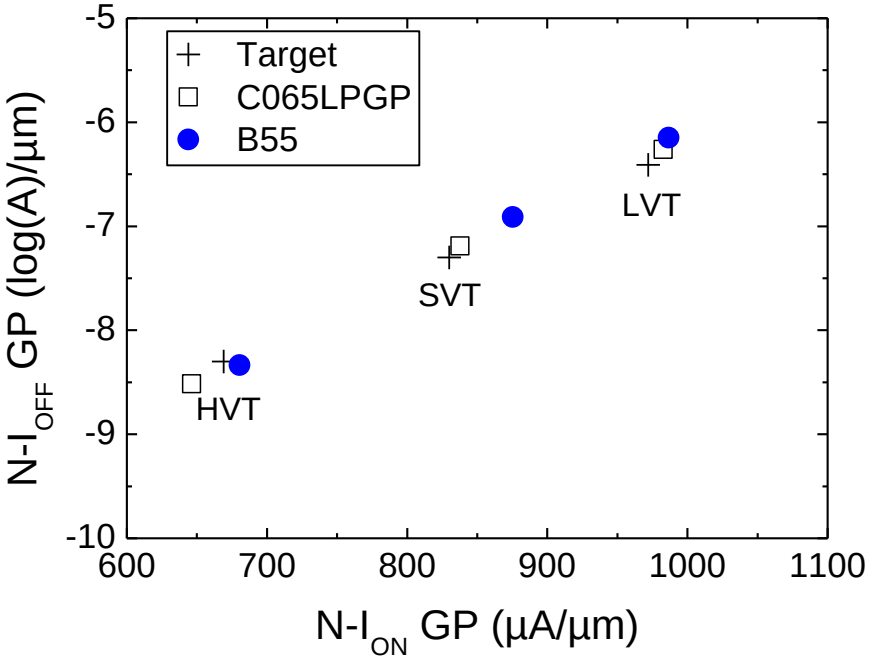


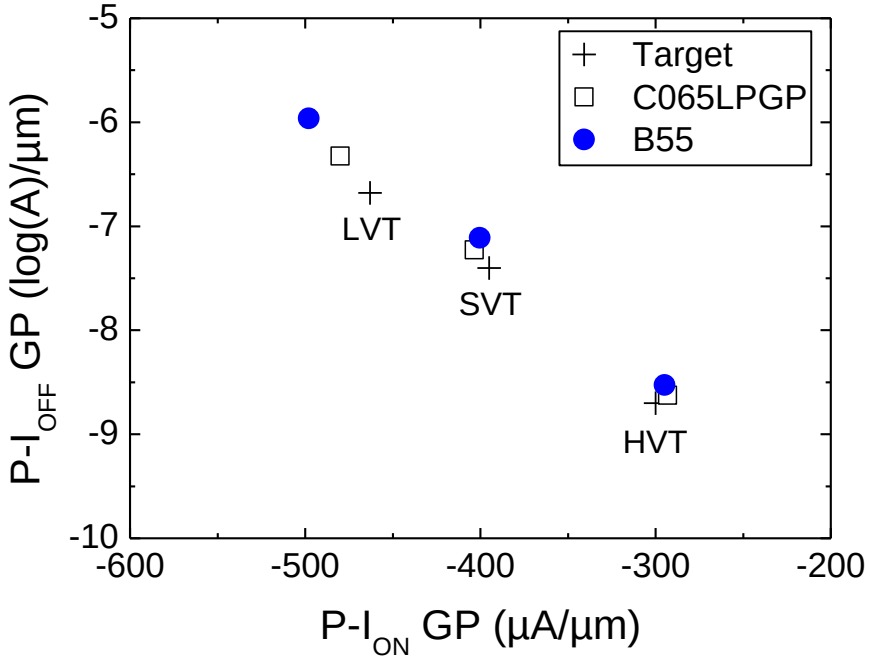


[Chevalier14]

CMOS GP devices

- CMOS centering for all the families (LP/GP) & flavors (HVT/SVT/LVT) demonstrated by the I_{OFF}-I_{ON} plots

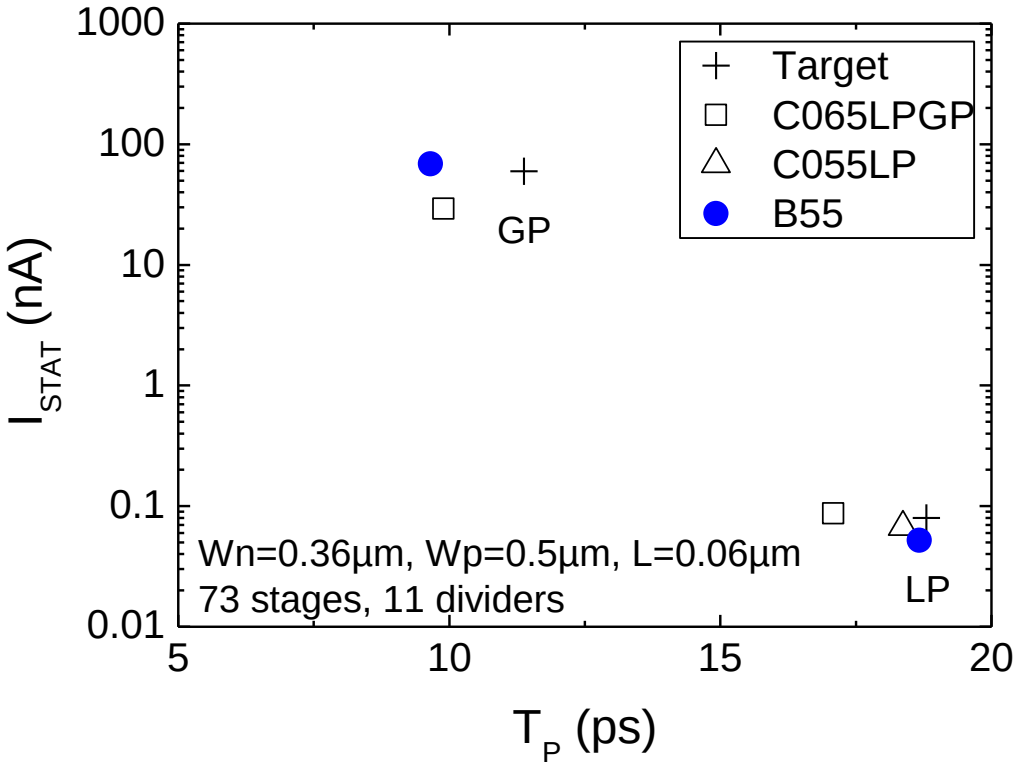




[Chevalier14]

CMOS logic devices

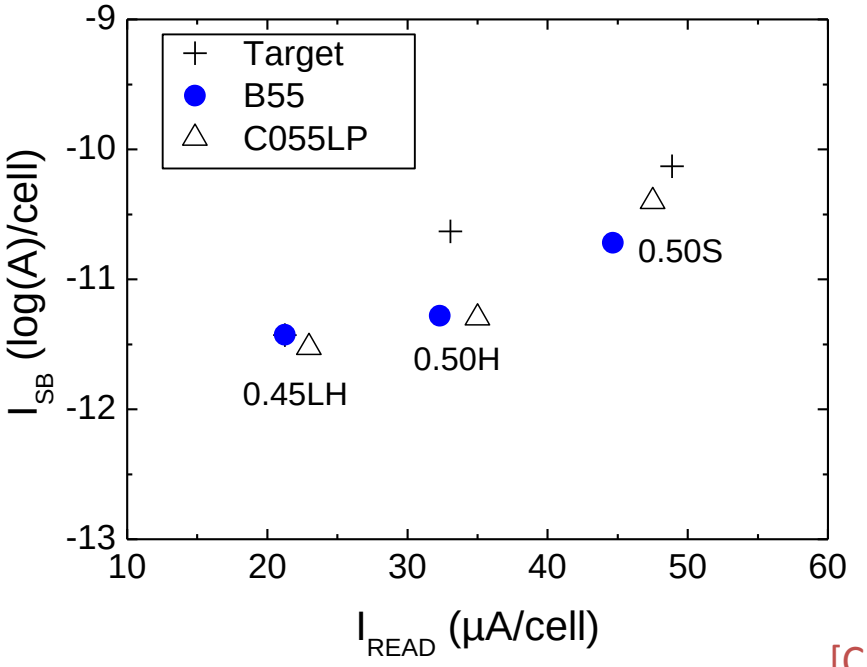
- CMOS centering is also assessed by the ring oscillator results

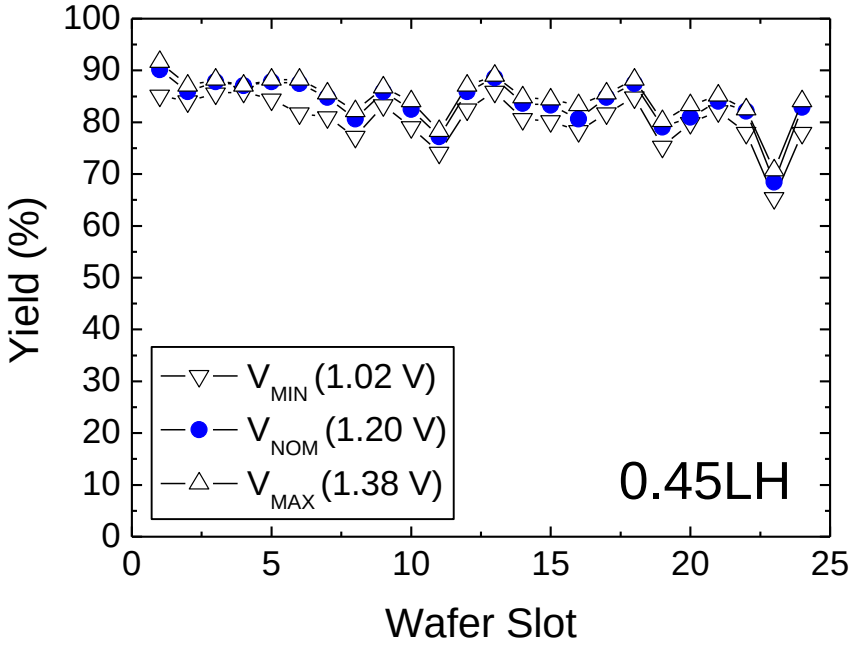


[Chevalier14]

SRAM bit cells

- I_{SB} vs I_{READ} aligned on C055LP
- Good yield and V_{DD} stability, even for the smallest (0.45 µm²) bit cell of 5.25 Mb

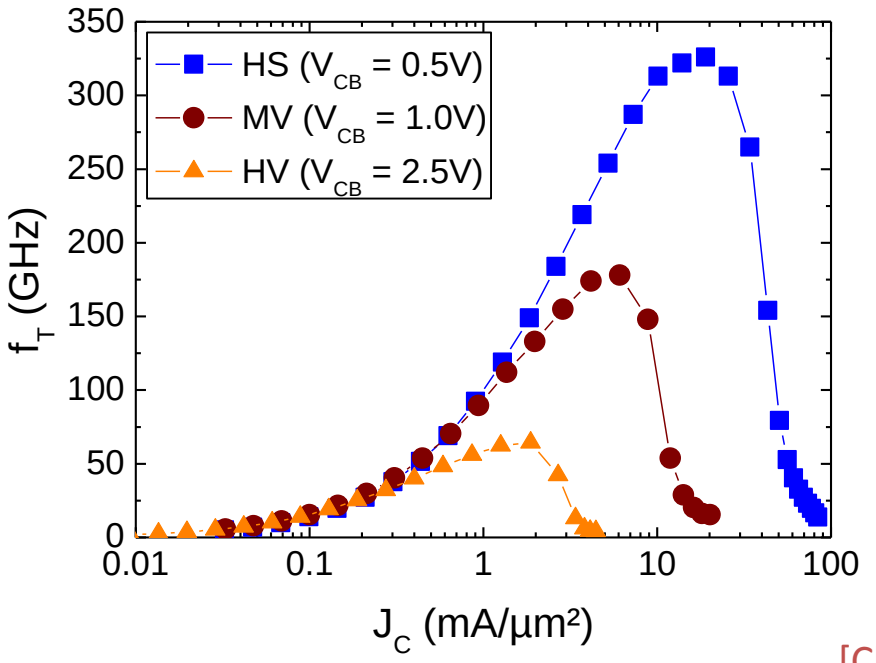


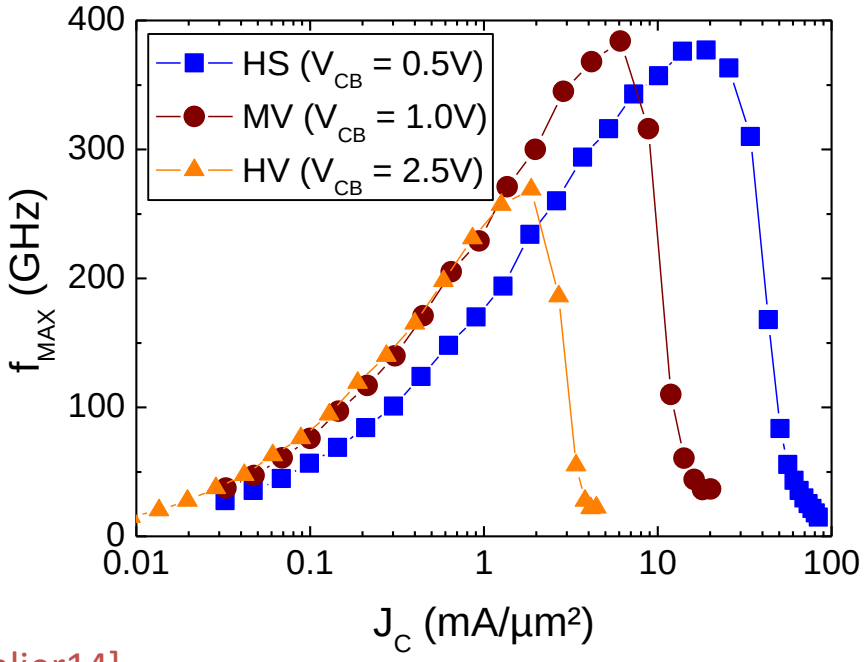


[Chevalier14]

NPN SiGe HBTs – HF

- 326 GHz f_T / 376 GHz f_{MAX} & 1.5 V BV_{CEO} demonstrated for the HS NPN

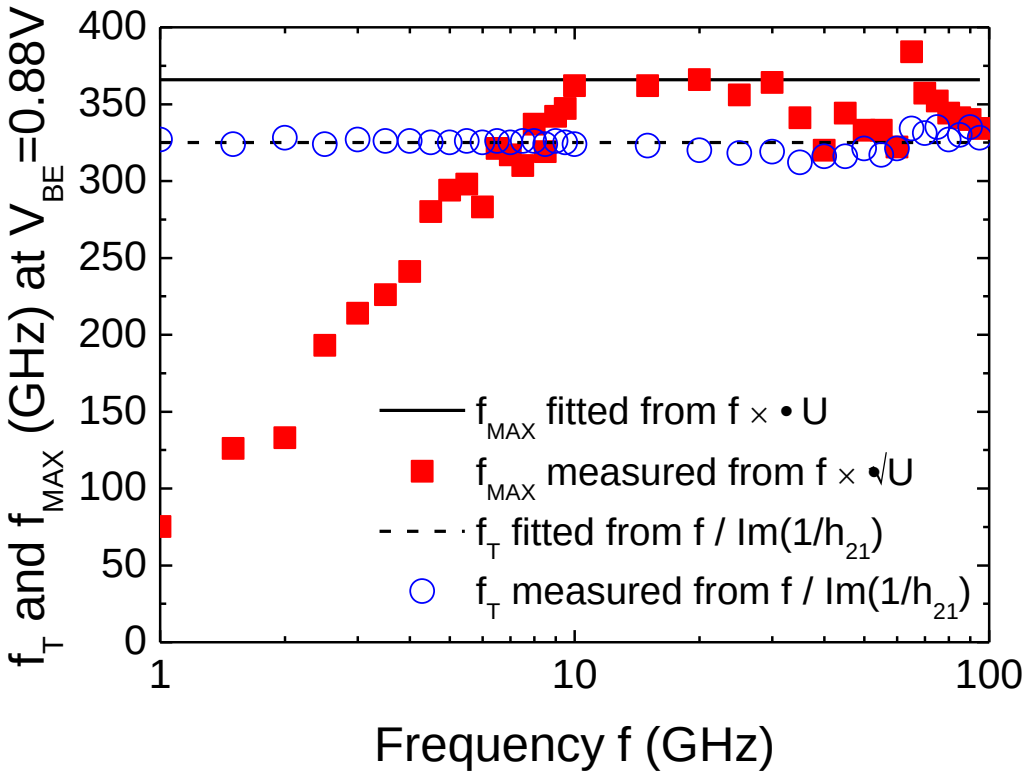




[Chevalier14]

NPN SiGe HBTs – HF

- f_T and f_{MAX} extractions



[Chevalier14]

NPN SiGe HBTs – Synthesis

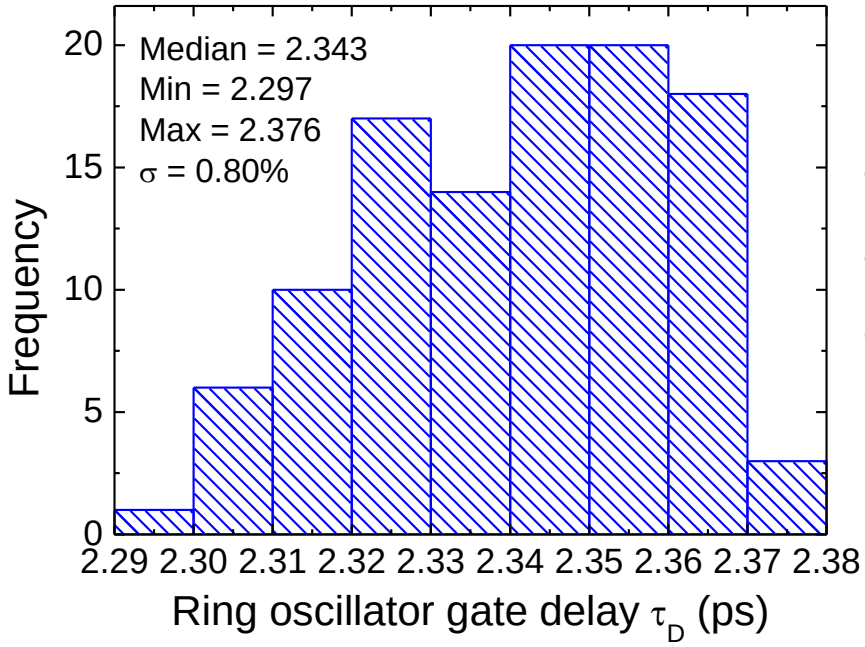
	NPN HS	NPN MV	NPN HV
Max f_T (GHz)	326 (V_{CB} = 0.5V)	178 (V_{CB} = 1V)	64 (V_{CB} = 2.5V)
Max f_{MAX} (GHz)	376 (V_{CB} = 0.5V)	384 (V_{CB} = 1V)	269 (V_{CB} = 2.5V)
J_C (mA/µm²) at max f_T & f_{MAX}	19	6.1	1.9
BV_{CBO} (V)	5.4	7.3	14.4
BV_{CEO} (V)	1.5	1.9	3.2

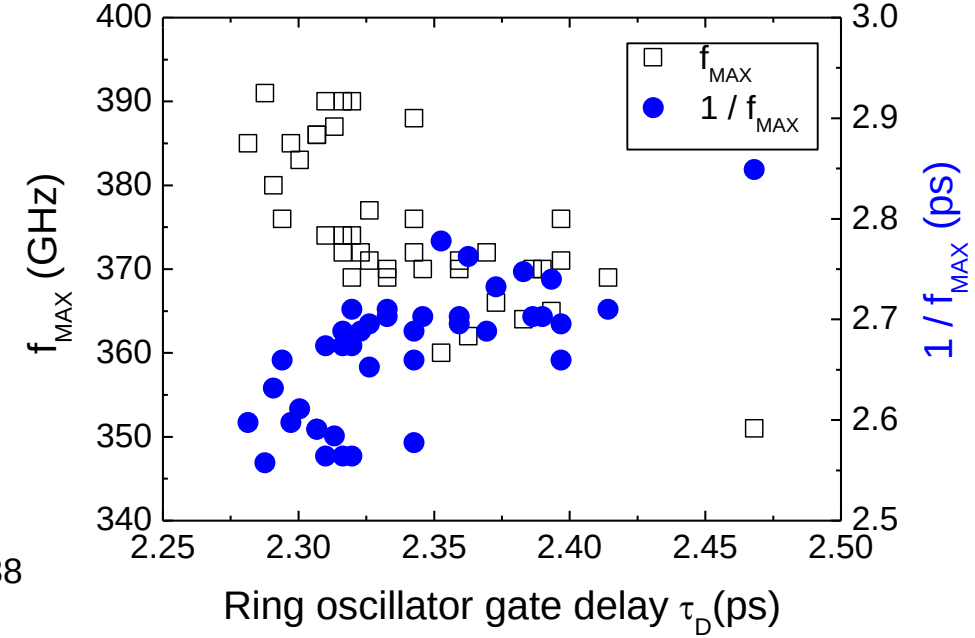
[Chevalier14]

SiGe for mm-Wave and THz / P. Chevalier

HS NPN ring oscillators

- 2.34 ps gate delay τ_D for the reference with very good on wafer uniformity
- 2.28 ps τ_D for 343 GHz f_T / 391 GHz f_{MAX} [Chevalier14]

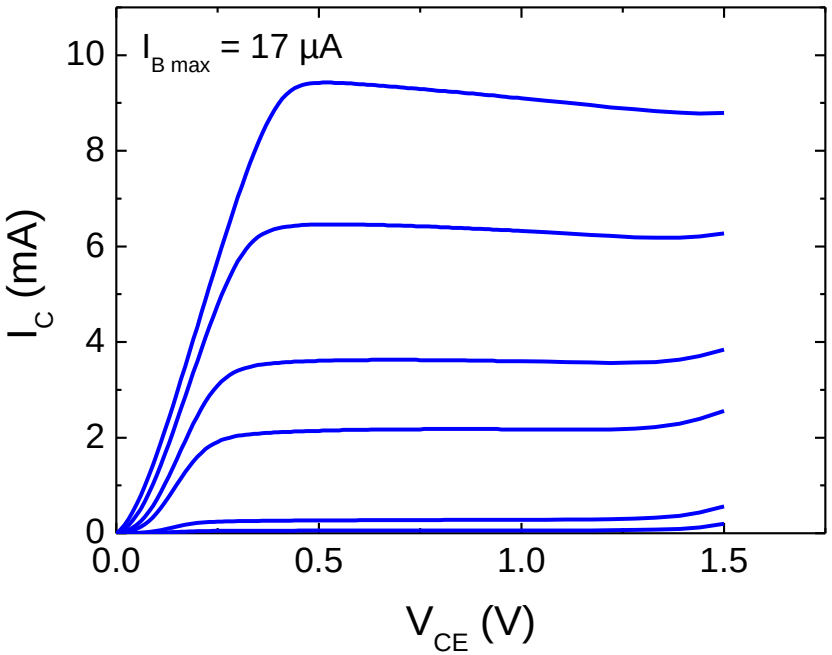


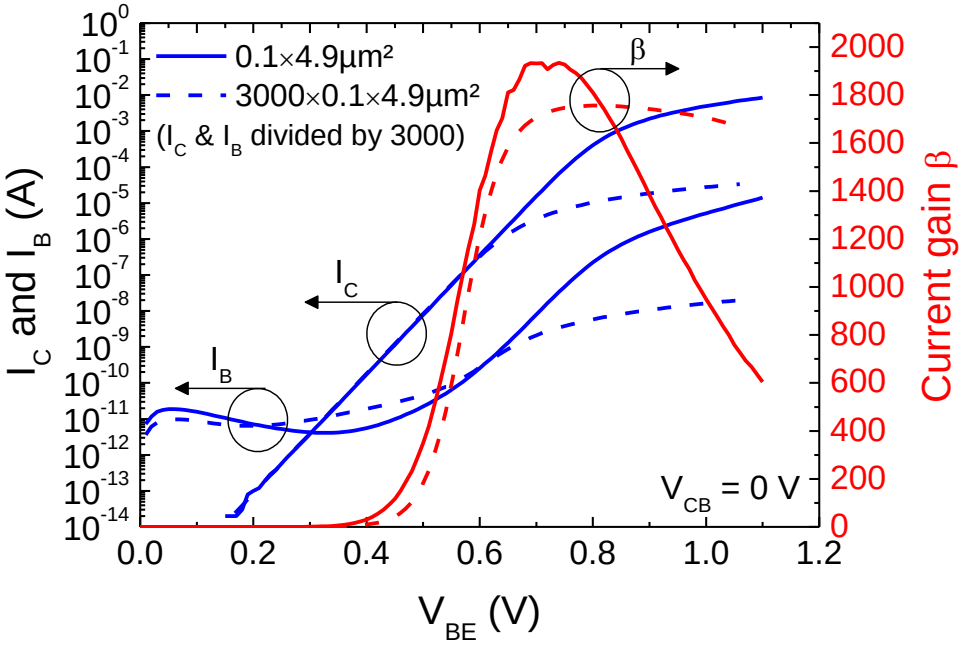


23-stage CML RO (L_E = 1.5 µm) with 1/2^{17} static CML frequency divider

HS NPN DC characteristics

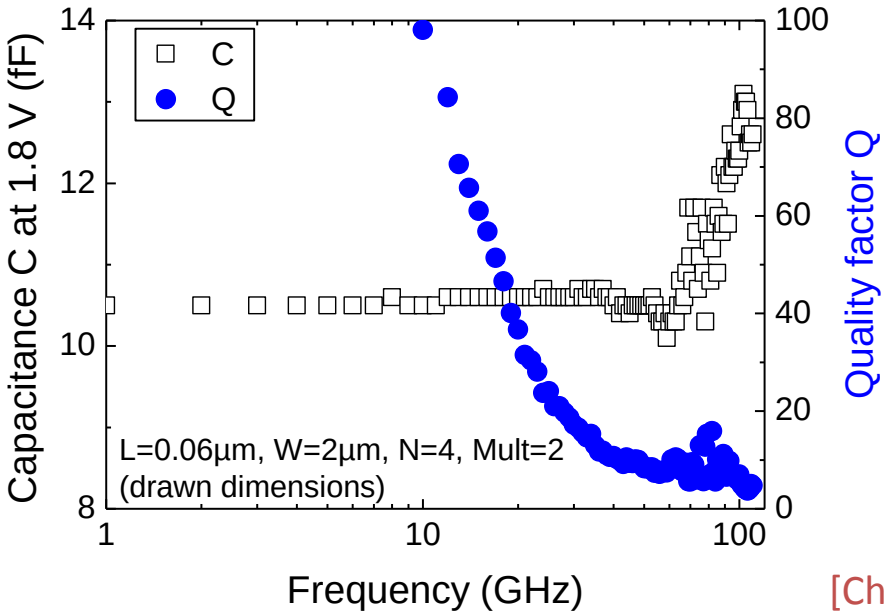
- Good DC characteristics & yield
- Peak of current gain (~1900) is reached at V_{BE} ~ 0.7 V





AMOS varactors

- P+ Poly / NWell GO1 & GO2 MOS varactors benefit from short MOS gate lengths
- GO2 (2.5V) varactors with minimum (GO1) gate lengths:

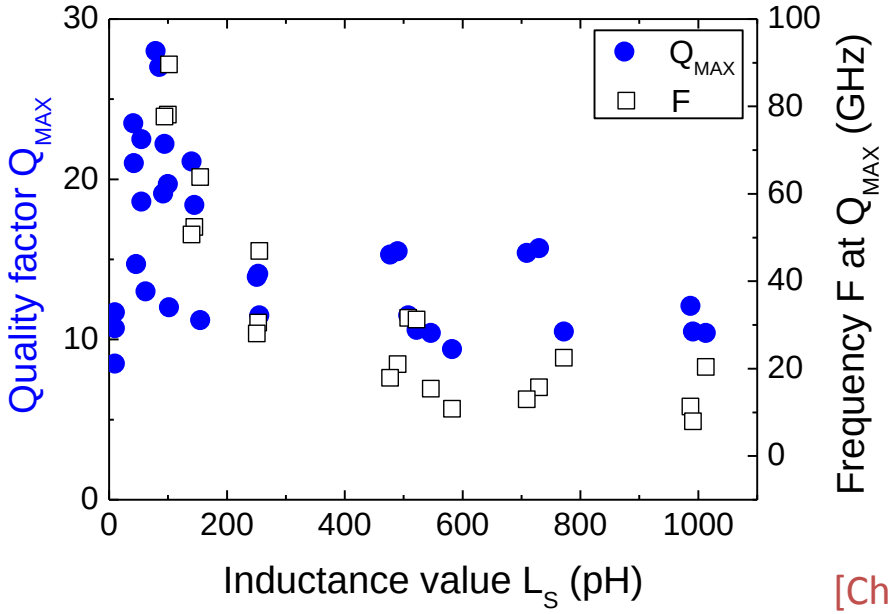


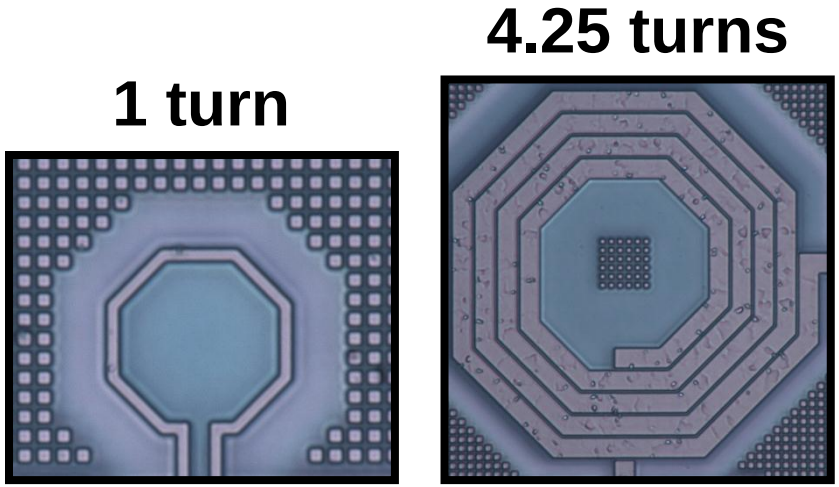
Parameters	GO2 Varactors P+ Poly / NWell
Capacitance range (Cmin / Cmax)	5 fF / 1 pF
Typical tuning ratio at 25 GHz & C=100 fF	3 (max 5)
Max Q at 25 GHz, C=100 fF, 2.5 V	30
Freq. of resonance at C=100 fF, 2.5 V	> 110 GHz

[Chevalier14]

Inductors & TL

- Transmission lines (TL) & inductors benefit from the specific thick BEOL (V7 + M8)
  - 50 Ω M8+Al TL: α = 0.51 dB/mm at 60 GHz
  - Inductors: 65 pH to 1.6 nH with Q > 10





[Chevalier14]

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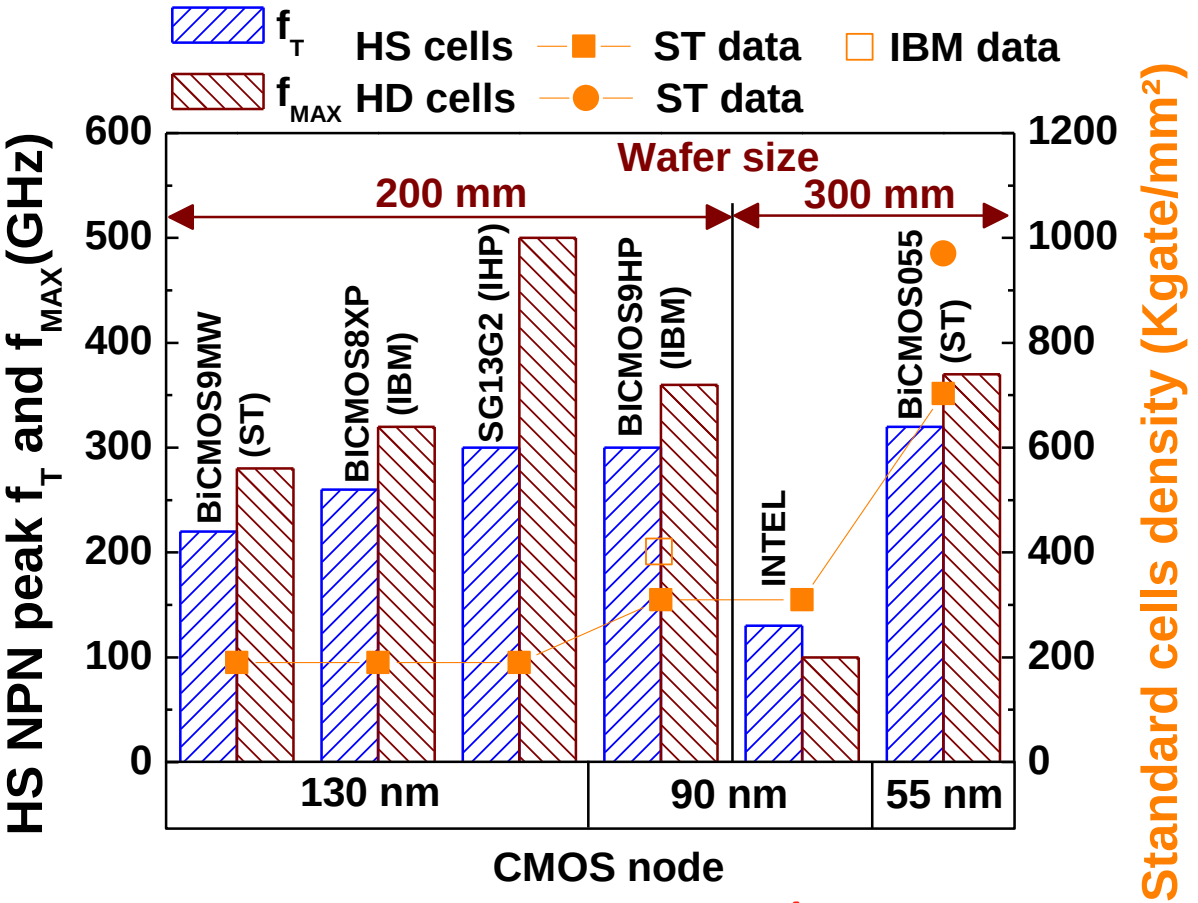
Summary

- BiCMOS055 provides a unique CMOS / SiGe HBT / passive devices combination



Perspectives

- 2nd 55nm BiCMOS generation (faster SiGe HBT)
  - Still some margin to improve the performance of DPSA-SEG architecture but a new HBT architecture would be required to reach or exceed 500 GHz f_{MAX}
- 28 nm FDSOI BiCMOS
  - Very challenging CMOS / HBT integration requiring the development of a new HBT architecture too

Acknowledgment & References

- Acknowledgment
  - Staff of STMicroelectronics, Crolles from TCAD, Process Development, Process Integration, Physical & Electrical Characterization, Modeling, Design, … involved in the development of High-Speed BiCMOS technologies with special thanks to G. Avenier, A. Montagné, G. Ribes, D. Céli, N. Derrier, D. Gloria, B. Sautreuil, and to the former PhD students T. Lacave & E. Canderle
  - Thanks to Pr. S. Voinigescu (University of Toronto, ECE), Pr. M. Schröter (University of Dresden / UC San Diego), Pr. C. Gaquière (University of Lille, IEMN) & Pr. T. Zimmer (University of Bordeaux, IMS) and their teams for their support in circuit design, device modeling & characterization
  - French Ministry of the Economy & of the Industry and the European Commission for their financial support through the projects:
    - SIAM: MEDEA+_2T206 "Silicon analogue to millimetre-wave technologies"
    - DOTFIVE: FP7-ICT_216110 "Towards 0.5 terahertz silicon / germanium heterojunction bipolar technology"
    - SUCCESS: FP7-ICT_248120 "Silicon-based ultra-compact cost-efficient sensor system design“
    - **RF2THZ SISoC: CATRENE_CT209 "From RF to MMW and THz Silicon SOC Technologies“**

- References

  - [Chevalier12] P. Chevalier et al, “Scaling of SiGe BiCMOS Technologies for Applications above 100 GHz”, Compound Semiconductor Integrated Circuits Symposium (CSICS) Digest, 2012
  - [Chevalier14] P. Chevalier et al, “A 55 nm Triple Gate Oxide 9 Metal Layers SiGe BiCMOS Technology Featuring 320 GHz f_T / 370 GHz f_{MAX} HBT and High-Q Millimeter-Wave Passives”, International Electron Devices Meeting Digest, 2014