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EUROPEAN MICROWAVE WEEK 2015

SIX DAYS • THREE CONFERENCES • ONE EXHIBITION

PALAIS DES CONGRÈS, PARIS, FRANCE
SEPTEMBER 6 - 11, 2015

Exhibition Opening Hours:
- Tuesday 8th September: 9.30 – 18.00
- Wednesday 9th September: 9:30 – 17.30
- Thursday 10th September: 9:30 – 16.30

# Optimization of Vertical Doping Profiles for High-Speed SiGe HBTs

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**WS12: EuMIC - *SiGe for mm-Wave and THz***

# Outline

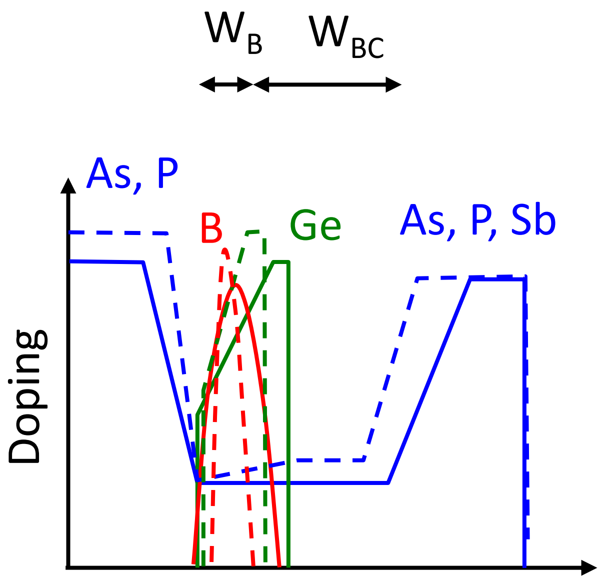
- Introduction
- HBT fabrication
- RF characterization
- Device simulation
- Analysis of profile variations
- Summary

# Introduction

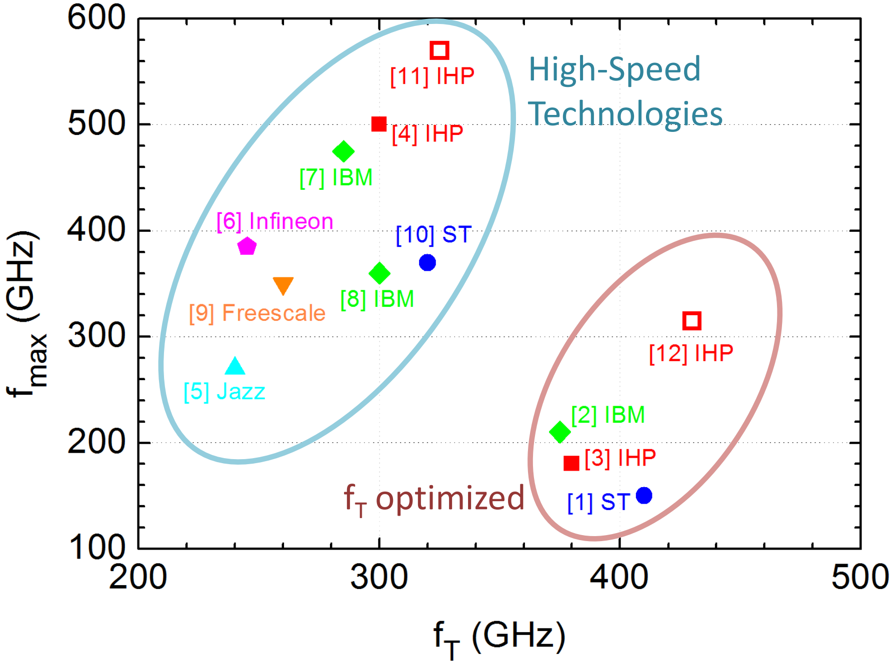
- Speed optimization of HBTs involves:
  - Scaling of vertical profiles for high $f_T$
  - Scaling of lateral dimensions and advanced device architectures for low external parasitics, high $f_{max}$
- This talk focused on vertical profile
  - Explore potential for $f_T$ improvement
  - Combine most promising profiles and advanced lateral device geometries in next step

# $f_T$ Improvement by Vertical Scaling

- Reduce base width ➔ low $\tau_B$
  - Narrow as-deposited profile
  - Low thermal budget
  - Challenge: maintain low resistances
- Steep Ge slope ➔ low $\tau_B$
- Reduce BC depletion width ➔ low $\tau_{BC}$
  - Increase collector doping (SIC)
  - Suppressed Kirk effect, higher $j_C$
- Reduce EB depletion width ➔ low $\tau_E$
  - Reduced compensated charge ($C_N$) in EB depletion region



# $f_T/f_{max}$ Performance





[1] Rieh et al. IPRM 2003
[2] Heinemann et al. IEDM 2004
[3] Geynet et al. BCTM 2008
[4] Heinemann et al. IEDM 2010
[5] Preisler et al. BCTM 2011
[6] Lachner et al. ECS 2014
[7] Liu et al. ECS 2014
[8] Pekarik et al. BCTM 2014
[9] John et al. BCTM 2014
[10] Chevalier et al. IEDM 2014
[11] Böck et al. BCTM 2015 (submitted)
[12] Korn et al. BCTM 2015 (submitted)


- Speed-optimized technologies demonstrate peak $f_T$ values of 300-320GHz and simultaneously $f_{max}$ up to 500 GHz
- Significant progress for $f_{max}$
- Only limited progress for $f_T$ over last years (often on cost of $f_{max}$)
- Simulations suggest that peak $f_T$ values close to 1 THz may be achievable [Schröter et al., TED 2011]

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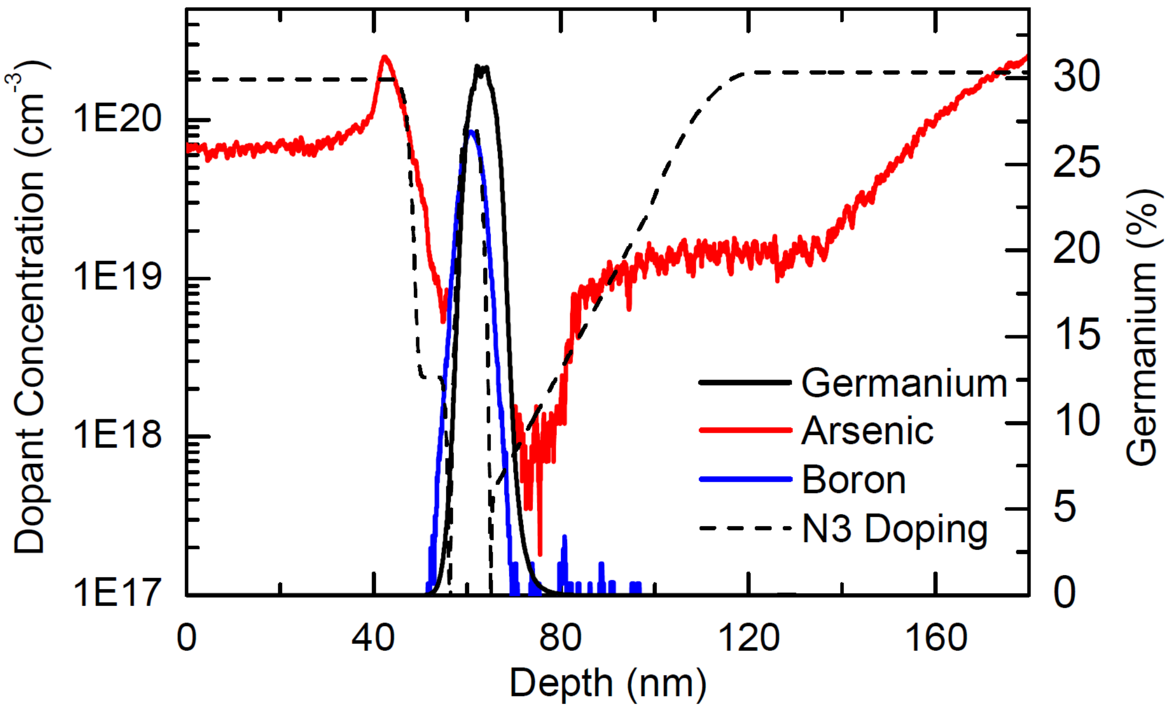
# Process Flow

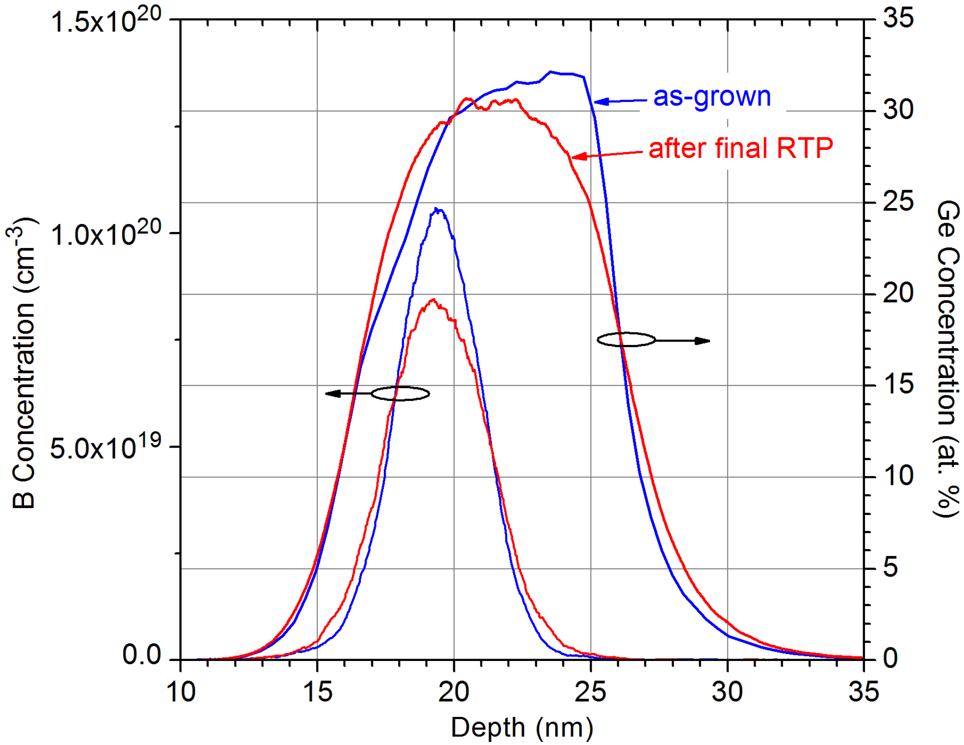
- Experimental process based on SG13G2 technology of IHP
  - CMOS process sequences skipped
  - HBT fabrication as in SG13G2
    - Collector regions isolated by STI
    - Non-selective base epitaxy
    - Elevated extrinsic base formed after emitter structuring
    - Dimensions of emitter windows and BE spacers relaxed here
    - For details: Rücker et al, SiRF 2012
  - Spike RTP reduced from 1050°C to 1030°C
  - Standard cobalt salicidation
  - Only 3 Al interconnect layers

# Doping Profile




- SIMS profiles of B, As, and Ge measured at the end of fabrication process
  - Profile N3 from a theoretical performance study served as starting point [Schröter et al SiRF 2014]
  - B and Ge profiles are close to theoretical suggestion
  - Proposed steep increase of collector doping could not be reproduced with present process

# Dopant diffusion




- Very little B diffusion during present low-temperature fabrication process
- Maintaining tailored Ge profiles is challenging due to enhanced Ge diffusion at high Ge concentrations

# Fabricated Profiles Variants

| | | P1 | P2 | P3 | P4 | P5 |
|---|---|---|---|---|---|---|
| | | Reference | Cap + 1.5nm | Cap + 3nm | Reduced SIC | Ge extended in BE junction |
| $R_{sbi}$ ($\Omega$) | Tetrode | 2.7 | 2.6 | 2.5 | 2.6 | 2.5 |
| $BV_{EBO}$ (V) | 10 µA/µm$^2$ | 1.0 | 1.2 | 1.5 | 1.2 | 1.2 |
| $BV_{CBO}$ (V) | 1 µA/µm$^2$ | 4.0 | 4.1 | 4.1 | 5.5 | 3.9 |
| $BV_{CEO}$ (V) | $I_B$ reversal | 1.45 | 1.45 | 1.5 | 1.55 | 1.6 |

- Variations of cap thickness, SIC doping, and Ge profile
- $R_{sbi}$ sufficiently low for high $f_{max}$ of scaled devices
- Breakdown voltages reduced do to smaller EB and BC depletion width but still in an acceptable range for targeted high-speed applications

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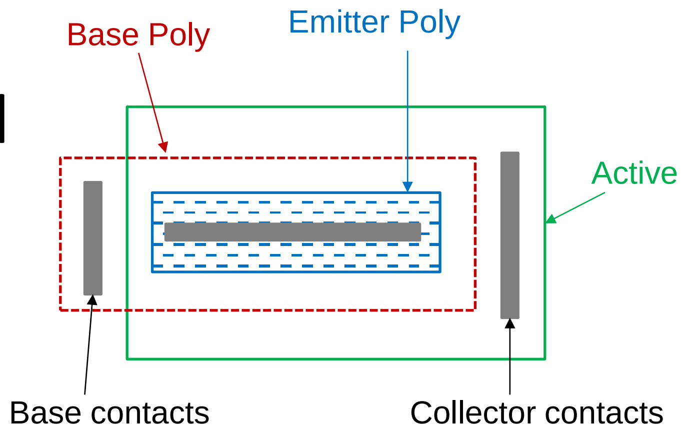
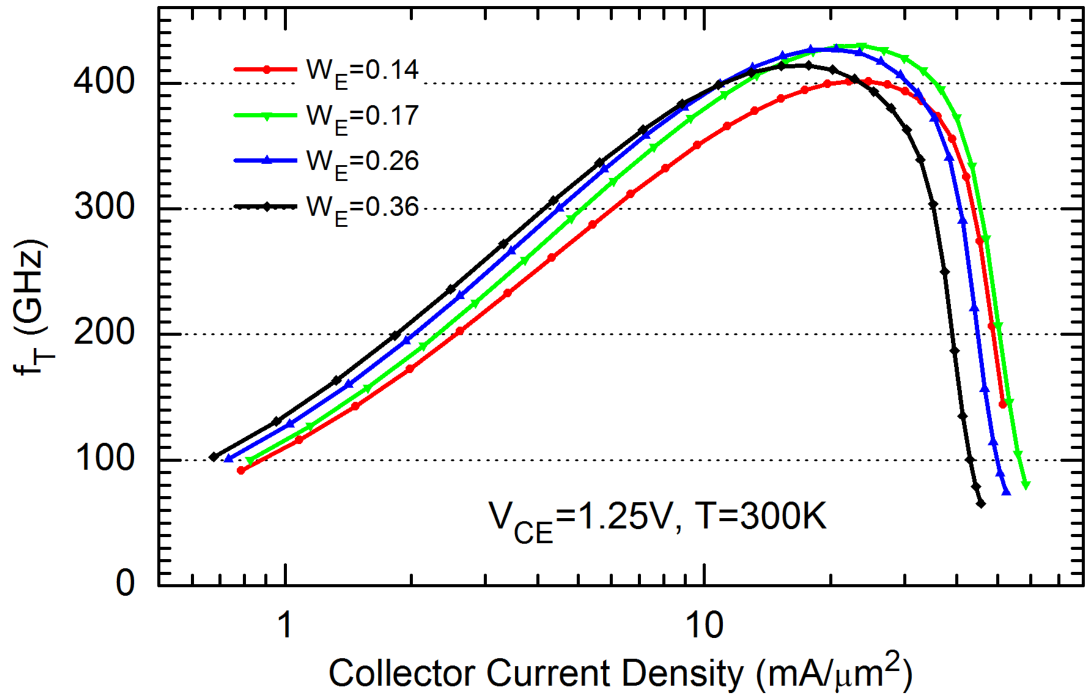
# HBT Layout

- Emitter and collector contacts formed in one active area
- Base and collector contacts formed at the edges of the emitter stripe
  - Minimizes overlap area of base poly and collector
  - Based on SG13G2 HBT layout
- Emitter widths ranging from 0.14 to 0.36 µm
  - Common emitter lengths 1 µm
  - RF measurements for 8 HBTs in parallel



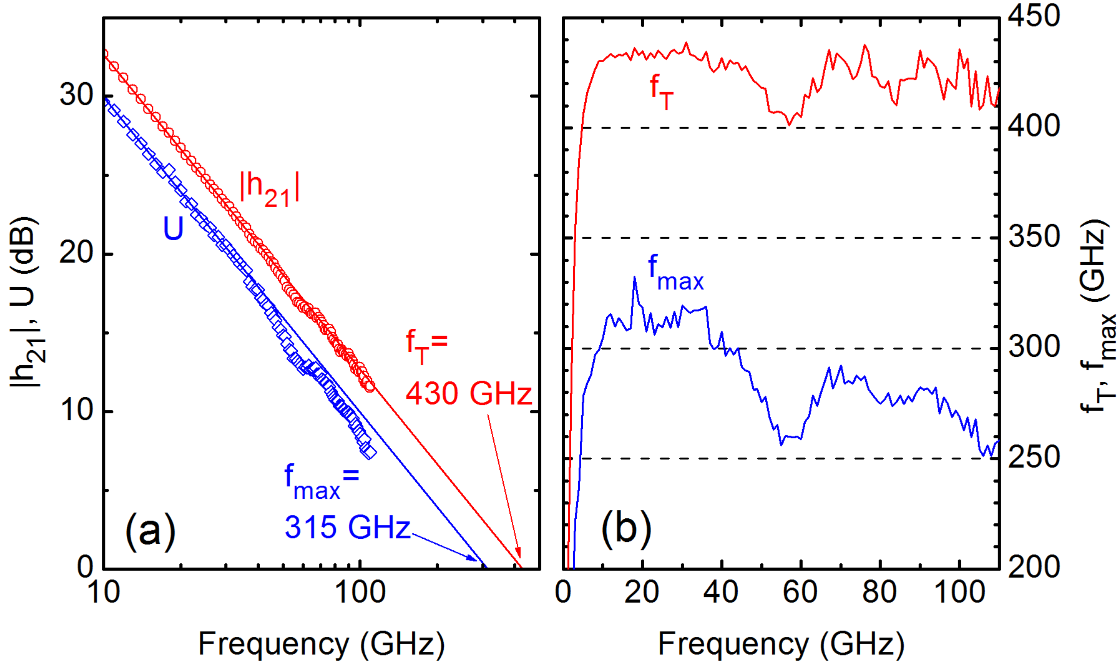
# Measured $f_T$ vs. $I_C$




Korn et al. BCTM 2015

- $f_T$ at low $I_C$ increases with increasing emitter width due to reduced impact of parasitic capacitances from device perimeter
- Larger devices show earlier roll-off of $f_T$ at high current densities
- Highest peak $f_T$ of 430 GHz for HBT with intermediate $W_E$ of 0.17µm

# Extraction of $f_T$ and $f_{max}$




- $f_T$ and $f_{max}$ extracted from $|h_{21}|$ and U with a slop of -20dB/dec and averaged over measurement frequencies from 10 to 40 GHz
- Peak $f_T/f_{max}$ values of 430 GHz/315 GHz for device with $A_E$=8x(0.17x1.01)μm$^2$

# Impact of Emitter Width

| Parameter | Method | D1 | D2 | D3 | D4 |
|---|---|---|---|---|---|
| $W_E$ (µm) | SEM | 0.14 | 0.17 | 0.26 | 0.36 |
| $L_E$ (µm) | SEM | 0.99 | 1.01 | 0.97 | 0.97 |
| Peak $f_T$ (GHz) | $V_{CE}$=1.25V | 402 | 430 | 426 | 414 |
| $j_C$ (mA/µm$^2$) | @ peak fT | 23 | 23 | 20 | 17 |
| $R_{TH}$ (K/W) | Russo, 2009 | 9340 | 9200 | 8870 | 8470 |
| $\Delta T_j$ (K) | @ peak fT | 37 | 45 | 56 | 63 |

- Larger devices reach peak $f_T$ at lower current density
  - Larger self heating
  - Increased impact of $R_C$
- Focus on device D2 for analysis of different vertical profiles
  - Compromise with respect to impact of parasitics from device perimeter and degradation due to self heating

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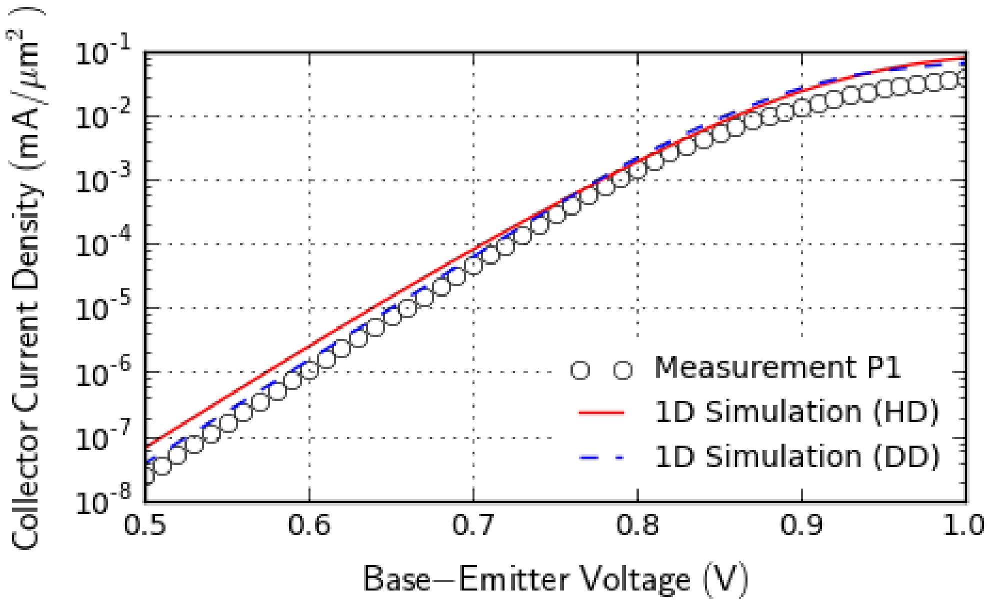
# Device Simulation

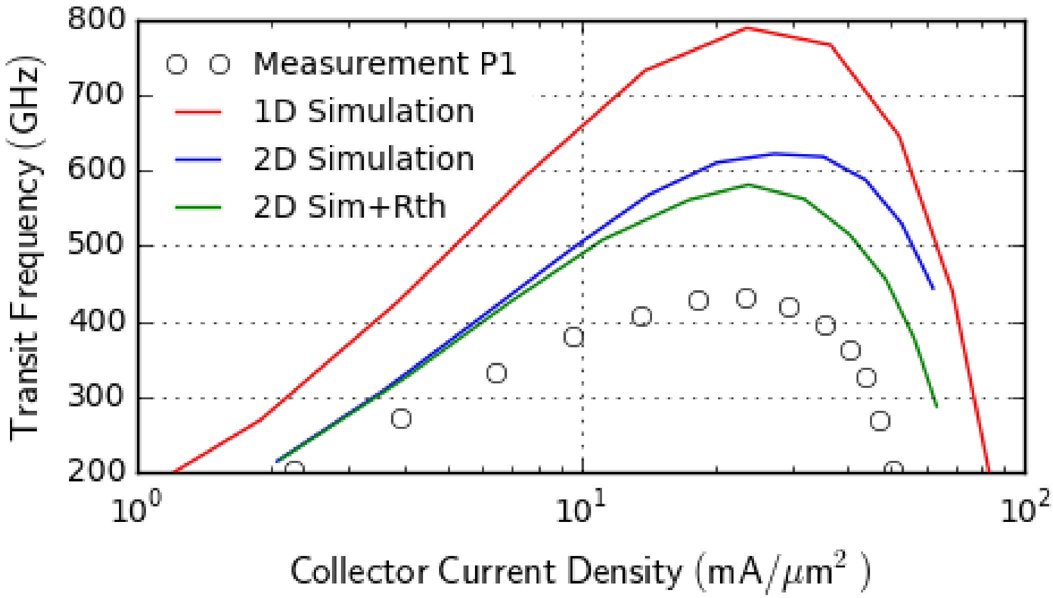
- Hydrodynamic simulation used for qualitative study of impact of profile variations on $f_T$
  - Sentaurus-Device
- Focus on 1D simulations
  - 2D and 3D profiles of real devices hardly accessible
  - Comparison of the performance potential of different vertical profiles

# Simulated $I_C$




- SIMS measurements of doping and Ge profiles used as input
- Simulation overestimates $I_C$ at $V_{BE}$>0.9V due to $R_E$ and $R_C$ components missing in the simulation domain
- Ideality factor $nI_C$ at $V_{BE}$~0.7V overestimated by hydrodynamic (HD) simulations

# Simulated $f_T$



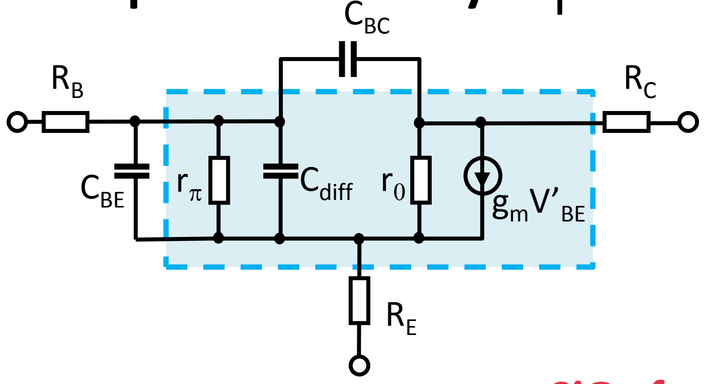

- 1D simulation of $f_T$ based on measured SIMS profiles
- Depletion widths and 2D doping at device edges adjusted to measured capacitances
- Measured $R_{TH}$ used for simulation with self heating
- Full inclusion of $R_E$, $R_C$, and 3D capacitances in simulation domain would decrease simulated $f_T$ further

# Transit Time

- Response of a transistor to AC signals related to modulation of charges inside the transistor

$$\frac{1}{2\pi f_T} = \tau_{EC} = q\int_0^{L_x} \left.\frac{\partial n(x)}{\partial j_C}\right|_{V_{CE}} dx = q\int_0^{L_x} \left.\frac{\partial p(x)}{\partial j_C}\right|_{V_{CE}} dx$$

- For a simplified equivalent circuit $\tau_{EC}$ is often expressed by $\tau_F$ and external parasitics




$$\tau_{EC} = \tau_F + \frac{C_{BE} + C_{BC}}{g_m} + (R_E + R_C)C_{BC}$$

# Regional Contributions to $\tau_{EC}$

- Segmentation into stored minority charges and depletion charges: $$\tau_{EC} = \tau_E + \tau_B + \tau_C + \tau_{EB} + \tau_{BC}$$
  [Van den Biesen, 1986]

- Minority holes in emitter: $$\tau_E = q \int_0^{x_{mE}} \frac{\partial p}{\partial j_C} dx$$

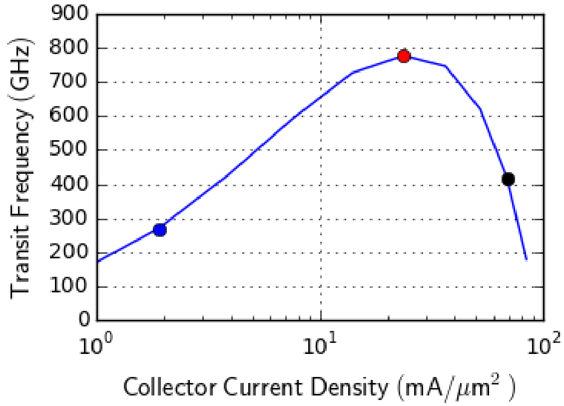
- Minority electrons in base: $$\tau_B = q \int_{x_{mE}}^{x_{mC}} \frac{\partial n}{\partial j_C} dx$$

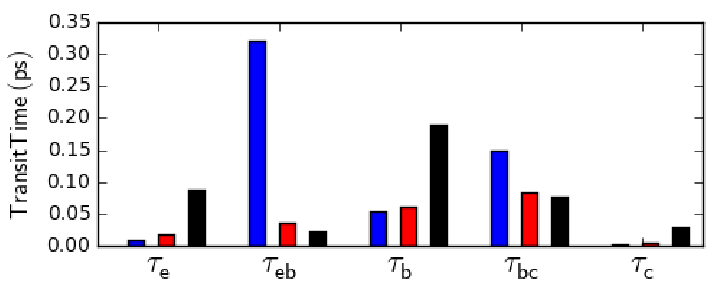
- Minority holes in collector: $$\tau_C = q \int_{x_{mC}}^{L_x} \frac{\partial p}{\partial j_C} dx$$

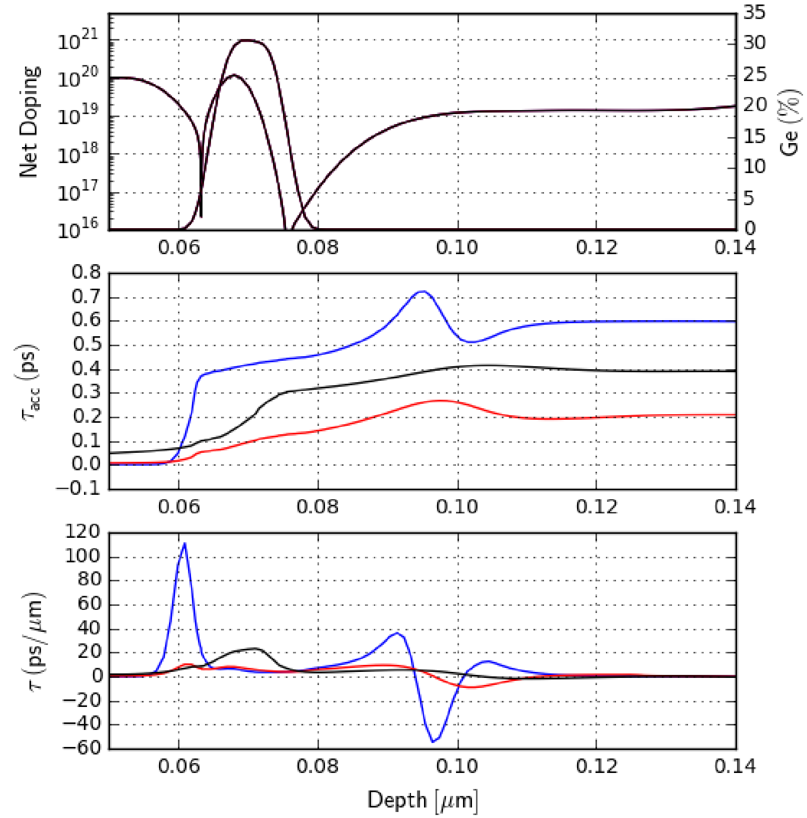
- EB depletion charge : $$\tau_{EB} = q \int_{x_{mE}}^{x_{mC}} \frac{\partial (n-p)}{\partial j_C} dx$$

- BC depletion charge: $$\tau_{BC} = q \int_{x_{mC}}^{L_x} \frac{\partial (n-p)}{\partial j_C} dx$$

# 1D Simulation: $f_T$ and delay times




- Depletion charges dominate $\tau_{EC}$ at low $I_C$
- Electrons accumulation in base dominate $\tau_{EC}$ at high $I_C$

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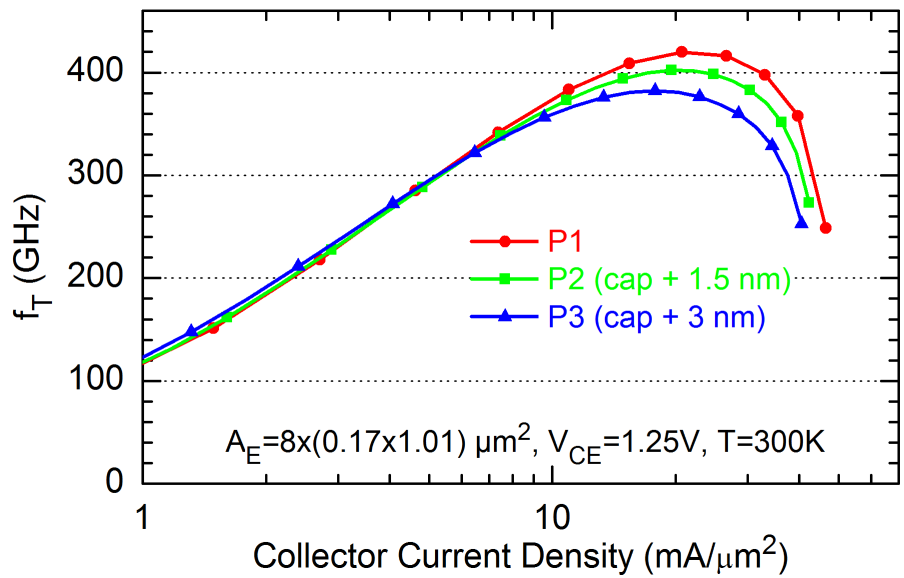
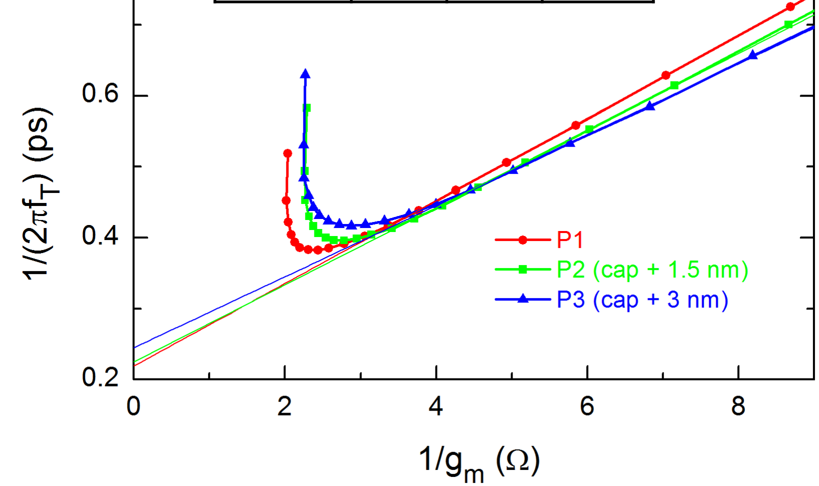
  - Base emitter junction width
  - Collector doping level
  - Ge profile
- Summary

# Experiment: EB junction width

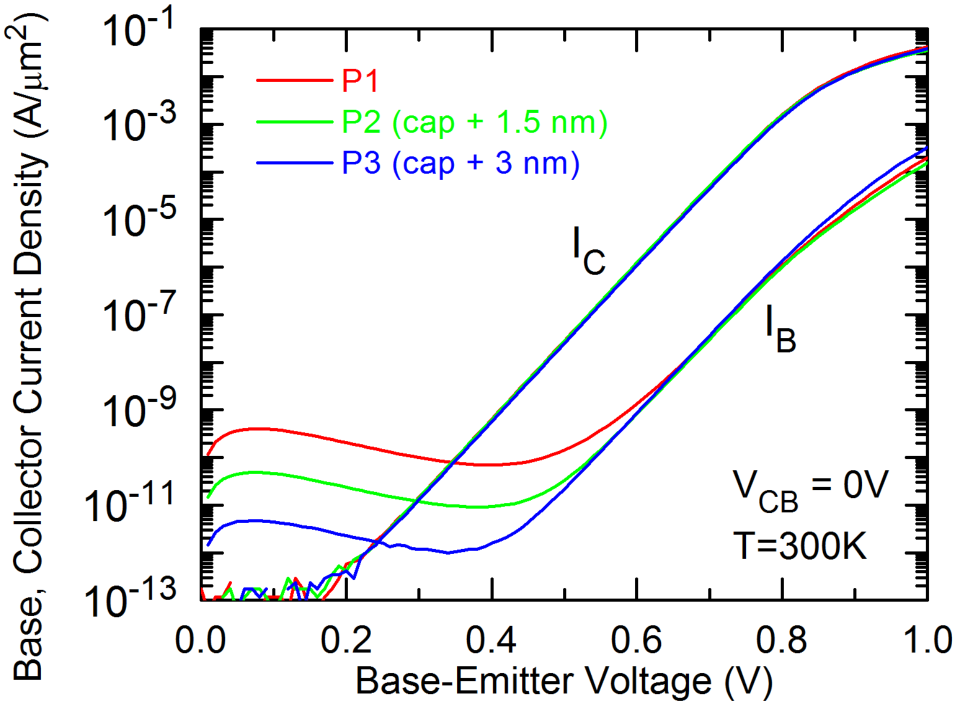



| | P1 | P2 | P3 |
|---|---|---|---|
| $\tau_{EC0}$ (ps) | 0.218 | 0.225 | 0.245 |
| slope (fF) | 58 | 54 | 50 |



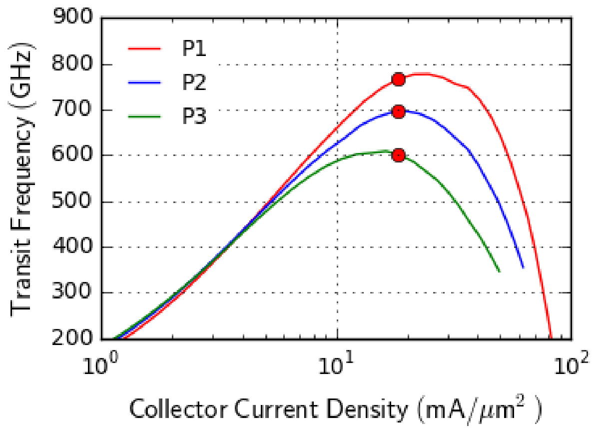

- Measured peak $f_T$ increases with reduced EB junction width (Si cap thickness)
- Thinner cap thickness resulted in reduced $\tau_{EC0}$ and increased depletion capacitance

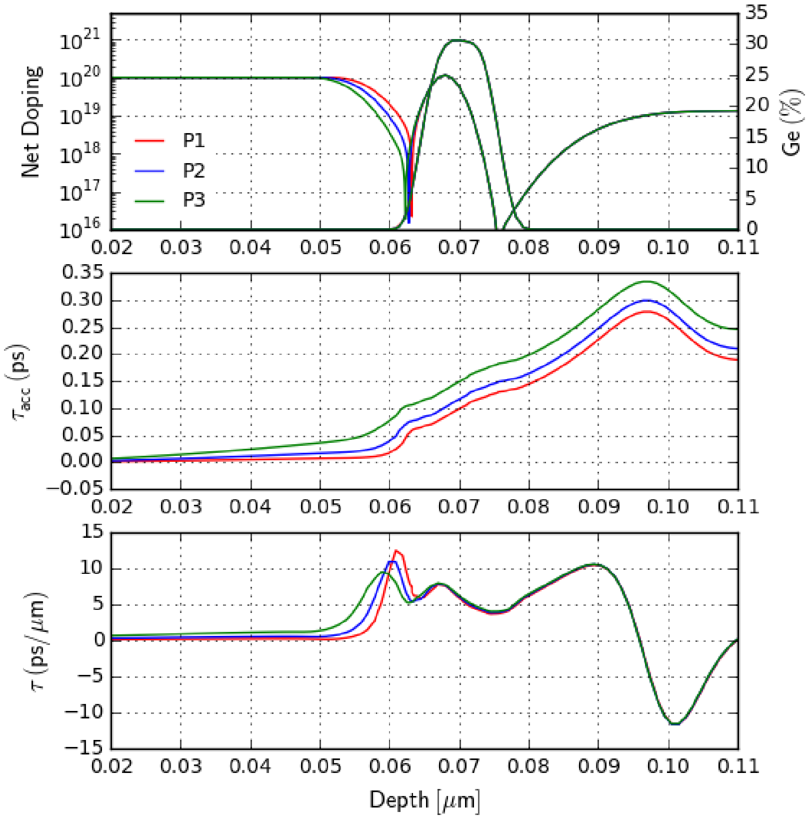
# Gummel Characteristics

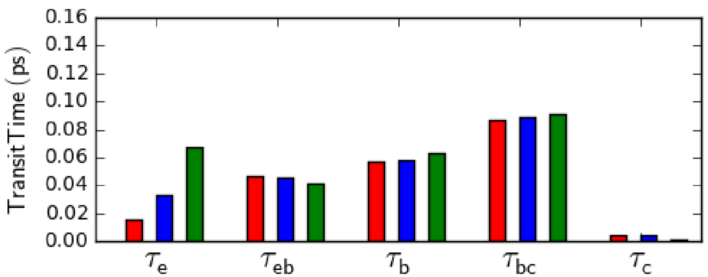



- Enhanced tunneling currents due to reduced EB junction widths result in non-ideal $I_B$ for $V_{BE} < 0.5$ V

# 1D Simulation: EB Junction Width

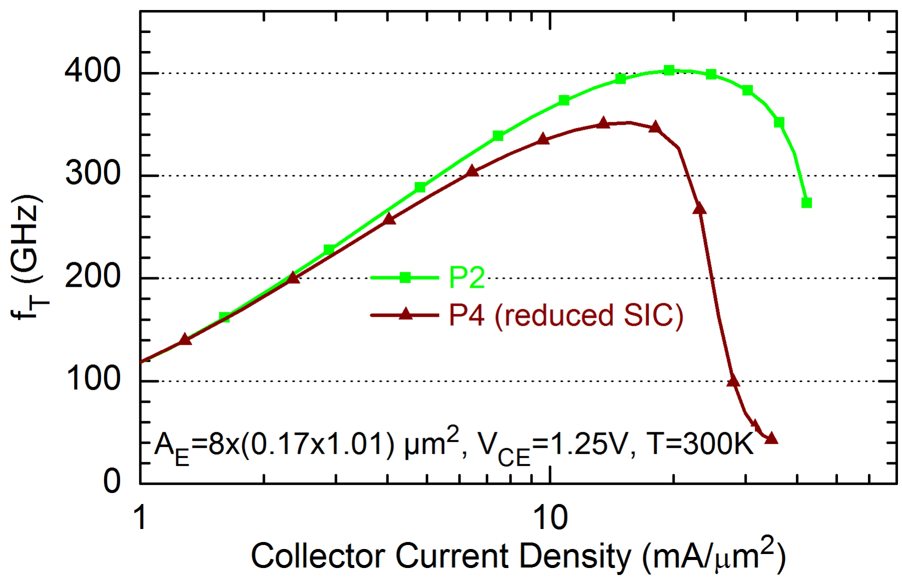


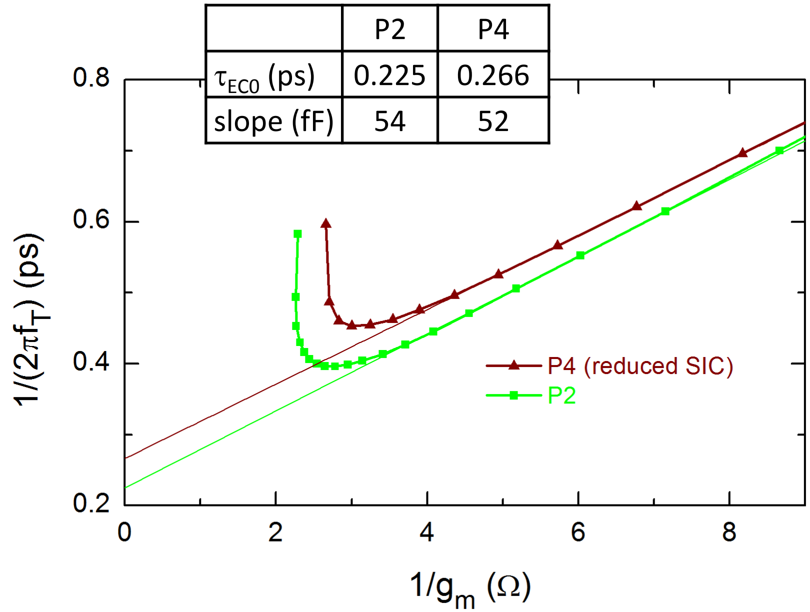




- Thinner EB junction width reduces storage of compensated electron and hole charges ($C_N$) in depletion region and emitter

# Experiment: Collector Doping

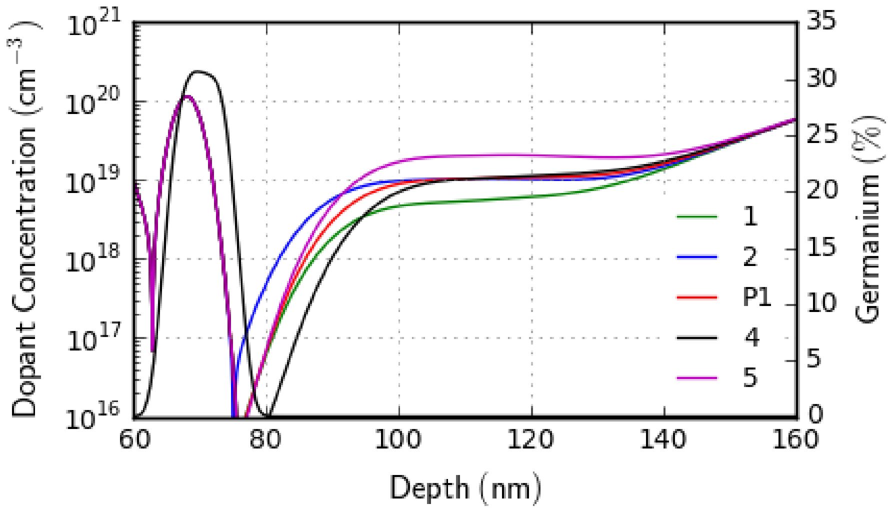


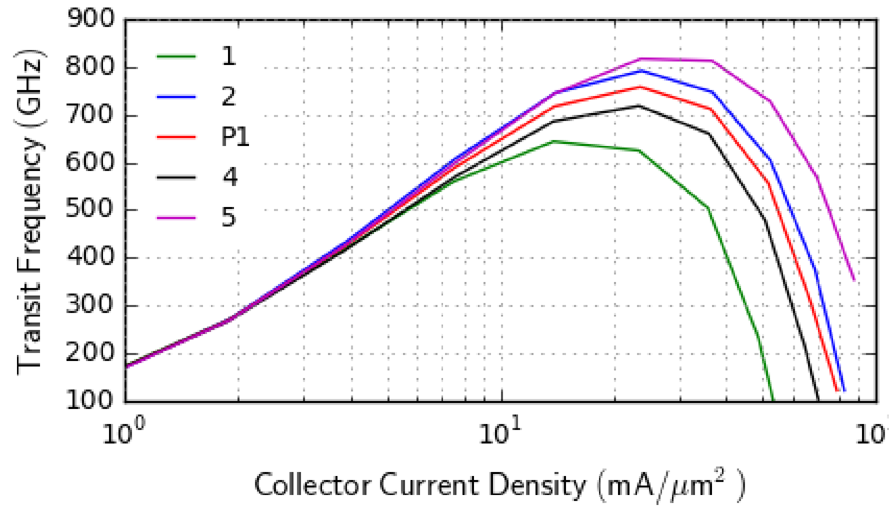




| | P2 | P4 |
|---|---|---|
| $\tau_{EC0}$ (ps) | 0.225 | 0.266 |
| slope (fF) | 54 | 52 |

- Increased doping level in SIC region from ~7E18 cm$^{-3}$ (P4) to ~1.5E19 (P2)
- Higher collector doping shifts peak $f_T$ to higher $j_C$
- Reduced $\tau_{EC0}$ due to reduced collector transit time

# 1D Simulation: Collector Doping

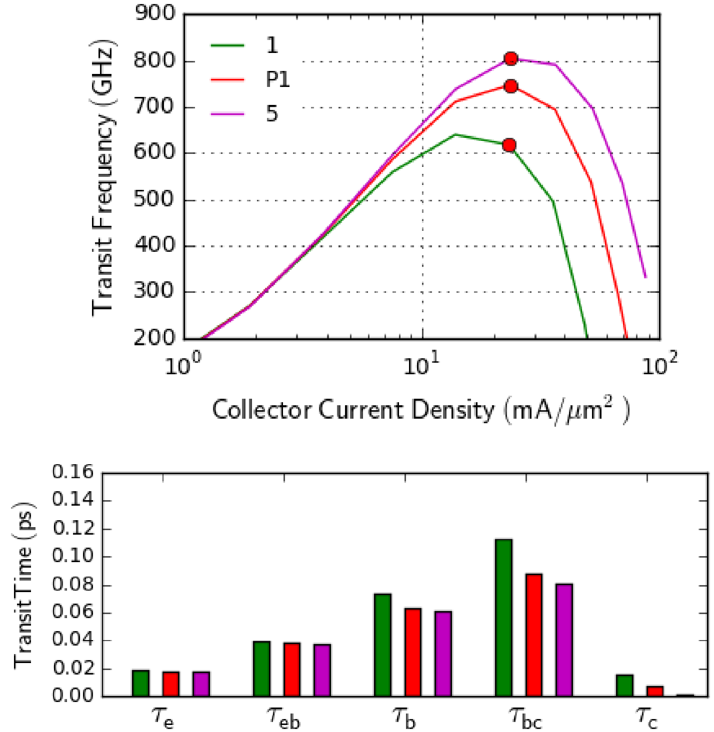


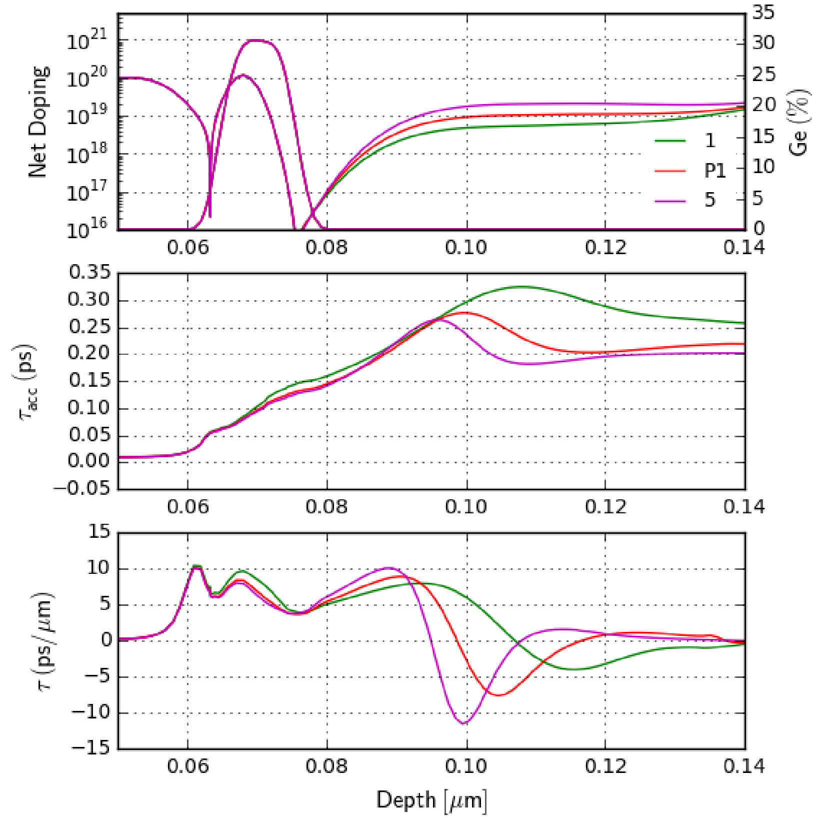




1. 50% lower SIC doping level
2. SIC shifted 4 nm towards base
3. Reference profile P1
4. SIC shifted 4 nm towards collector
5. 2X higher SIC doping

➔ Peak $f_T$ most sensitive to variation of doping level at the edge of the depletion region

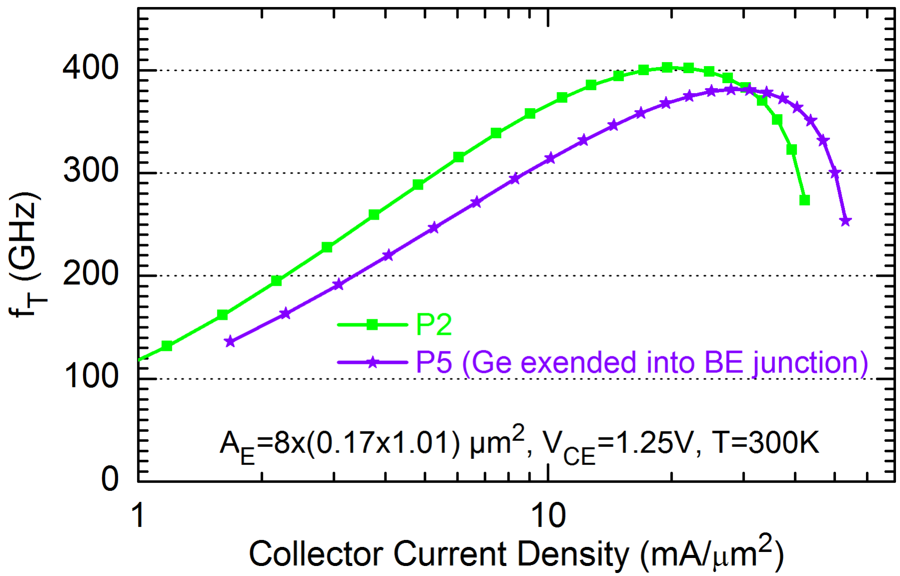
# 1D Simulation: SIC Doping Level

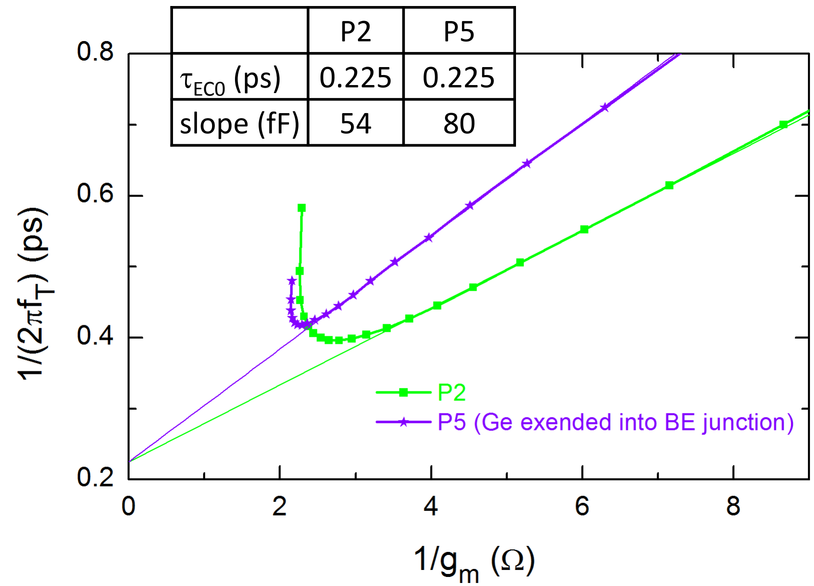



- Higher collector doping shifts degradation of $f_T$ to high $j_C$
- Reduced charge storage in thinner BC depletion region

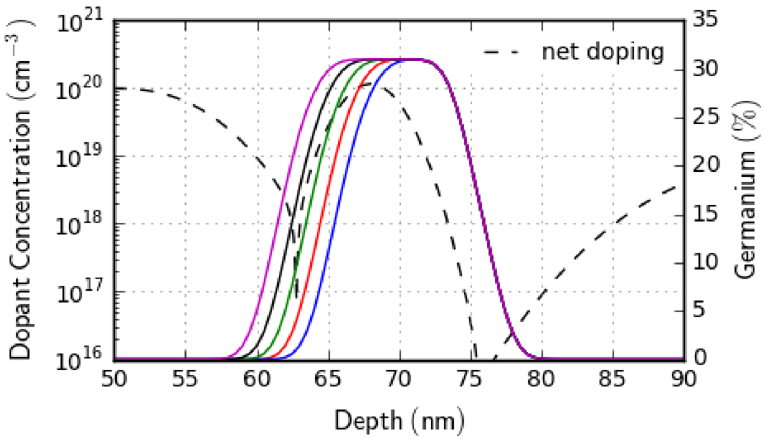
# Experiment: Ge Profile Split

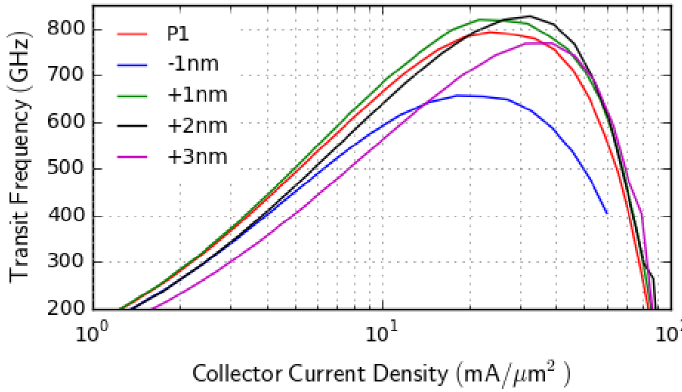


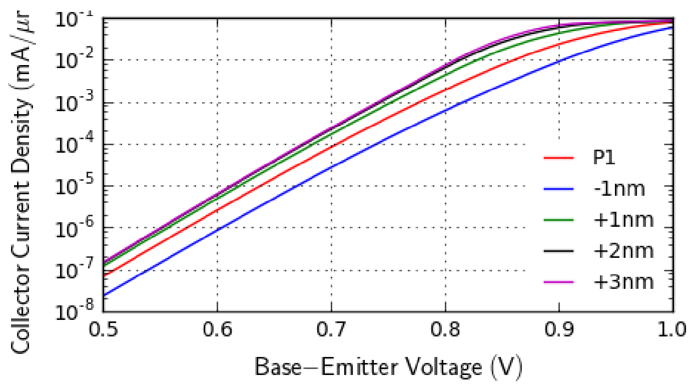




- Ge profile P5 extends about 3 nm deeper into BE junction than Ge profile P2
- Profile P5 requires higher $j_C$ for the same $f_T$
- Enhanced slope of $1/f_T$ vs. $1/g_m$ for P5 (higher $C_{BE}$+$C_{BC}$)

# 1D Simulation: Various Ge Profiles

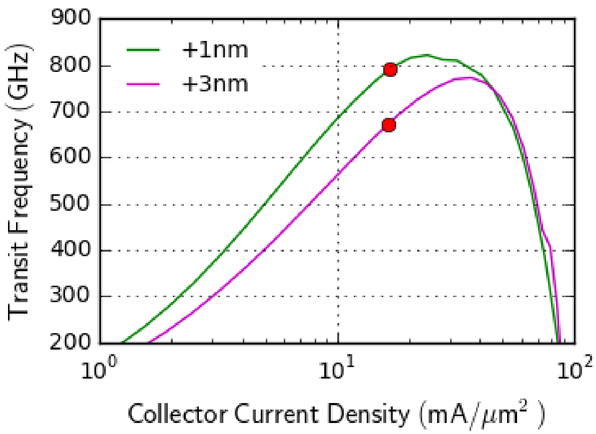


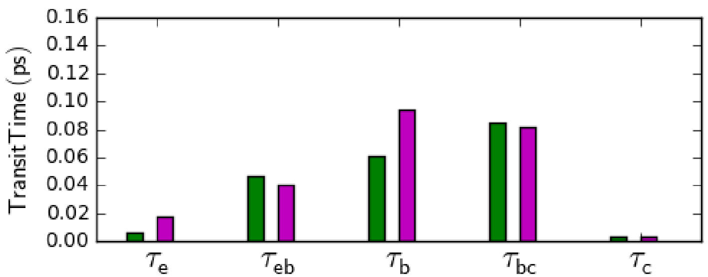



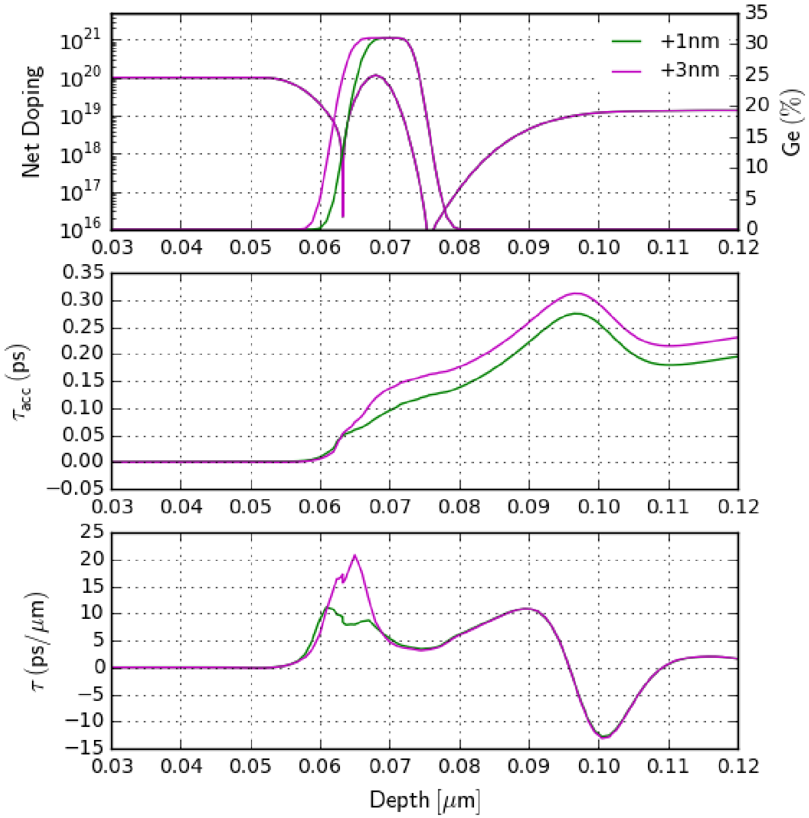




- Onset of Ge gradient shifted in steps of 1 nm towards emitter
  - Similar $f_T$ for profiles P1 and +1nm shift of Ge towards emitter
  - Degradation of $f_T$ for further shift of Ge flank towards emitter or base

# 1D Simulation: Various Ge Profiles




- Extension of Ge into BE depletion region results in enhanced electron and hole storage there ($C_N$↑)
  - Reduction of $f_T$ at all current levels

# Conclusions

- Peak $f_T/f_{max}$ of 430 GHz/315 GHz realized for HBTs with optimized vertical doping profile
  - Further increase of $f_{max}$ expected from lateral scaling
- About 5 nm wide B profiles with $R_{sbi}$ of 2.7 k$\Omega$ measured at end of fabrication process
- Charging times $\tau_E$ and $\tau_{EB}$ were significantly reduced at cost of higher tunneling currents at low $V_{BE}$
- Higher collector doping ($N_C$>1.5E19 $cm^{-3}$) at edge of BC depletion region could reduce charging time $\tau_C$ further
- Reduction of parasitic capacitances at device perimeter and restriction of self heating essential for highest $f_T$