Reliability of SiGe-THz devices
Grazia Sasso
Outline

- SiGe HBTs in BiCMOS technology
- Reliability and SOA with scaling and RF
  - DOTSEVEN project
  - SiGe HBTs development framework
  - Electrical instability phenomena
  - Thermal resistance and self-heating
- Hot-carrier phenomena
  - Reverse emitter-base stress
  - Mixed mode stress
  - Stress at the SOA edge
Outline

- **Reverse emitter-base stress**
  - Methods and techniques
  - Evaluation and modeling of results
  - Recovery

- **Mixed mode stress**
  - Evaluation of results, modeling and TCAD
  - Recovery

- **Stress at the SOA edge**
  - Evaluation and modeling of results
  - TCAD and SHE simulations
SiGe HBTs in BiCMOS technology

RF and mmWave applications
SiGe vs. III-V (compound)

- BiCMOS technology and SoC
- Scaling and bandgap engineering
- Low cost

European research founding: dotfive dot seven
Performance and reliability

FoM: \( f_T, f_{\text{MAX}}, BV_{\text{CEO}}, BV_{\text{CBO}}, \beta \)

Scaling and trade-offs

\[
 f_T \approx \frac{1}{2\pi \left( \tau_{TB} + \frac{V_T}{I_C} C_{jC} \right)} 
\]

\[
 f_{\text{MAX}} \approx \sqrt{\frac{f_T}{8\pi R_B C_{CB}}} 
\]

\[
 f_T \cdot BV_{\text{CBO}} = k \left( N_C \right) 
\]

\[
 BV_{\text{CEO}} = \frac{BV_{\text{CBO}}}{\beta^{1/n}}, \quad n = 3 \div 6 
\]
Performance and reliability

\[ f_T \approx \frac{1}{2\pi \left( \tau_{TB} + \frac{V_T}{I_C} C_{jC} \right)} \]

\[ f_{MAX} \approx \sqrt{\frac{f_T}{8\pi R_B C_{CB}}} \]

\[ f_T \cdot BV_{CBO} = k \left( N_C \right) \]

\[ BV_{CEO} = BV_{CBO} / \beta^{1/n} \]

Performance improvement reduces safe-operating-area (SOA) due to electrical and thermal issues.

Performance improvement
Scaling improvement
High doping
Impact ionization
Self-heating
Hot-carrier

Higher electric field
Higher current density
Higher thermal resistance
DOTSEVEN european project: motivation

- The European project DOTSEVEN supports the development of SiGe HBTs with $f_{\text{MAX}}$ of 700 GHz
- Highly-scaled and doped architectures are explored and aggressive operating conditions are applied
- Higher electric fields and current densities may cause performance degradation and might jeopardize speed and long-time reliability
- Device reliability is an increasingly important topic in circuit and system design

http://www.dotseven.eu.
Device development framework

**SIMULATION**  
**CHARACTERIZATION**  
**MODELING**

Calibrated TCAD:
- predicts device characteristics of anticipated wafer fabrication technology
- explores the physics of scaled devices and investigate new device architectures

- Reduce time-to-market and cost
- Manage performance vs. reliability constraints
SiGe HBT development framework

- Calibration of hydrodynamic (HD) models for TCAD
- Development of transport parameters for HD simulation in TCAD
- DC, pulsed and RF on wafer experimental measurements
- Reliability and SOA reduction with scaling and RF improvements

SIMULATION  CHARACTERIZATION  MODELING
Reliability and SOA with scaling and RF improvements

- Electrical instability phenomena
  - Impact ionization
  - Tunneling
  - Pinch-in
- Thermal resistance and self-heating
- Hot-carrier phenomena

SIMULATION  CHARACTERIZATION  MODELING
Electrical instability phenomena - breakdown

Impact ionization
Avalanche breakdown

Tunneling
Zener breakdown
SiGe HBTs electrical breakdown measurements

**$\text{BV}_{\text{CBO}}$, Open emitter**  
Collector-base breakdown voltage

**$\text{BV}_{\text{CEO}}$, Open base**  
Collector-emitter breakdown voltage

Impact ionization model calibration (*Okuto, Van Overstraeten* models, etc.)

**$\text{BV}_{\text{CEB}}$, Open collector**  
Emitter-base breakdown voltage

Tunneling models calibration supported by low temperature measurements.
Thermal resistance and self-heating

Impact of scaling on the thermal behavior

Thermal resistance extraction

\[ R_{TH} = \frac{\Delta T}{P_D} \implies T_J = R_{TH} \cdot P_D + T_0 \]

- #2 is slightly laterally/vertically scaled compared to #1
- #3 devices aggressively lateral scaled with respect to #2
Thermal resistance and self-heating

Impact of scaling on the thermal behavior

Thermal resistance extraction

\[ R_{TH} = \frac{\Delta T}{P_D} \Rightarrow T_J = R_{TH} \cdot P_D + T_0 \]

- #2 is slightly laterally/vertically scaled compared to #1
- #3 devices aggressively lateral scaled with respect to #2
Hot-carrier damage standard stress techniques

- Reverse emitter-base stress (high $V_{EB}$)
- Forward stress (high $J_C$ and $T$)
- Mixed-mode stress (high $J_E$ and high $V_{CB}$)

Studied (experiments and TCAD) for HBTs fabricated by:

[Infineon logo]
Hot-carrier damage: trap formation

- Very high localized electrical fields

- Generated hot carriers:
  1. Damage the Si/SiO$_2$ interface $\rightarrow$ interface traps
  2. Surmount the Si/SiO$_2$ barrier $\rightarrow$ oxide traps/charges
Hot-carrier damage

Aging mechanisms are related to impact ionization and tunneling phenomena.

Degradation worsen with RF performance improvement.
Outline

- Reverse emitter-base stress
  - Methods and techniques
  - Evaluation and modeling of results
  - Recovery experiments

- Mixed mode stress
  - Evaluation of results, modeling and TCAD
  - Recovery experiments

- Stress at the SOA edge
  - Evaluation and modeling of results
  - TCAD and SHE simulations
Reverse emitter-base stress methods

- Open collector (OC)
  \( V_{EB} < 0, \ OC \ or \ V_{BC} = 0 \) Hot holes
- Forward collector (FC)
  \( V_{EB} < 0, \ V_{BC} > 0 \) Hot electrons and hot holes

Standard methods are not exploitable when AC measurements are to be performed
Proposed technique for EB stress

\[ V_{EB} < 0, \ V_{CE} = 0 \quad (i.e., \ V_{EB} = V_{CB} > 0) \]

- \( I_C \) is negligible during stress
- An uncontrolled forward biasing of the SC junction is avoided
- Monitoring of the RF performance during stress interruptions is allowed without any mechanical movement in the experimental setup
Verification of the stress technique

$9 \times (0.13 \times 0.93)$

- $V_{EB\text{-stress}} = 3.5 \text{ V}$, $V_{CE} = 0 \text{ V} \leftrightarrow V_{CB} = 3.5 \text{ V}$
  - $I_C = 7 \mu\text{A}$, $I_B = 120 \mu\text{A}$
  - $I_E = -(I_B + I_C) \approx I_{stress}$

$9 \times (0.15 \times 0.93)$

- $V_{EB\text{-stress}} = 3.5 \text{ V}$, $V_{CE} = -1.5 \text{ V} \leftrightarrow V_{CB} = 2.0 \text{ V}$
  - $I_C = -68 \text{ mA}$, $I_B = -2 \text{ mA}$
  - $I_E = -(I_B + I_C) - I_S \neq I_{stress}$
Verification of the stress technique

The stress current is unchanged and the slight discrepancy can be ascribed to the small difference in the aspect ratio.
Reverse EB stress experiments – 130 nm SiGe:C

**Infineon Technologies (IFAG) devices:**
- \( f_{\text{MAX}}/f_T = 380/240 \text{ GHz} \)
- \( n = 1 \div 9 \), several combinations of \( W_E/L_E \)
- BEC & BEBC configuration
- RF layout, GSG pads configuration, \( T_A = 300 \text{ K} \)

**Innovation for high performance microelectronics (IHP) devices:**
- \( f_{\text{MAX}}/f_T = 300/240 \text{ GHz} \)
- \( n = 4 \), several combinations of \( W_E/L_E \)
- CBE configuration
- RF layout, GSG pads configuration, \( T_A = 300 \text{ K} \)
- Statistics: 3 dies
Technology under test, IHP

<table>
<thead>
<tr>
<th>$A_E=Nx(W_E\times L_E)$ [$\mu m^2$]</th>
<th>Configuration</th>
<th>$A_E$ [$\mu m^2$]</th>
<th>$P_E$ [$\mu m$]</th>
</tr>
</thead>
<tbody>
<tr>
<td>4x(0.13x0.88)</td>
<td>CBE</td>
<td>0.4576</td>
<td>8.08</td>
</tr>
<tr>
<td>4x(0.16x0.88)</td>
<td>CBE</td>
<td>0.5632</td>
<td>8.32</td>
</tr>
<tr>
<td>4x(0.19x0.88)</td>
<td>CBE</td>
<td>0.6688</td>
<td>8.56</td>
</tr>
</tbody>
</table>

- $f_{\text{MAX}}/f_T$=300/240 GHz
- CBE configuration
- $n=4$, $A_E=n\cdot(W_E\cdot L_E)$, $P_E=2\cdot n\cdot(W_E+L_E)$
- RF layout, GSG pads configuration, $T_A$=300 K
- Statistics: 3 dies
Stress conditions, IHP

\[ V_{\text{EB-stress}} = 3.75 \div 4.50 \text{ V} \]
\[ V_{\text{CE}} = 0, \quad V_C = V_E = 0 \]
Degradation results: Gummel plot

- $I_B$ increases, $I_C$ is not affected $\rightarrow \beta_F = \frac{I_C}{I_B}$ decreases
- Degradation strongly shrinks in the high-bias region

**Gummel plot**

- Before stress ($t=0s$)
- After stress ($t=1000s$)

**Parameters**
- $V_{EB-stress} = 3.75 \text{ V}$
- $A_E = 4 \times (0.16 \times 0.88) \mu\text{m}^2$
Degradation results: Gummel plot

- $I_B$ increases, $I_C$ is not affected $\rightarrow \beta_F = \frac{I_C}{I_B}$ decreases
- Degradation strongly shrinks in the high-bias region

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Before stress ($t=0\,s$)

After stress ($t=1000\,s$)

$V_{EB\text{-stress}} = 3.75\,V$

$A_E = 4 \times (0.16 \times 0.88) \, \mu m^2$
Traps formation

- Very high localized electrical fields
- Generated hot carriers:
  - Damage the Si/SiO$_2$ interface → interface traps
  - Surmount the Si/SiO$_2$ barrier → oxide traps/charges
Degradation results: $\Delta I_B(t) = I_B(t) - I_B(0)$ vs. $t$

Degradation kinetic depends on the voltage stress…
Degradation results: $\Delta I_B(t) = I_B(t) - I_B(0)$ vs. $t$

1. **Low**: Power law density increase with stress time
2. **High**: Very fast degradation only in the first few seconds
3. **Very-high**: common saturation trend
Degradation results: $\Delta \beta_{F-MAX}$ vs. $t$

- $V_{EB-stress} = 4.00$ V
- $V_{EB-stress} = 4.50$ V
- $V_{CB} = 0.0$ V

Decrease of maximum current gain [%] vs. Stress time $t$ [s]
- $A_E = 4 \times (0.13 \times 0.88) \, \mu m^2$
- $A_E = 4 \times (0.16 \times 0.88) \, \mu m^2$
- $A_E = 4 \times (0.19 \times 0.88) \, \mu m^2$
Degradation results: $\Delta \beta_{F-\text{MAX}}$ vs. $t$

- For a given emitter layout, maximum gain degradation follows the same trends of $\Delta I_B(t)$
- Performance of the smallest device degrades more rapidly $\rightarrow$ increasing of $P_E/A_E$
Degradation results: $\Delta I_B(t)/P_E$ vs. $t$
Degradation results: $\Delta I_B(t)/P_E$ vs. $t$

- Damage is mostly located around the emitter perimeter, adjacent to the space charge region between the emitter and the base.
Stress effects on the AC performance

- Different samples, fast measurements evaluation
- Junction capacitances, AC current gain $H_{21}$, $f_T$, and $f_{\text{MAX}}$

![Graph](image-url)
Stress effects on the AC performance

- No significant variations have been detected for RF parameters (exception $H_{21}$)
## Technology under test and stress conditions, IFAG

<table>
<thead>
<tr>
<th>$A_E = N x (W_E x L_E) \ [\mu m^2]$</th>
<th>Configuration</th>
<th>$V_{EB\text{-stress}} [V]$</th>
<th>$V_{CB} [V]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>9x(0.13x0.93)</td>
<td>BEC</td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>9x(0.15x0.93)</td>
<td>BEC</td>
<td>3.5</td>
<td>2.0</td>
</tr>
<tr>
<td>3x(0.13x2.73)</td>
<td>BEC</td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>3x(0.13x2.73)</td>
<td>BEBC</td>
<td>3.5</td>
<td>3.5</td>
</tr>
<tr>
<td>1x(0.13x9.93)</td>
<td>BEC</td>
<td>2.5</td>
<td>2.5</td>
</tr>
<tr>
<td>1x(0.23x9.93)</td>
<td>BEC</td>
<td>3.0</td>
<td>3.0</td>
</tr>
</tbody>
</table>

- $f_{\text{MAX}}/f_T = 380/240 \text{ GHz}$
- $n=1 \div 9$, several combinations of $W_E/L_E$
- BEC & BEBC configuration
Degradation results: $\Delta I_B(t)$ vs. $t$

$\Delta I_B(t) = I_B(t) - I_B(0)$

$= I_{SR}(t) \cdot \exp\left[\frac{q \cdot V_{BE}}{n_R(t) \cdot k \cdot T}\right]$
Degradation results: $n_R$ vs. $t$

$n_R$ slightly exceeds 2 and mildly decreases with stress time.

SRH recombination mechanism via midgap traps, but...
Degradation results: $n_R$ vs. $V_{BE}$

$$\Delta I_B(t) = I_B(t) - I_B(0) = I_{SR}(t) \cdot \exp \left[ \frac{q \cdot V_{BE}}{n_R(t) \cdot k \cdot T} \right]$$

... tunneling at very low injection levels (TAT)
Model for base current degradation

\[ \Delta I_B(t) = P_E \cdot I_{SRP} \left( \frac{t}{t_0} \right)^\alpha \cdot \exp \left( \frac{q \cdot V_{BE}}{n_R \cdot k \cdot T} \right) \]

\[ n_R = f(V_{EB\text{-stress}}, V_{BE}) \text{ mean value over various devices} \]
Model for base current degradation

\[ \Delta I_B (t) = P_E \cdot I_{SRP} \left( \frac{t}{t_0} \right)^\alpha \cdot \exp \left( \frac{q \cdot V_{BE}}{n_R \cdot k \cdot T} \right) \]

\[ I_{SRP} = I_{SRP0} \cdot \exp \left( \frac{q \cdot \Delta \Psi_S}{k \cdot T} \right) \]

![Graph showing the model for base current degradation](image-url)
Model for base current degradation

\[ I_{SRP} = I_{SRP0} \cdot \exp \left( \frac{q \cdot \Delta \Psi_S}{k \cdot T} \right) \]

\[ \Delta \Psi_S = \frac{V_{EB-\text{stress}}}{5} \]

\[ I_{SRP0} = A \cdot \exp \left( -\frac{q \cdot V_{BE}}{2 \cdot k \cdot T} \right) \]

\( \Delta \Psi_S \): variation of the surface potential induced by the charge trapped in the oxide.
Model vs. experimental results (1)

3x(0.23x2.73) µm²

$V_{EB}$-stress = 3.5 V

Total $t$ = 1000s
Model for base current degradation

\[ \Delta I_B (t) = P_E \cdot I_{SRP} \left( \frac{t}{t_0} \right)^\alpha \cdot \exp \left( \frac{q \cdot V_{BE}}{n_R \cdot k \cdot T} \right) \]

\[ I_{SRP} = I_{SRP0} \cdot \exp \left( \frac{q \cdot \Delta \Psi_S}{k \cdot T} \right) \]

\[ \Delta \Psi_S = \frac{V_{EB \text{--stress}}}{5} , \quad I_{SRP0} = A \cdot \exp \left( -\frac{q \cdot V_{BE}}{2 \cdot k \cdot T} \right) \]

Model includes the degradation due to generation of interface traps (1) and includes the generation of charge in the oxide (2) for all the geometries.

Model provides a complete description for \( \Delta I_B \) and helps understand the physical background.
Model for base current degradation

\[ \Delta I_B(t) = P_E \cdot I_{SRP} \left( \frac{t}{t_0} \right) \alpha \cdot \exp \left( \frac{q \cdot V_{BE}}{n_R \cdot k \cdot T} \right) \]

\[ I_{SRP} = I_{SRP0} \cdot \exp \left( \frac{q \cdot \Delta \Psi_S}{k \cdot T} \right) \]

\[ \Delta \Psi_S = \frac{V_{EB-stress}}{5}, \quad I_{SRP0} = A \cdot \exp \left( -\frac{q \cdot V_{BE}}{2 \cdot k \cdot T} \right) \]

Generation of interface traps

Generation of charge in the oxide

Low stress bias

The creation of interface traps dominates
Model for base current degradation

\[ \Delta I_B(t) = P_E \cdot I_{SRP} \left( \frac{t}{t_0} \right)^\alpha \cdot \exp \left( \frac{q \cdot V_{BE}}{n_R \cdot k \cdot T} \right) \]

\[ I_{SRP} = I_{SRP0} \cdot \exp \left( \frac{q \cdot \Delta \Psi_S}{k \cdot T} \right) \]

\[ \Delta \Psi_S = \frac{V_{EB-stress}}{5}, \quad I_{SRP0} = A \cdot \exp \left( -\frac{q \cdot V_{BE}}{2 \cdot k \cdot T} \right) \]

**Generation of interface traps**

**Generation of charge in the oxide**

High stress bias

The creation of charge in the oxide prevails and the trap generation rate is lower.

\[ V_{BE} = 0.5 \text{ V} \]
\[ V_{BE} = 0.6 \text{ V} \]
\[ V_{BE} = 0.7 \text{ V} \]
\[ V_{BE} = 0.8 \text{ V} \]
Model vs. experiments: summary

- Results span over a longer duration for milder stress
- Model is compared to experiments over aspect ratios, $V_{EB}$-stress, and $V_{BE}$

The unified model can be used to describe and predict base current degradation over stress time including all the involved variables (e.g., in compact models for circuit simulation and aging function extraction)
Recovery mechanisms after stress

- Natural recovery
- Forward bias recovery
- Thermal recovery

Physical background provides insight into the stress mechanisms
Natural recovery vs. geometry

- Semi-logarithmic time dependence
- Emitter layout does not affect the shape/slope

Detrapping of oxide trapped carriers and not annihilation of interface states
Natural recovery vs. stress condition

- Applied stress affects the slope
- The density of hot holes is expected to exceed the density of hot electrons at low stress voltages
- The decrease in positive (negative) oxide charge produces decrease (increase) of the positive surface potential $\Delta V_S$

$$I_B(t) = I_{BO} \exp\left[\frac{q\Delta V_S(t)}{kT}\right]$$
Thermal recovery, introduction

- **Standard procedure:**
  - $T_{\text{annealing}} \neq T_{\text{measurement}} \rightarrow \text{low accuracy}$
  - $T_{\text{annealing}} = T_{\text{measurement}} \rightarrow \text{strong restrictions}$

- **Proposed approach:**
  - ✓ Self-heating as a means to accurately study the thermal recovery, its activation and rate
Thermal recovery by self-heating

Controlled self-heating can be applied to reliably evaluate thermal and kinetics properties of recovery:

\[ T_A=300 \, \text{K}, \, R_{\text{TH}} \, \text{known} \rightarrow T_J = T_A + R_{\text{TH}} \cdot P_D \]

- Annealing steps of given duration and temperature are obtained by setting \( P_D \)
- At preselected times, the annealing experiments are interrupted and the recovery rate is evaluated by switching the applied voltage bias
- Controlled self-heating at higher dissipated power allows increasing recovery temperature of one’s choice
- Recovery effects vs. \( P_D \), cumulated energy, cumulated heating time, junction-to-ambient temperature increase.
Output characteristics of a fresh sample

Each bias point was applied for 10s and alternated to the measurement of the Gummel-plot at $V_{CB}=0$

$P_D = V_{CE} \cdot I_C + V_{BE} \cdot I_B$

$T_J = T_A + R_{TH} \cdot P_D$

Collector-emitter voltage $V_{CE}$ [V]

Junction temperature rise $\Delta T_J$ [K]

V$_{BE}$ = 0.92 V

Dissipated power $P_D$ [mW]

$A_E = 4 \times (0.16 \times 0.88) \, \mu$m$^2$

$R_{TH} = 5 \times 10^3$ K/W
Self-heating recovery results vs. stress voltage

- $f_I(t)$ increases with the heating time
- Weaker recovery when the stress voltage was stronger

$$f_I(t) = \frac{I_B(t)}{I_B(0)}$$

Unannealed fraction $f_I(t)$

Heating time $t$ [s]

$V_{EB-stress} = 4.00$ V

$V_{EB-stress} = 4.25$ V

$V_{EB-stress} = 4.50$ V

$A_E = 4 \times (0.16 \times 0.88) \, \mu m^2$
Self-heating recovery results vs. stress voltage

\[ f_I(t) = \frac{I_B(t)}{I_B(0)} = \exp\left(-\frac{t}{\tau}\right) \]

Low temperature → detrapping of carriers in the oxide
High temperature → interface trap density passivation
Annealing rate not proportional to the trap density.
Modulation of the potential distribution due to trapped charges still occurs.
Self-heating recovery results vs. geometry

1. Higher rate for smallest device; reduction as the temperature increases
2. The largest device is the fastest to recover; increase with temperature
Self-heating recovery results

Constant self-heating and thermal annealing

\[ 1 \text{ h (ΔT=200 C)} + 8 \text{ h (T_A=125 C)} \rightarrow T_J \approx 300 \text{ C} \]

I_B % recovery of HBT #2 @ \( V_{BE}=0.5 \text{ V} \) and \( V_{BC}=0.0 \text{ V} \)

<table>
<thead>
<tr>
<th>HBT #2</th>
<th>SH (180s)</th>
<th>SH+T (1+8 h)</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.00</td>
<td>37%</td>
<td>43%</td>
</tr>
<tr>
<td>4.25</td>
<td>25%</td>
<td>34%</td>
</tr>
<tr>
<td>4.50</td>
<td>21%</td>
<td>42%</td>
</tr>
</tbody>
</table>

Recovery is faster for the strongly stressed devices

Annihilation of interface traps finally prevails
Outline

- Reverse emitter-base stress
  - Methods and techniques
  - Evaluation and modeling of results
  - Recovery experiments

- Mixed mode stress
  - Evaluation of results, modeling and TCAD
  - Recovery experiments

- Stress at the SOA edge
  - Evaluation and modeling of results
  - TCAD and SHE simulations
Mixed-mode stressed devices

<table>
<thead>
<tr>
<th></th>
<th>$A_E = W_E \times L_E$ [(\mu m^2)]</th>
<th>$f_{\text{MAX}}/f_T$ [GHz]</th>
<th>$BV_{\text{CEO}}$ [V]</th>
<th>$BV_{\text{CBO}}$ [V]</th>
<th>$BV_{\text{EBO}}$ [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>HS HBT</td>
<td>0.16x0.52</td>
<td>300/250</td>
<td>1.7</td>
<td>5</td>
<td>1.8</td>
</tr>
<tr>
<td>HV HBT</td>
<td>0.22x1.04</td>
<td>120/45</td>
<td>3.7</td>
<td>15</td>
<td>1.9</td>
</tr>
</tbody>
</table>
Mixed-mode stress and instability

Mixed-mode stress (high $J_E$ and high $V_{CB}$)

- HF
- HV
- Instability
- MM stress
- Pinch-in
Mixed-mode stress results

\[ N_{it}(t) \sim (D \cdot t_{\text{stress}})^\alpha \]

\[ \Delta I_B \propto (I_E \cdot t_{\text{stress}})^{0.5} \]
Mixed-mode recovery results

\[ T_{\text{amb}} = 125^\circ \text{C} \]

(a) Base Current Change \( \Delta I_B \) vs. Anneal Time [h]

(b) Current Gain \( \beta \) vs. \( V_{\text{CB, stress}} \) [V]

- Pre stress
- Post anneal
- Post stress
Mixed-mode stress and TCAD
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Stress experiments at the SOA edge

- Collector current $I_C$ [A]
- Collector-emitter voltage $V_{CE}$ [V]

Excess base current $\Delta I_B(t)$

- $P_1$: $V_{CE}=1$ V, $J_C=10$ mA/$\mu$m$^2$
- $P_2$: $V_{CE}=2$ V, $J_C=5$ mA/$\mu$m$^2$
- $P_3$: $V_{CE}=3$ V, $J_C=1$ mA/$\mu$m$^2$

Stress time $t$ [h]

$V_{BE}=0.65$ V, $V_{CB}=0$ V
TCAD simulation of the aging at the SOA edge

Simulation of the aging dynamics adding trap density at the EB junction/EB spacer interface over stress time in the TCAD.

\[ N_T(t) = N_{T, \text{final}} \left( 1 - \left( 1 - \frac{N_{T, \text{initial}}}{N_{T, \text{final}}} \right) \exp \left( -\frac{t}{\tau} \right) \right) \]
TCAD simulation of the aging at the SOA edge

Calibration of the aging dynamics models available in TCAD.

\[
\frac{dN_T(t)}{dt} = \nu N - (\gamma + \nu) N_T(t)
\]

\[
\nu = \frac{N_{T,f}}{\tau \cdot N} \quad \text{and} \quad \gamma = \frac{1}{\tau} \left(1 - \frac{N_{T,f}}{N}\right)
\]
TCAD simulation of the aging at the SOA edge

Simulation of the aging dynamics using degradation models available in TCAD.

\[
\frac{dN_T(t)}{dt} = v N - (\gamma + v) N_T(t)
\]

\[
v = \frac{N_{T,f}}{\tau \cdot N} \quad \text{and} \quad \gamma = \frac{1}{\tau} \left( 1 - \frac{N_{T,f}}{N} \right)
\]
TCAD simulation of the aging at the SOA edge

Simulation of the aging conditions

P3 most effective degradation

\[ G^{ii}(P2) = G^{ii}(P3) \]

in the B-C RCS

\[ |E| \] @ EB spacer increases from P1 to P3 (second order effect)
SHE simulation of the aging at the SOA edge

Tool based on the spherical harmonic expansion solution of the BTE. More reliable results: hot carrier holes included.
SHE simulation of the aging at the SOA edge

P3 has much more high energy holes than P2.
Acknowledgement

- This project has received funding from the European Union's Seventh Programme for research, technological development and demonstration under grant agreement No 316755.
- I would like to thank my research group and friends at UNINA for their support, Prof. Niccolò Rinaldi, Prof. Vincenzo d’Alessandro and Dr. Alessandro Magnani.
- I also would like to acknowledge Prof. Thomas Zimmer, Prof. Cristell Maneux and their research team for the fruitful cooperation we had in the last years.
- I thank Klaus Aufinger and Gerhard Fischer, with IFAG and IHP, respectively, for providing experimental data and actively supporting the research cooperation.
Essential bibliography


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