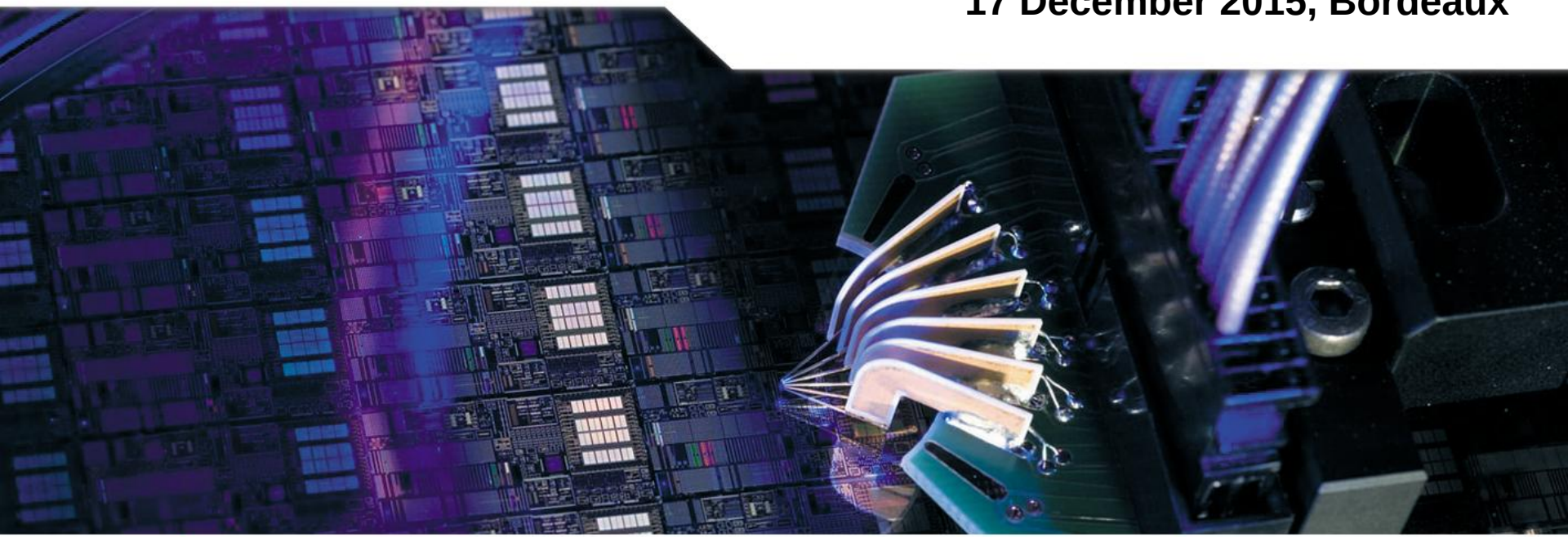
Reliability of SiGe-THz devices

Grazia Sasso

SiGe-THz devices:
Physics and reliability
17 December 2015, Bordeaux



A European Project supported within the Seventh Framework Programme for Research and Technological Development

Outline

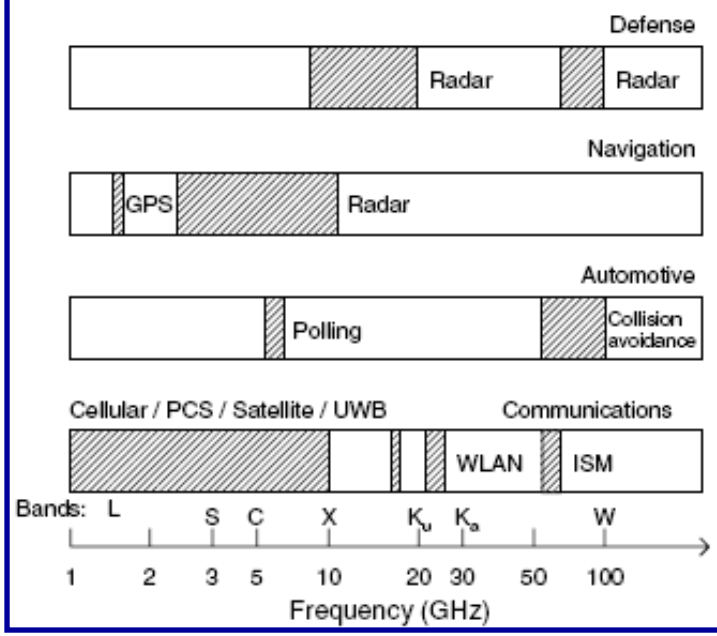
- SiGe HBTs in BiCMOS technology
- Reliability and SOA with scaling and RF
  - DOTSEVEN project
  - SiGe HBTs development framework
  - Electrical instability phenomena
  - Thermal resistance and self-heating
- Hot-carrier phenomena
  - Reverse emitter-base stress
  - Mixed mode stress
  - Stress at the SOA edge

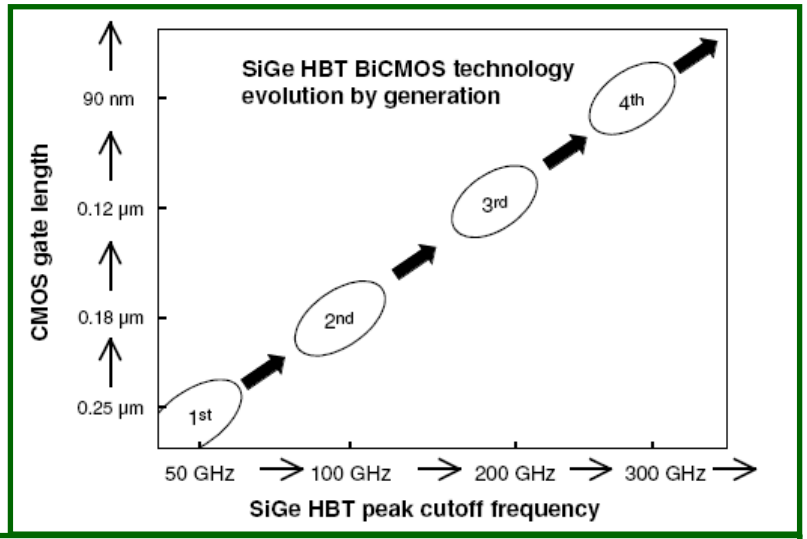
Outline

- Reverse emitter-base stress
  - Methods and techniques
  - Evaluation and modeling of results
  - Recovery
- Mixed mode stress
  - Evaluation of results, modeling and TCAD
  - Recovery
- Stress at the SOA edge
  - Evaluation and modeling of results
  - TCAD and SHE simulations

SiGe HBTs in BiCMOS technology

RF and mmWave applications
SiGe vs. **III-V** (compound)





- ✓ BiCMOS technology and SoC
- ✓ Scaling and bandgap engineering

⇩

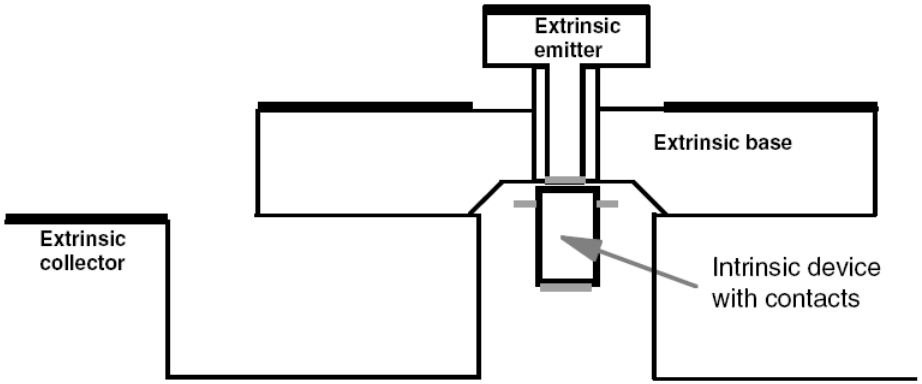
Low cost

European research founding: dotfive dot seven

Performance and reliability

FoM: f_T, f_{MAX}, BV_{CEO}, BV_{CBO}, β
Scaling and trade-offs

$$f_T \cong \frac{1}{2\pi\left(\tau_{TB} + \frac{V_T}{I_C} C_{jC}\right)}$$



$$f_{MAX} \cong \sqrt{\frac{f_T}{8\pi R_B C_{CB}}}$$

$$f_T \cdot BV_{CBO} = k\left(N_C\right)$$

$$BV_{CEO} = \frac{BV_{CBO}}{\beta^{1/n}}, \quad n = 3 \div 6$$

Performance and reliability

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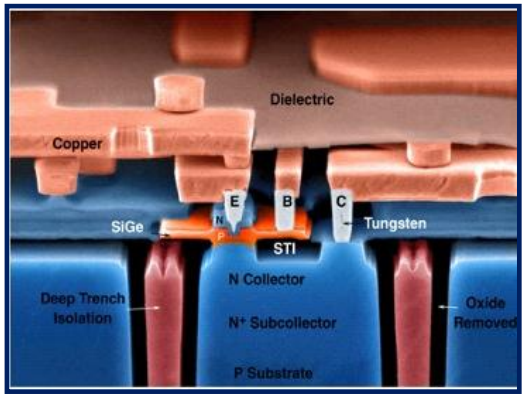


Performance improvement → Scaling, High doping → Higher electric field, Higher current density, Higher thermal resistance → Impact ionization, Self-heating, Hot-carrier

Performance improvement reduces safe-operating-area (SOA) due to electrical and thermal issues.

DOTSEVEN european project: motivation

- The European project DOTSEVEN supports the development of SiGe HBTs with f_{MAX} of 700 GHz
- Highly-scaled and doped architectures are explored and aggressive operating conditions are applied
- Higher electric fields and current densities may cause performance degradation and might jeopardize speed and long-time reliability
- Device reliability is an increasingly important topic in circuit and system design

http://www.dotseven.eu.

Device development framework

SIMULATION ⟷ **CHARACTERIZATION**

MODELING

Calibrated TCAD:

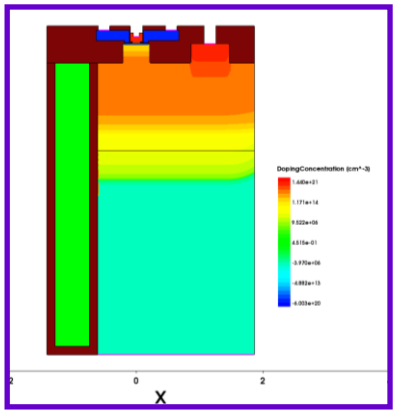
- predicts device characteristics of anticipated wafer fabrication technology
- explores the physics of scaled devices and investigate new device architectures

✓ Reduce time-to-market and cost
✓ Manage performance vs. reliability constrains

SiGe HBT development framework

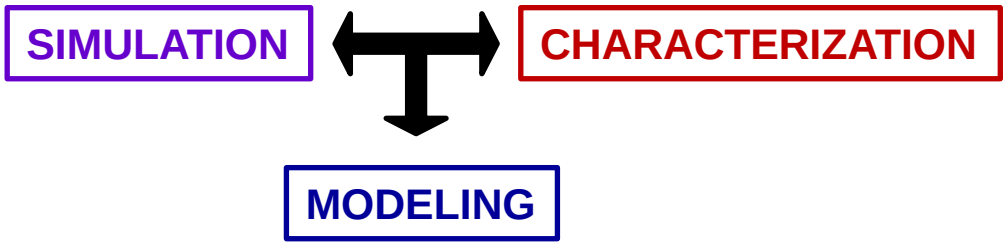
SIMULATION ⟷ **CHARACTERIZATION**

MODELING



- Calibration of hydrodynamic (HD) models for TCAD
- Development of transport parameters for HD simulation in TCAD
- DC, pulsed and RF on wafer experimental measurements
- Reliability and SOA reduction with scaling and RF improvements

Reliability and SOA with scaling and RF improvements

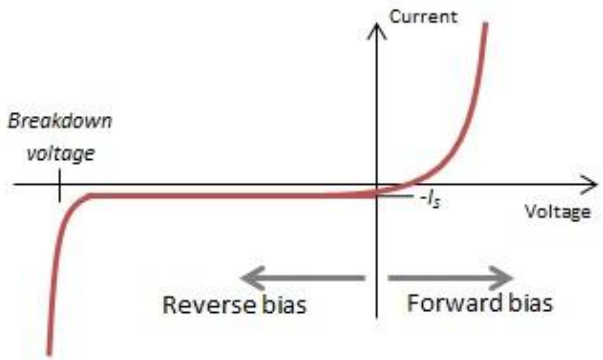


- Electrical instability phenomena
  - Impact ionization
  - Tunneling
  - Pinch-in
- Thermal resistance and self-heating
- Hot-carrier phenomena

Electrical instability phenomena - breakdown

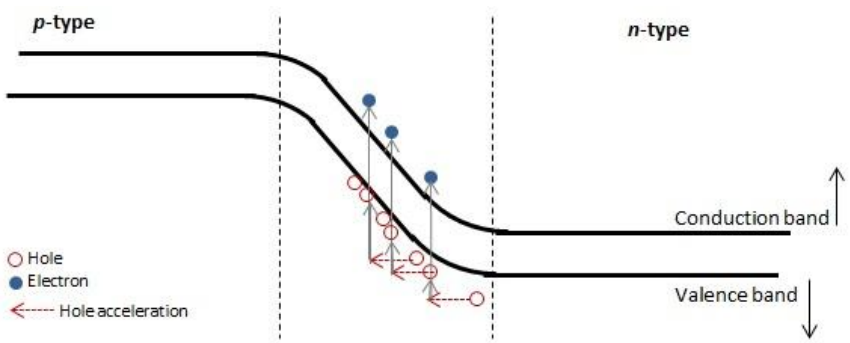
Impact ionization

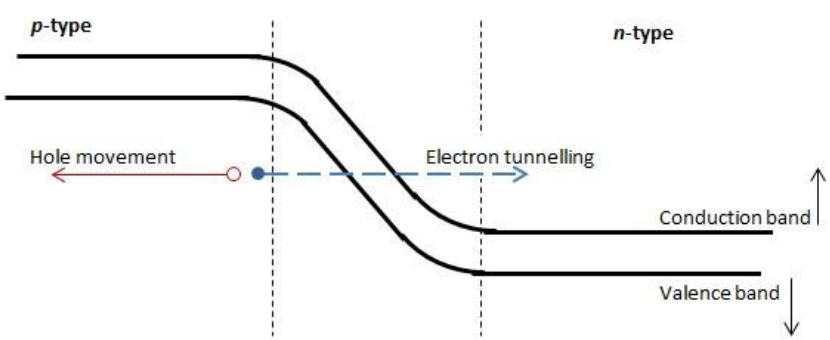
Avalanche breakdown



Tunneling

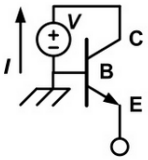
Zener breakdown

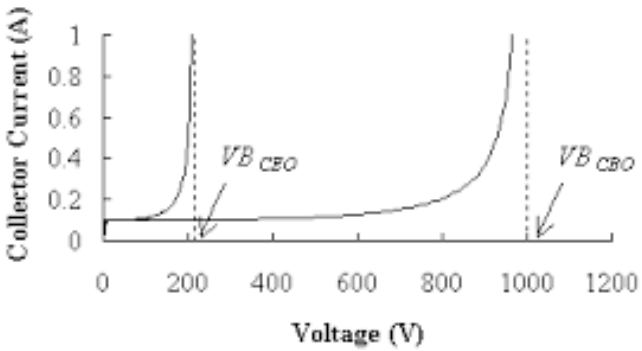




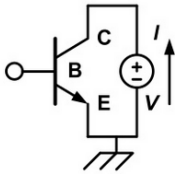
SiGe HBTs electrical breakdown measurements

BV_{CBO}, Open emitter
Collector-base breakdown voltage



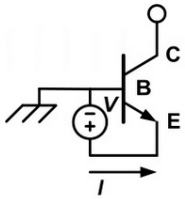


BV_{CEO}, Open base
Collector-emitter breakdown voltage



Impact ionization model calibration (*Okuto*, *Van Overstraeten* models, etc.)

BV_{CEB}, Open collector
Emitter-base breakdown voltage



Tunneling models calibration supported by low temperature measurements.

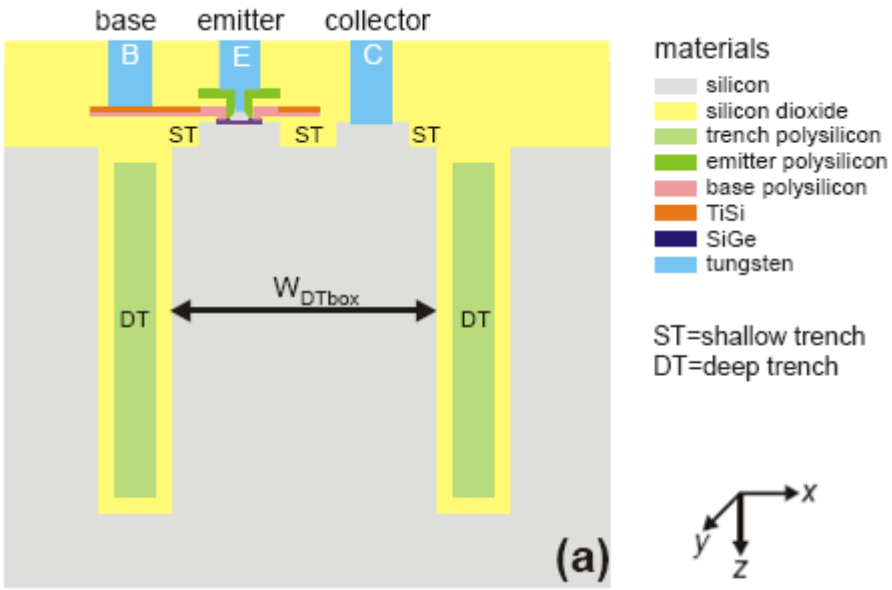
Thermal resistance and self-heating

Impact of scaling on the thermal behavior

Thermal resistance extraction

$$R_{TH} = \frac{\Delta T}{P_D} \Rightarrow T_J = R_{TH} \cdot P_D + T_0$$

- #2 is slightly laterally/vertically scaled compared to #1
- #3 devices aggressively lateral scaled with respect to #2



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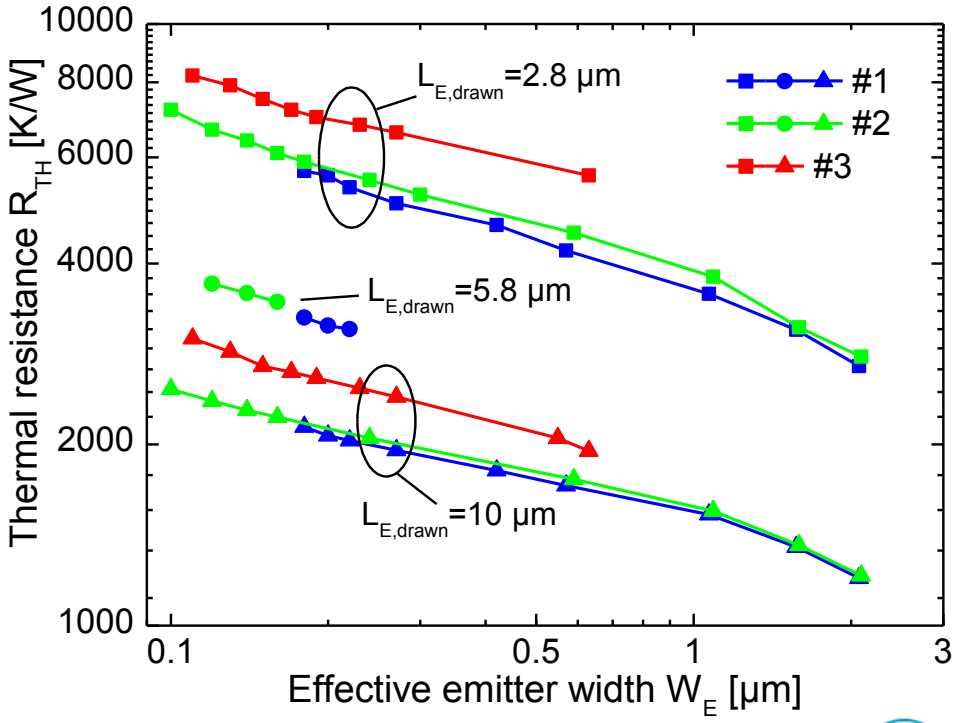
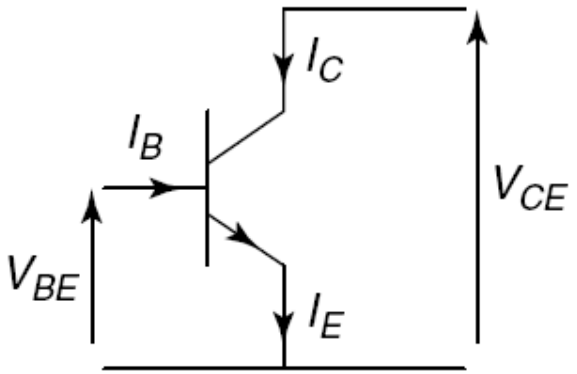


Hot-carrier damage standard stress techniques

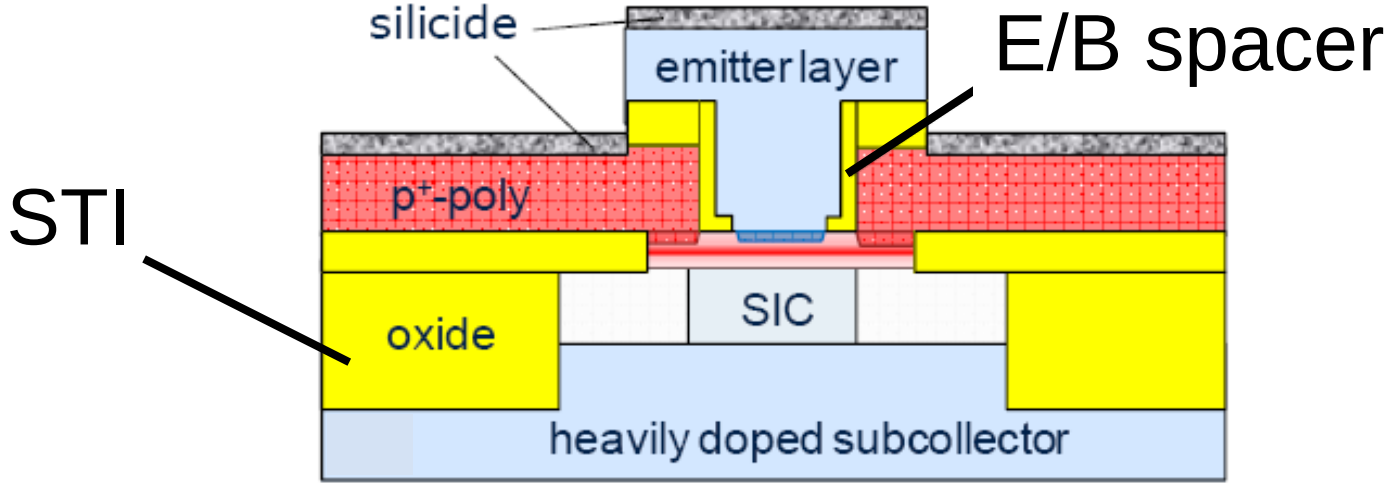
- Reverse emitter-base stress (high V_{EB})
- Forward stress (high J_C and T)
- Mixed-mode stress (high J_E and high V_{CB})



Studied (experiments and TCAD) for HBTs fabricated by:

Hot-carrier damage: trap formation

- Very high localized electrical fields
- Generated hot carriers:
  1. Damage the Si/SiO_2 interface → interface traps
  2. Surmount the Si/SiO_2 barrier → oxide traps/charges



Hot-carrier damage

Aging mechanisms are related to impact ionization and tunneling phenomena

↓

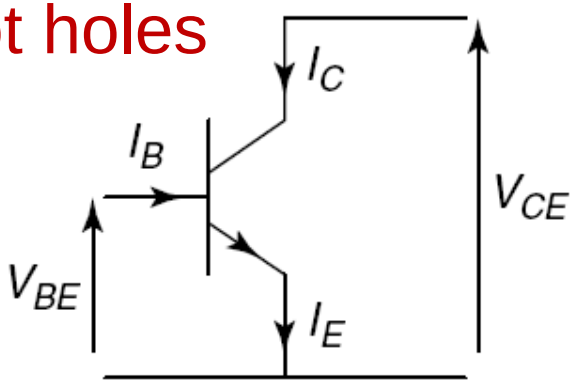
Degradation worsen with RF performance improvement

Outline

- Reverse emitter-base stress
  - Methods and techniques
  - Evaluation and modeling of results
  - Recovery experiments
- Mixed mode stress
  - Evaluation of results, modeling and TCAD
  - Recovery experiments
- Stress at the SOA edge
  - Evaluation and modeling of results
  - TCAD and SHE simulations

Reverse emitter-base stress methods

- Open collector (OC)
  $V_{EB}<0$, OC or $V_{BC}=0$ Hot holes
- Forward collector (FC)
  $V_{EB}<0$, $V_{BC}>0$ Hot electrons and hot holes



Standard methods are not exploitable when AC measurements are to be performed

Proposed technique for EB stress

$V_{EB}<0$, $V_{CE}=0$ (i.e., $V_{EB}=V_{CB}>0$)

- I_C is negligible during stress
- An uncontrolled forward biasing of the SC junction is avoided
- Monitoring of the RF performance during stress interruptions is allowed without any mechanical movement in the experimental setup

Verification of the stress technique

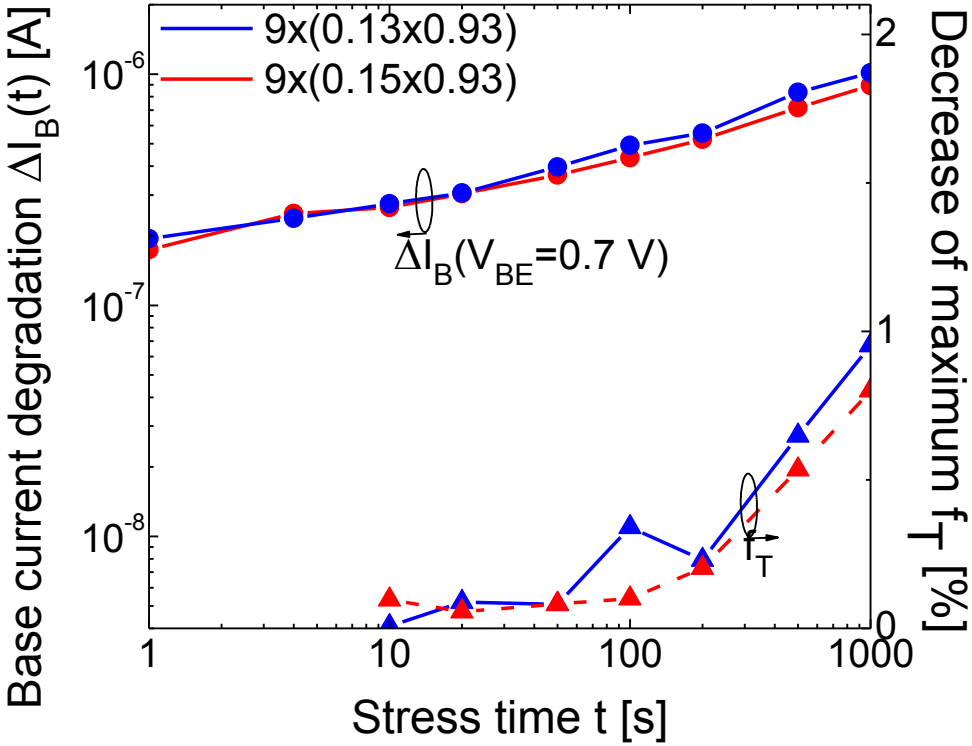
9x(0.13x0.93)

- $V_{EB\text{-}stress}$=3.5 V, V_{CE}=0 V ↔ V_{CB}=3.5 V
  - I_C=7 µA, I_B=120 µA
  - I_E=-(I_B+I_C)≈I_{stress}

9x(0.15x0.93)

- $V_{EB\text{-}stress}$=3.5 V, V_{CE}=-1.5 V ↔ V_{CB}=2.0 V
  - I_C=-68 mA, I_B=-2mA
  - I_E=-(I_B+I_C)-I_S≠I_{stress}

Verification of the stress technique



The stress current is unchanged and the slight discrepancy can be ascribed to the small difference in the aspect ratio

Reverse EB stress experiments – 130 nm SiGe:C

Infineon Technologies (IFAG) devices:

- f_{MAX}/f_T=380/240 GHz
- n=1÷ 9, several combinations of W_E/L_E
- BEC & BEBC configuration
- RF layout, GSG pads configuration, T_A=300 K

Innovation for high performance microelectronics (IHP) devices:

- f_{MAX}/f_T=300/240 GHz
- n=4, several combinations of W_E/L_E
- CBE configuration
- RF layout, GSG pads configuration, T_A=300 K
- Statistics: 3 dies

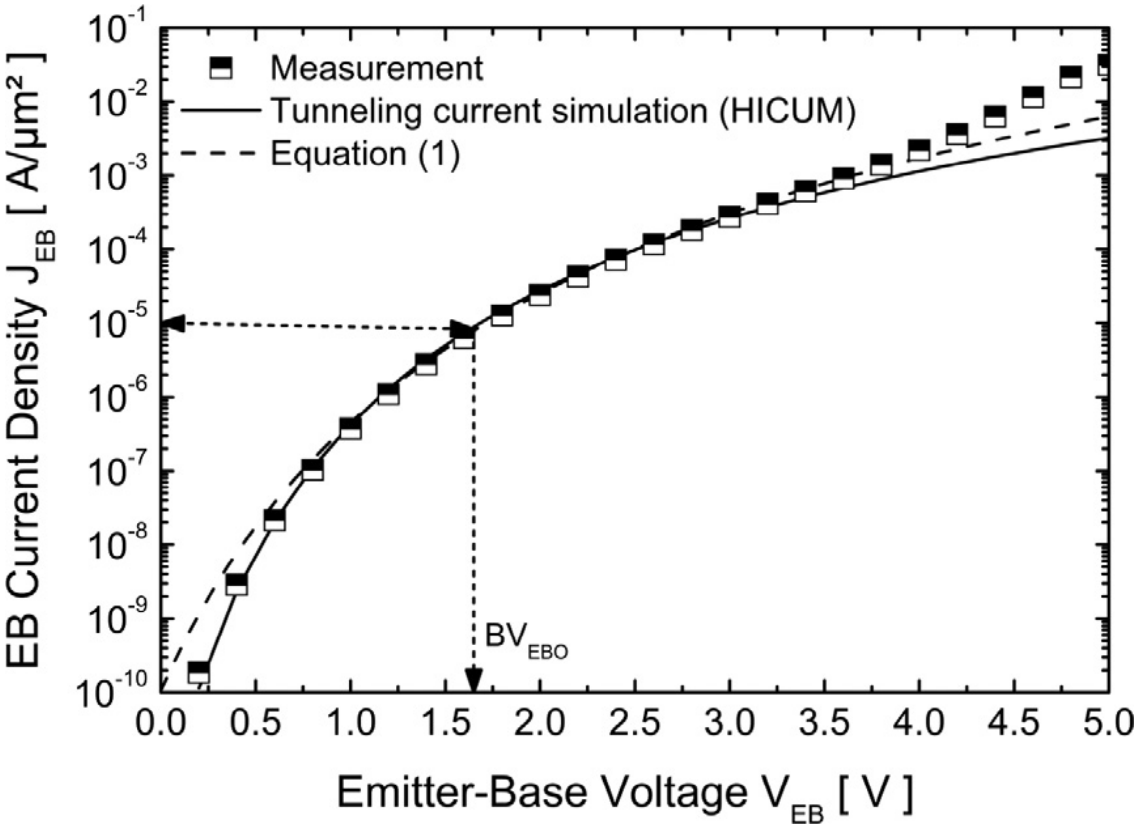
Technology under test, IHP

$A_E=Nx(W_E x L_E)$ [µm²]	Configuration	A_E [µm2]	P_E [µm]
4x(0.13x0.88)	CBE	0.4576	8.08
4x(0.16x0.88)	CBE	0.5632	8.32
4x(0.19x0.88)	CBE	0.6688	8.56

- f_{MAX}/f_T=300/240 GHz
- CBE configuration
- n=4, , $A_E=n\cdot(W_E\cdot L_E)$, $P_E=2\cdot n\cdot(W_E+L_E)$
- RF layout, GSG pads configuration, T_A=300 K
- Statistics: 3 dies

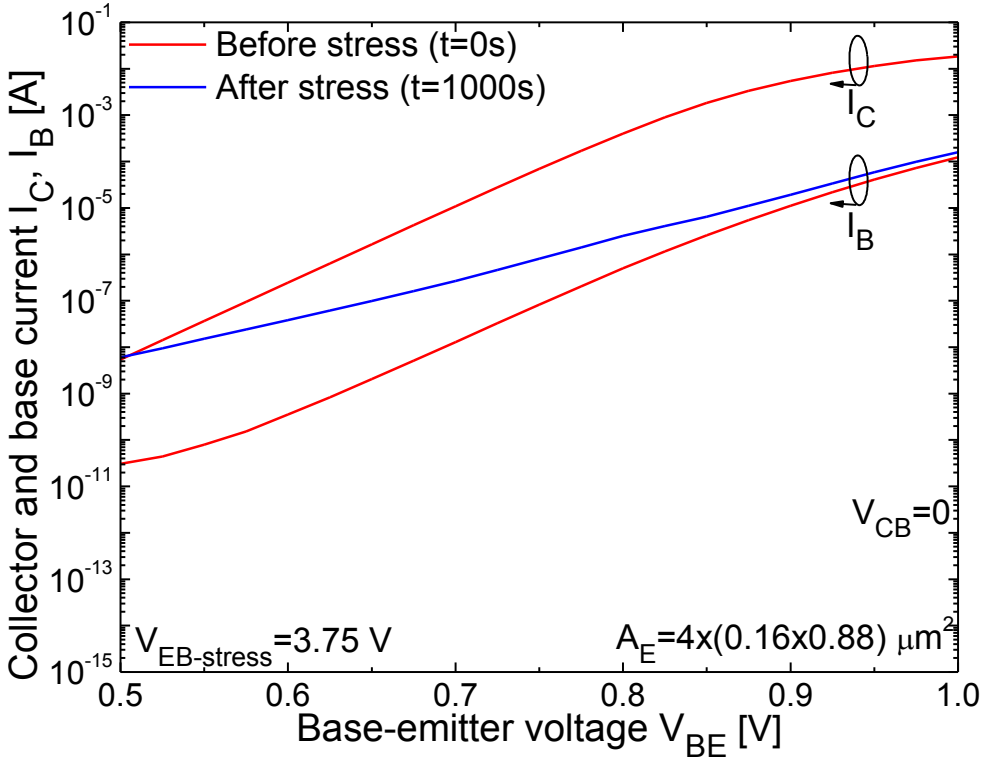
innovations for high performance microelectronics
Leibniz-Institut für innovative Mikroelektronik

Stress conditions, IHP



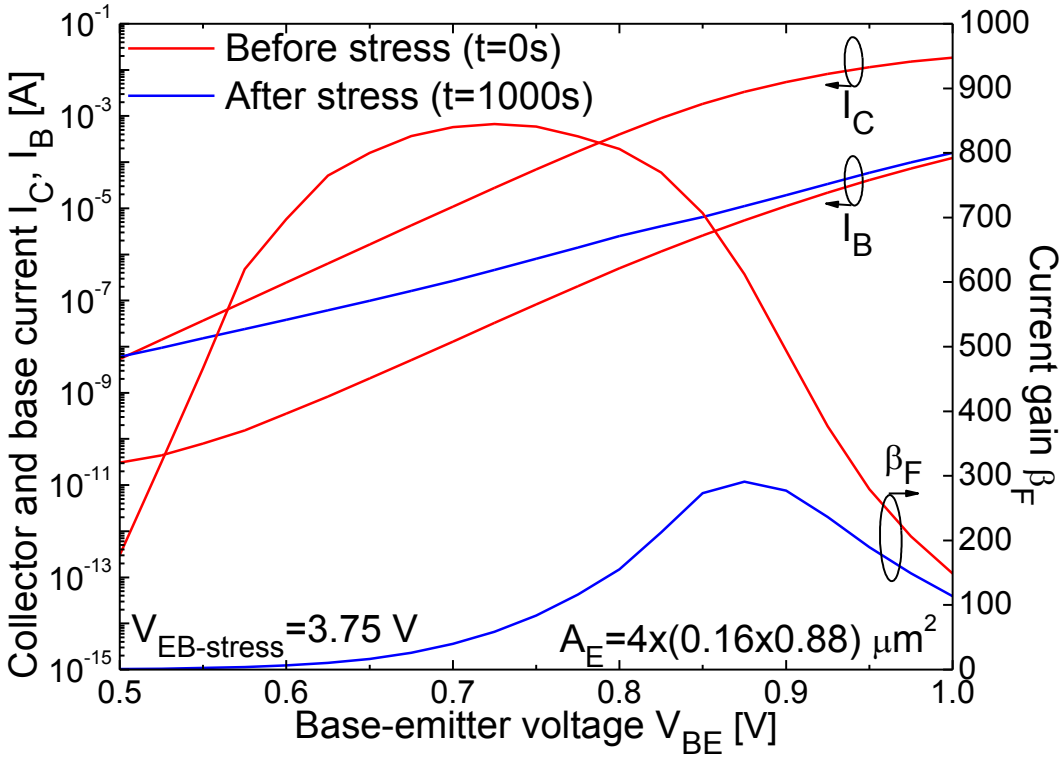
$V_{EB\text{-}stress}$=3.75÷4.50 V
V_{CE}=0, V_C=V_E=0

Degradation results: Gummel plot



- I_B increases, I_C is not affected → $\beta_F = I_C/I_B$ decreases
- Degradation strongly shrinks in the high-bias region

Degradation results: Gummel plot



- I_B increases, I_C is not affected → $\beta_F = I_C/I_B$ decreases
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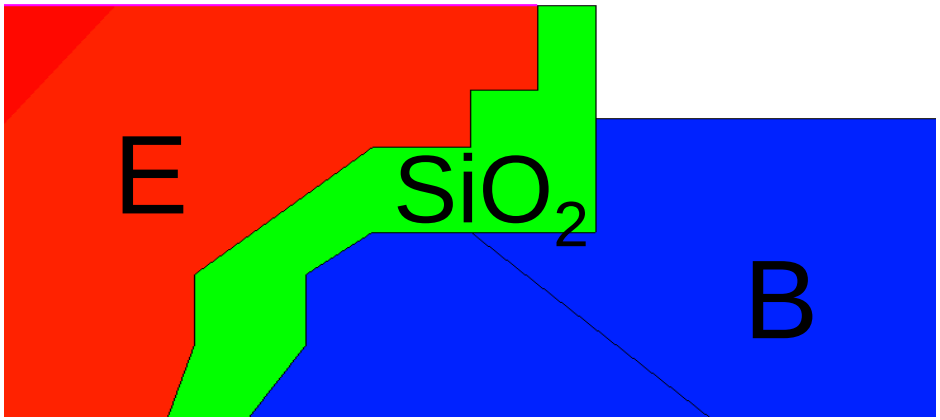
Traps formation

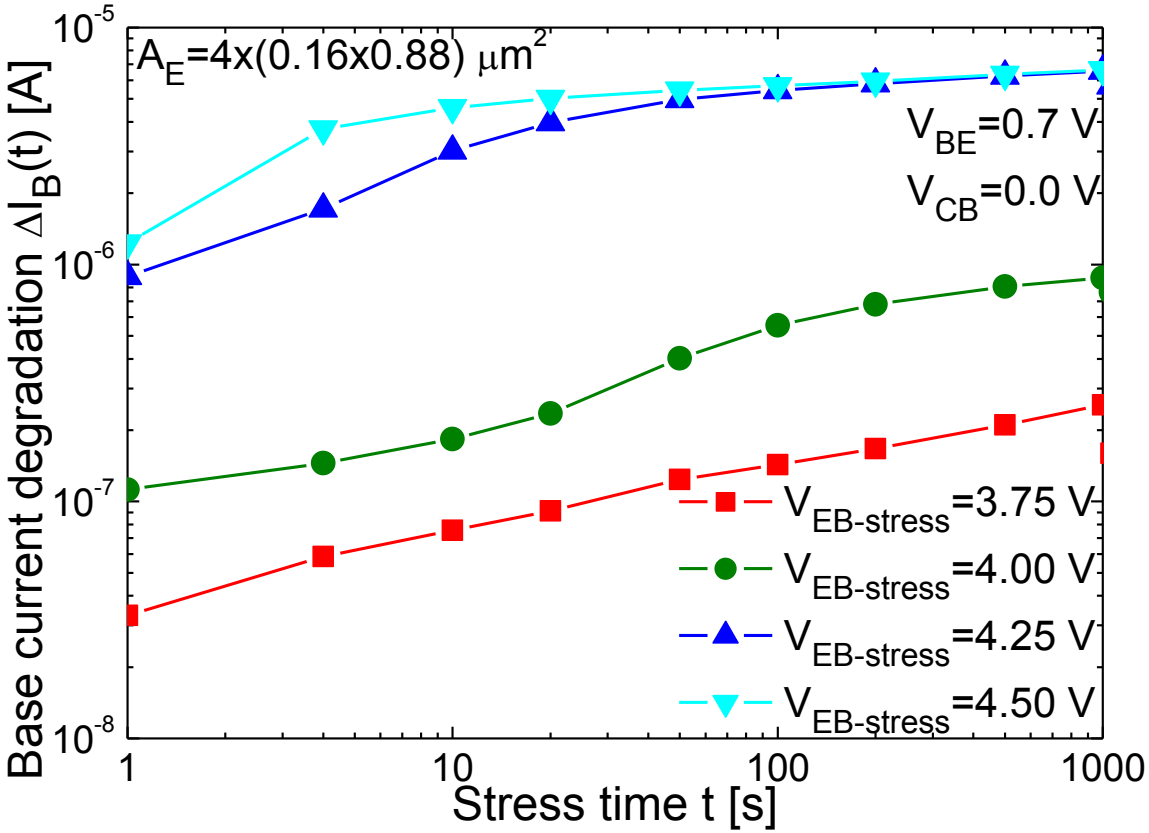


- Very high localized electrical fields
- Generated hot carriers:

  Damage the Si/SiO2 interface ➡ interface traps

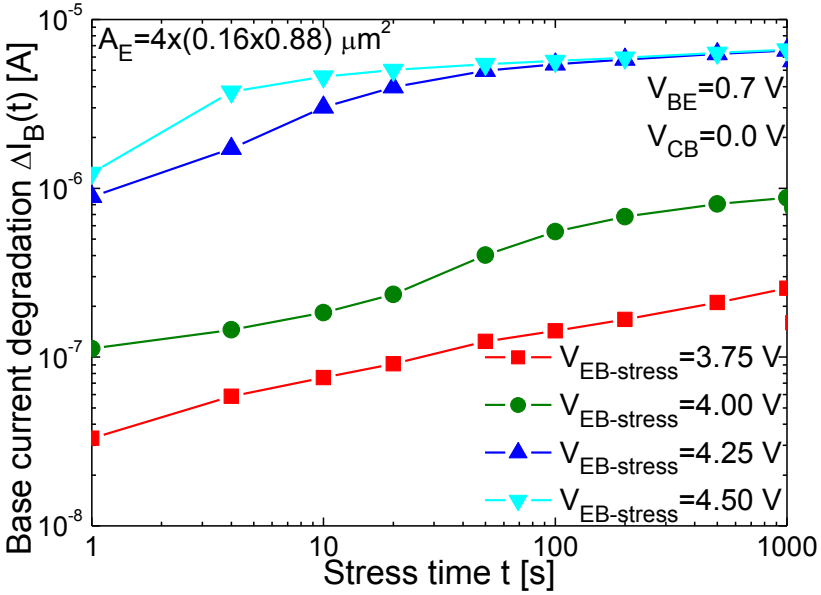
  Surmount the Si/SiO2 barrier ➡ oxide traps/charges

Degradation results: $\Delta I_B(t)=I_B(t)-I_B(0)$ vs. t



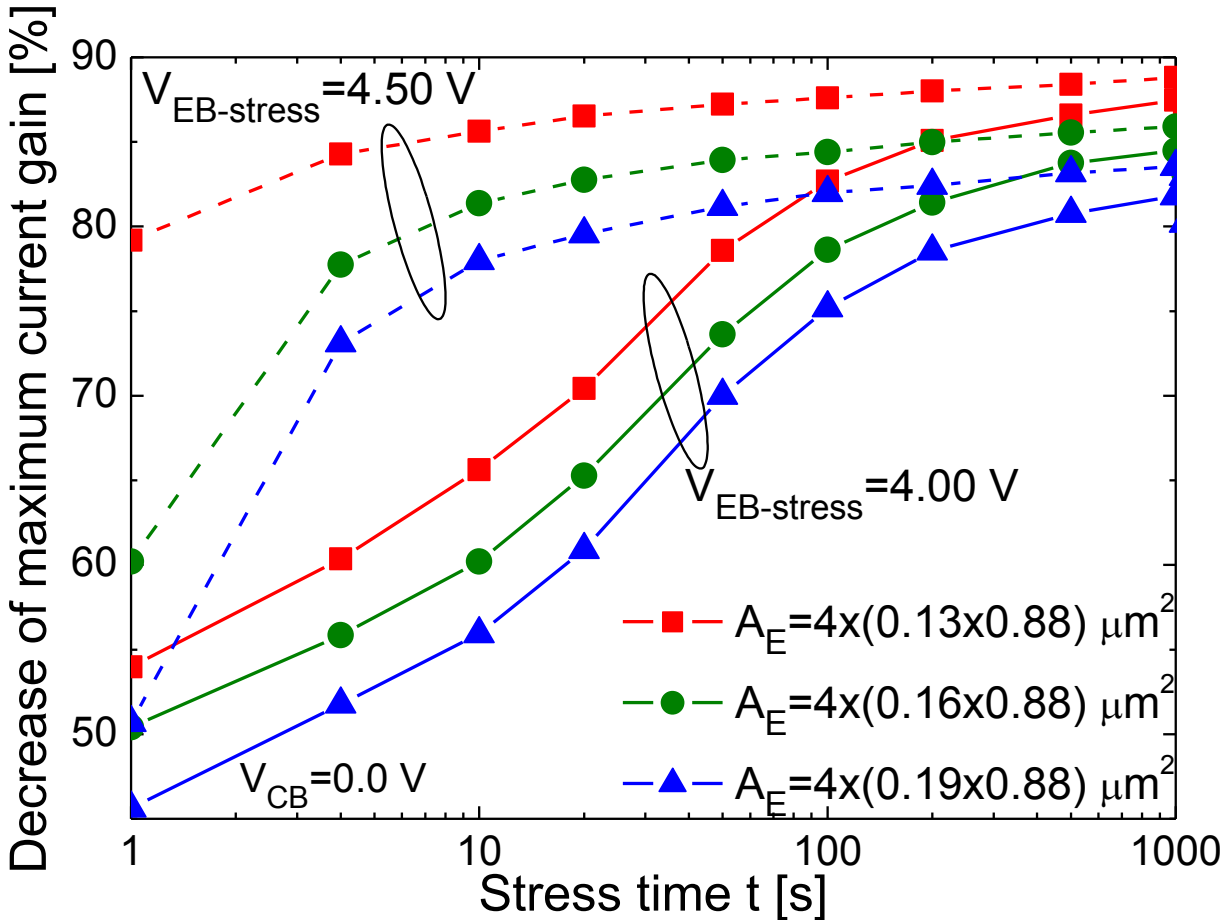
Degradation kinetic depends on the voltage stress…

Degradation results: $\Delta I_B(t)=I_B(t)-I_B(0)$ vs. t

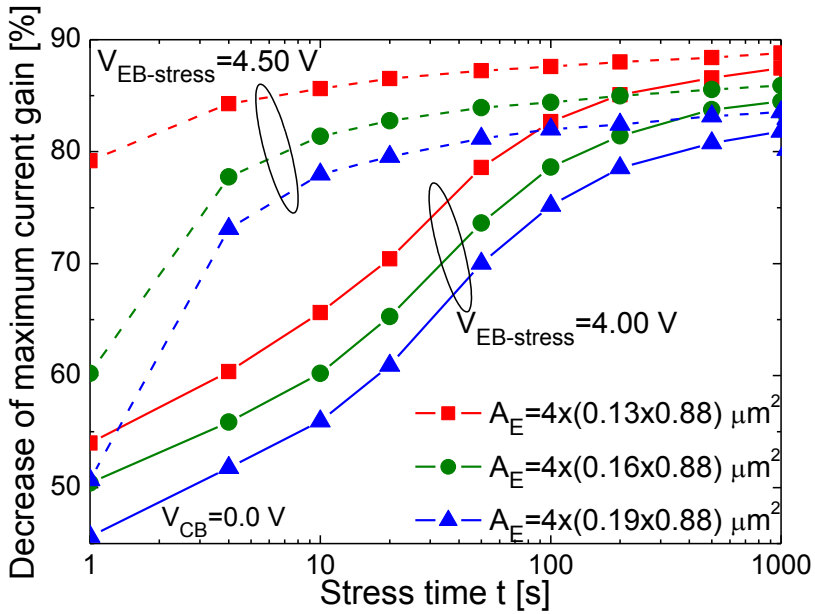


1. Low: Power law density increase with stress time
2. High: Very fast degradation only in the first few seconds
3. Very-high: common saturation trend

Degradation results: $\Delta\beta_{F\text{-}MAX}$ vs. t

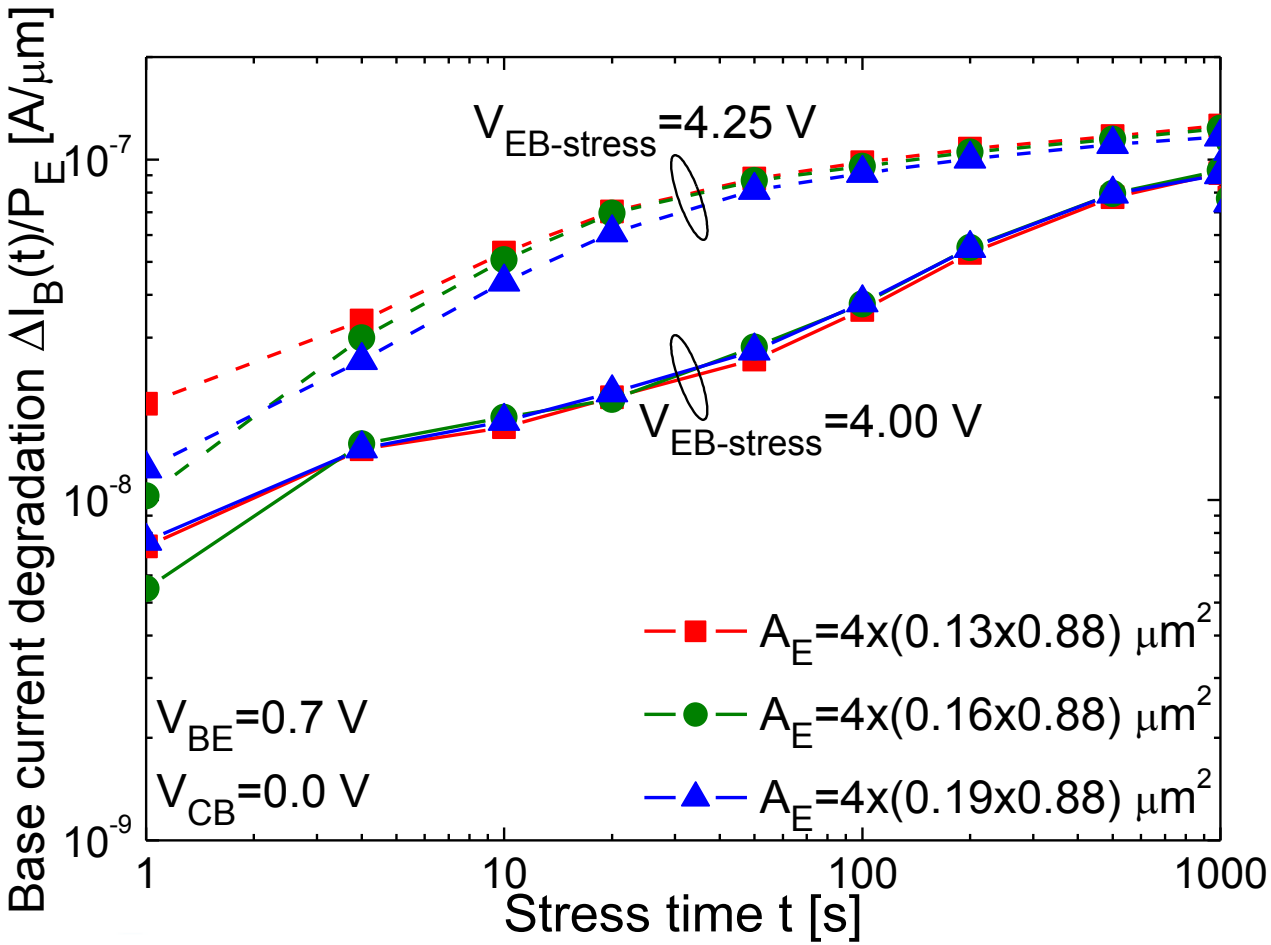


Degradation results: $\Delta\beta_{F\text{-}MAX}$ vs. t

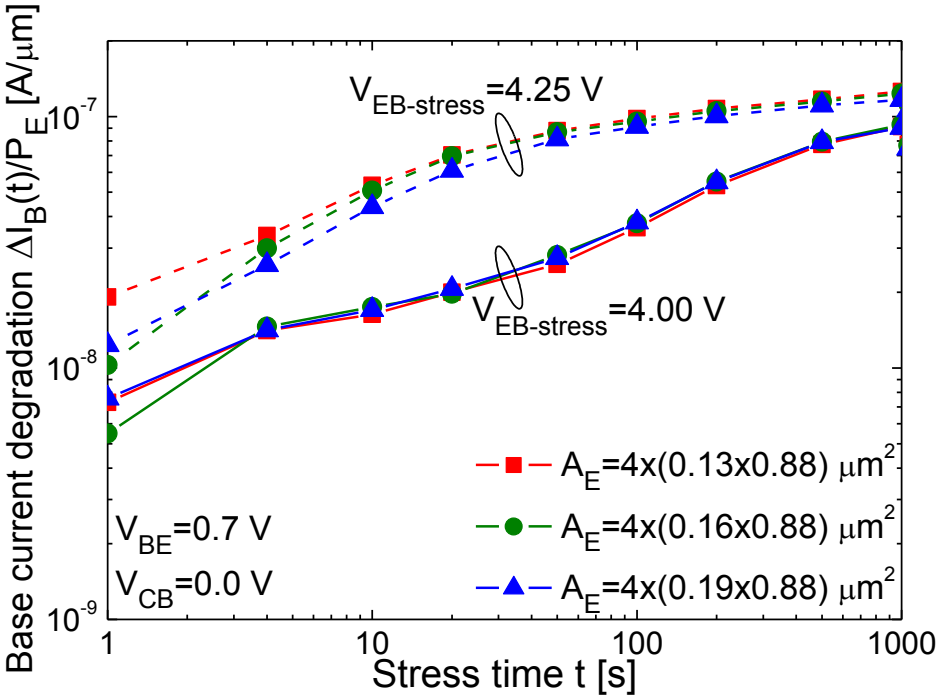


- For a given emitter layout, maximum gain degradation follows the same trends of $\Delta I_B(t)$
- Performance of the smallest device degrades more rapidly → increasing of P_E/A_E

Degradation results: $\Delta I_B(t)/P_E$ vs. t

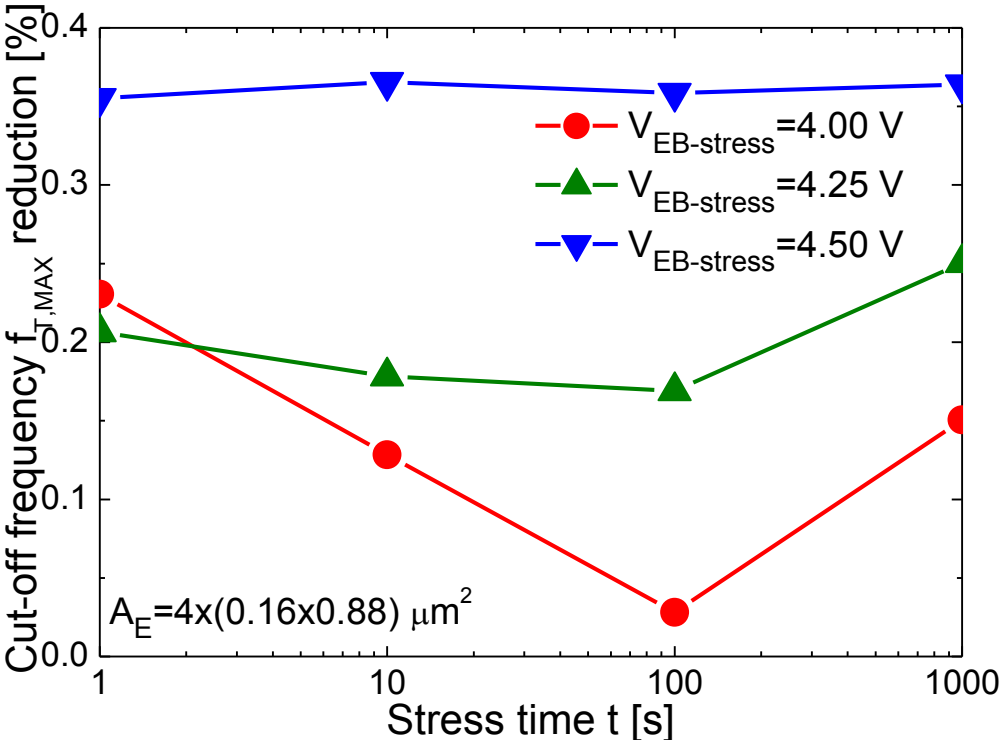


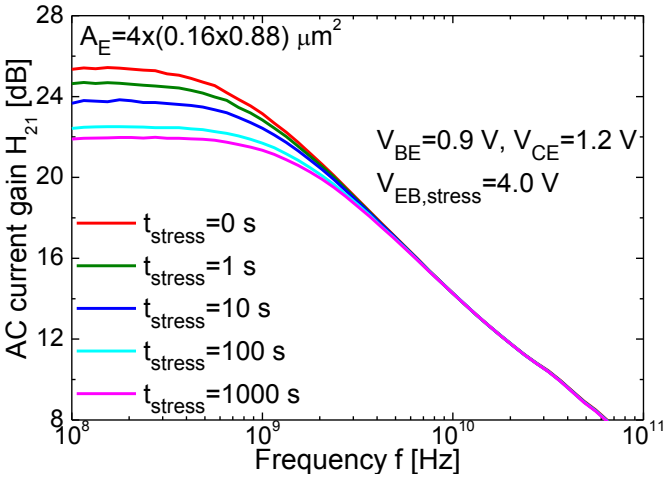
Degradation results: $\Delta I_B(t)/P_E$ vs. t



- Damage is mostly located around the emitter perimeter, adjacent to the space charge region between the emitter and the base

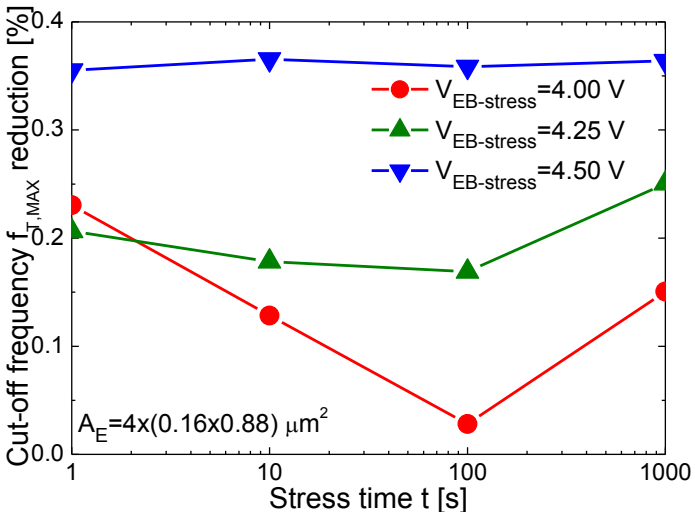
Stress effects on the AC performance

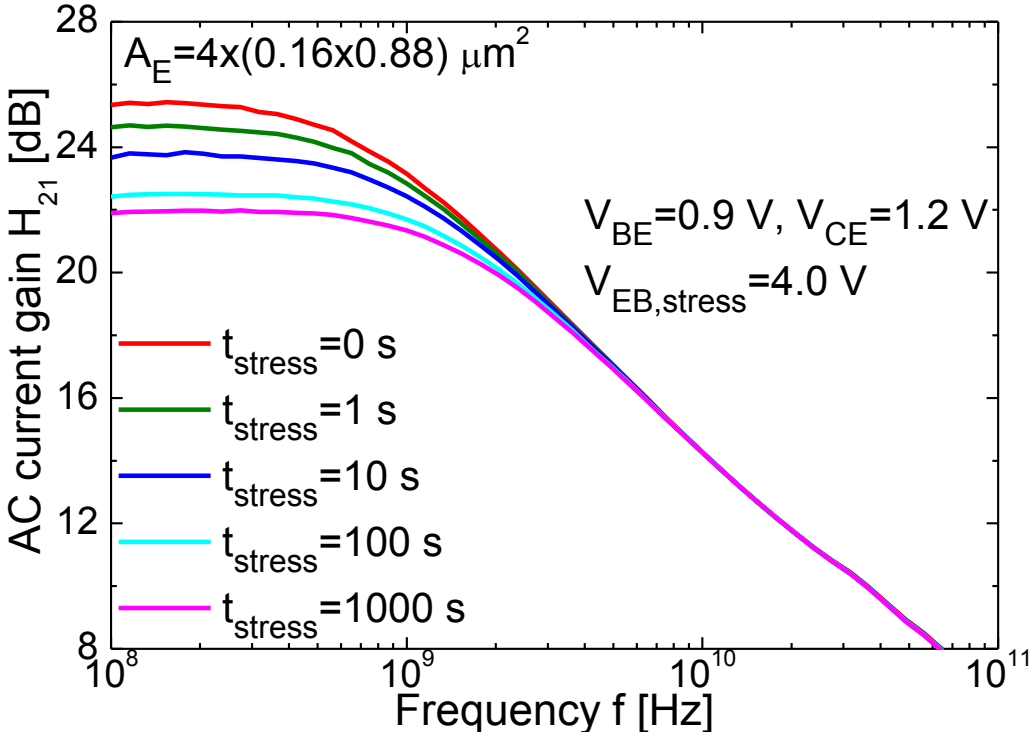




- Different samples, fast measurements evaluation
- Junction capacitances, AC current gain H_{21}, f_T, and f_{MAX}

Stress effects on the AC performance





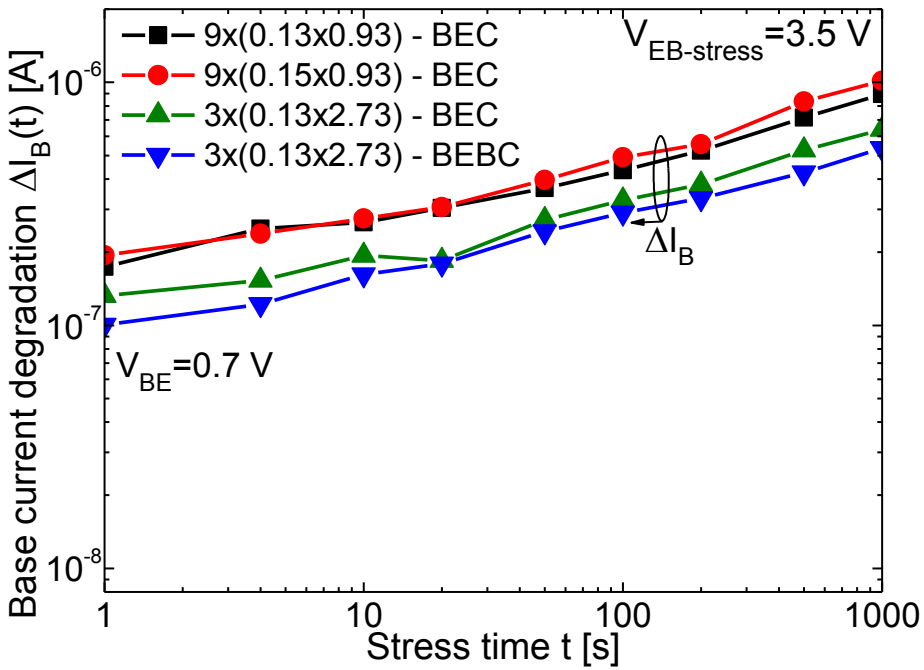
- No significant variations have been detected for RF parameters (exception H_{21})

Technology under test and stress conditions, IFAG

$A_E=Nx(W_E x L_E)$ [µm²]	Configuration	$V_{EB\text{-}stress}$ [V]	V_{CB} [V]
9x(0.13x0.93)	BEC	3.5	3.5
9x(0.15x0.93)	BEC	3.5	2.0
3x(0.13x2.73)	BEC	3.5	3.5
3x(0.13x2.73)	BEBC	3.5	3.5
1x(0.13x9.93)	BEC	2.5	2.5
1x(0.23x9.93)	BEC	3.0	3.0

- f_{MAX}/f_T=380/240 GHz
- n=1÷ 9, several combinations of W_E/L_E
- BEC & BEBC configuration

Degradation results: $\Delta I_B(t)$ vs. t



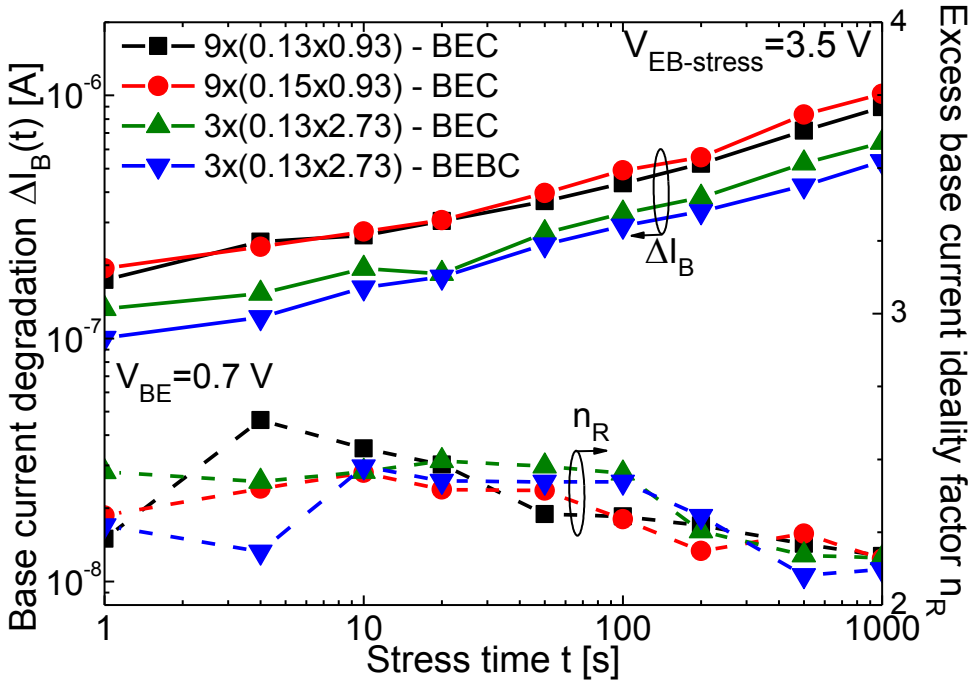
$$\Delta I_B(t) = I_B(t) - I_B(0)$$

$$= I_{SR}(t) \cdot \exp\left[\frac{q \cdot V_{BE}}{n_R(t) \cdot k \cdot T}\right]$$

$\Delta I_B(t)/P_E$ is almost comparable for different devices

Interface traps are mostly located along the emitter perimeter

Degradation results: n_R vs. t



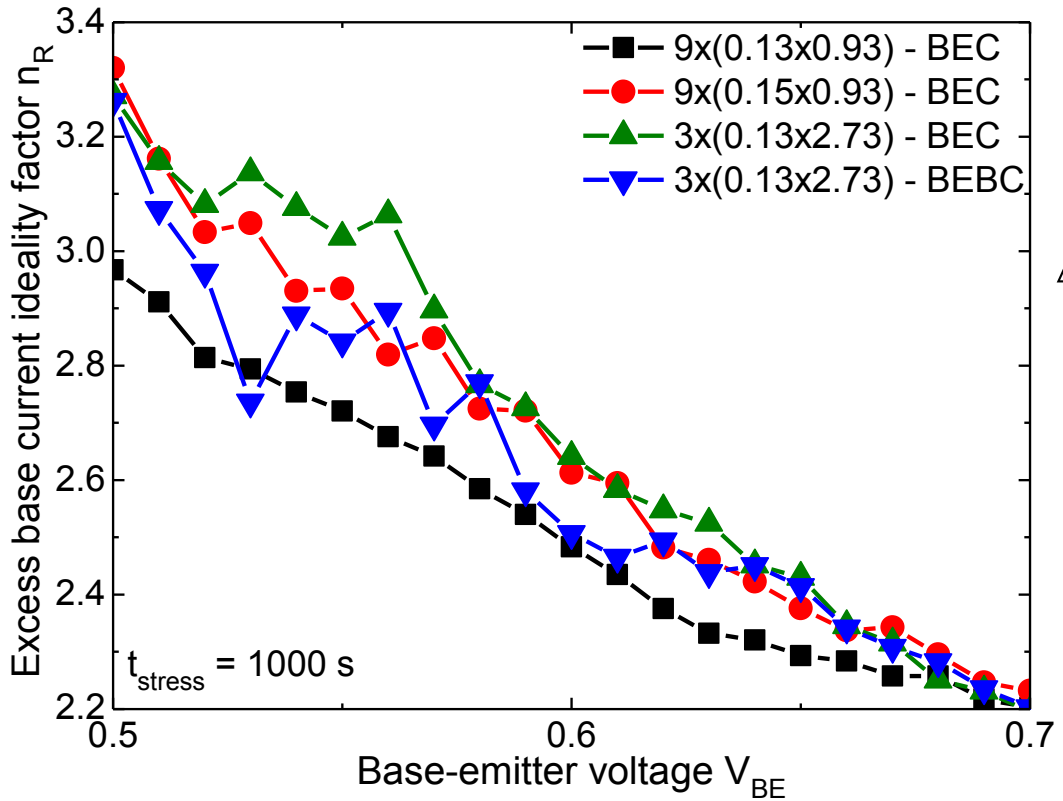
$$\Delta I_B(t) = I_B(t) - I_B(0)$$

$$= I_{SR}(t) \cdot \exp\left[\frac{q \cdot V_{BE}}{n_R(t) \cdot k \cdot T}\right]$$

n_R slightly exceeds 2 and mildly decreases with stress time

SRH recombination mechanism via midgap traps, but…

Degradation results: n_R vs. V_{BE}



$$\Delta I_B(t) = I_B(t) - I_B(0)$$

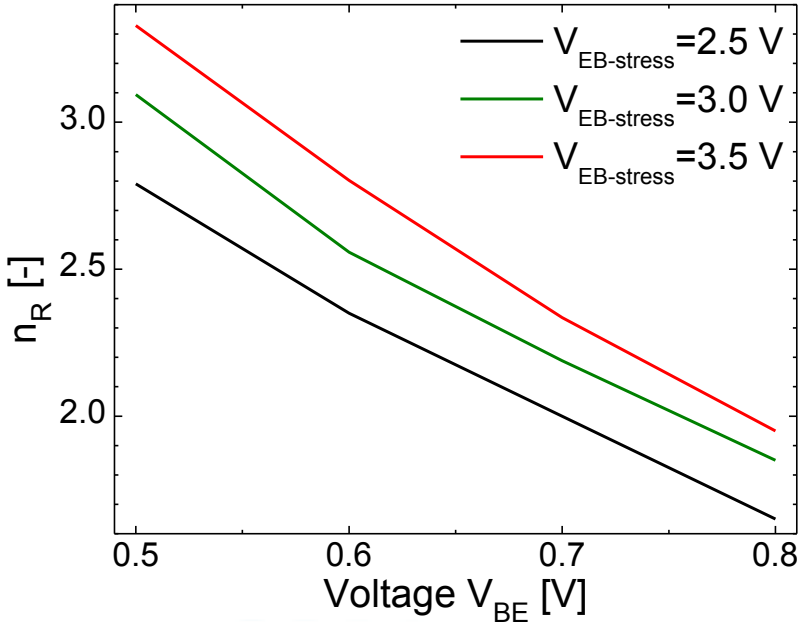
$$= I_{SR}(t) \cdot \exp\left[\frac{q \cdot V_{BE}}{n_R(t) \cdot k \cdot T}\right]$$

… tunneling at very low injection levels (TAT)

Model for base current degradation

$$\Delta I_B(t) = P_E \cdot I_{SRP} \left(\frac{t}{t_0}\right)^{\alpha} \cdot \exp\left(\frac{q \cdot V_{BE}}{n_R \cdot k \cdot T}\right)$$

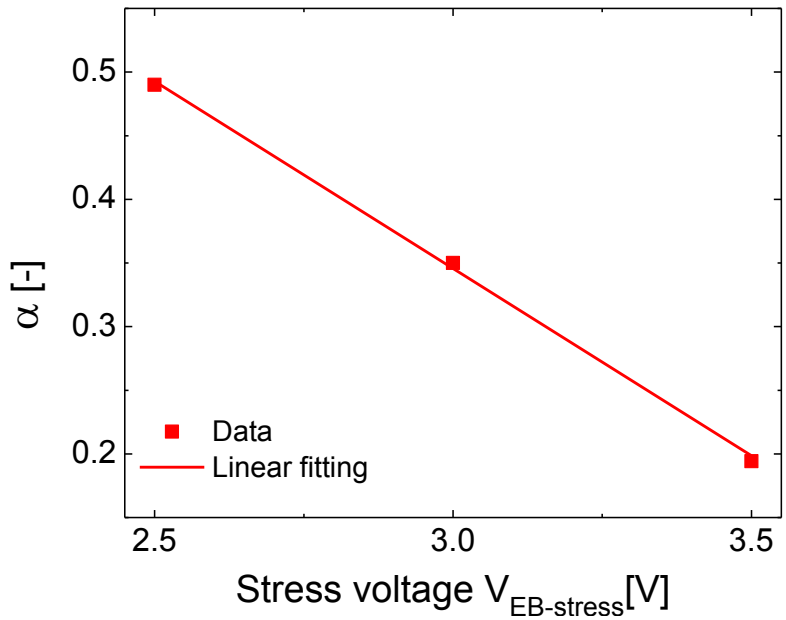
$n_R = f(V_{EB\text{-}stress}, V_{BE})$ mean value over various devices

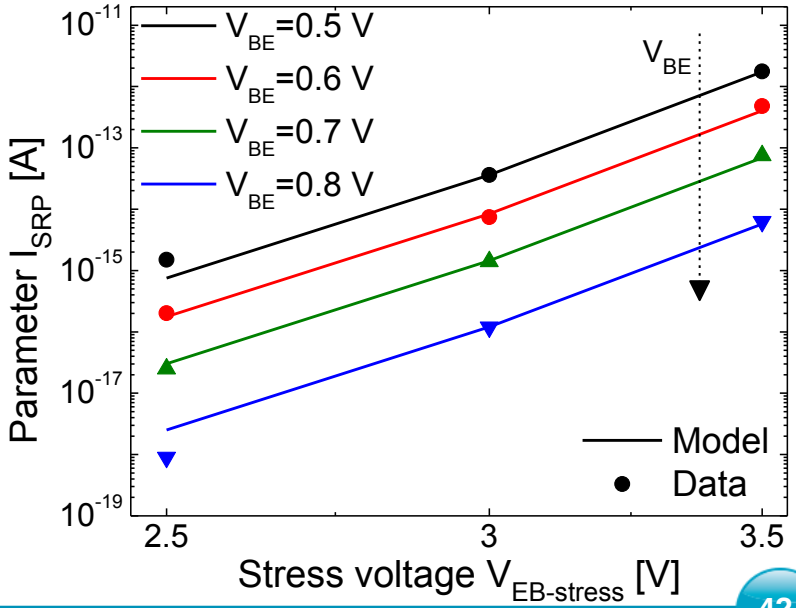


Model for base current degradation

$$\Delta I_B(t) = P_E \cdot I_{SRP} \left(\frac{t}{t_0}\right)^{\alpha} \cdot \exp\left(\frac{q \cdot V_{BE}}{n_R \cdot k \cdot T}\right)$$

$$I_{SRP} = I_{SRP0} \cdot \exp\left(\frac{q \cdot \Delta\Psi_S}{k \cdot T}\right)$$





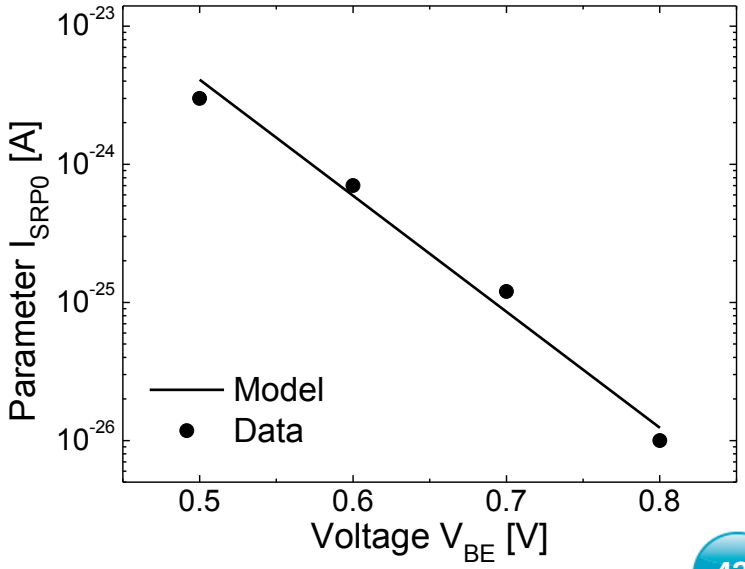
Model for base current degradation

$$I_{SRP} = I_{SRP0} \cdot \exp\left(\frac{q \cdot \Delta\Psi_S}{k \cdot T}\right)$$

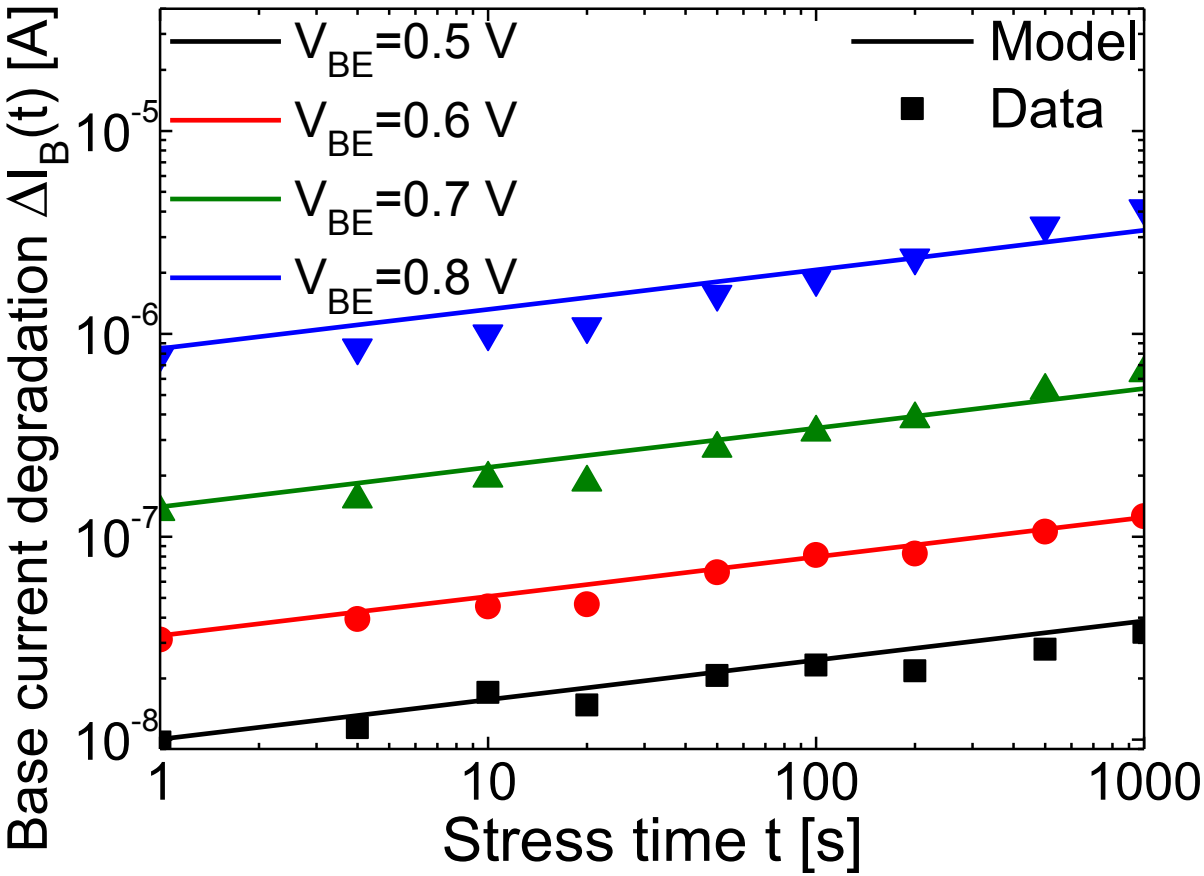
$$\Delta\Psi_S = \frac{V_{EB-stress}}{5}$$

$$I_{SRP0} = A \cdot \exp\left(-\frac{q \cdot V_{BE}}{2 \cdot k \cdot T}\right)$$

$\Delta\Psi_S$: variation of the surface potential induced by the charge trapped in the oxide



Model vs. experimental results (1)



3x(0.23x2.73) µm^2

$V_{EB\text{-}stress}$=3.5 V

Total t=1000s

Model for base current degradation

$$\Delta I_B(t) = P_E \cdot I_{SRP} \left(\frac{t}{t_0}\right)^{\alpha} \cdot \exp\left(\frac{q \cdot V_{BE}}{n_R \cdot k \cdot T}\right) \quad (1)$$

$$\left.\begin{aligned} I_{SRP} &= I_{SRP0} \cdot \exp\left(\frac{q \cdot \Delta\Psi_S}{k \cdot T}\right) \\ \Delta\Psi_S &= \frac{V_{EB-stress}}{5}, \qquad I_{SRP0} = A \cdot \exp\left(-\frac{q \cdot V_{BE}}{2 \cdot k \cdot T}\right) \end{aligned}\right\} \quad (2)$$

Model includes the degradation due to generation of interface traps (1) and includes the generation of charge in the oxide (2) for all the geometries

Model provides a complete description for ΔI_B and helps understand the physical background

Model for base current degradation

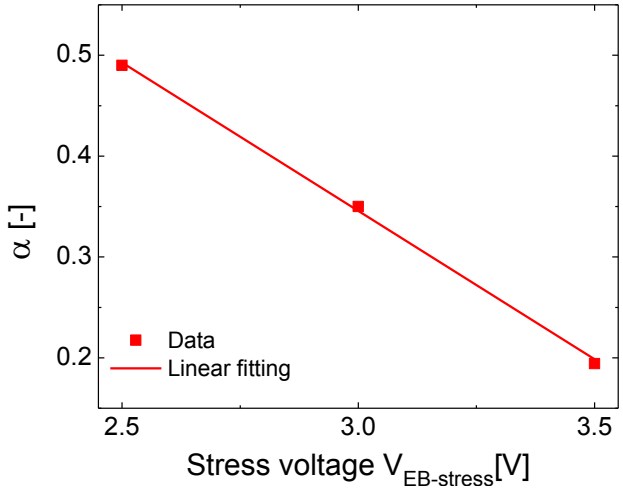
$$\Delta I_B(t) = P_E \cdot I_{SRP} \left(\frac{t}{t_0}\right)^{\alpha} \cdot \exp\left(\frac{q \cdot V_{BE}}{n_R \cdot k \cdot T}\right)$$

(1) Generation of interface traps

$$I_{SRP} = I_{SRP0} \cdot \exp\left(\frac{q \cdot \Delta\Psi_S}{k \cdot T}\right)$$

$$\Delta\Psi_S = \frac{V_{EB-stress}}{5}, \qquad I_{SRP0} = A \cdot \exp\left(-\frac{q \cdot V_{BE}}{2 \cdot k \cdot T}\right)$$

(2) Generation of charge in the oxide



Low stress bias

The creation of interface traps dominates

Model for base current degradation

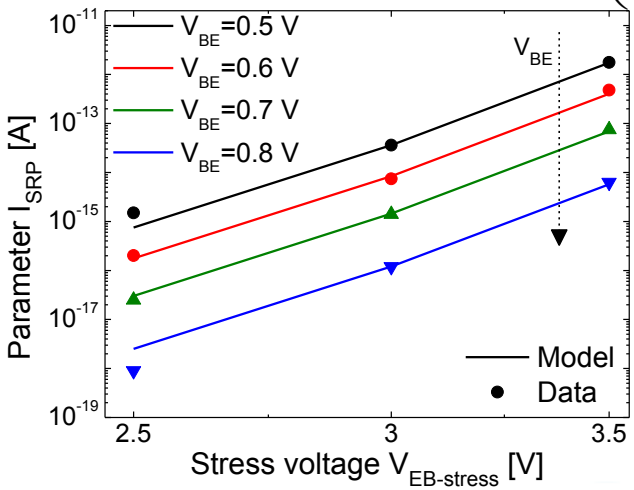
$$\Delta I_B(t) = P_E \cdot I_{SRP} \left(\frac{t}{t_0}\right)^{\alpha} \cdot \exp\left(\frac{q \cdot V_{BE}}{n_R \cdot k \cdot T}\right)$$

(1) Generation of interface traps

$$I_{SRP} = I_{SRP0} \cdot \exp\left(\frac{q \cdot \Delta\Psi_S}{k \cdot T}\right)$$

$$\Delta\Psi_S = \frac{V_{EB-stress}}{5}, \qquad I_{SRP0} = A \cdot \exp\left(-\frac{q \cdot V_{BE}}{2 \cdot k \cdot T}\right)$$

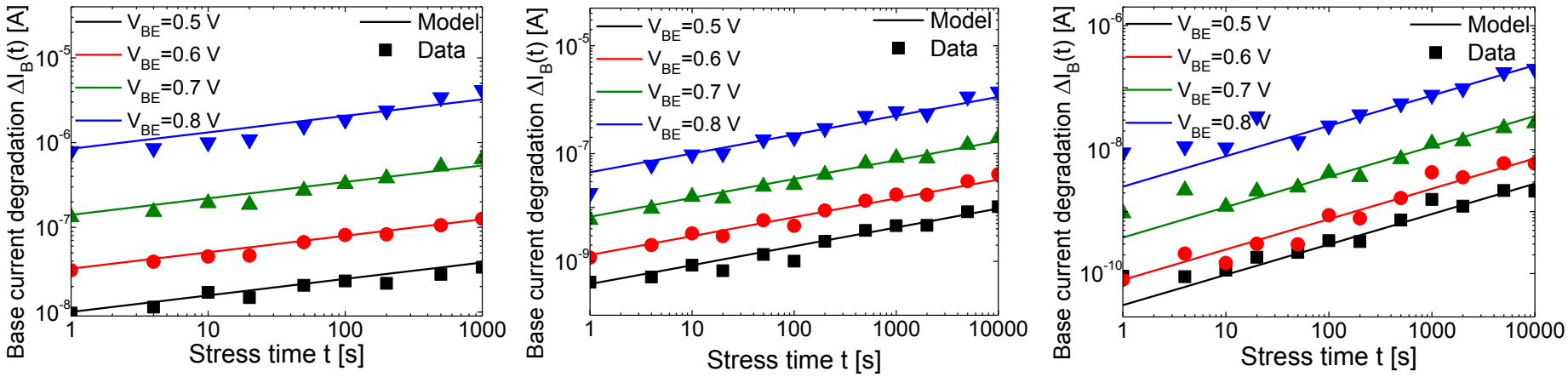
(2) Generation of charge in the oxide



High stress bias

The creation of charge in the oxide prevails and the trap generation rate is lower

Model vs. experiments: summary



- Results span over a longer duration for milder stress
- Model is compared to experiments over aspect ratios, $V_{EB\text{-}stress}$, and V_{BE}

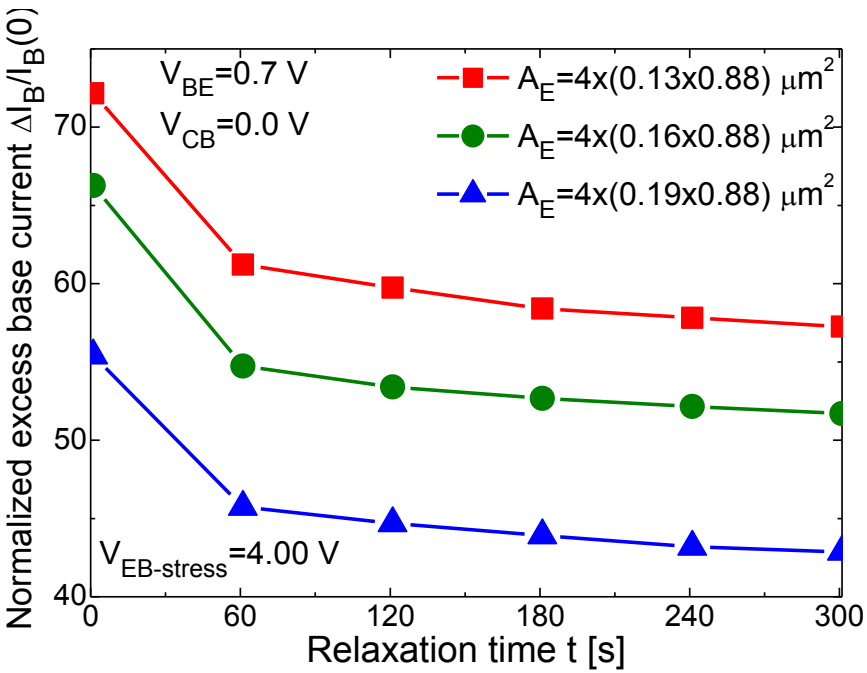
The unified model can be used to describe and predict base current degradation over stress time including all the involved variables (e.g., in compact models for circuit simulation and aging function extraction)

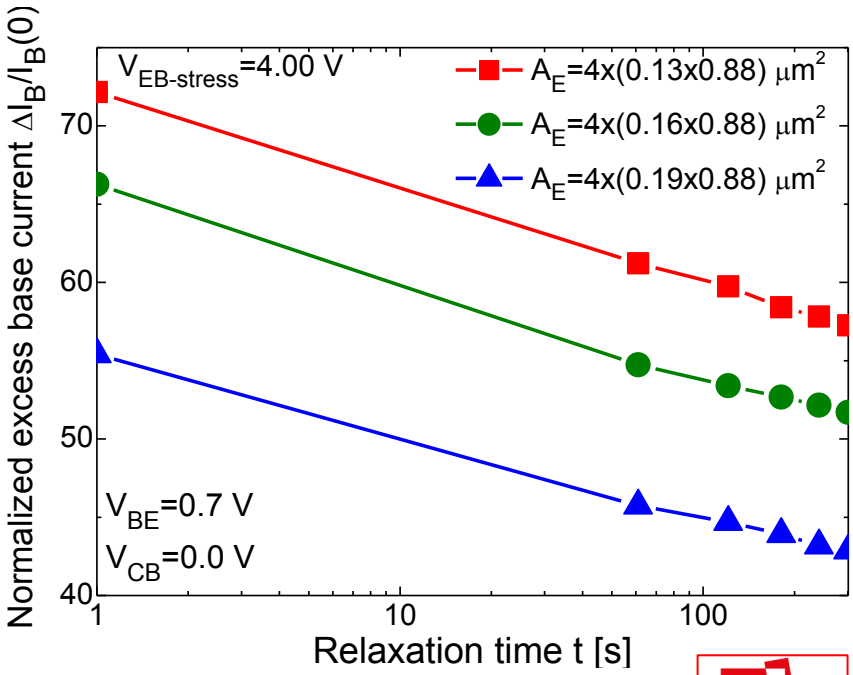
Recovery mechanisms after stress

- Natural recovery
- Forward bias recovery
- Thermal recovery

Physical background provides insight into the stress mechanisms

Natural recovery vs. geometry

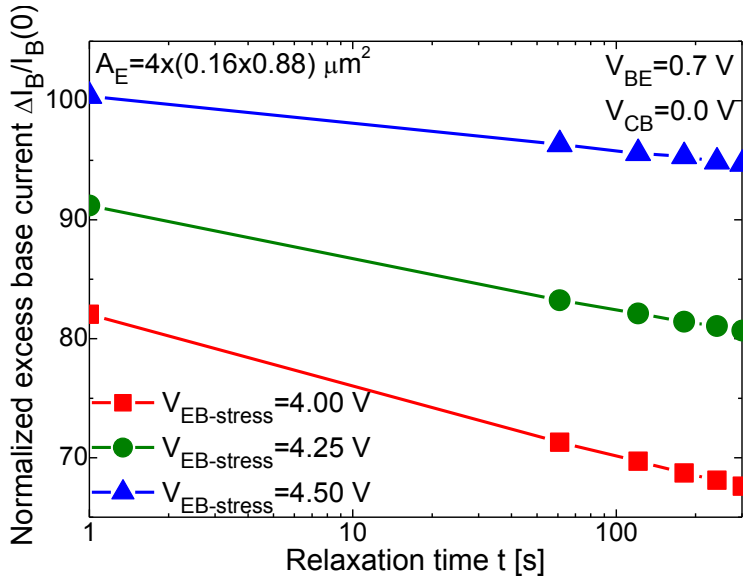




- Semi-logarithmic time dependence
- Emitter layout does not affect the shape/slope

Detrapping of oxide trapped carriers and not annihilation of interface states

Natural recovery vs. stress condition



$$I_B(t) = I_{BO} \exp[q\Delta V_S(t)/kT]$$

- Applied stress affects the slope
- The density of hot holes is expected to exceed the density of hot electrons at low stress voltages
- The decrease in positive (negative) oxide charge produces decrease (increase) of the positive surface potential ΔV_S

Thermal recovery, introduction

- Standard procedure:
  - ✗ $T_{annealing} \neq T_{measurement} \rightarrow$ low accuracy
  - ✗ $T_{annealing} = T_{measurement} \rightarrow$ strong restrictions

- Proposed approach:
  - ✓ Self-heating as a means to accurately study the thermal recovery, its activation and rate

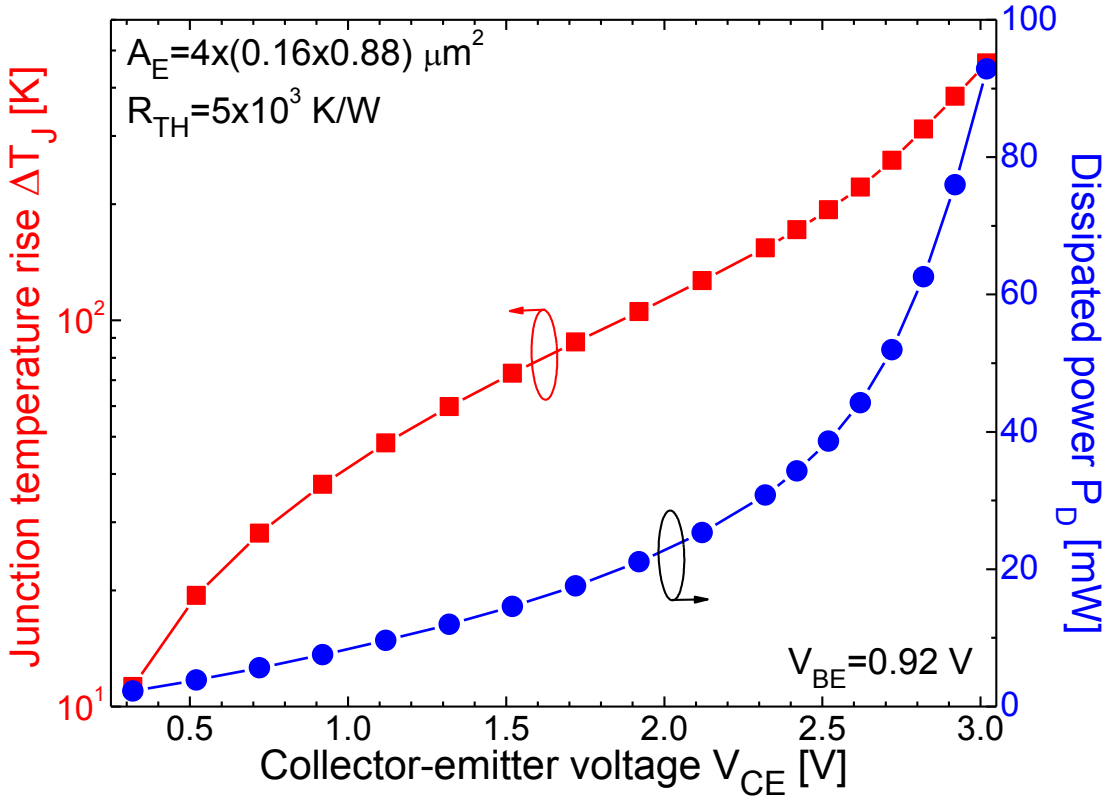
Thermal recovery by self-heating

Controlled self-heating can be applied to reliably evaluate thermal and kinetics properties of recovery:

T_A=300 K, R_{TH} known → $T_J = T_A + R_{TH} \cdot P_D$

- ✓ Annealing steps of given duration and temperature are obtained by setting P_D
- ✓ At preselected times, the annealing experiments are interrupted and the recovery rate is evaluated by switching the applied voltage bias
- ✓ Controlled self-heating at higher dissipated power allows increasing recovery temperature of one's choice
- ✓ Recovery effects vs. P_D, cumulated energy, cumulated heating time, junction-to-ambient temperature increase.

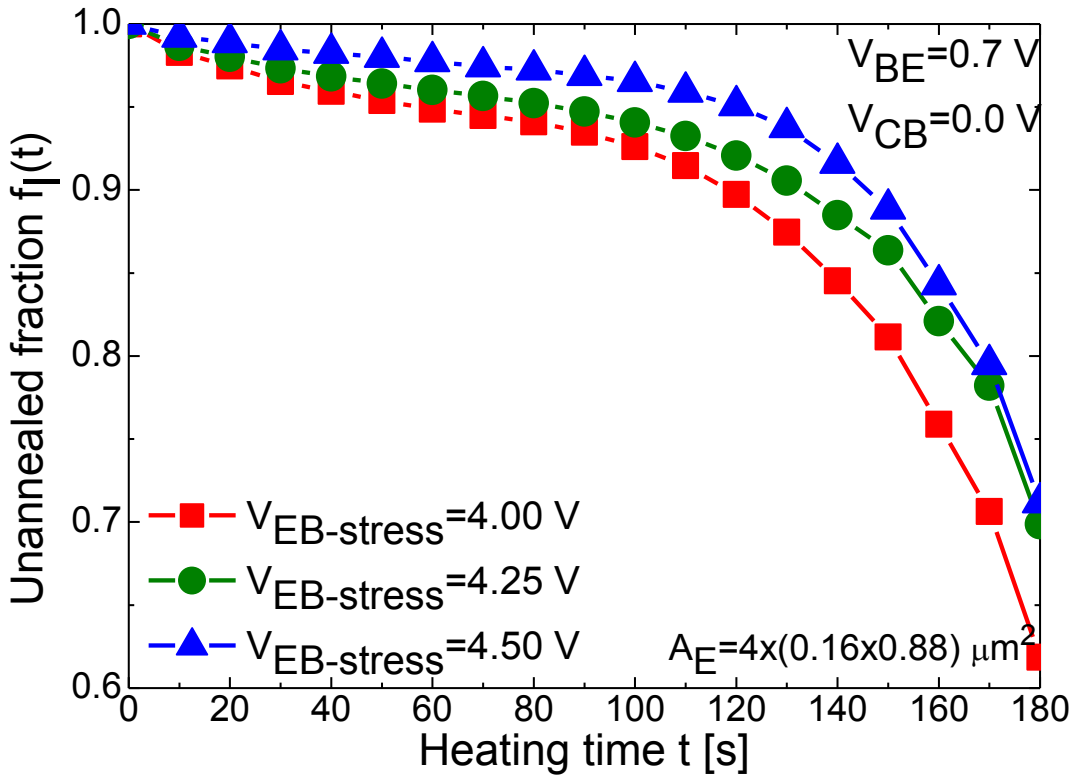
Output characteristics of a fresh sample



$$P_D = V_{CE} \cdot I_C + V_{BE} \cdot I_B$$
$$T_J = T_A + R_{TH} \cdot P_D$$

Each bias point was applied for 10s and alternated to the measurement of the Gummel-plot at V_{CB}=0

Self-heating recovery results vs. stress voltage

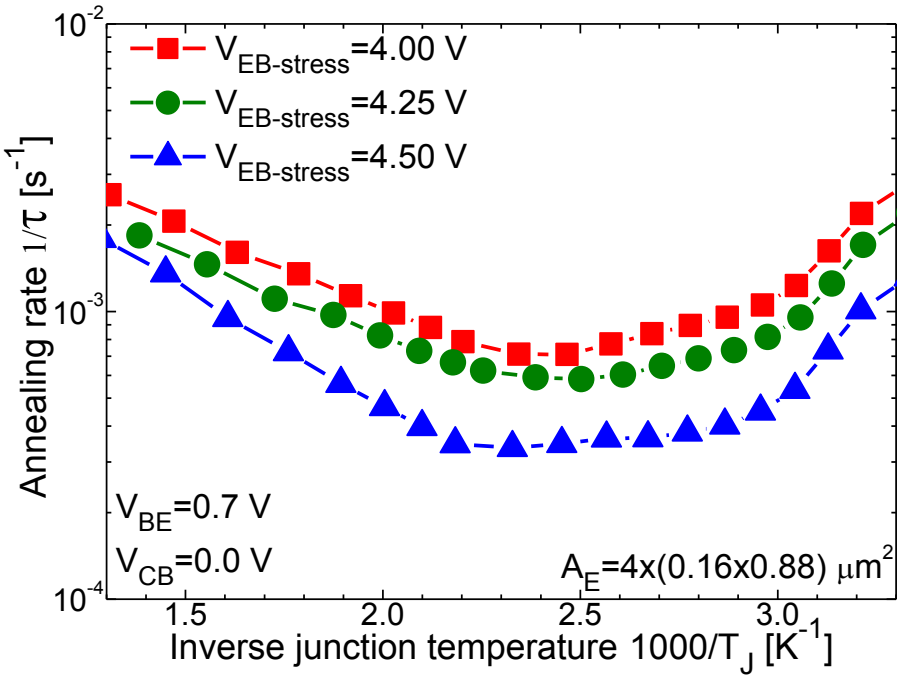


$$f_I(t) = \frac{I_B(t)}{I_B(0)}$$

- $f_I(t)$ increases with the heating time
- Weaker recovery when the stress voltage was stronger

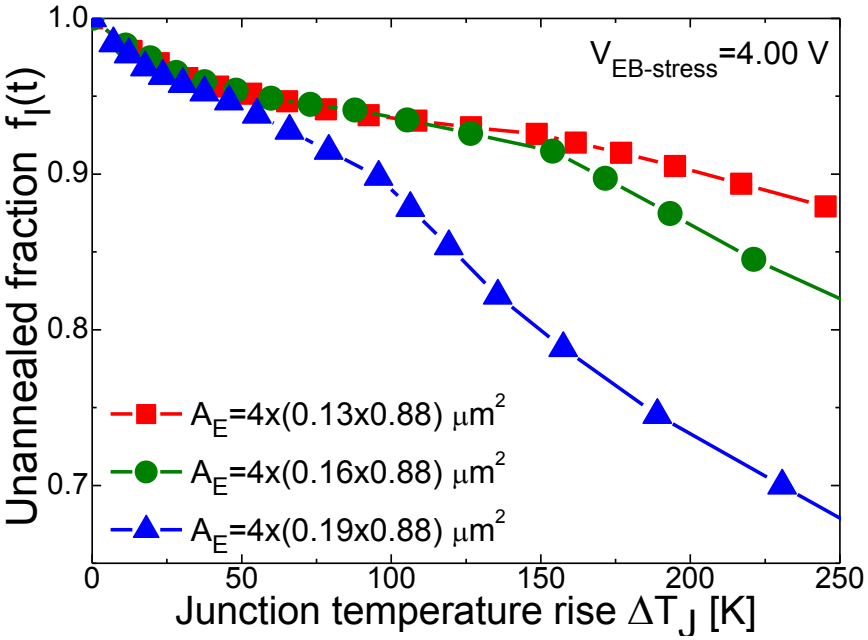
Self-heating recovery results vs. stress voltage

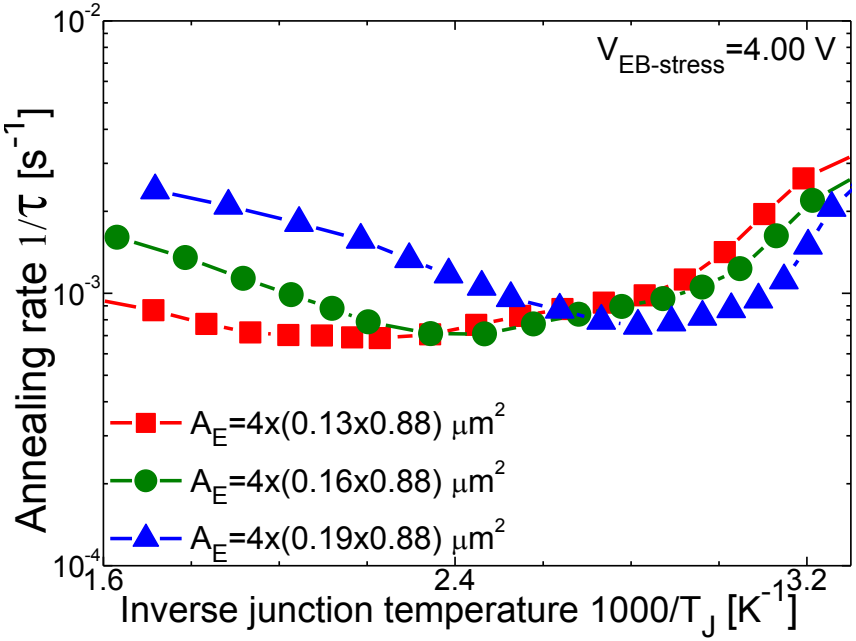
$$f_I(t) = \frac{I_B(t)}{I_B(0)} = \exp\left(-\frac{t}{\tau}\right)$$



Low temperature → detrapping of carriers in the oxide
High temperature → interface trap density passivation
Annealing rate not proportional to the trap density.
Modulation of the potential distribution due to trapped charges still occurs.

Self-heating recovery results vs. geometry





1. Higher rate for smallest device; reduction as the temperature increases
2. The largest device is the fastest to recover; increase with temperature

Self-heating recovery results

Constant self-heating and thermal annealing

1 h (ΔT=200 C) + 8 h (T_A=125 C) → T_J≈300 C

I_B % recovery of HBT #2 @ V_{BE}=0.5 V and V_{BC}=0.0 V

HBT #2	***SH (180s)***	***SH+T (1+8 h)***
4.00	37%	43%
4.25	25%	34%
4.50	21%	42%

Recovery is faster for the strongly stressed devices

Annihilation of interface traps finally prevails

Outline

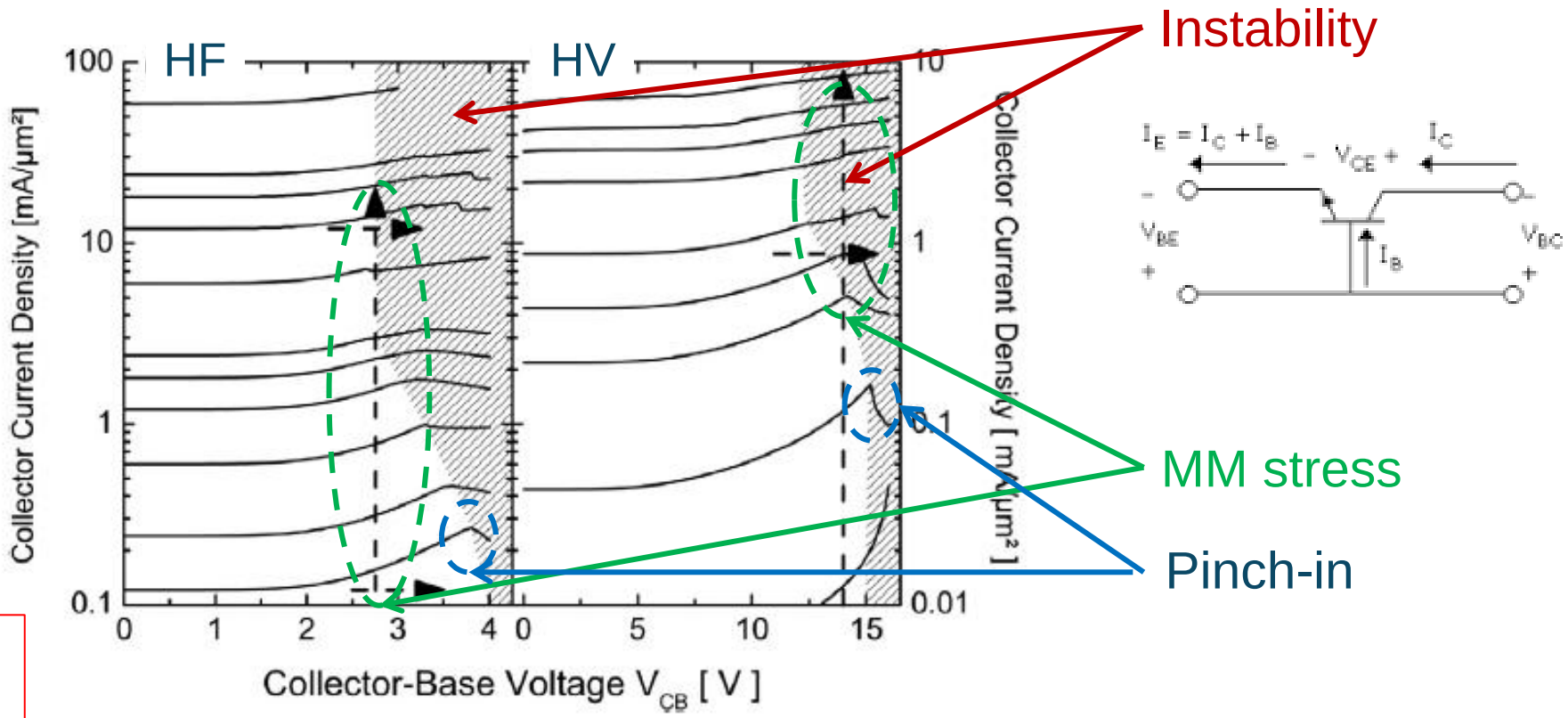
- Reverse emitter-base stress
  - Methods and techniques
  - Evaluation and modeling of results
  - Recovery experiments
- Mixed mode stress
  - Evaluation of results, modeling and TCAD
  - Recovery experiments
- Stress at the SOA edge
  - Evaluation and modeling of results
  - TCAD and SHE simulations

Mixed-mode stressed devices

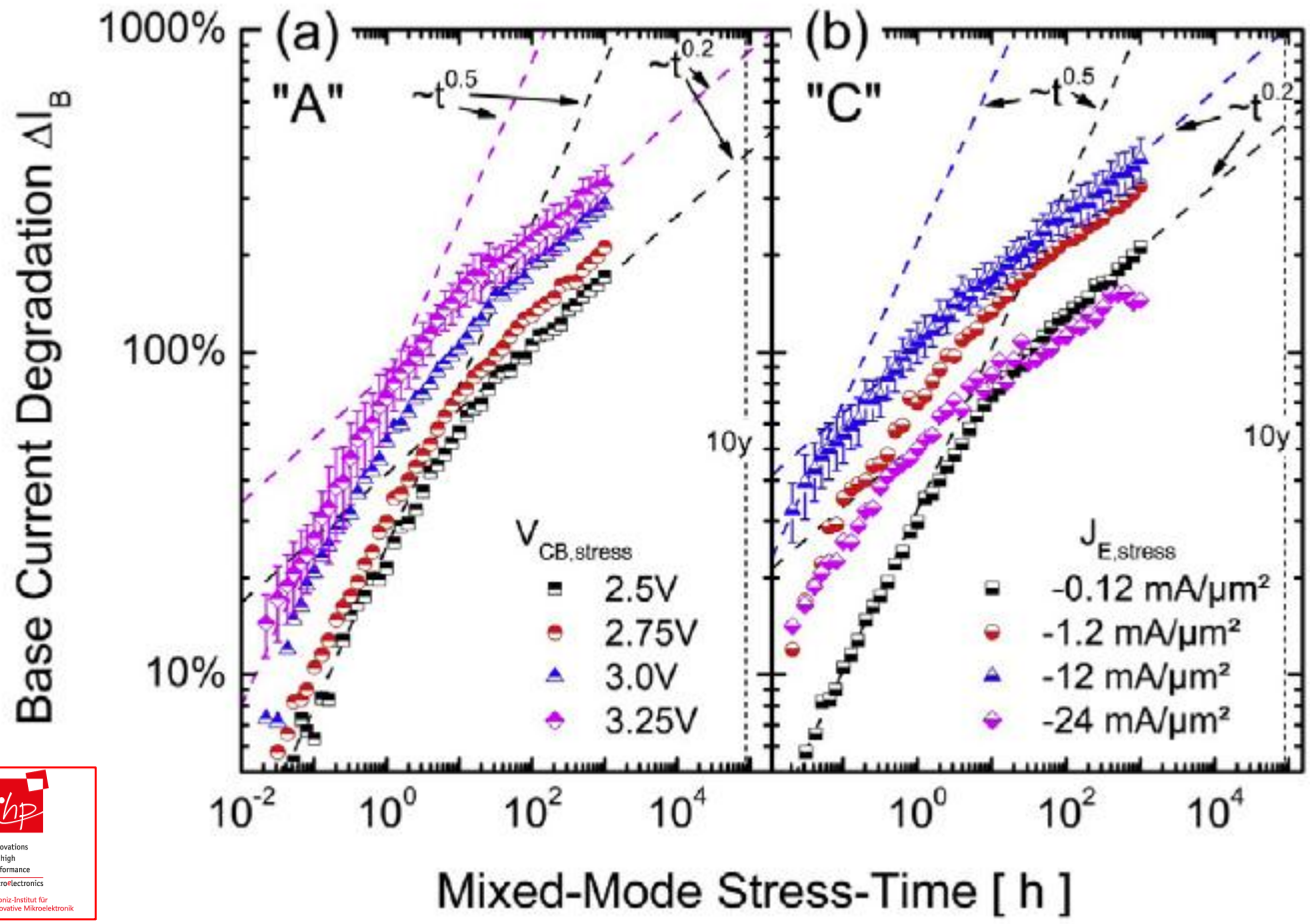
	$A_E=W_E x L_E$ [μm^2]	f_{MAX}/f_T [GHz]	BV_{CEO} [V]	BV_{CBO} [V]	BV_{EBO} [V]
HS HBT	0.16x0.52	300/250	1.7	5	1.8
HV HBT	0.22x1.04	120/45	3.7	15	1.9

Mixed-mode stress and instability

Mixed-mode stress (high J_E and high V_{CB})



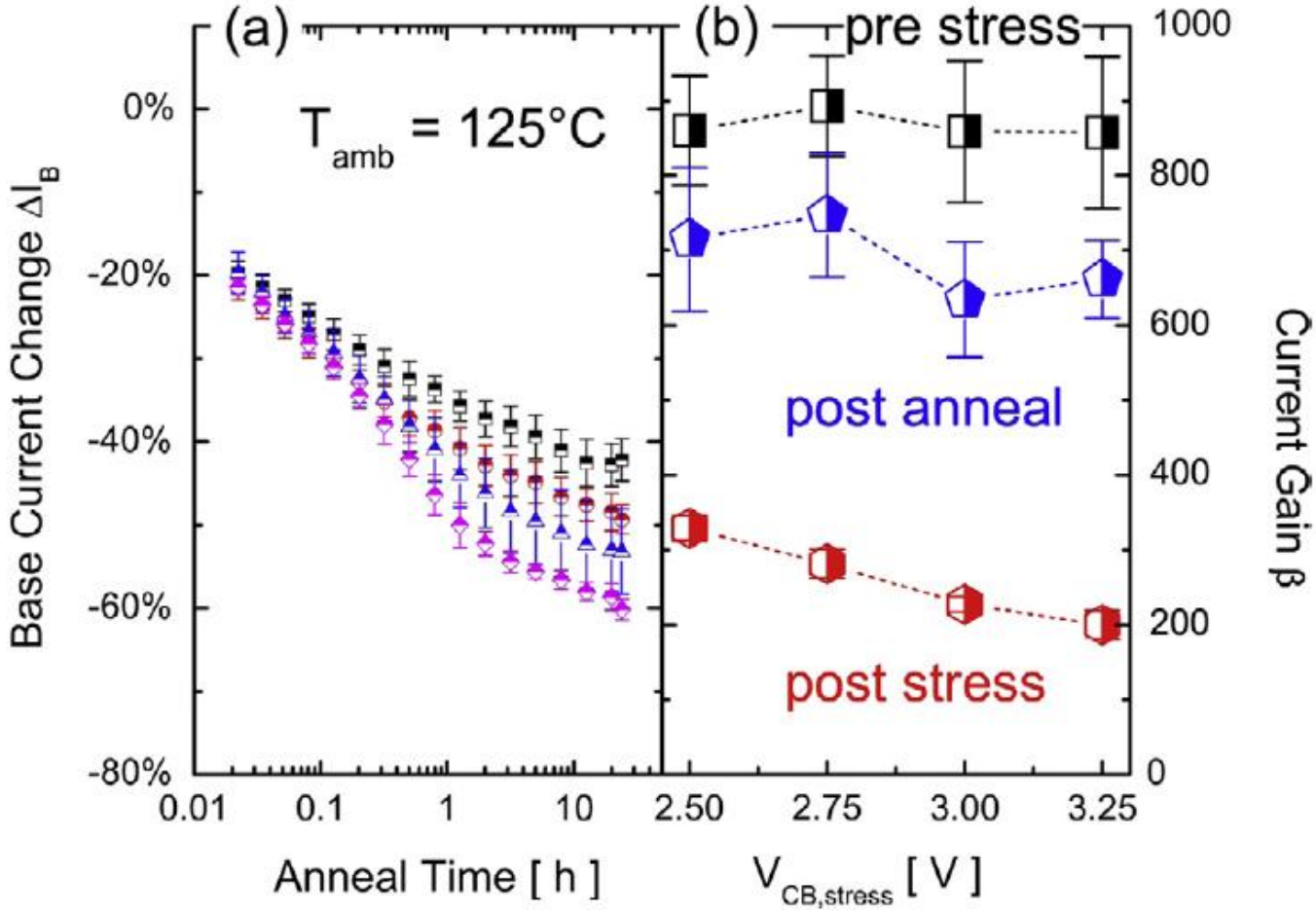
Mixed-mode stress results



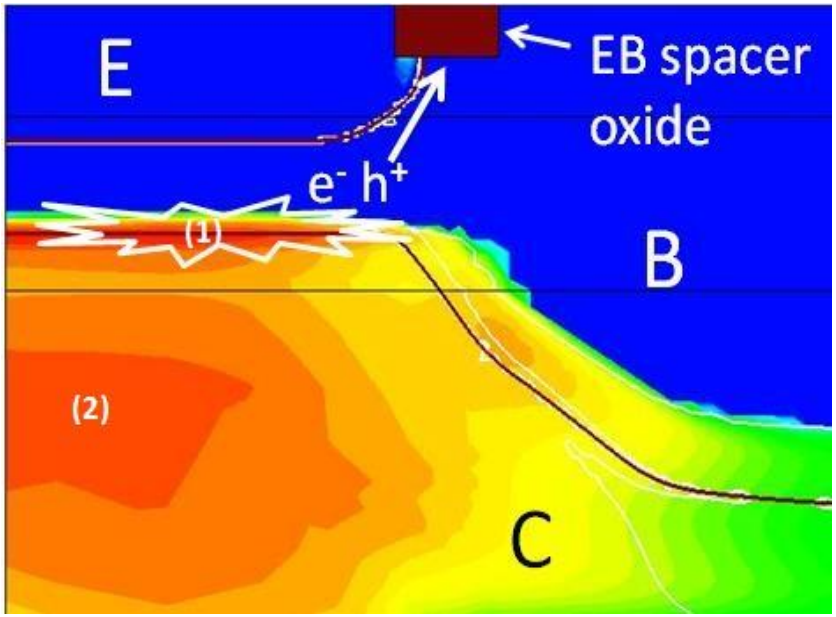
$$N_{it}(t) \sim (D \cdot t_{stress})^{\alpha}$$

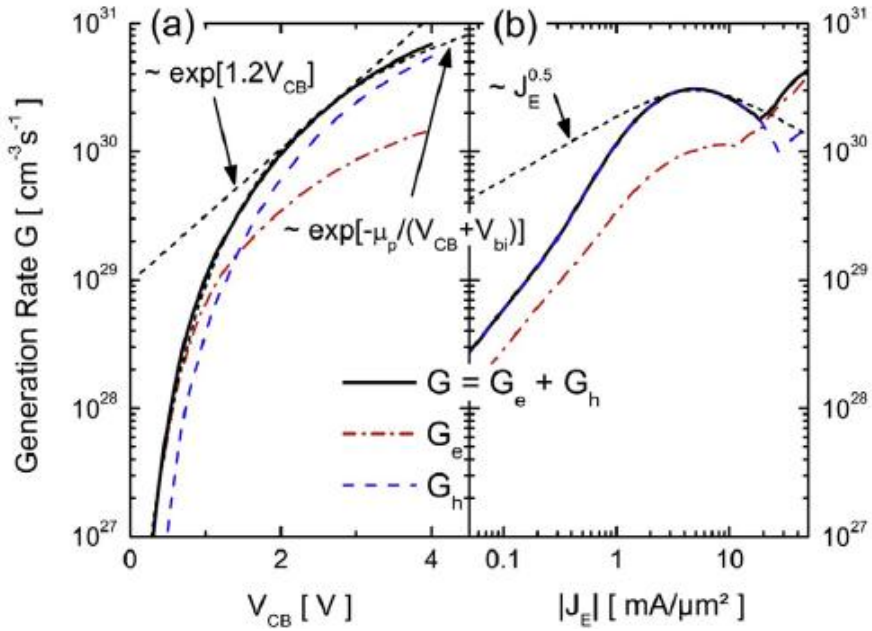
$$\Delta I_B \propto (I_E \cdot t_{stress})^{0.5}$$

Mixed-mode recovery results



Mixed-mode stress and TCAD





Outline

- Reverse emitter-base stress
  - Methods and techniques
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  - Evaluation of results, modeling and TCAD
  - Recovery experiments
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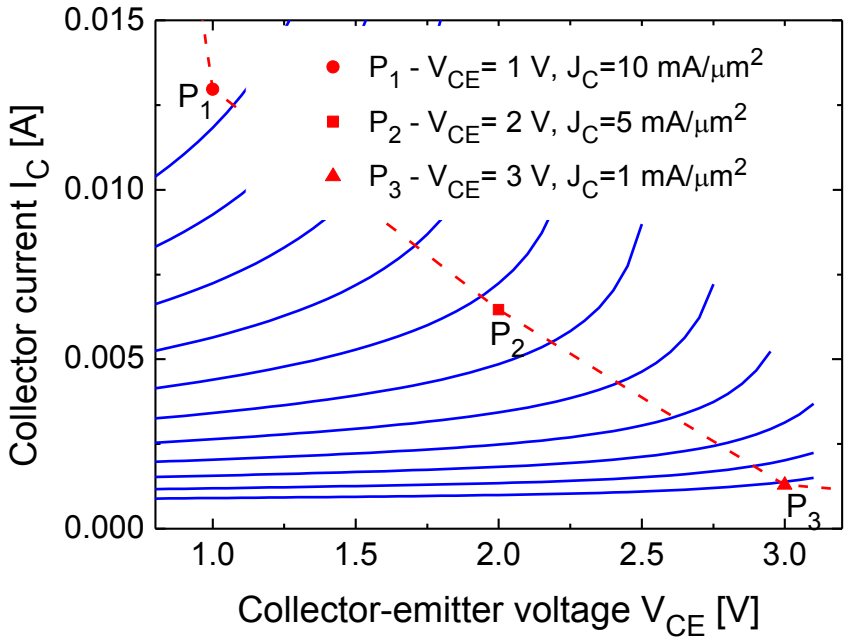
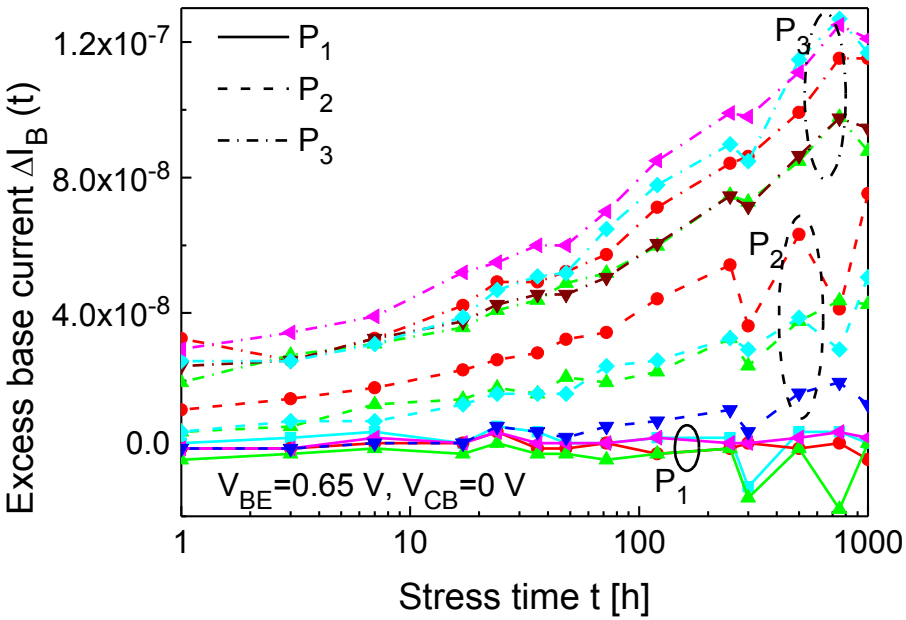
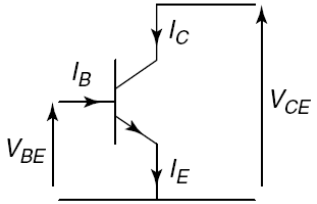
  - Evaluation and modeling of results
  - TCAD and SHE simulations

Stress experiments at the SOA edge

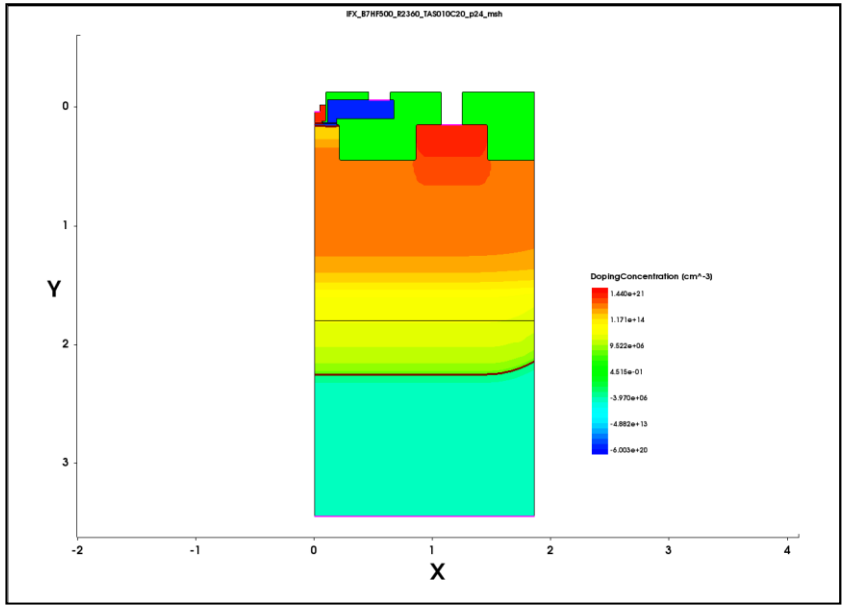


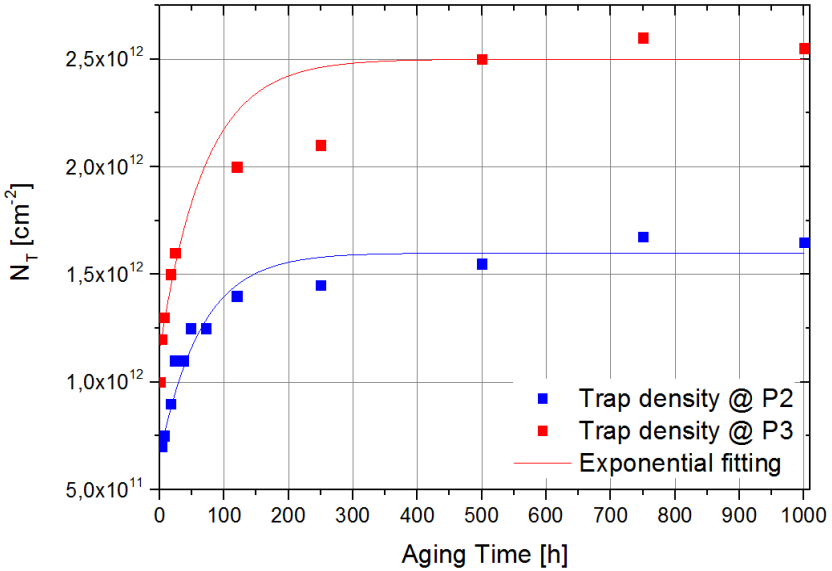




TCAD simulation of the aging at the SOA edge

Simulation of the aging dynamics adding trap density at the EB junction/EB spacer interface over stress time in the TCAD.





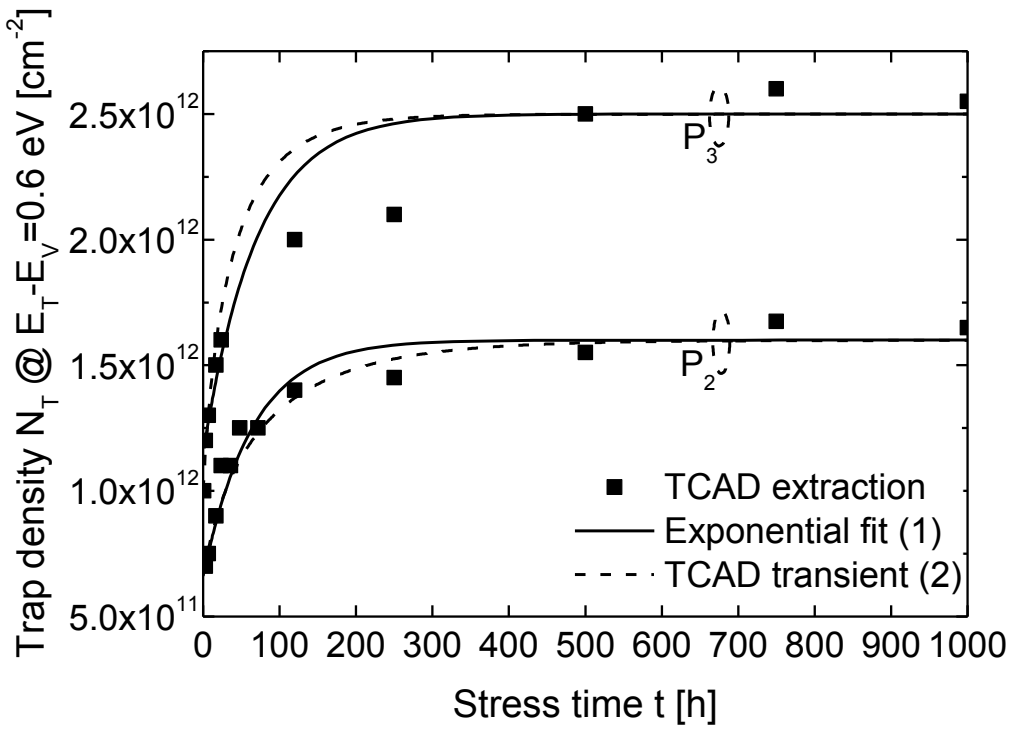
$$N_T(t) = N_{T,final} \cdot \left(1 - \left(1 - \frac{N_{T,initial}}{N_{T,final}}\right) \exp\left(-\frac{t}{\tau}\right)\right)$$

TCAD simulation of the aging at the SOA edge

Calibration of the aging dynamics models available in TCAD.

$$\frac{dN_T(t)}{dt} = \nu N - (\gamma + \nu) N_T(t)$$

$$\nu = \frac{N_{T,f}}{\tau \cdot N} \quad and \quad \gamma = \frac{1}{\tau}\left(1 - \frac{N_{T,f}}{N}\right)$$

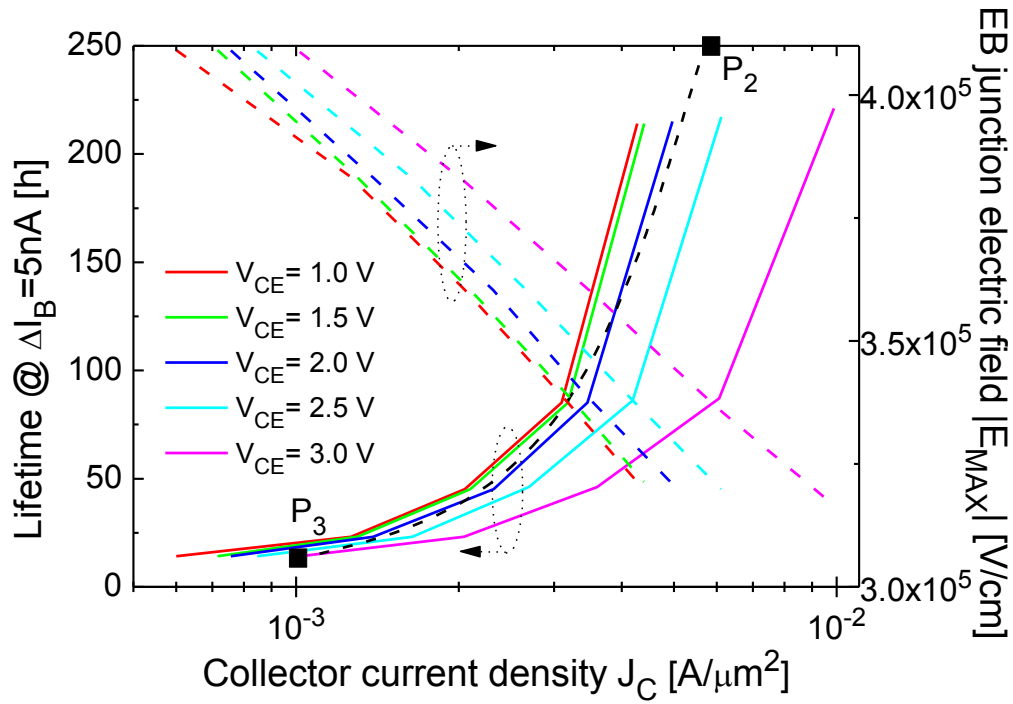


TCAD simulation of the aging at the SOA edge

Simulation of the aging dynamics using degradation models available in TCAD.

$$\frac{dN_T(t)}{dt} = \nu N - (\gamma + \nu) N_T(t)$$

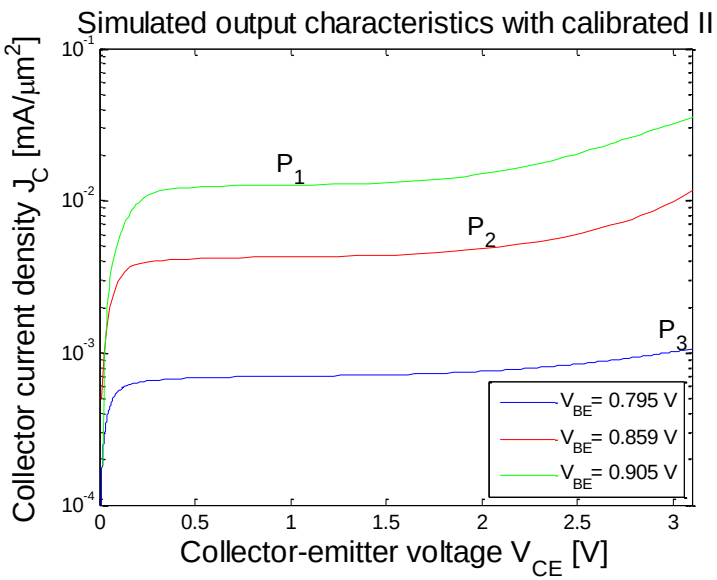
$$\nu = \frac{N_{T,f}}{\tau \cdot N} \quad and \quad \gamma = \frac{1}{\tau}\left(1 - \frac{N_{T,f}}{N}\right)$$

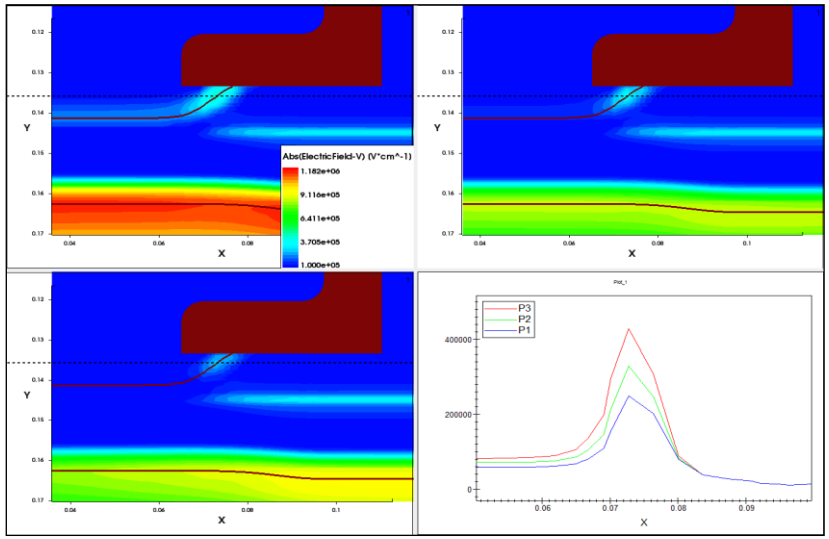


$$\frac{dN_T(t)}{N_{T,final}} = K_{T,final}^{N-(\gamma+\nu)} N_T(t) \left(1 - \left(1 - \frac{N_{T,initial}}{N_{T,final}}\right) \exp\left(-\frac{t}{\tau}\right)\right)$$

TCAD simulation of the aging at the SOA edge

Simulation of the aging conditions





P3 most effective degradation

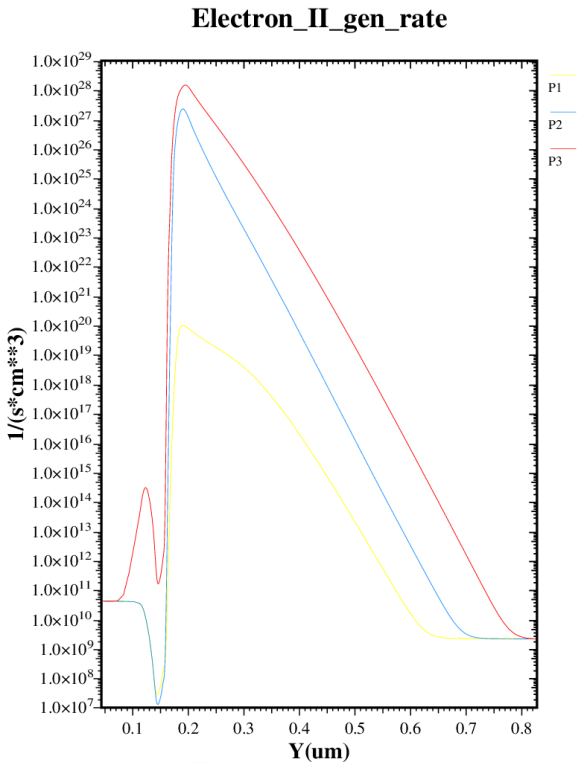
$G^{ii}(P2)=G^{ii}(P3)$ in the B-C RCS

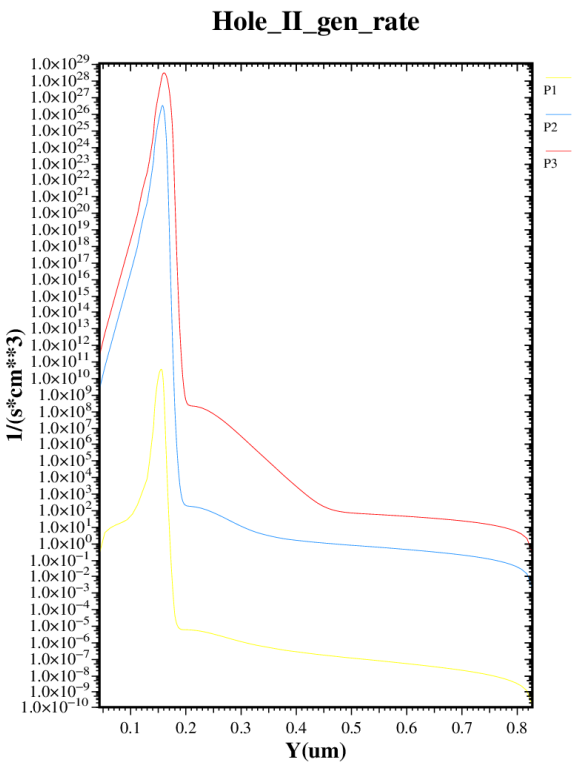
|E| @ EB spacer increases from P1 to P3 (<u>second order effect</u>)

$$\frac{dN_T(t)}{N_{T,final}} = K_{T,final}^{N-(\gamma+\nu)} \left(1 - \left(1 - \frac{N_{T,initial}}{N_{T,final}}\right) \exp\left(-\frac{t}{\tau}\right)\right)$$

SHE simulation of the aging at the SOA edge

Tool based on the spherical harmonic expansion solution of the BTE.
More reliable results: hot carrier holes included.

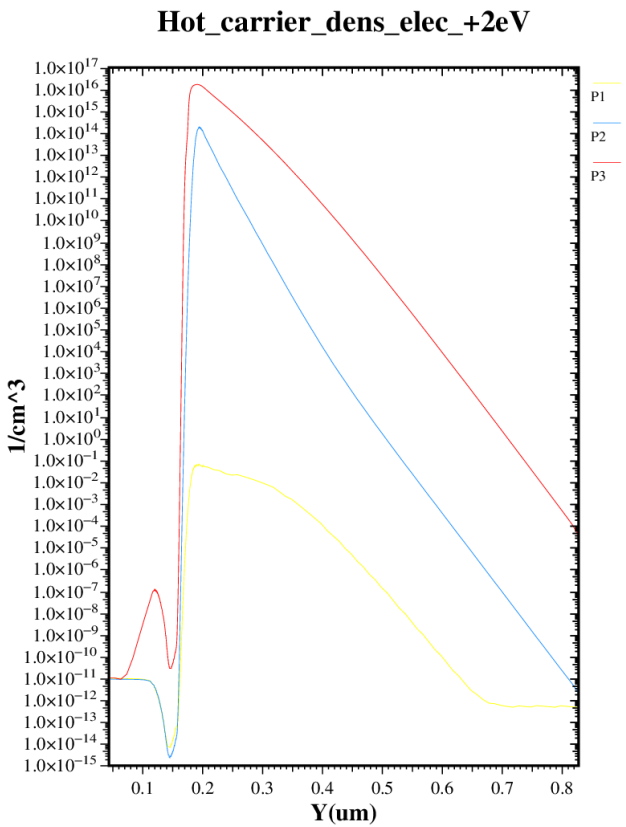


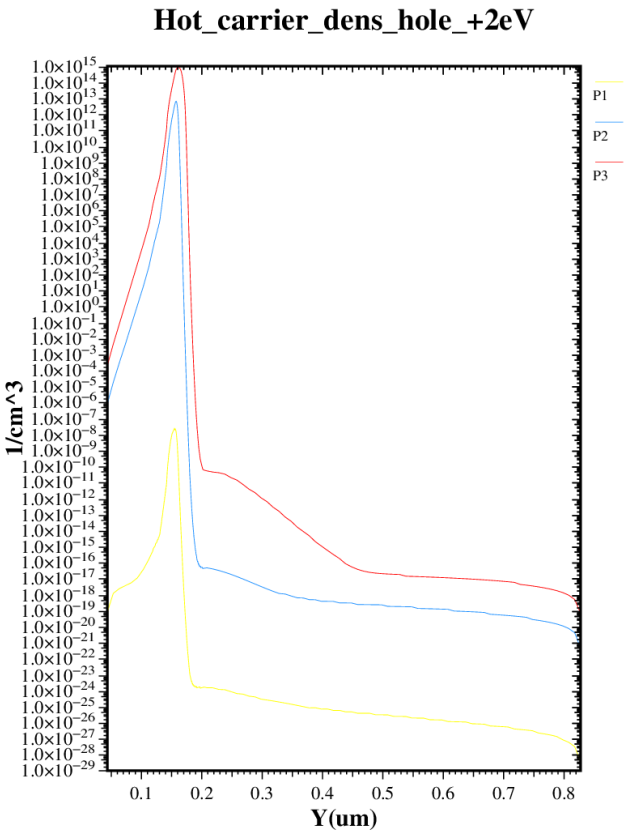


$$\frac{dN_T(t)}{dt} = K_{T,final}^{N-(\gamma+\nu)} N_T(t) \left(1 - \left(1 - \frac{N_{T,initial}}{N_{T,final}}\right) \exp\left(-\frac{t}{\tau}\right)\right)$$

SHE simulation of the aging at the SOA edge

P3 has much more high energy holes than P2.





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- I thank Klaus Aufinger and Gerhard Fischer, with IFAG and IHP, respectively, for providing experimental data and actively supporting the research cooperation.

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