Reliability aware circuit design

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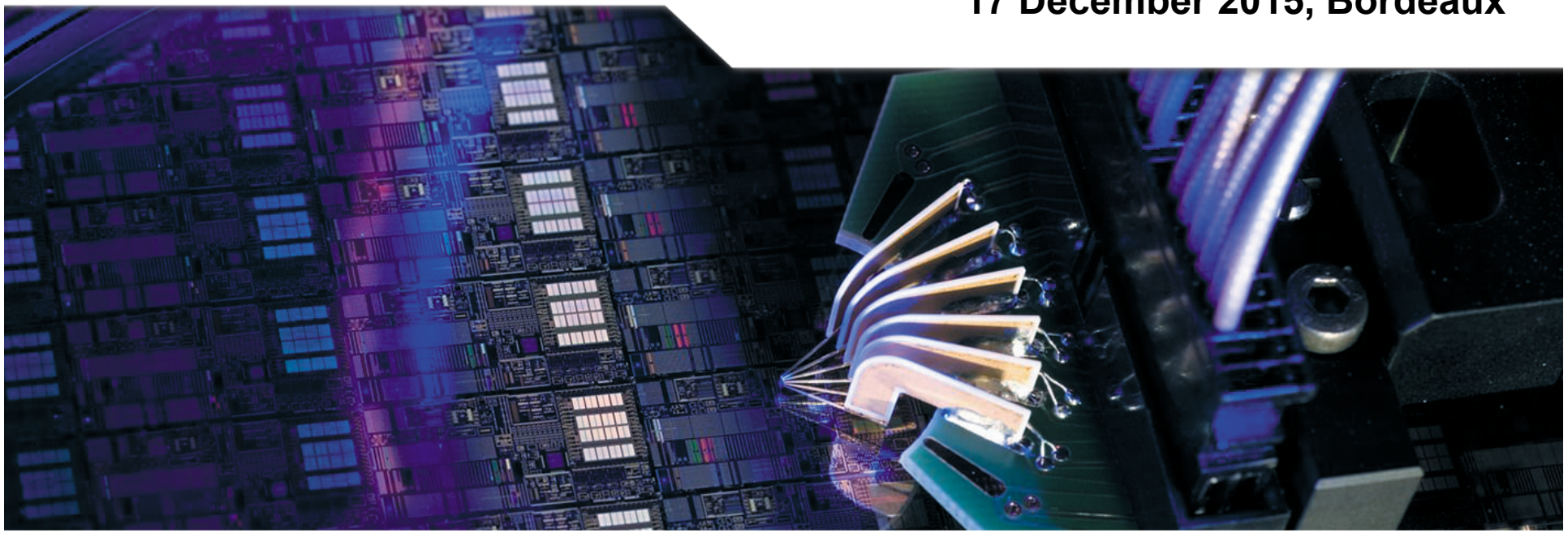
SiGe-THz devices:
Physics and reliability
17 December 2015, Bordeaux

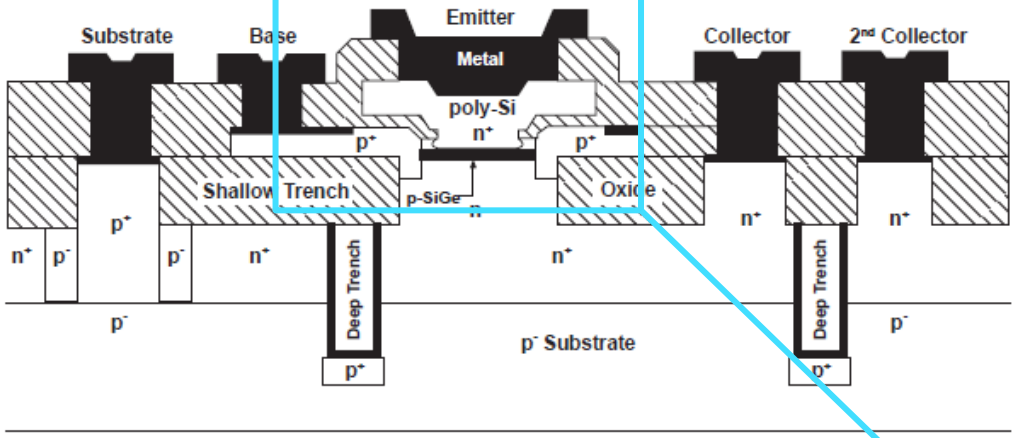


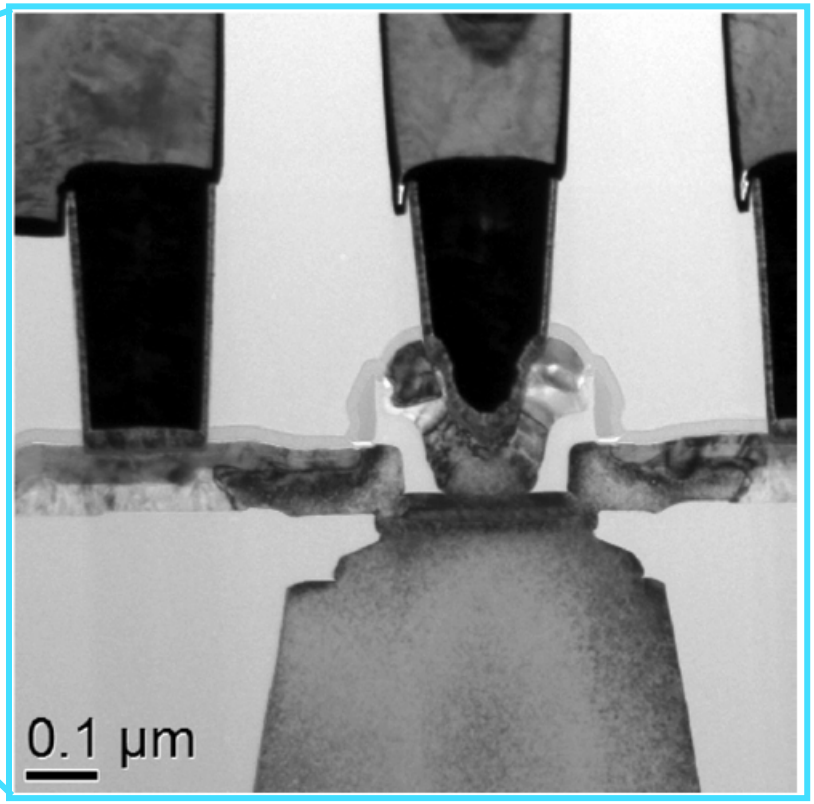
A European Project supported within the Seventh Framework Programme for Research and Technological Development

Outline

- Context :
  - Impact of dimensions shrinking on device operation margins
  - Impact of device operation margins on the device failure mechanisms
- From device to circuit reliability
  - Circuit aging simulation : Why ?
  - Circuit aging simulation : How?
    - Conventional way of doing
    - IMS proposal for circuit aging simulation
- A study case : InP Bipolar Submicron devices for robust design of 112Gb/s optical transport network
- DOTSEVEN SiGe HBT technology
  - Operation
  - Aging tests results
  - Aging laws implementation in HiCUM model
  - Towards the evaluation of reliability at circuit level

SiGe HBT basics : device architecture





$W_E x L_E$ = 0.13x2.69µm^2
f_T =300GHz
f_{MAX} =500GHz
J_C (peak f_T)=17mA/µm^2
BV_{CE0}=1.5V

Fox et al., ''Heterojunction bipolar transistor for Half-THz SiGe BiCMOS technology'', IEEE Electron Device Letters, Vol. 36, N°7, July 2015.

DOTSEVEN SiGe HBTs: Performances

Parameter	Unit	Infineon/IHP joint flow		IHP ref.*)	Infineon ref. **)
Process		DPSA-SEG		with EBL	DPSA-SEG without EBL
Layout		BEBC	BEC	BEC	BEC
$W_E \times L_E$	µm²	0.13×2.7		0.155×1.0	0.13×2.69
f_T	GHz	300	305	320	240
f_{max}	GHz	500	465	**445**	**380**
j_C (peak f_T)	mA/µm²	17		16	10
BV_{CEO}	V	1.5		1.75	1.5
BV_{CBO}	V	4.8		4.1	5.5
BV_{EBO}	V	1.5		1.35	2.3
$(R_B + R_E) \times L_E$	Ω ×µm	46	51	52	**86**
C_{CB}/L_E	fF/µm	1.45	1.4	2.2	**1.3**
C_{BE}/L_E	fF/µm	2.1	1.9	2.4	2.1
R_{SBi}	KΩ	3.0		2.6	2.6

Fox et al., ”Heterojunction bipolar transistor for Half-THz SiGe BiCMOS technology”, IEEE Electron Device Letters, Vol. 36, N°7, July 2015.

SiGe HBT basics : performances and scaling

- Device performance is improved through reduction in transit time and parasitic resistances and capacitances.
- f_T improvement is achieved through improvement in each of the delay components, related to f_T in the well-established approximation :

$$\frac{1}{2\pi f_T} = \tau_{EC} = \tau_E + \tau_C + \tau_B + \tau_{CSCL} \approx \frac{kT}{qI_C} C_{EB} + \left(\frac{kT}{qI_C} + R_C + R_E \right) C_{CB} + \frac{W_B^2}{\gamma D_n} + \frac{W_{CSCL}}{2\upsilon_{SAT}}$$

- f_T is probably the most common figure of merit for an RF transistor. However, in many cases the f_{MAX} figure of merit is more predictive for circuit performance.

$$F_{MAX} \approx \sqrt{\frac{f_T}{8\pi R_B C_{CB}}}$$

SiGe HBT basics : performances and scaling

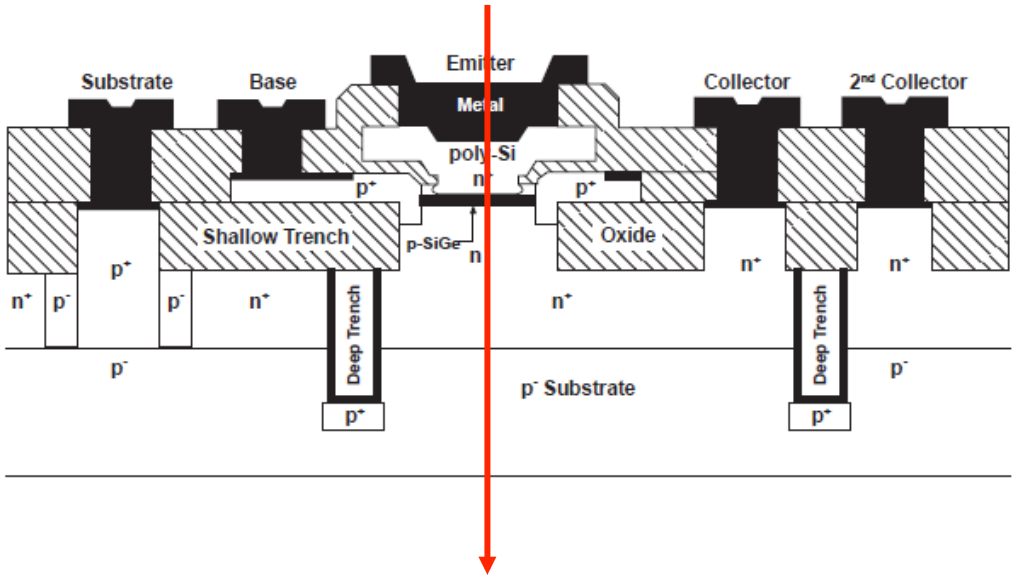
- Segmentation into stored minority charges and depletion charges:

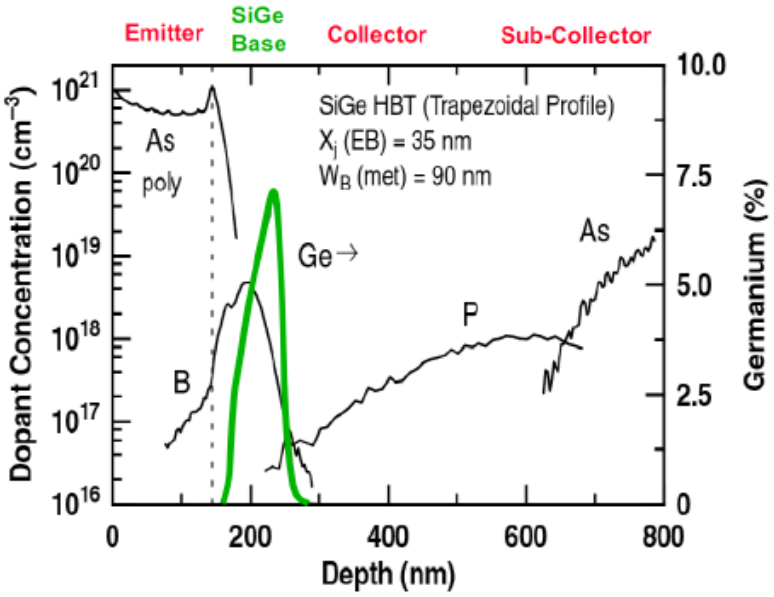
$$\frac{1}{2\pi f_T} = \tau_E + \tau_C + \tau_B + \tau_{BC} + \tau_{EB}$$

- Minority holes in emitter: $\tau_E = q\int_0^{x_{mE}} \frac{\partial p}{\partial j_C} dx$
- Minority electrons in base: $\tau_B = q\int_{x_{mE}}^{x_{mC}} \frac{\partial n}{\partial j_C} dx$
- Minority holes in collector: $\tau_C = q\int_{x_{mC}}^{L_x} \frac{\partial p}{\partial j_C} dx$
- EB depletion charge : $\tau_{EB} = q\int_{x_{mE}}^{x_{mC}} \frac{\partial (n-p)}{\partial j_C} dx$
- BC depletion charge: $\tau_{BC} = q\int_{x_{mC}}^{L_x} \frac{\partial (n-p)}{\partial j_C} dx$

Van den Biesen, J. J. H., ‘’A simple regional analysis of transit times in bipolar transistors, Solid State Electronics, Volume 29, Issue 5, p. 529-534, mai 1986

SiGe HBT basics : device epitaxial structure



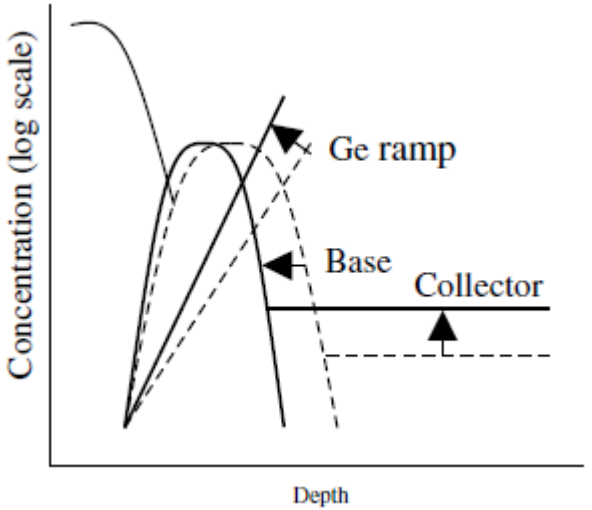


- Measured doping profile of a first-generation SiGe HBT from IBM

J.D. Cressler, "Emerging Reliability Issues for SiGe HBTs for Mixed-Signal Circuit Applications," IEEE Transactions on Device and Materials Reliability, vol. 4, pp. 222-236, 2004.

Impact of dimensions shrinking on HBT structure

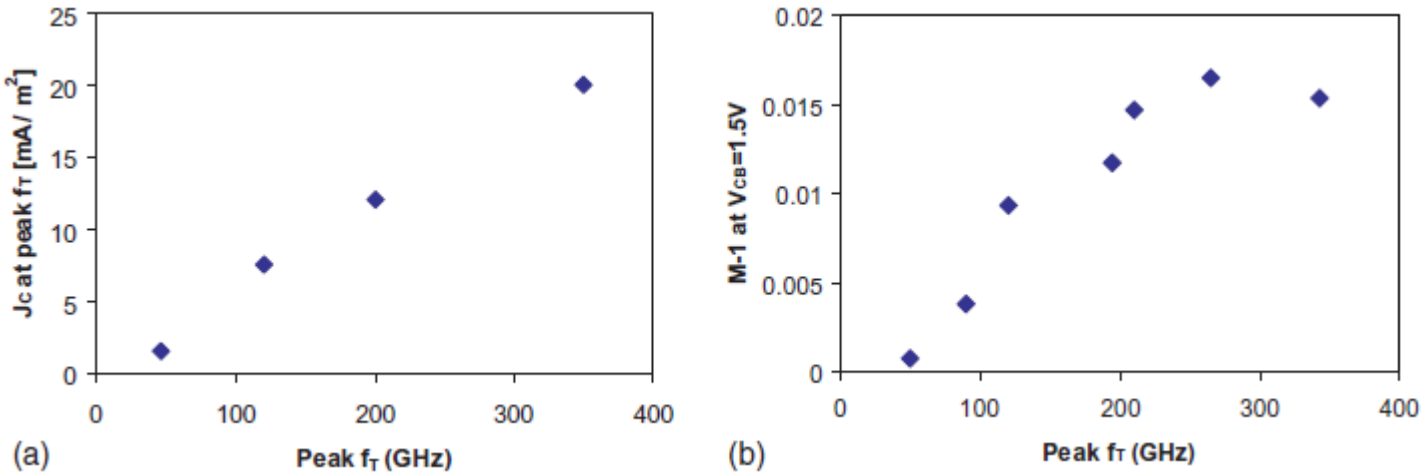
- SiGe HBT device scaling



Greg Freeman et al., ''Reliability and performance scaling of very high speed SiGe HBTs'', Microelectronics Reliability 44, pp397–410, 2004

	Emitter	Base	Collector
Structure	Replace Arsenic with Phos. Reduce interface layer	Narrow base Reduce base dose Increase Ge ramp Add Carbon Improve extrinsic structure	Increase concentration Improve extrinsic structure
Electrical	Lower R_E Higher I_B	Lower V_{BE} Reduce total R_B	Higher avalanche Higher peak f_T J_C Higher C_{CB}

Effect of collector design



- (a) peak f_T current density
- (b) excess collector and base current from avalanche in the collector–base space-charge region.

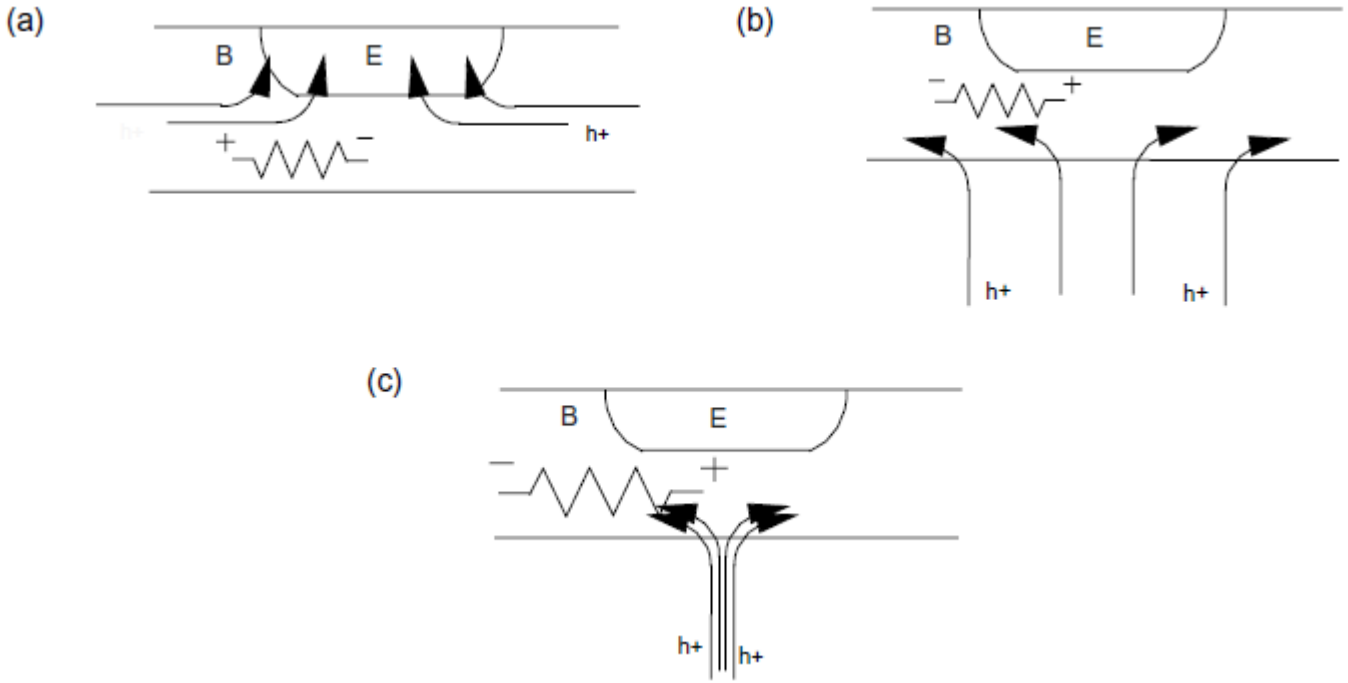
Greg Freeman et al., ''Reliability and performance scaling of very high speed SiGe HBTs'', Microelectronics Reliability, 44, pp397–410, 2004

Bipolar reliability overview and performance trend related issues

Operation region	Stress condition V_{BE}	Stress condition V_{BC}	Typical signature	Mechanism	Stress condition in typical circuit?	Trend with scaling	Remedy	Refs.
Reverse	–		Low bias I_B non-ideality	E–B oxide interface states	Limited	Neutral	Limit reverse voltage in design	[19–21]
Saturation	+	+	Low bias I_B non-ideality	E–B oxide interface states	Limited	Neutral	Limit saturation voltage in design	[22]
Forward mode	+	–	Low bias I_B non-ideality, parallel I_B shift, R_E shift, self-heating	E–B oxide interface states, poly–sc interface oxide, metal migration	Yes	Worse	Min. interface oxide, min. e-fields at surface, narrow W_E	[22–30]
Avalanche	+	–	Low bias I_B non-ideality, self-heating	E–B oxide interface states	Yes	Worse	Design robust to I_B variations, limit voltage in design	[33–35]

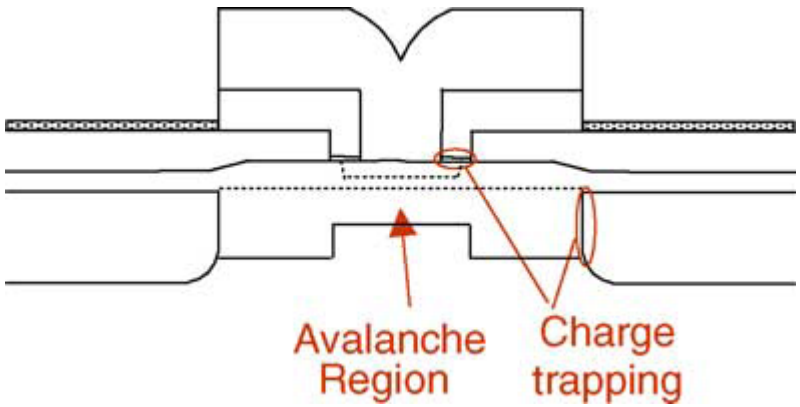
Greg Freeman et al., ''Reliability and performance scaling of very high speed SiGe HBTs'', Microelectronics Reliability, 44, pp397–410, 2004

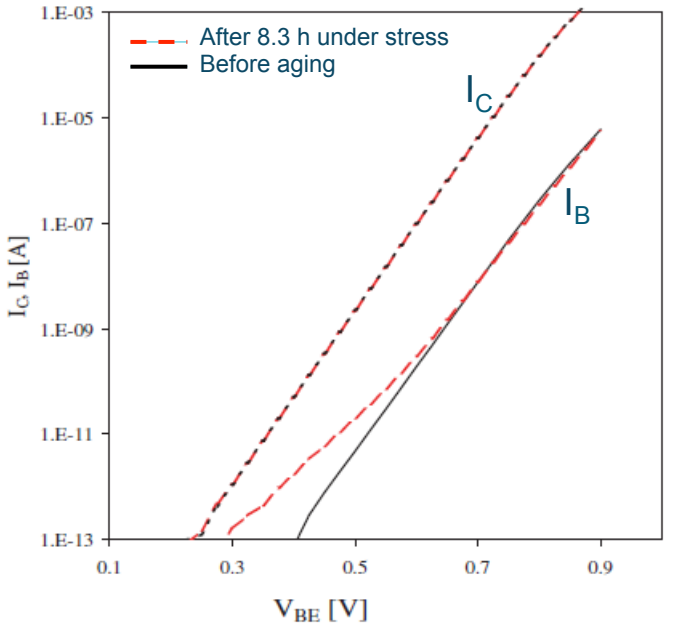
Avalanche effect on device operation



- (a) low V_{CB}
- (b) moderate avalanche
- (c) ‘‘pinch-in’’ resulting from high voltage drop across base resistance

Hot carrier generation from avalanche and trapping in dielectric layers





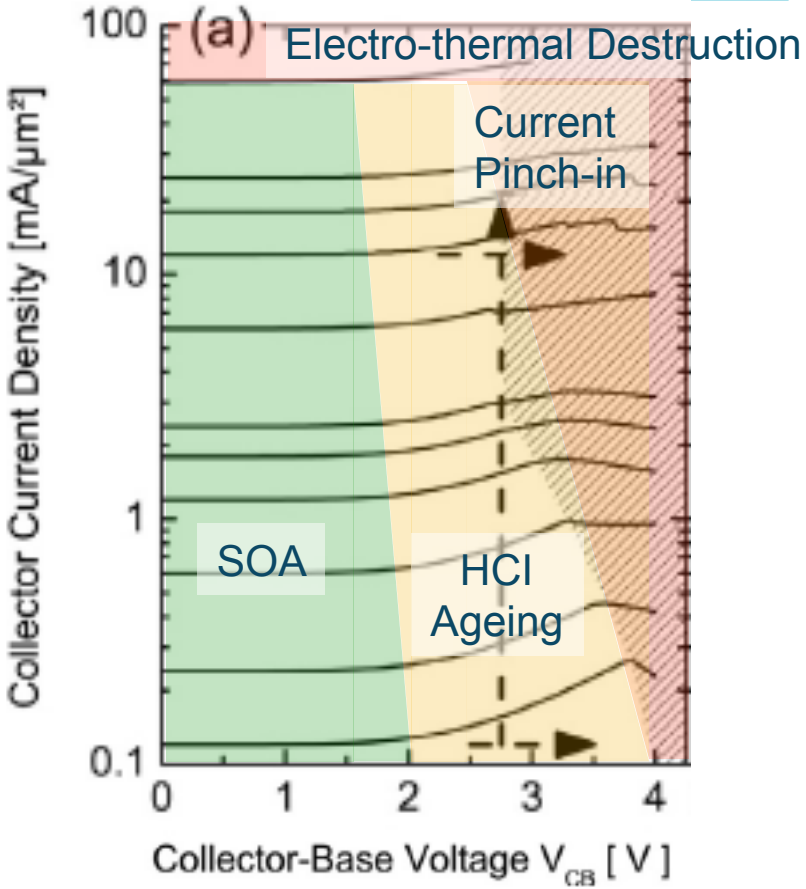
Avalanche generated base current degradation for 200 GHz SiGe HBT

- Emitter area: 0.12 x 2.0 μm^2.
- Stress conditions: V_{CB}=2.5 V, I_E=1.92 mA.
- Before aging and after 8.3 h under the stress

Greg Freeman et al., ''Reliability and performance scaling of very high speed SiGe HBTs'', Microelectronics Reliability, 44, pp397–410, 2004

Safe Operating Area :SOA

- Safe Operating Area
- High-performances HBT
  f_T/f_{MAX} = 250/300 GHz
- Common base configuration
- Forced J_E output characterictics
- Breakdown voltages:
  - BV_{CE0} = 1,7V
  - BV_{CB0} = 5,0V



G.G. Fischer , G. Sasso, “Ageing and thermal recovery of advanced SiGe heterojunction bipolar transistors under long-term mixed-mode and reverse stress conditions” Microelectronics Reliability 55, pp.498–507, 2015.

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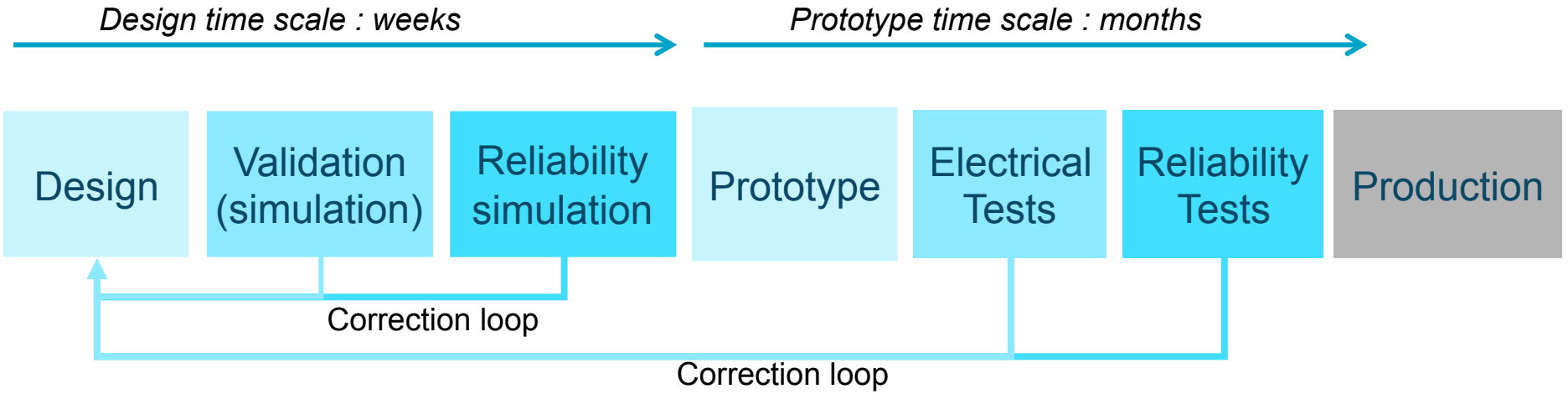
From device to circuit reliability

- How to predict the circuit reliability during the design ?
- Key points:
  - Taking into account mission profile (including signals)
  - Taking into account the circuit/transistor interaction
  - Relevance of electrical stress
- Device ageing test objective: wear out mechanisms

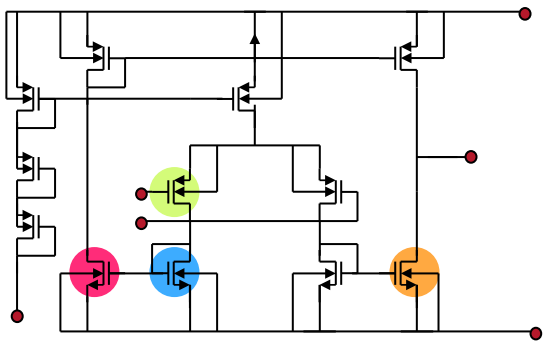
Aging circuit simulation : why ?



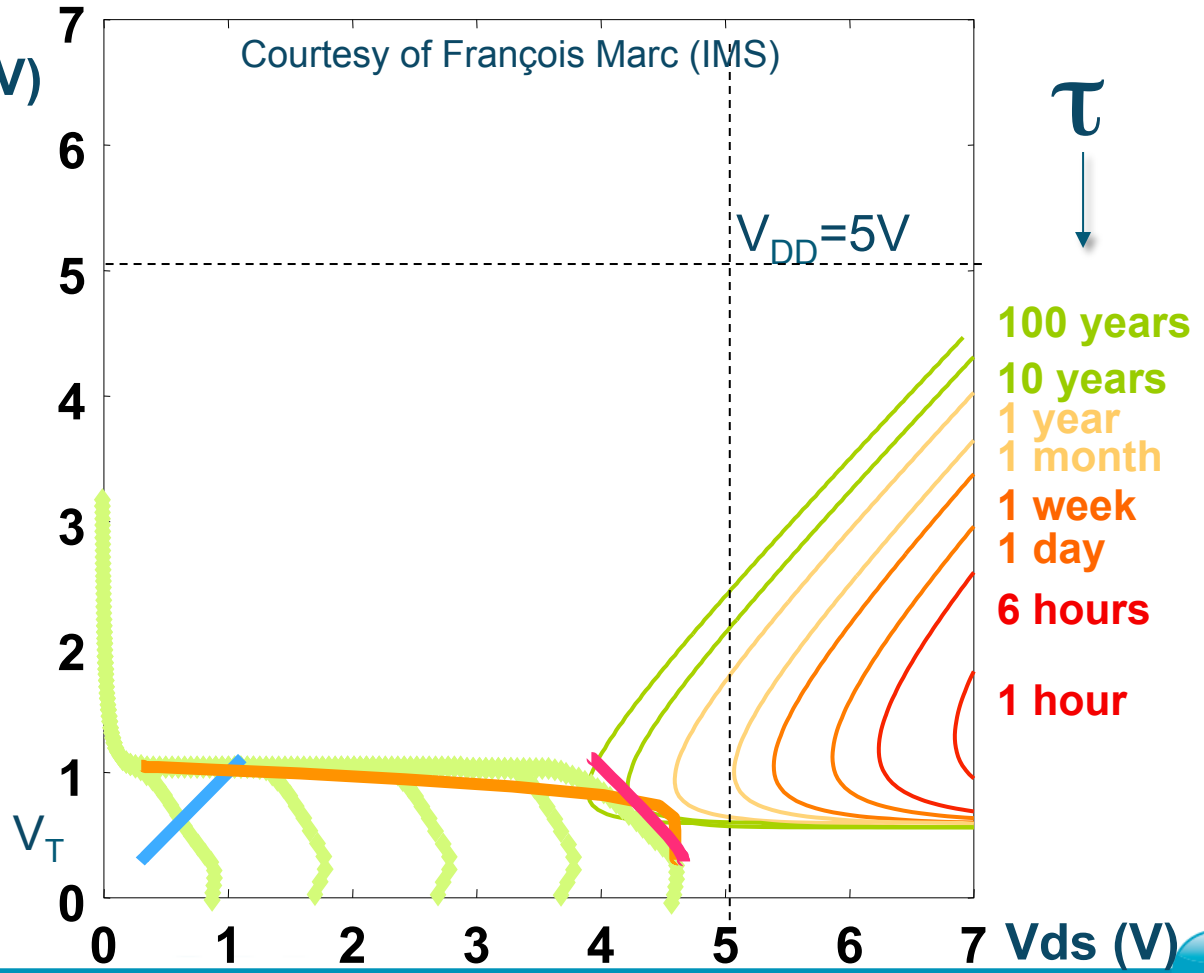
Design For Reliability :

- ✓ Predict during the design phase the effect of transistors and architecture choices on the circuit reliability according to the application

Effect of circuit operation on each transistor stress



Operationnal amplifier



Circuit reliability simulation

Simulations to predict the impact of transistor failure mechanisms on the circuit operation:

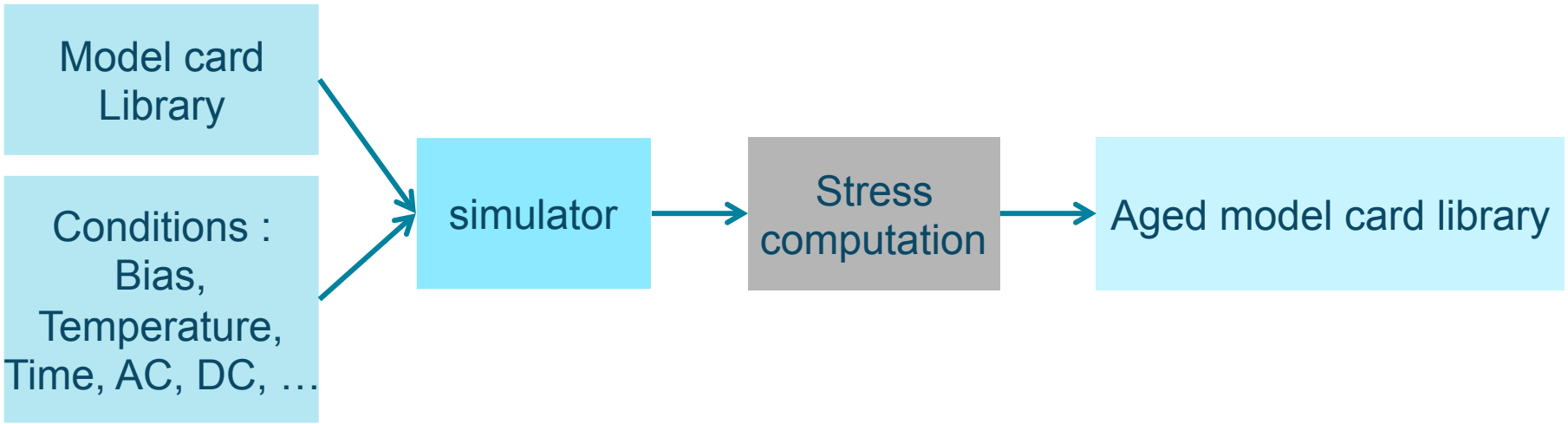
- life time
- electrical parameters
- outputs evolution

As a function of operating conditions:

- environment : temperature, pressure, radiations ...
- supply voltages
- Input signals

➢ *Circuit Aging simulation*

Conventional approach : Design in Reliability (DiR)

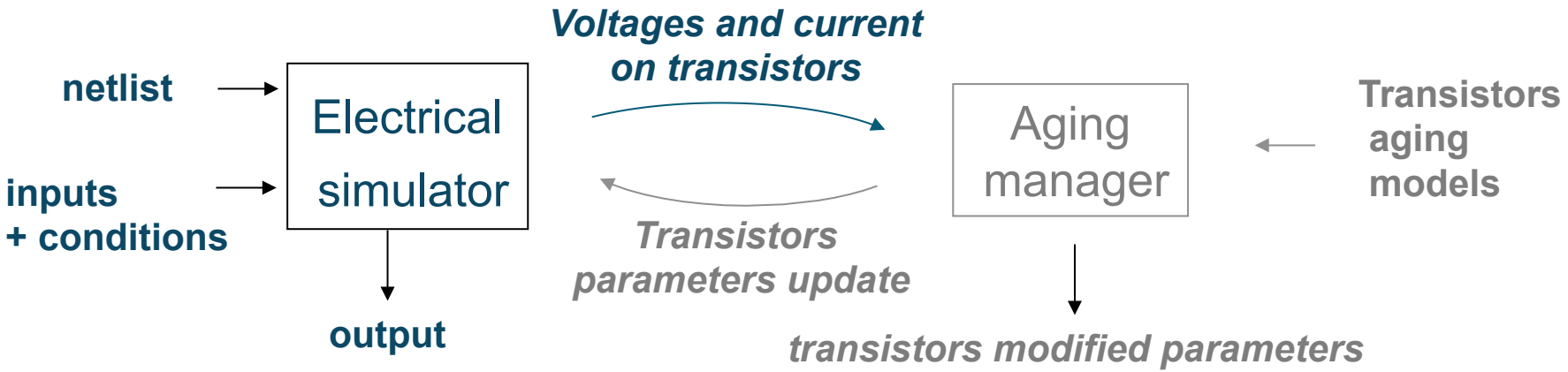


➢ *DiR model flow highlights interactions between simulator, stress computation program and model cards.*

S.Ighilahriz et al., ''Reliability study uner DC stress On mmW LNA, Mixer and VCO'', IEEE International Reliability Physics Symposium (IRPS), 2012

Design in Reliability (DiR): an iterative method

2 software's associated through an iterative method



➢ *A dedicated software has to be developed*

Circuit aging simulation : IMS approach

A single simulator (with VHDL-AMS or Verilog-A)

Transistor aging model

- Based on the transistor compact model
- Takes into account the aging models/laws/failure mechanisms (providing they are known)
- Need to access to model code

Requirements for circuit aging simulation

- Use VHDL-AMS or Verilog-A to build compact models including aging
  - Compact model code
  - Add physical quantities in the compact model
  - Implementation of the aging laws in the compact model
    - Physics of failure
    - Ageing tests @ transistor level
  - Change compact model parameters into (slowly) variable quantities
    - Parameters extraction of the failure laws
- Virtual acceleration of degradation mechanism to obtain electrical times (<1 second) and ageing time (> 1 week) in a same simulation

➢ *Versatility and efficiency for ageing simulation*

Benefits of a “real-time” dynamic aging model

- Directly integrated in CAD commercial software tools
  - ➢ in PDK to ease the circuit designer handling
  - ➢ can be realized easily in VerilogA language
- Use compact model with slowly varying parameters as a function of bias and temperature
  - ✓ under real circuit operating conditions
- Small performance penalty
  - ✓ compiled code

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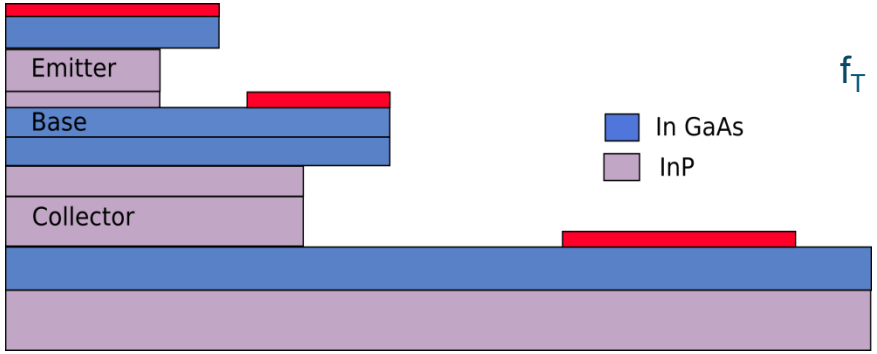
A study case : InP Bipolar Submicron devices for robust design of 112 Gb/s optical transport network

This methodology is not process specific

Alcatel·Lucent

- Alcatel Lucent
  - InP/InGaAs HBT technology
- Challenging applications
  - High speed optical communications systems working above 100 Gbit/s per channel
- Very high reliability requirements
  - e.g., submarine communication systems
- Accurate reliability modeling is mandatory

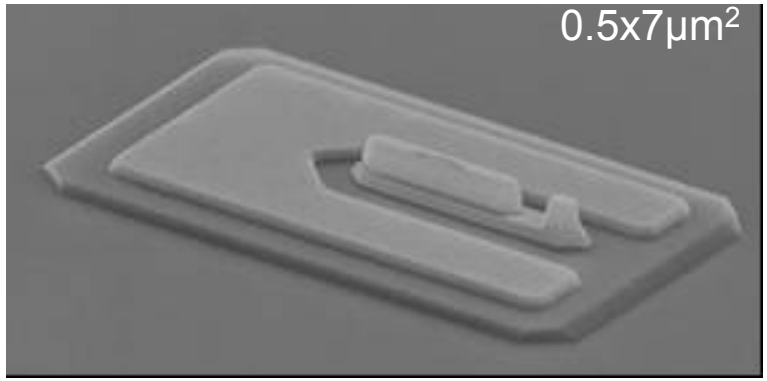


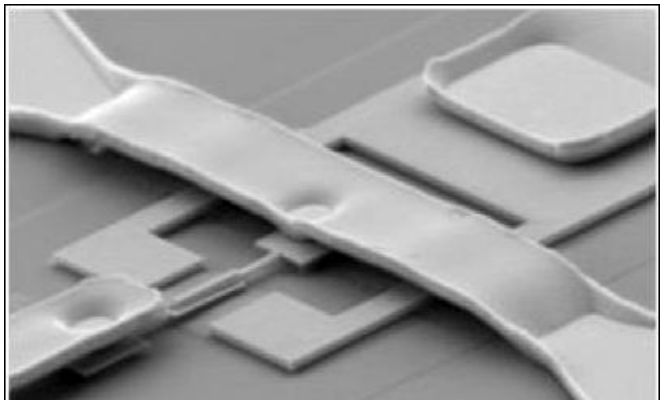
$0.5x7\mu m^2$

f_T and f_{MAX} are around 350 GHz

InP HBT technologies

- In general, less complicated implementation than Si technologies
  - Two metal levels
  - Triple mesa process technology
  - Mesa isolation
- Suffer from important self heating mechanism





Courtesy of Mohammed Zaknoune (IEMN)

Grandchamp et al., ''Trends in submicrometer InP-based HBT architecture targeting thermal management'', IEEE Trans. On Electron Device, pp. 2566-2572 , Vol. 58, N°8, 2011.

HiCuM compact model

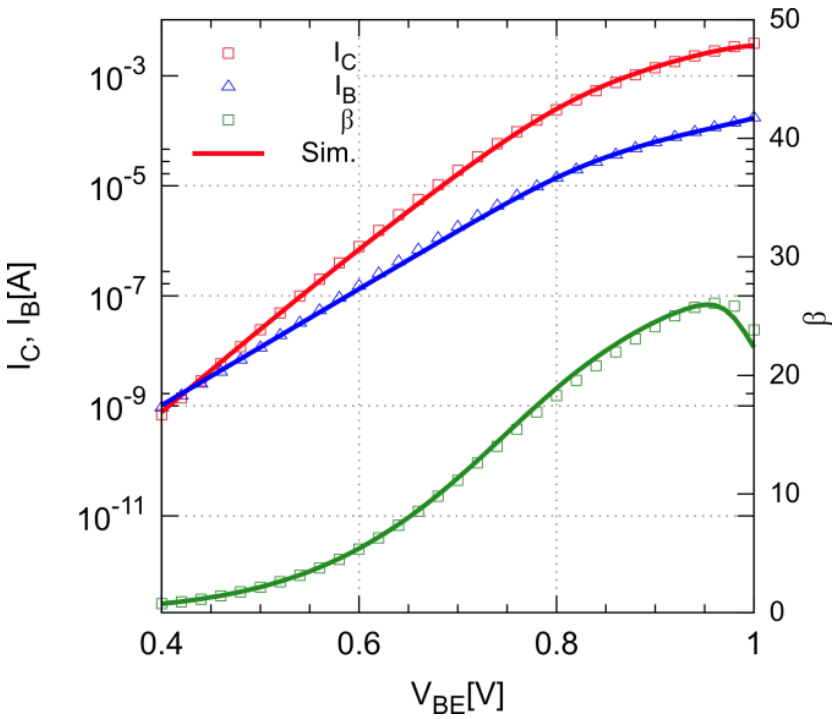
Why choosing HiCuM L2 v2.30 compact model ?

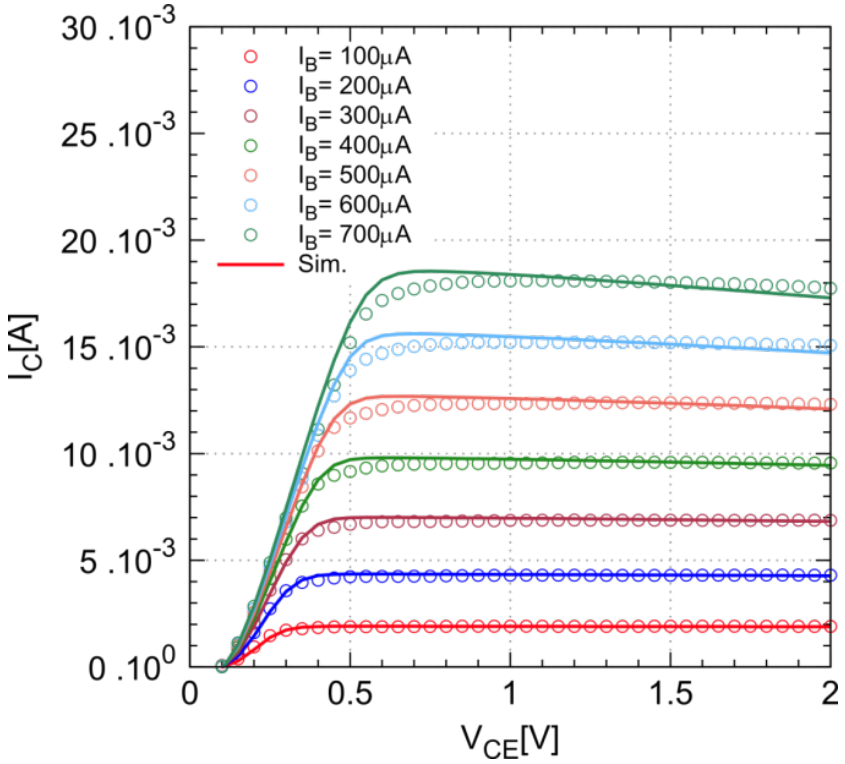
- CMC labeled model (Available in most commercial simulators)
- VerilogA code available
- HiCuM accuracy + Specific improvements of version v2.30
- Modeling of advanced HBTs

➢ Parameter extraction for good initial model is already challenging

INITIAL parameter extraction : DC operation

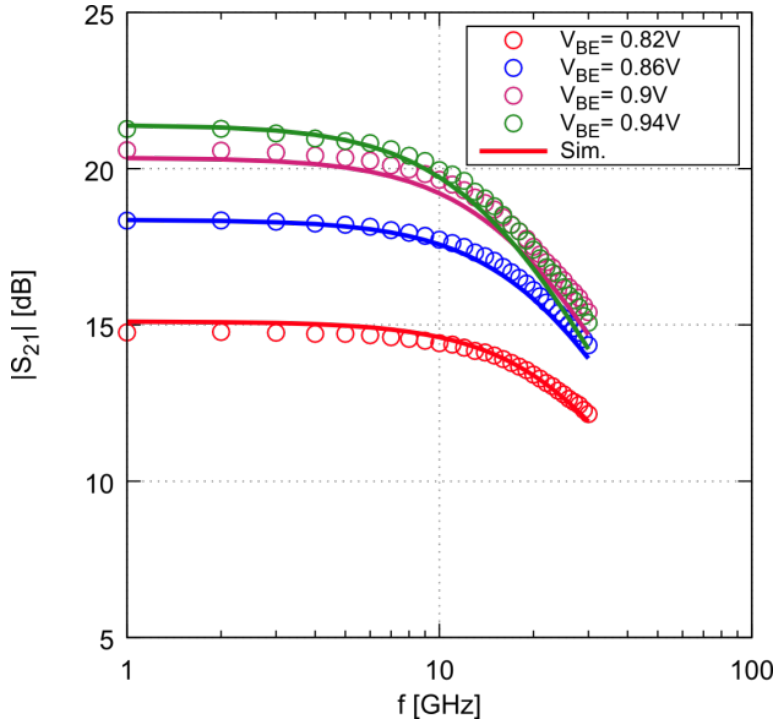
Results for T7 (W_E=0.5µm and L_E=7µm)

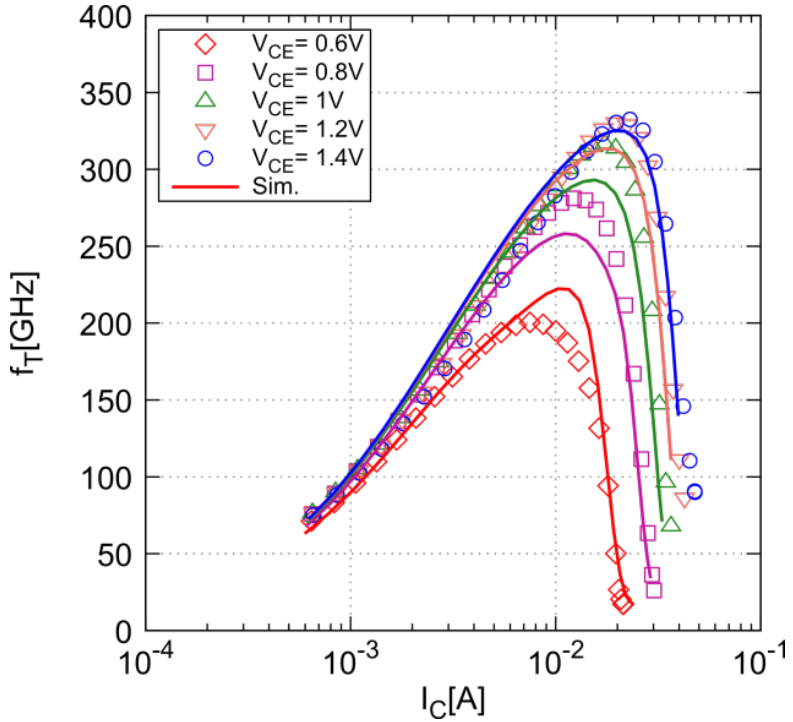




Initial parameter extraction : Dynamic operation

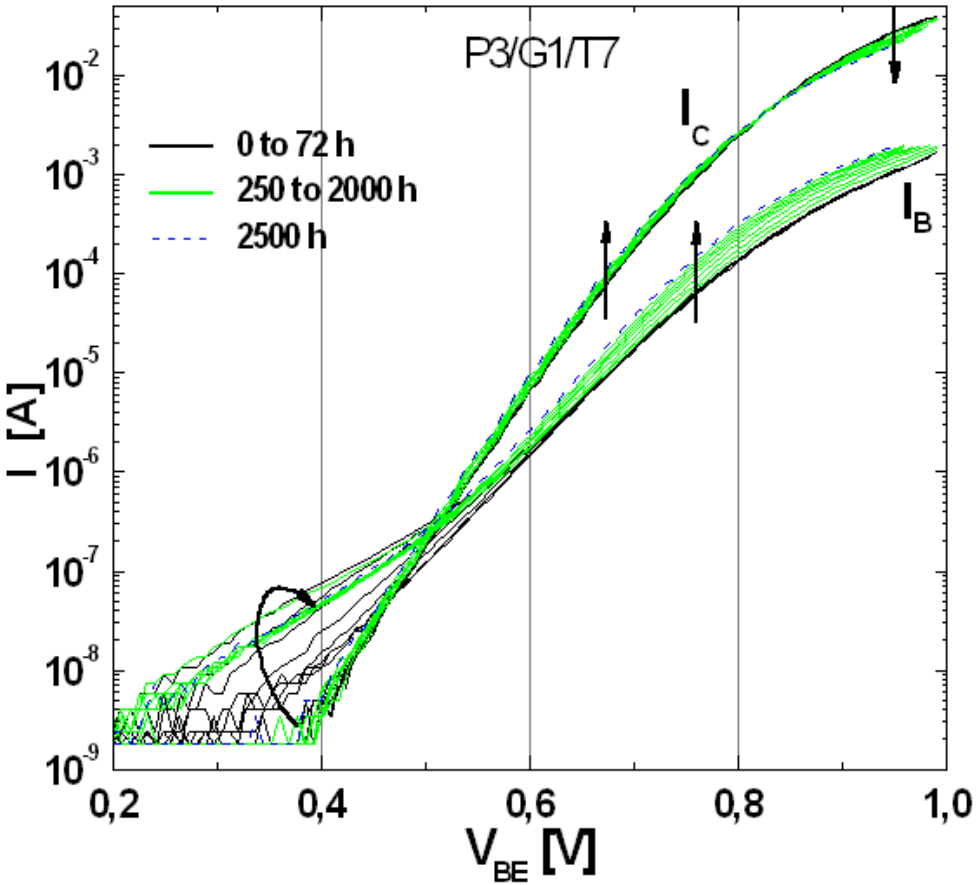
Results for T7 (W_E=0.5µm and L_E=7µm)





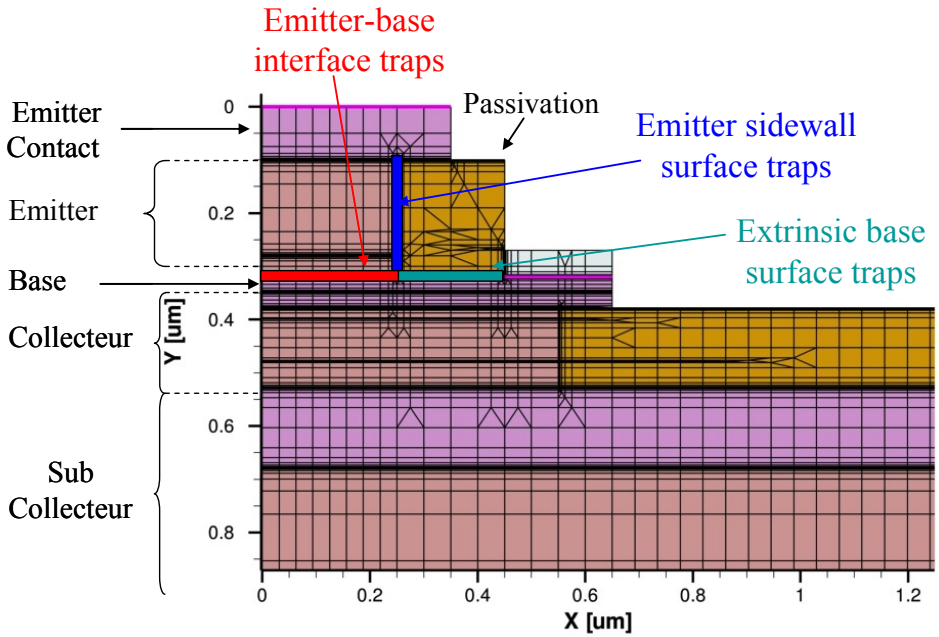
Aging tests results

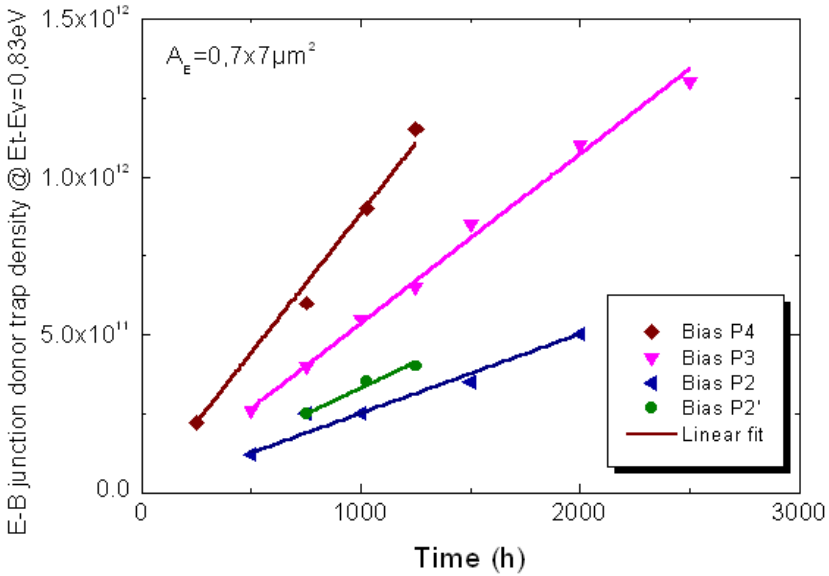
- Extensive aging tests campaign (J_C, V_{CE}, T_J)
- Moderate I_C variation
  - increase @ low level injection
  - decrease @ high level injection
- Important I_B increase
  - @ low level injection



Extensive 2D/3D Calibrated TCAD Hydrodynamic simulations

- ✓ Donor traps at E-B junction surroundings are responsible for the current variations
- ✓ Trap concentration increase linearly with stress time





Koné et al, ''Submicrometer InP/InGaAs DHBT Architecture Enhancements Targeting Reliability Improvements'', IEEE Trans. On Electron Device, pp.1068-1074 , Vol. 60, N°3, 2013.

Aging laws parameters

- Trap density is not a compact model parameter
  - ✓ need diode saturation currents

$$i_{jBEi} = I_{BEiS}\left[\exp\left(\frac{v_{B'E'}}{m_{BEi}V_T}\right)-1\right] + I_{REiS}\left[\exp\left(\frac{v_{B'E'}}{m_{REi}V_T}\right)-1\right]$$

$$i_{Tf} = \frac{I_S}{Q_{p,T}/Q_{p0}}\left[\exp\left(\frac{v_{B'E'}}{V_T}\right)-\exp\left(\frac{v_{B'C'}}{V_T}\right)\right]$$

- I_S and I_{BEIS} are extracted from post stress measurements
- I_S and I_{BEIS} follow the same variation as traps density according to aging time
- I_S and I_{BEIS} can be used as variables of the aging model

Aging laws implementation

- Donor trap density can be modeled as a generation mechanism
  - ✓ Same holds for I_{BEis} and I_S

$$\frac{dN_{trap}(t)}{dt} = G(T, J_C)$$

$$\frac{dI_{BEiS}(t)}{dt} = A_{IBEIS}(T, J_C) \qquad \frac{dI_S(t)}{dt} = A_{IS}(T, J_C)$$

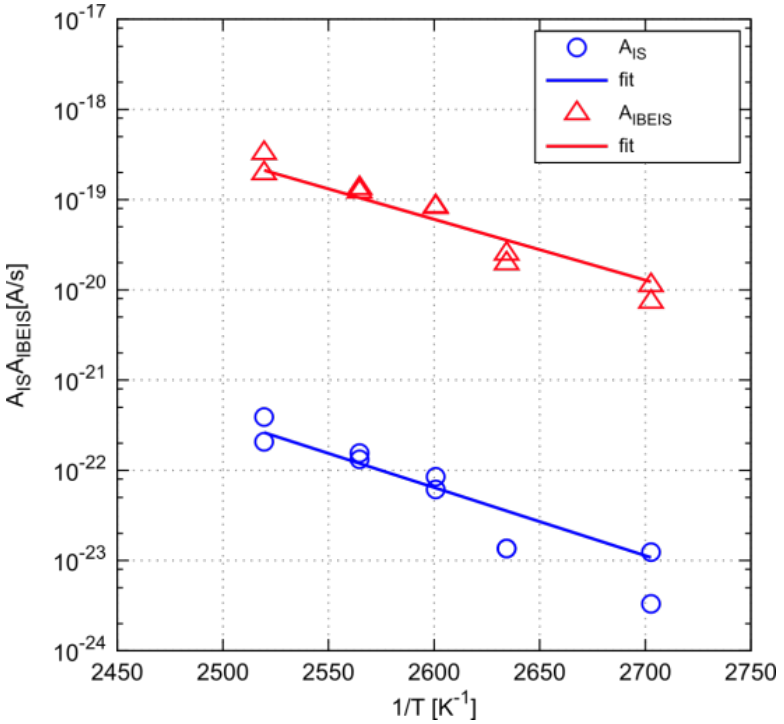
- Constant increasing rates follow an Arrhenius law

$$A_{IBEIS}(T, J_C) = B_{IBEIS}\left[\exp\left(\frac{-E_{IBEIS}}{k_B T}\right)\right] J_C^{\alpha_1} \qquad A_{IS}(T, J_C) = B_{IS}\left[\exp\left(\frac{-E_{IS}}{k_B T}\right)\right] J_C^{\alpha 2}$$

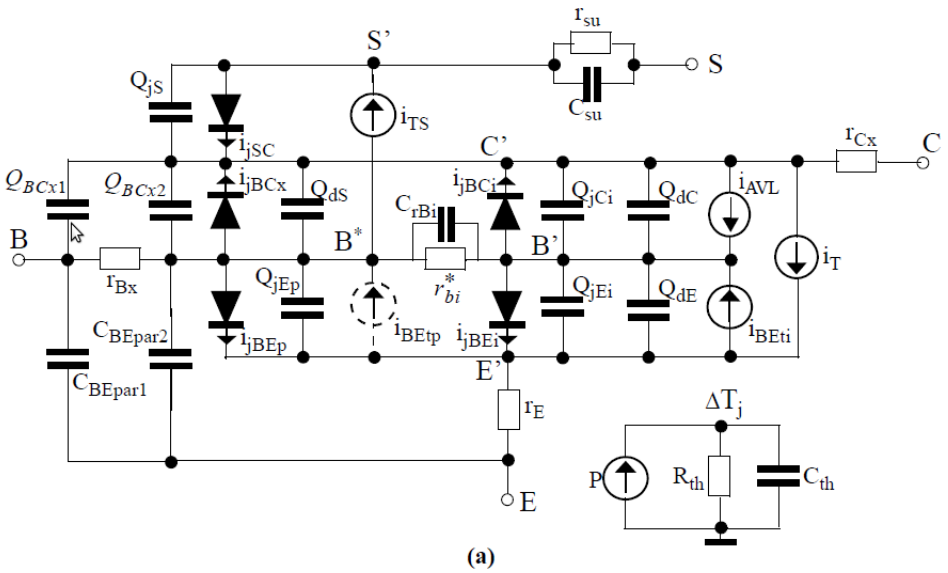
- B_{IBEIS} , E_{IBEIS} , B_{IS} , E_{IS} are new model parameters

Aging laws evolution

- Parameter extraction of I_S and I_{BEIS}
  - ✓ @ different bias point P2, P3, P4
  - ✓ For the three HBT sizes : T5, T7, T10
- Extraction of generation rates
  - ✓ A_{IS} and A_{IBEIS}
- A_{IS} and A_{IBEIS} follow an Arrhenius law
  - ✓ EIBEIS = 1.34 eV
  - ✓ EIS =1.5 eV

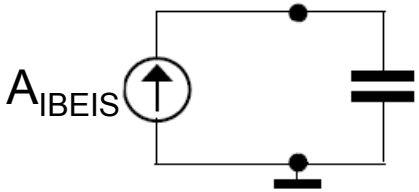


VerilogA implementation in HiCuM Model



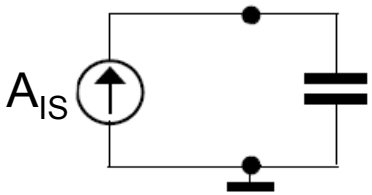
2 new nodes

Ibeis_out



$$\frac{dI_{BEiS}(t)}{dt} = A_{IBEIS}(T, J_C)$$

Is_out



$$\frac{dI_S(t)}{dt} = A_{IS}(T, J_C)$$

Indepth into code description

```
module hic2_full_XDK (c,b,e,s,tnode,          ibeis_out,  is_out);
…
branch                  (ibeis_out)  br_ibeisout
branch                  (is_out)     br_isout;
```

New nodes and branch

```
ibeis       = V(br_ibeisout)        +ibeis0;
is          = V(br_isout)           +is0;
```

Update model parameters: new nodes voltage represent degradation

```
aibeis      = bibeis*exp(-eibeis/((`P_K/`P_Q)*Tdev))      *pow( jc ),alpha1);
ais         = bis*exp(-eis/((`P_K/`P_Q)*Tdev))                        *pow( jc ),alpha2);
```

Temp & J_C dependencies

```
            I(br_ibeisout)          <+ -aibeis;
            I(br_ibeisout)          <+ ddt(V(br_ibeisout));

            I(br_isout)             <+ -ais;
            I(br_isout)             <+ ddt(V(br_isout));
```

Branch equations

Indepth into Code description cont'

```
module hic2_full_XDK (c,b,e,s,tnode,          ibeis_out,   is_out);
…
branch                  (ibeis_out)  br_ibeisout
branch                  (is_out)     br_isout;
```

Simulation of degradations is too slow: 10000 years of CPU time !!!

```
ibeis       = V(br_ibeisout)        +ibeis0;
is          = V(br_isout)           +is0;
```

```
aibeis      = bibeis*exp(-eibeis/((`P_K/`P_Q)*Tdev))      *pow( jc ),alpha1);
ais         = bis*exp(-eis/((`P_K/`P_Q)*Tdev))                    *pow( jc ),alpha2);
```

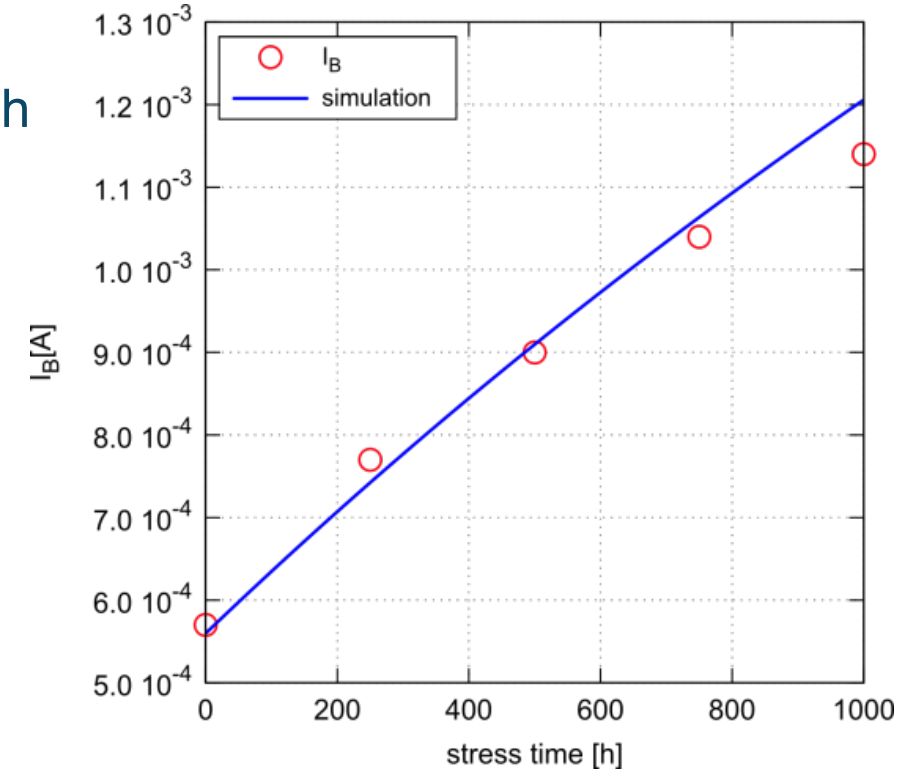
```
            I(br_ibeisout)          <+ -atsf * aibeis;
            I(br_ibeisout)          <+ ddt(V(br_ibeisout));

            I(br_isout)             <+ -atsf * ais;
            I(br_isout)             <+ ddt(V(br_isout));
```

ATSF : Accelerating Time Scale Factor new parameter

ATSF=3.6E13 100ns ➔1000 h
ATSF=3.15E15 100ns ➔10 years

Validation @ transistor level

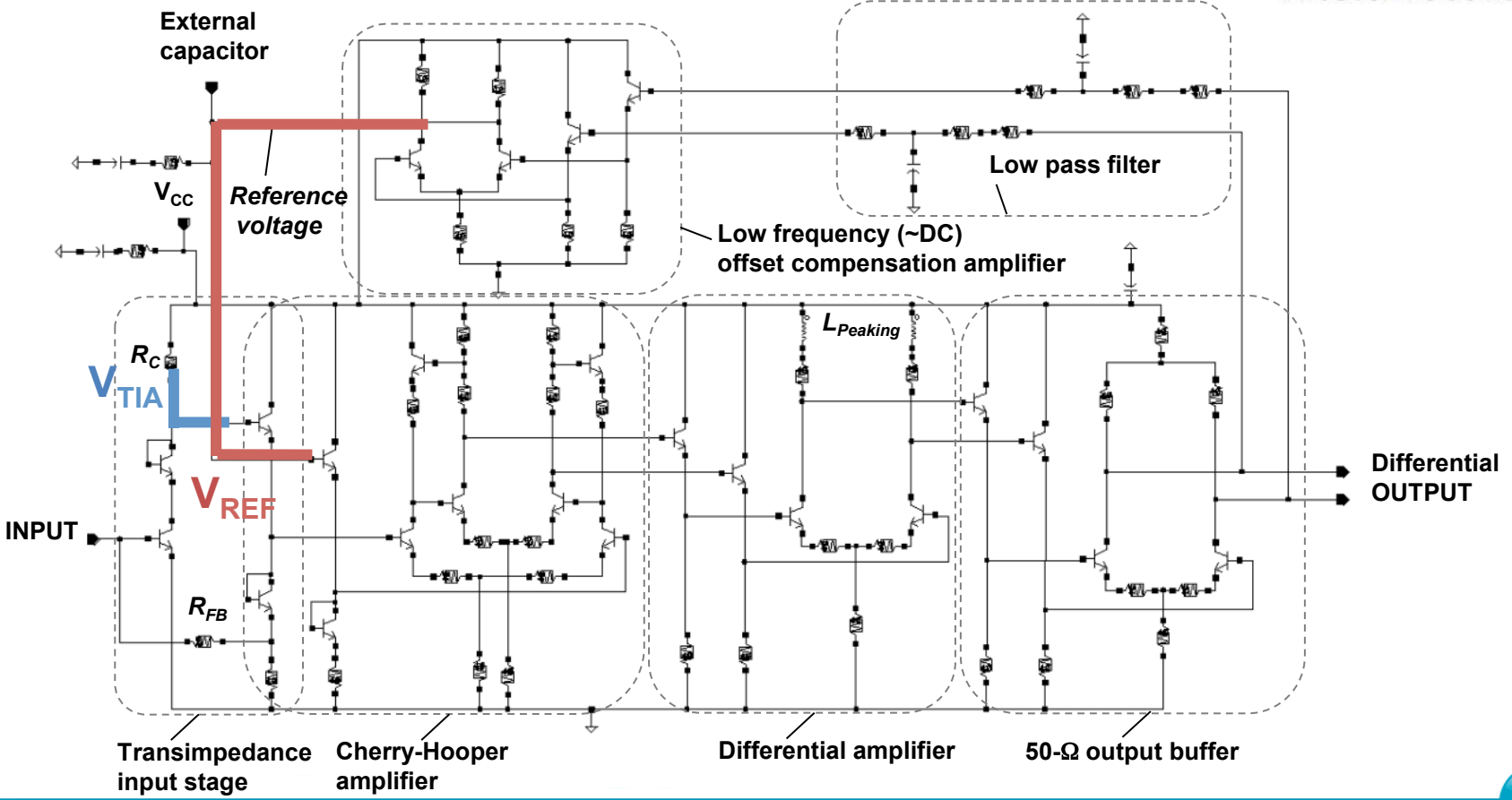
- Verification on base current
  - ✓ monitored during ageing – 1000 h
- Transistor T7 (0.5x7µm^2)
- Bias condition P4



➢ Compact model is accurate at transistor level

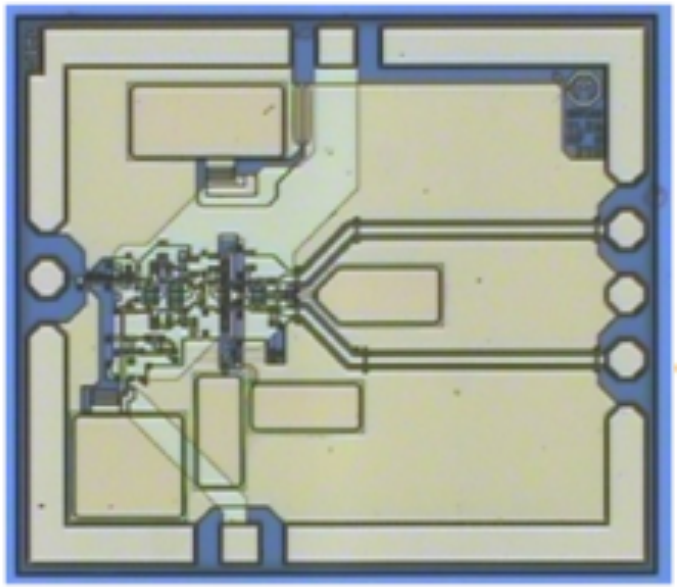
@ Circuit level : Transimpedance Amplifier (TIA)

- Featuring complex offest compensation loop



TIA description

- 2 versions of the TIA available for aging tests
  - ✓ TLIA (high DC gain – low cutoff frequency)
  - ✓ TIA-HF (lower DC gain – Higher bandwidth)
  - ✓ 22 circuits samples submitted to accelerated aging test for 1008 hours
  - ✓ Chuck temperature = 70°C
  - ✓ T_j up 125°C



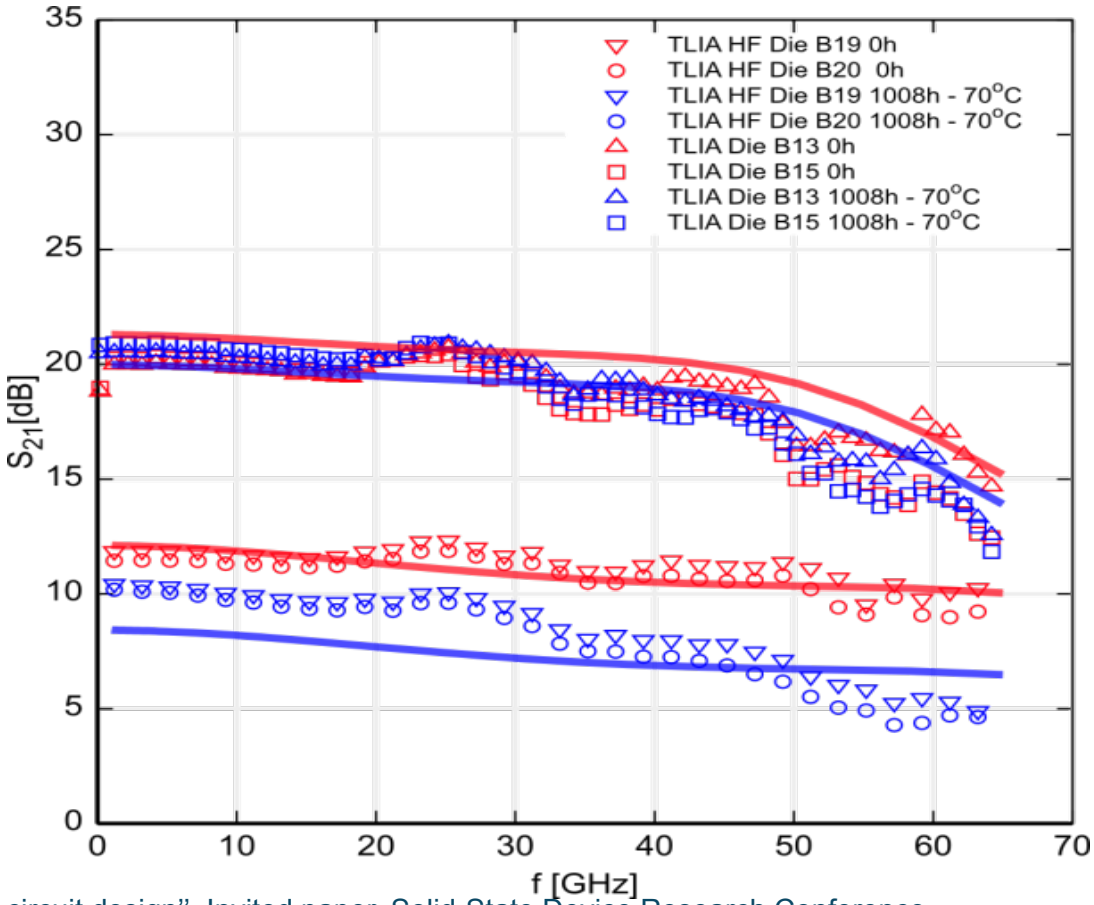
TLIA S parameters measured up to 65GHz

- Measurements versus simulations
- Perl scripting is used to automate ''aged'' circuit simulation
- Software : Agilent ADS

✓Excellent initial model

✓Slightly pessimistic aging

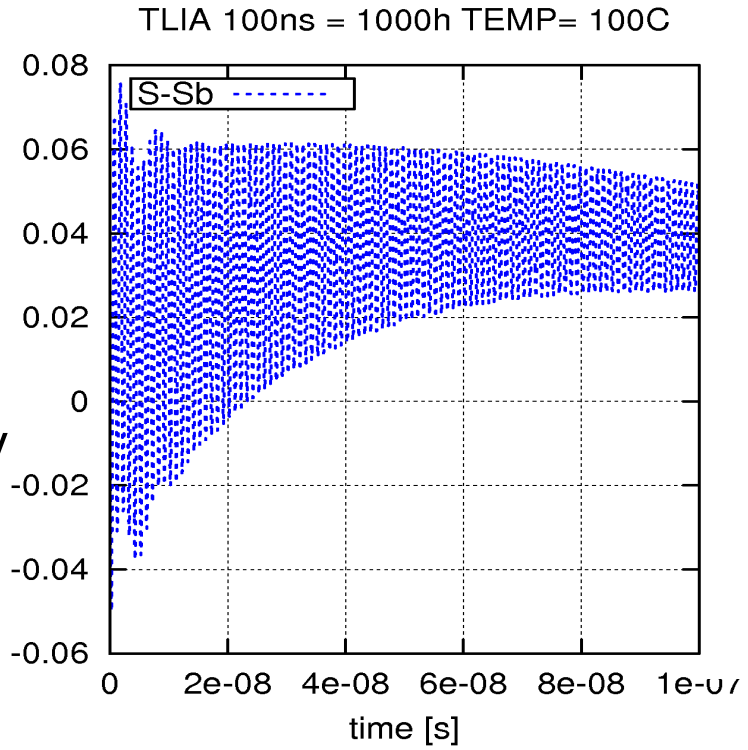
✓But fairly accurate predictions



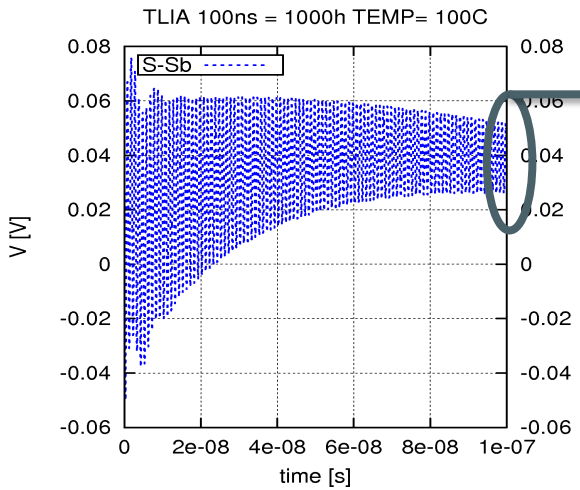
Ardouin et al., '' Advancements on reliability-aware analog circuit design'', Invited paper, Solid-State Device Research Conference (ESSDERC), 2012 Proceedings of the European, pp.62-68, 17-21 Sept 2012,

@ Circuit level : TLIA Transient simulation

- ATSF=36x10^{12} (100ns=10years)
- Temperature=100°C
- Dynamic observation of all circuit nodes
  - ✓Differential output voltage (S-Sb)
- Circuit instances can be extracted at any time step



TLIA Transient simulation

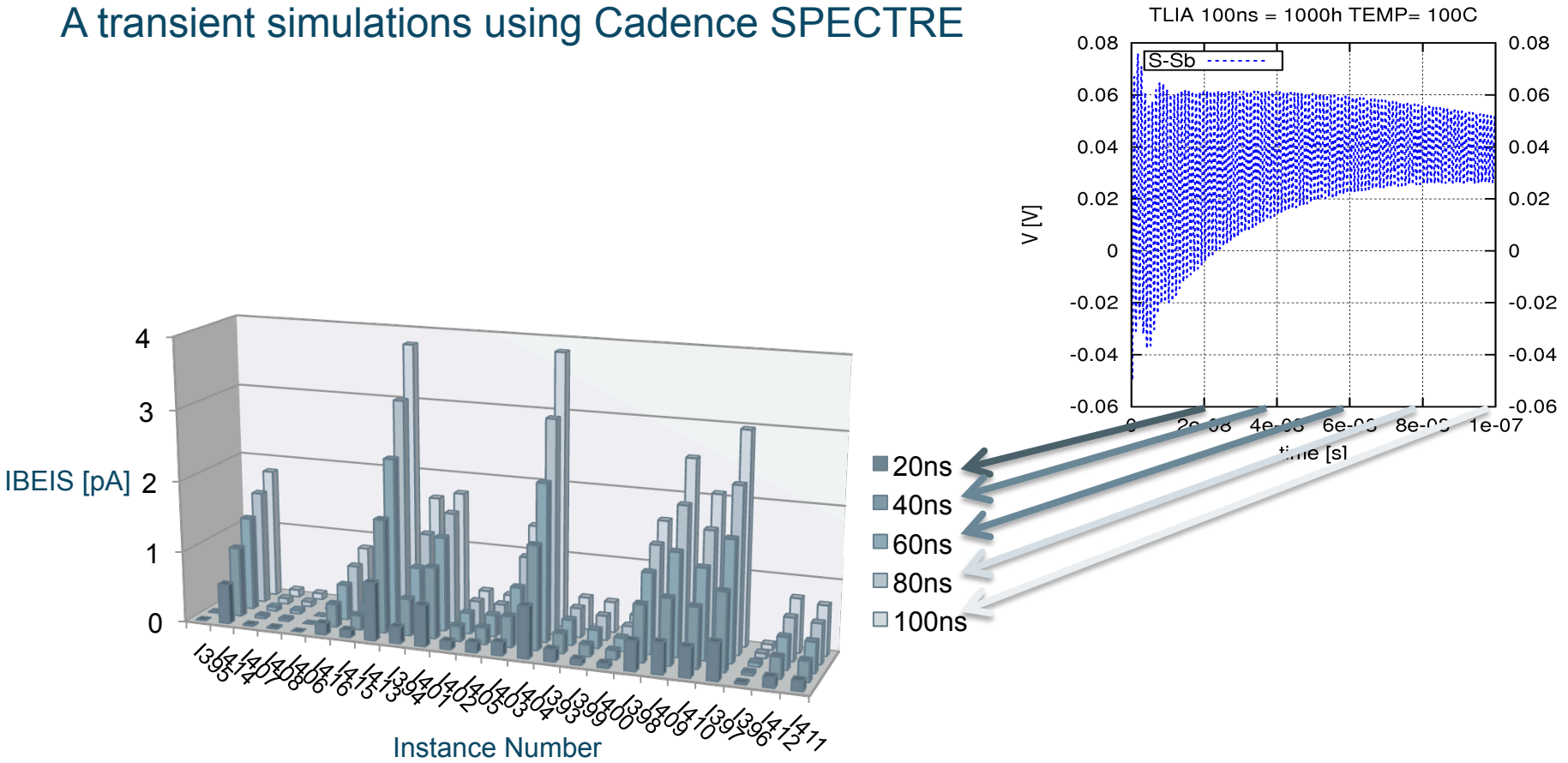


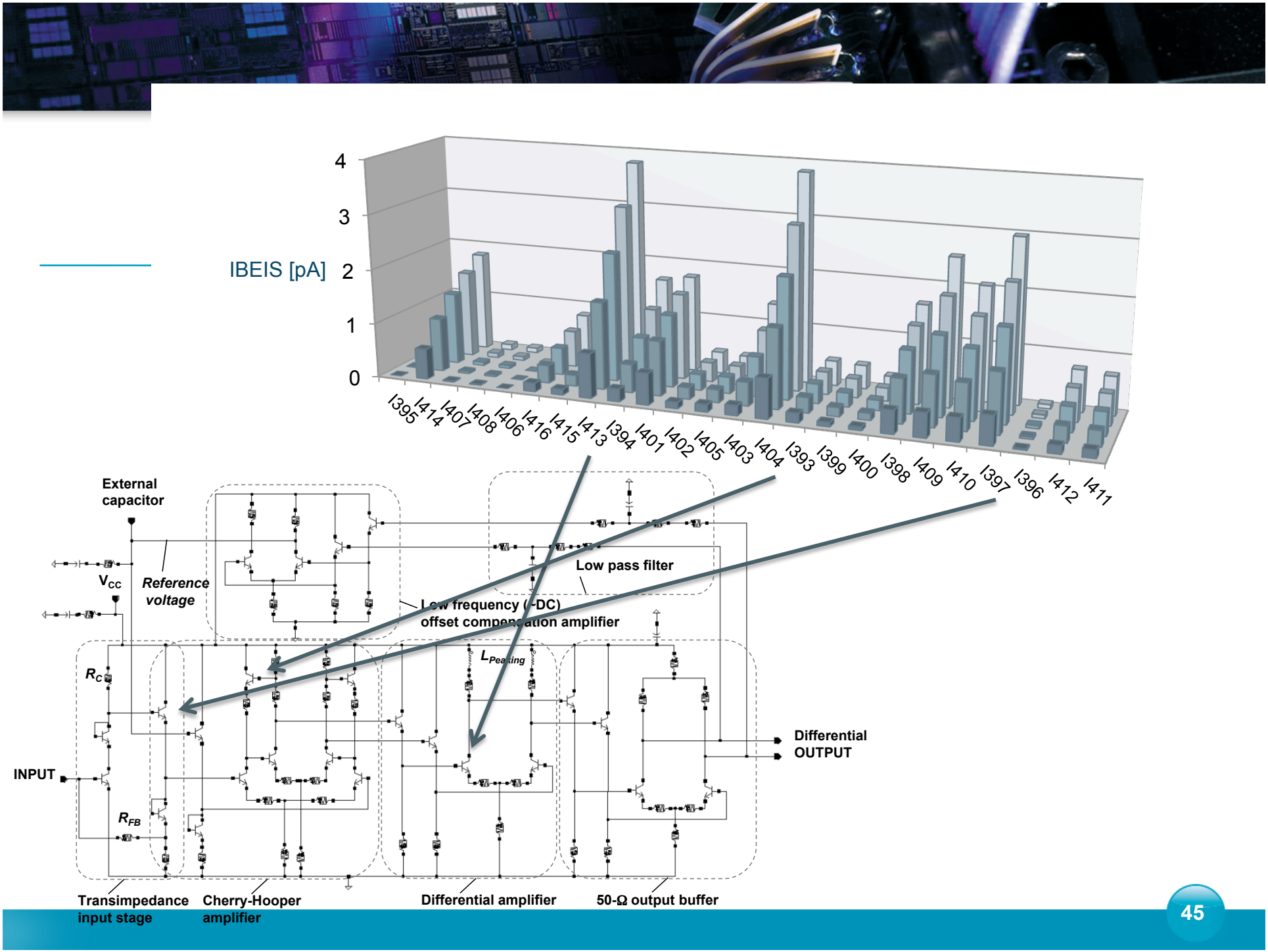
Steady state @ selected time step:
run AC simulation with aged parameters
Using a script to generate “alter” statements gathered in a include file

```
Alter:AGINGalter0 var="I182.I395.Q1.AGED_RE0" VarValue=1.051097526541248e+00
Alter:AGINGalter1 var="I182.I395.Q1.AGED_IS0" VarValue=2.296752299864880e-05
Alter:AGINGalter2 var="I182.I395.Q1.AGED_IBEIS0" VarValue=2.720399978065819e-02
Alter:AGINGalter4 var="I182.I414.Q1.AGED_IS0" VarValue=2.477855478244199e-03
Alter:AGINGalter5 var="I182.I414.Q1.AGED_IBEIS0" VarValue=1.822901099996015e+00
Alter:AGINGalter7 var="I182.I407.Q1.AGED_IS0" VarValue=1.003050582644627e-04
Alter:AGINGalter8 var="I182.I407.Q1.AGED_IBEIS0" VarValue=1.021350703026095e-01
Alter:AGINGalter10 var="I182.I408.Q1.AGED_IS0" VarValue=8.399430332061722e-05
..
```

Circuit element parameter during simulated aging time

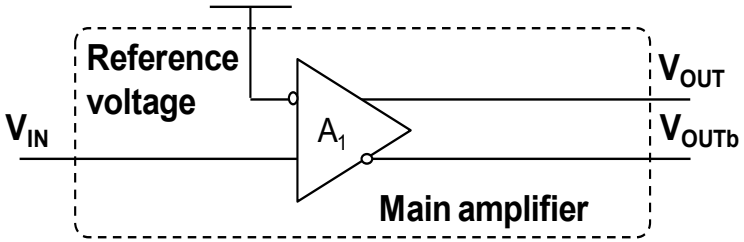
A transient simulations using Cadence SPECTRE

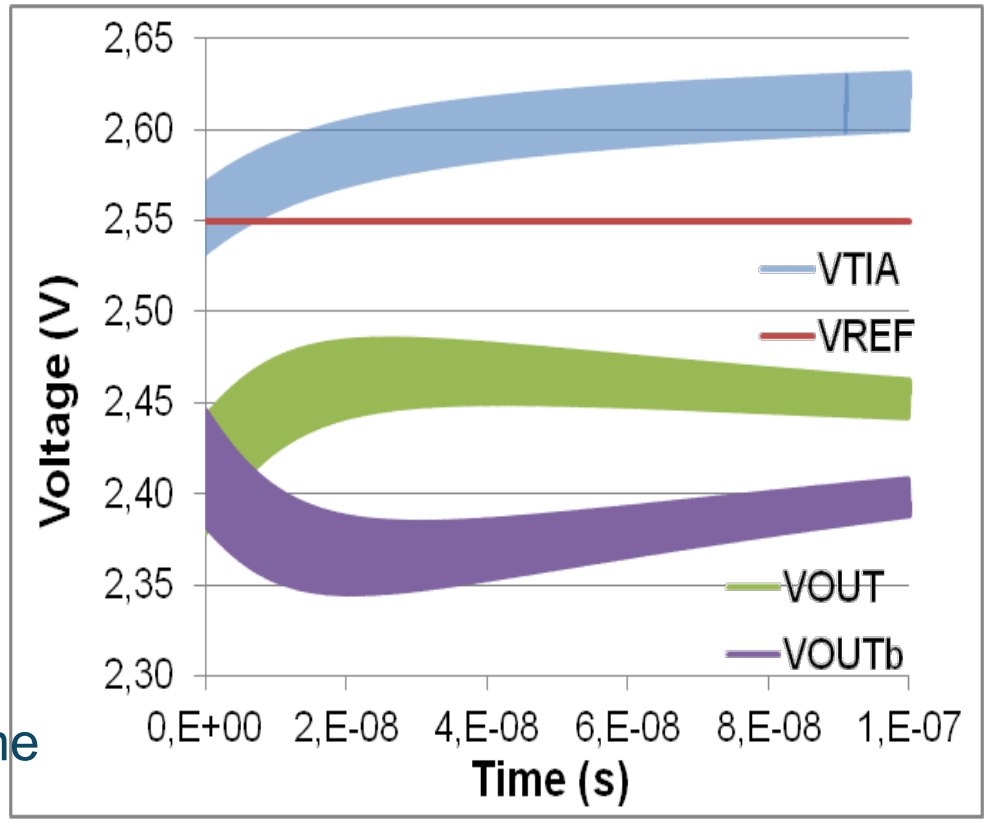



IBEIS [pA]
4
3
2
1
0
I395
I414
I407
I408
I406
I416
I415
I413
I394
I401
I402
I405
I403
I404
I393
I399
I400
I398
I409
I410
I397
I396
I412
I411
External capacitor
V_{CC}
Reference voltage
Low pass filter
Low frequency (~DC) offset compensation amplifier
$L_{Peaking}$
R_C
R_{FB}
INPUT
Differential OUTPUT
Transimpedance input stage
Cherry-Hooper amplifier
Differential amplifier
50-Ω output buffer

Reliability aware design example 1/3

- No DC offset compensation loop

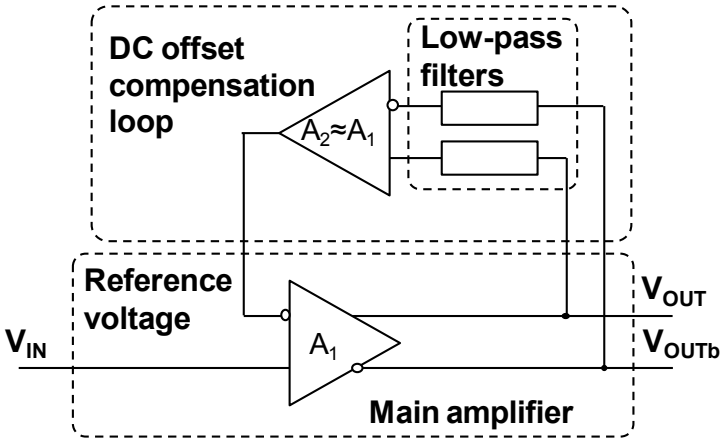


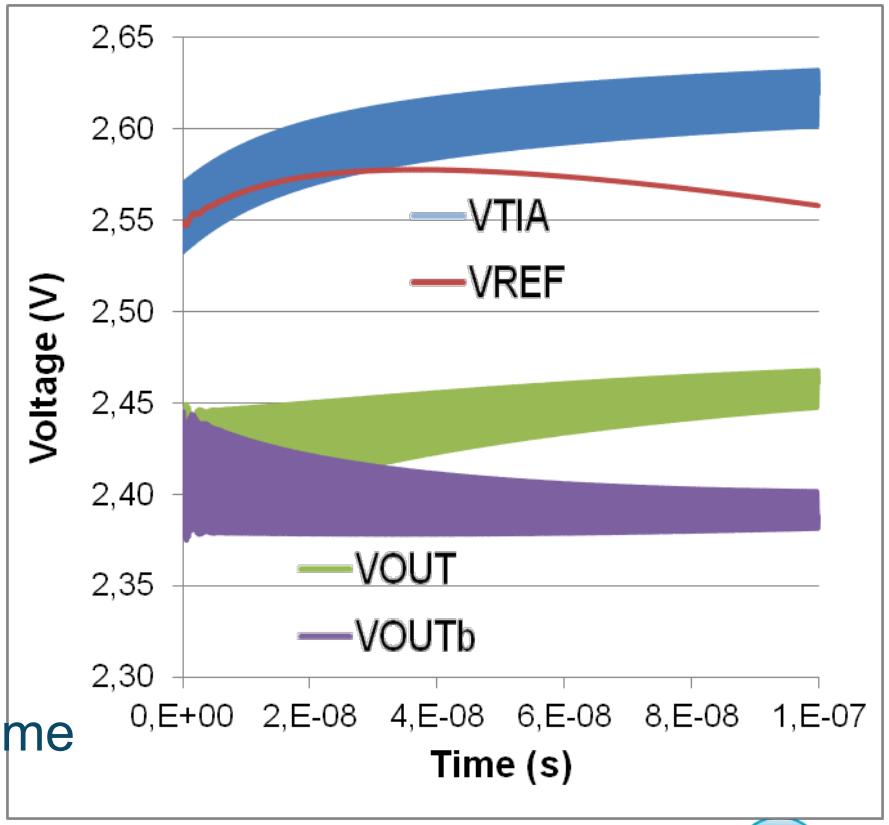


✓ VREF is constant over aging time

Reliability aware design example 2/3

- DC offset compensation loop with small gain

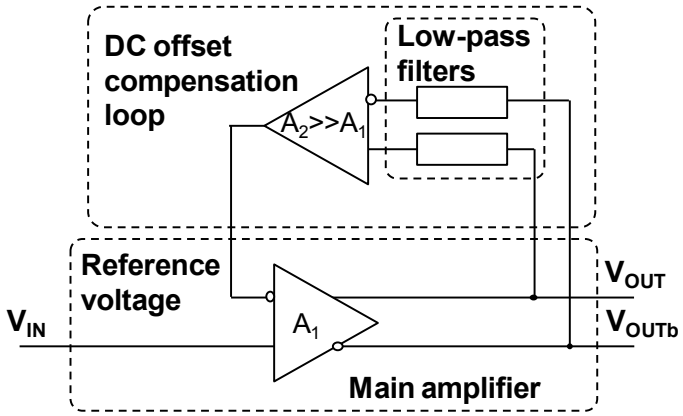


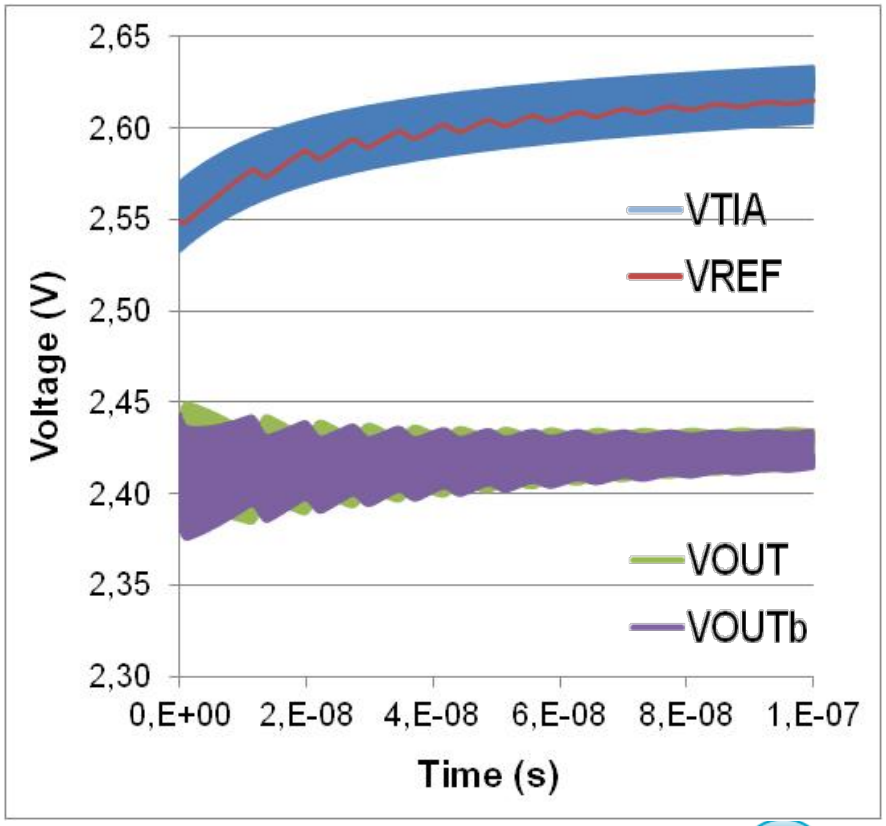


- ✓ VREF can't follow VTIA over aging time

Reliability aware design example 3/3

- DC offset compensation loop with high gain





✓ VREF follows VTIA over aging time thanks to higher loop gain

Conclusion : Augmented compact model for reliability-aware circuit design

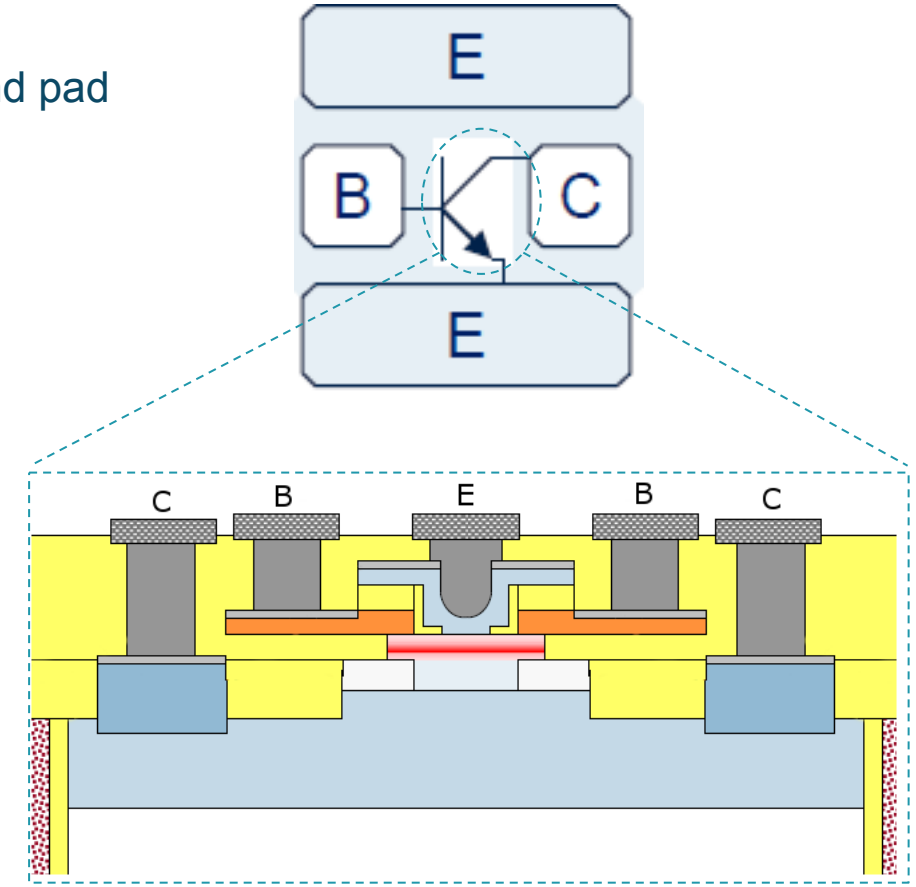
- ✓ New method for device dynamic reliability simulation
- ✓ Straightforward initial implementation in software design simulators (VerilogA) : Available in a standard PDK (easy to adopt)
- ✓ Simulates complex interactions between stress conditions (bias/ temperature) and device characteristics evolution
- ✓ Physics based methodology
- ✓ Validated at transistor level (InP/InGaAs HBT process)
- ✓ Validated at circuit level (24 transistors TIA – working above 100GHZ and using a complex offest compensation loops)
- ✓ Allows reliability aware circuit design
- ✓ Shortens circuit reliability improvement feedback loops

Outline

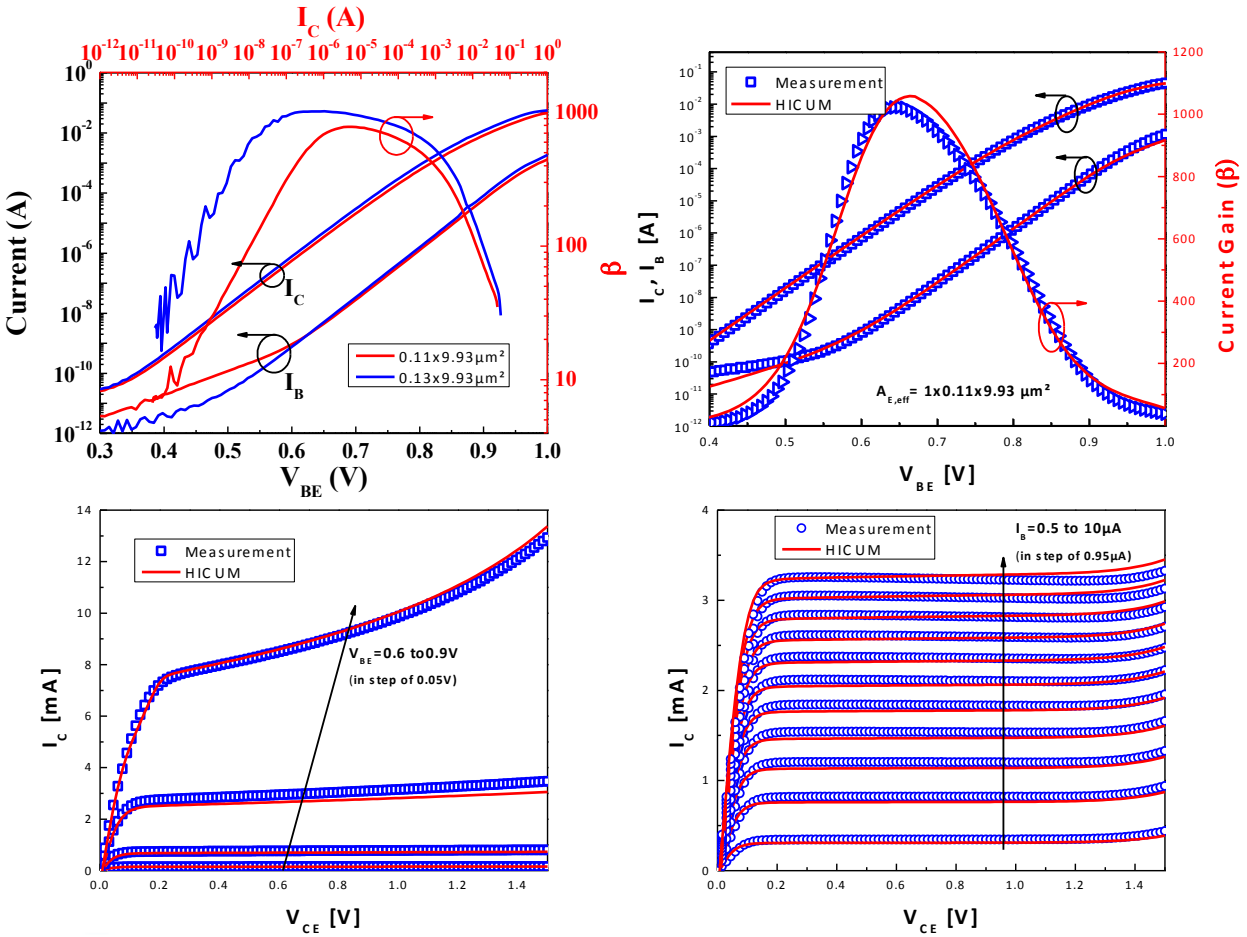
- Context :
  - Impact of dimensions shrinking on device operation margins
  - Impact of device operation margins on the device failure mechanisms
- From device to circuit reliability
  - Circuit aging simulation : Why ?
  - Circuit aging simulation : How?
    - Conventional way of doing
    - IMS proposal for circuit aging simulation
- A study case : InP Bipolar Submicron devices for robust design of 112Gb/s optical transport network
- DOTSEVEN SiGe HBT technology
  - Operation
  - Aging tests results
  - Aging laws implementation in HiCUM model
  - Towards the evaluation of reliability at circuit level

Infineon SiGe:C HBT technology

- Test structure: GSG configuration
  - Emitter and substrate connected to ground pad
- CBEBC Configuration
  - Single emitter finger
  - Emitter size of 0.2x10µm²
- SiGe:C NPN transistor
  - F_t/F_{max}= 240/380GHz
  - BVceo = 1.5V



Device under test: DC characterization



Aging test campaigns

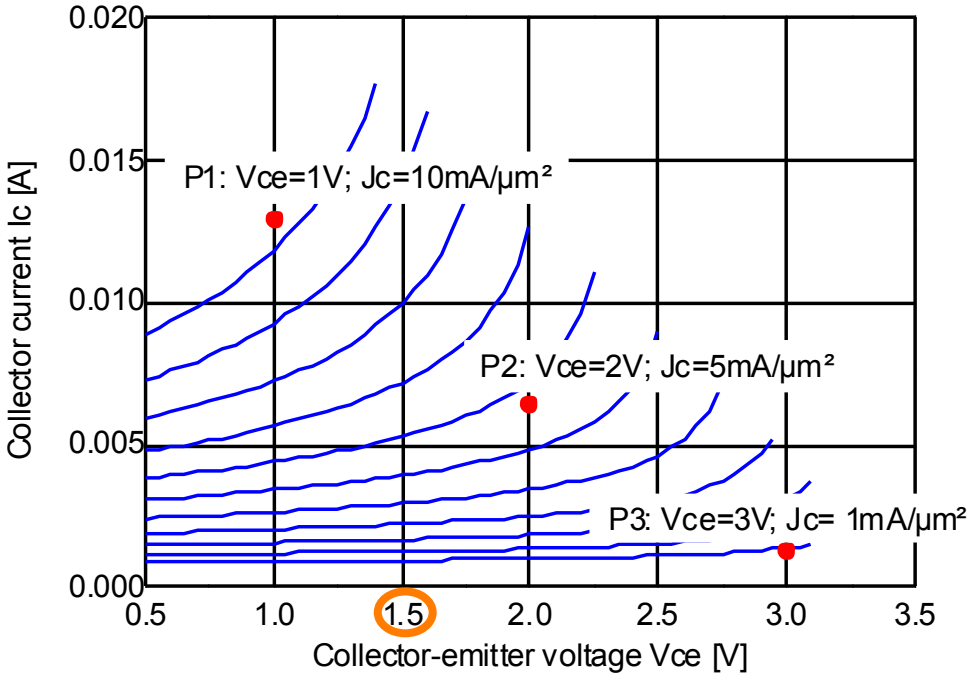
- Requirements : to identify wear out mechanisms
  - Slowly evolving with time
  - At the edge of the Safe Operating Area
- Long-time stress tests (i.e. 1000 h)
  - Stress tests and measurements realized using encapsulated devices
  - Samples biased in a common-emitter configuration at constant and controlled ambient temperature of 300K.
- Evolution characterization
  - DC characterization is performed at fixed time of 1h, 3h, 7h, 24h, 36h, 48h, 72h, 120h, 250h, 500h, 750h and 1000h.
  - At 300h, an additional point is added with 24h between the end of the stress test and the measurement ➔Evaluation of recovery mechanism
  - Base-emitter junction characterization : forward Gummel plot at Vbc=0V
  - Base-collector junction characterization : Reverse Gummel plot at Vbe=0V

Aging test campaigns: Bias conditions

Size	Drawn dimension		Bias conditions		
	We (µm)	Le (µm)	P1 Vce= 1V Jc=10mA/µm²	P2 Vce= 2V Jc=5mA/µm²	P3 Vce= 3V Jc=1mA/µm²
			Ic(mA)	Ic (mA)	Ic (mA)
Size 1	0.2	1	1.21	0.6	0.29
Size 2	0.2	2.8	3.55	1.75	0.35
Size 3	0.2	10	12.91	6.46	1.29

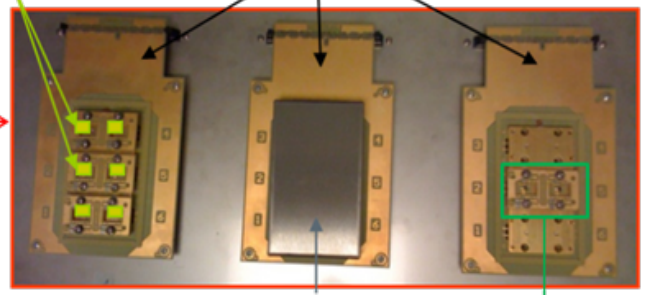
Aging tests description

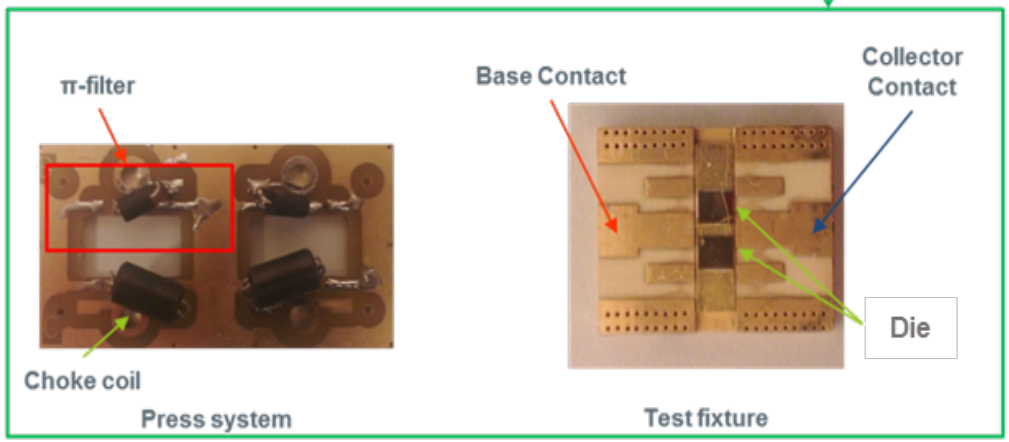
- Emitter common configuration
  - ➢ Vce fixed
  - ➢ Ic forward control
  - ➢ Ib monitoring
- Bias conditions :
  - ✓ Wear out mechanisms
  - ✓ SOA edge
    - ➢ 1 bias point below BVceo
    - ➢ 2 bias points above BVceo
    - ➢ 6 HBT per bias conditions
- Aging time up to 1000h



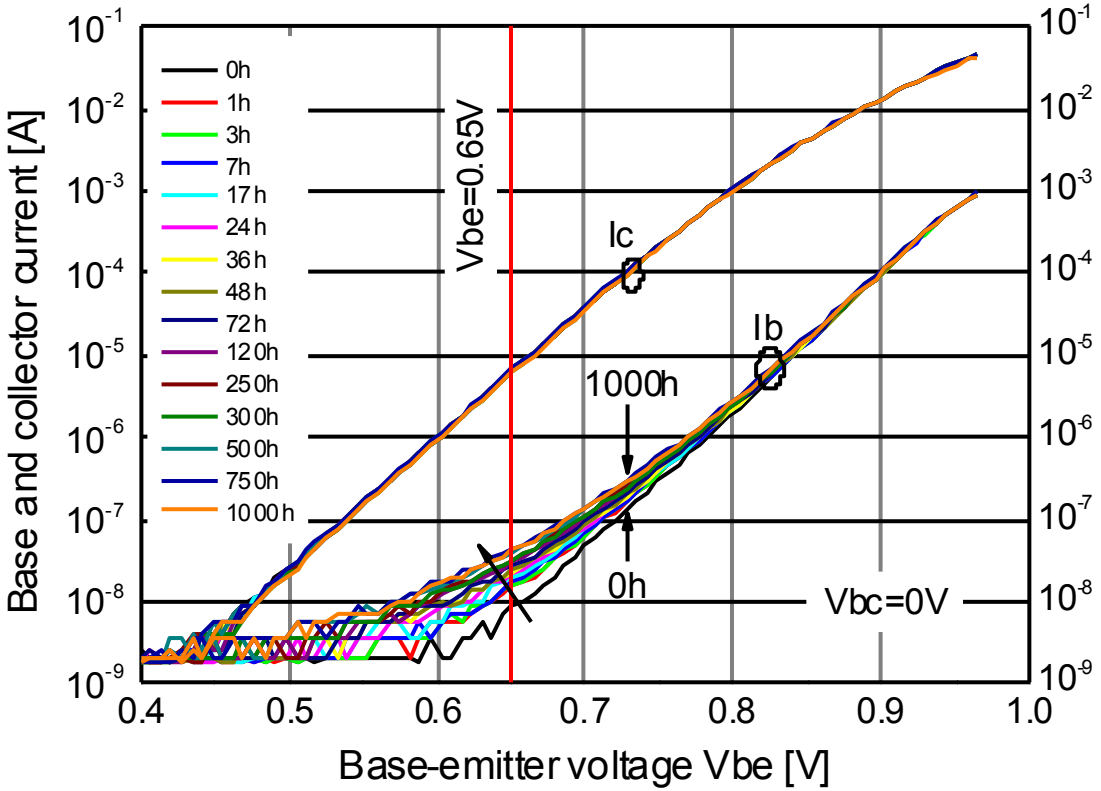
Test bench description

Test bench



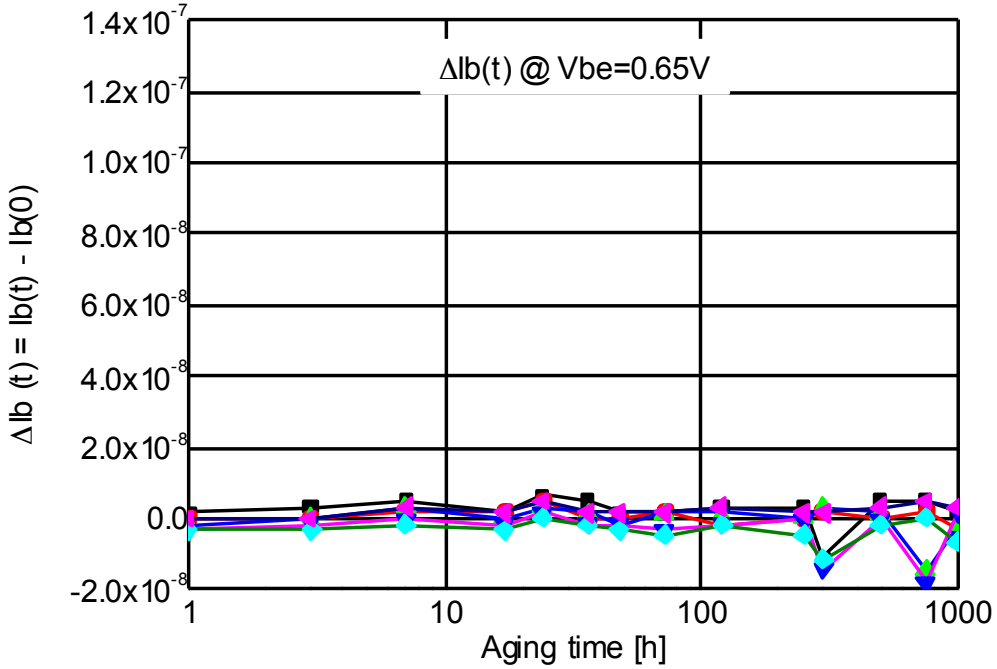


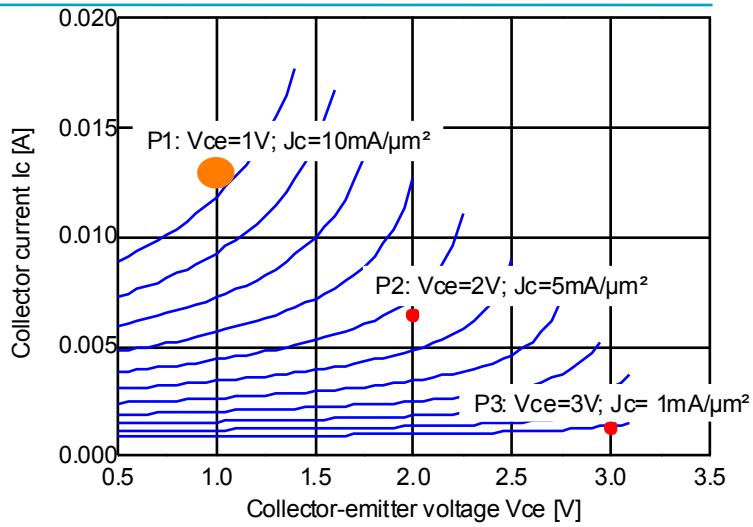
Aging tests results



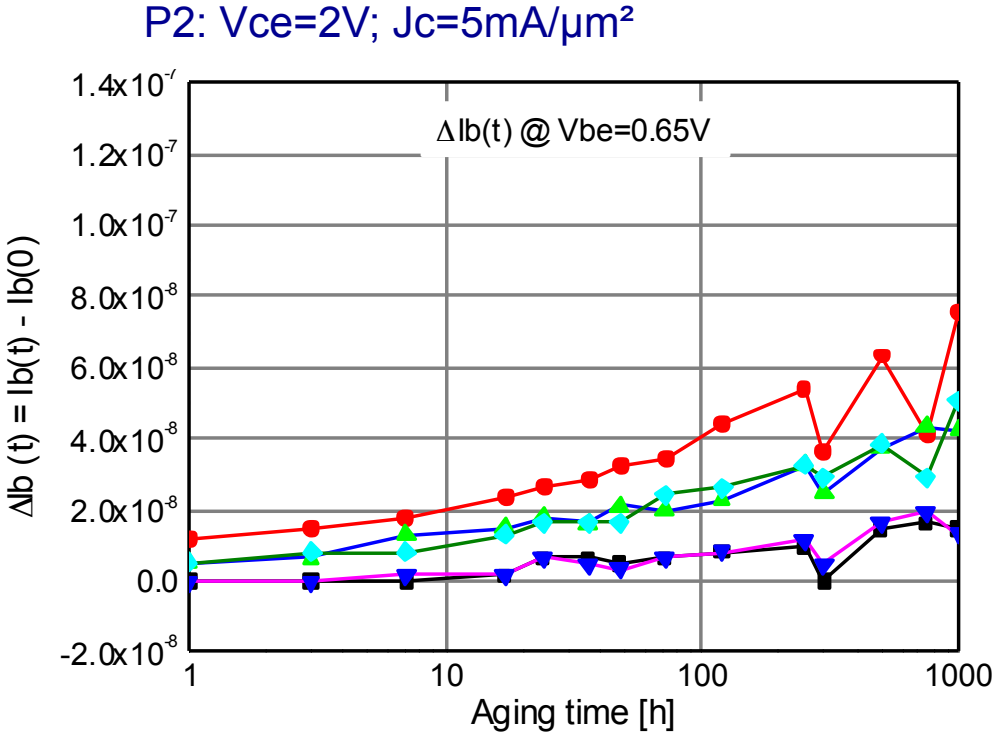
Aging tests results analysis @P1

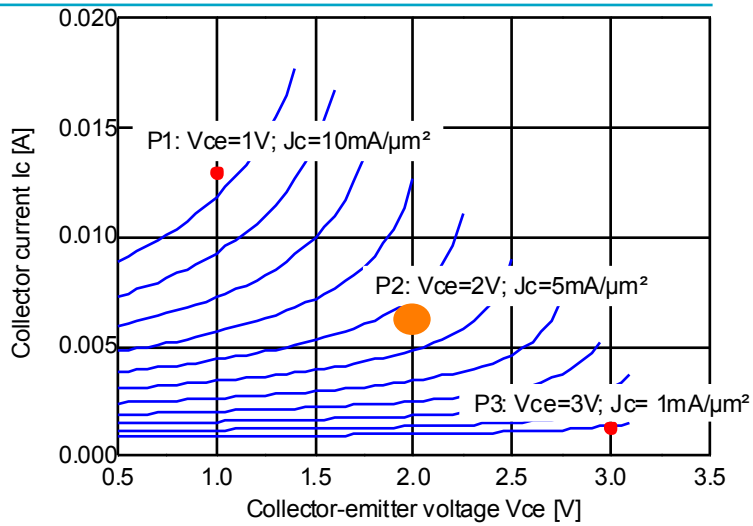
P1: Vce=1V; Jc=10mA/µm²



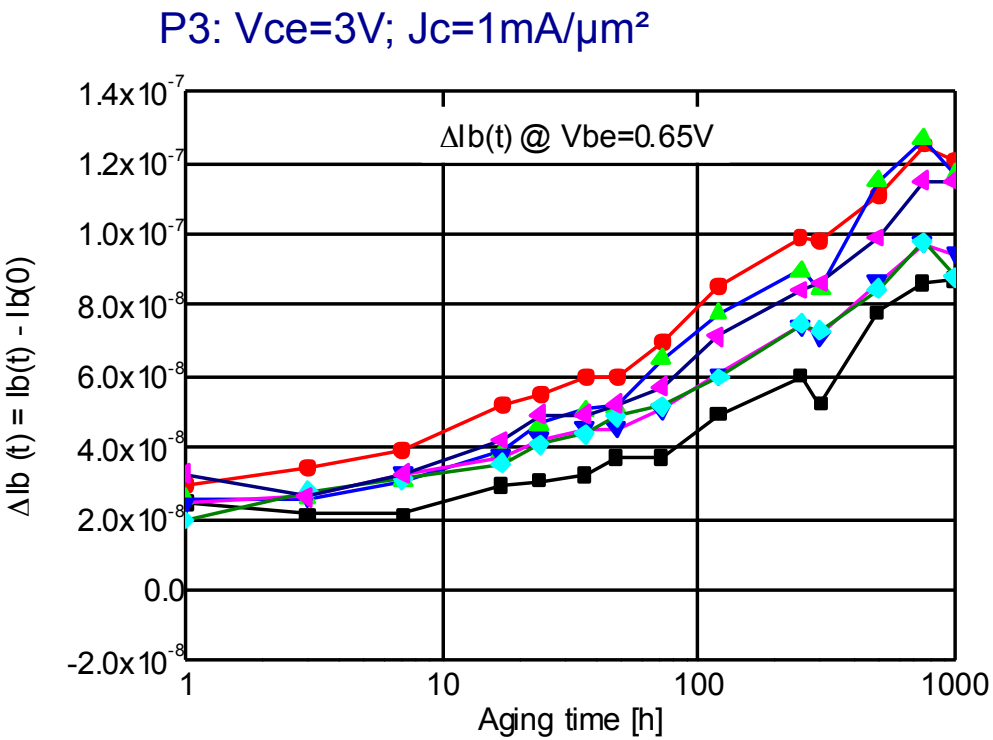


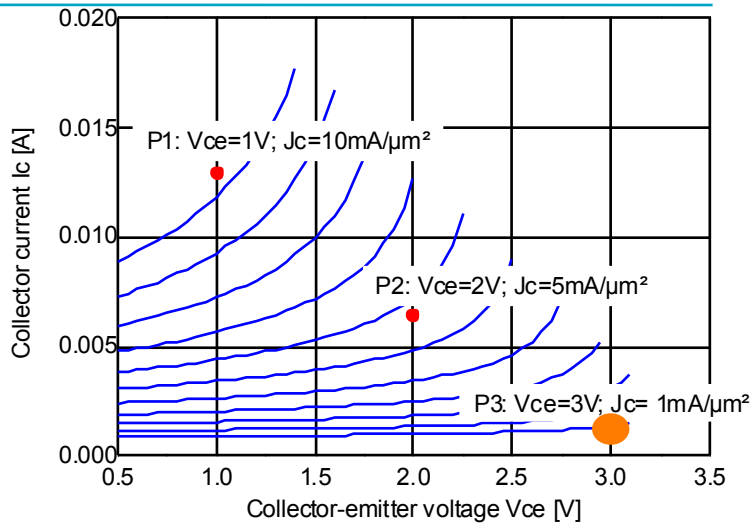
Aging tests results analysis @P2





Aging tests results analysis @P3





Aging mechanism analysis

High Vce
(>BVceo)

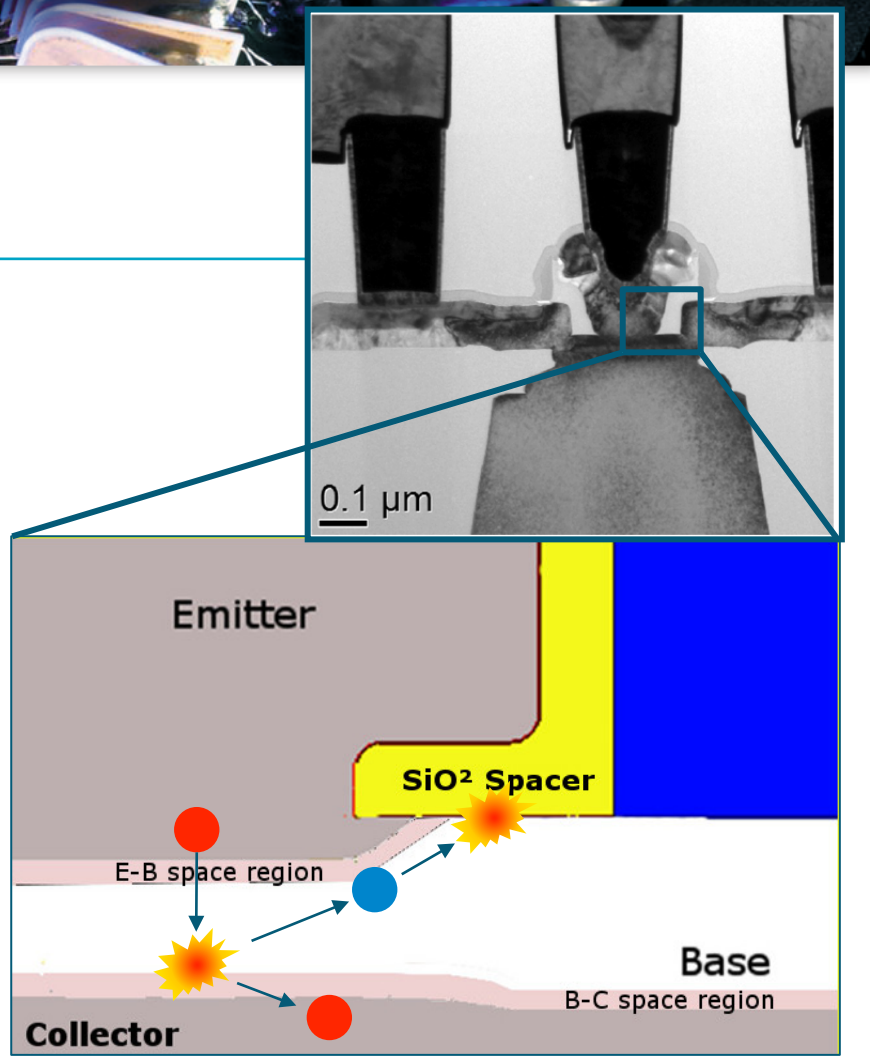
Electrons accelerate in BC space region

Creation of electron-hole pairs
(Impact ionization)

Hot carriers injected in E-B spacer

Carriers break dangling bond *

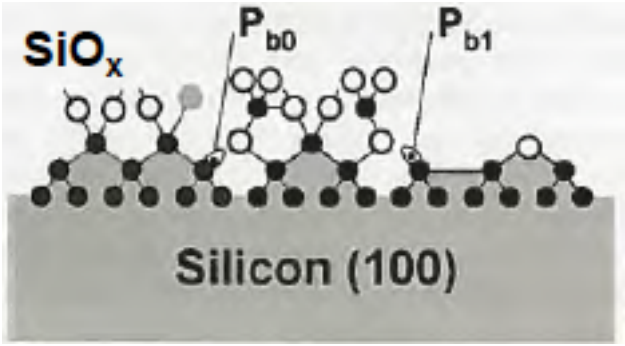
Increase of trap density



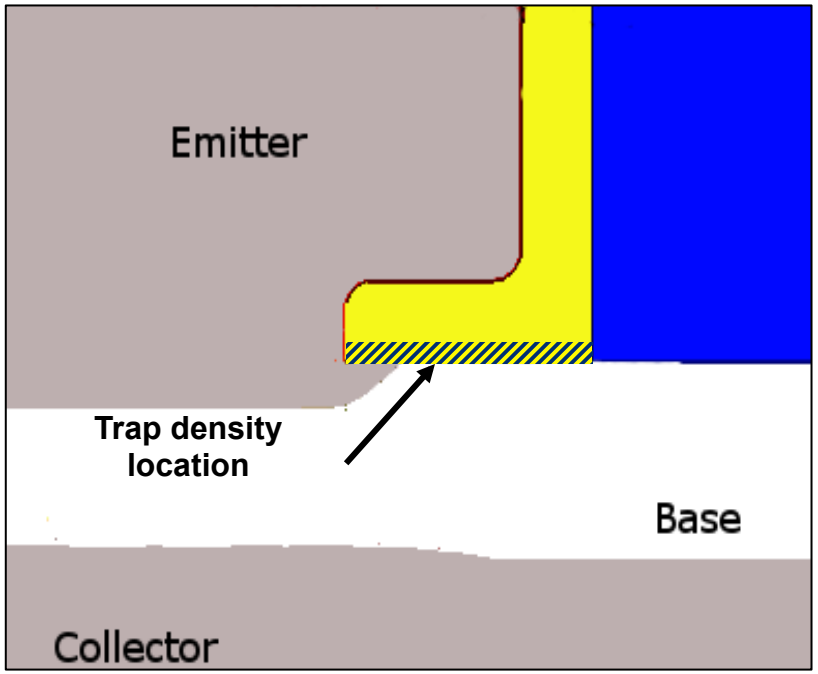
- Z. Chendong et al., Damage mechanisms in impact-ionization-induced mixed-mode reliability degradation of SiGe HBTs", IEEE Transaction on Device and Materials Reliability, vol. 5, n. 1, March 2005, pp 142-149.

Trap density simulation

- Uniform acceptor type trap density
  - Trap energy level: E_T-E_V=0.6 eV



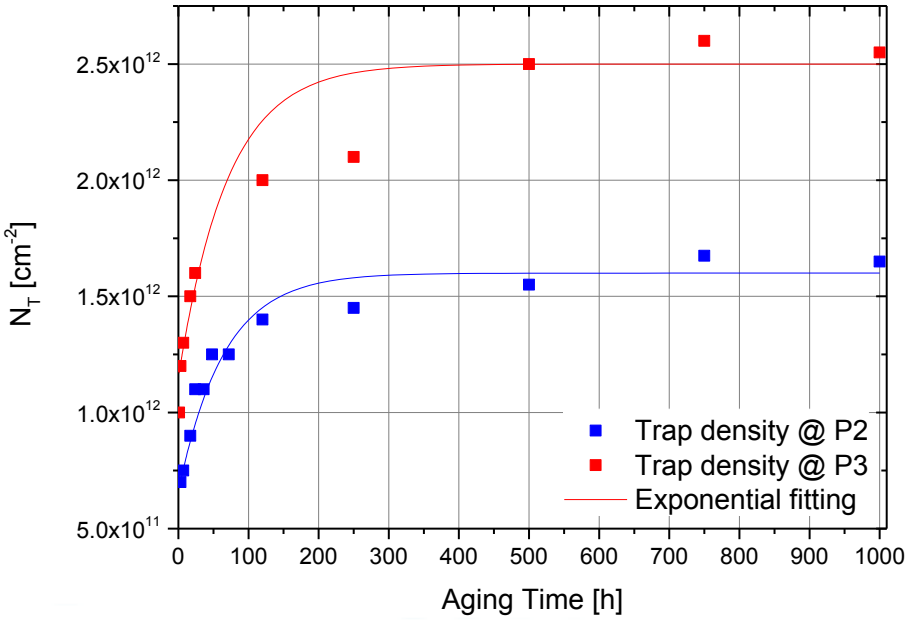
$$Si_3 \equiv SiH + h^+ \rightarrow Si \equiv Si \cdot + H^+$$
$$Si_3 \equiv SiOH + h^+ \rightarrow Si \equiv SiO \cdot + H^+$$



Schroder et al., ''Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing'', J. Appl. Phys. 94(1), 2003

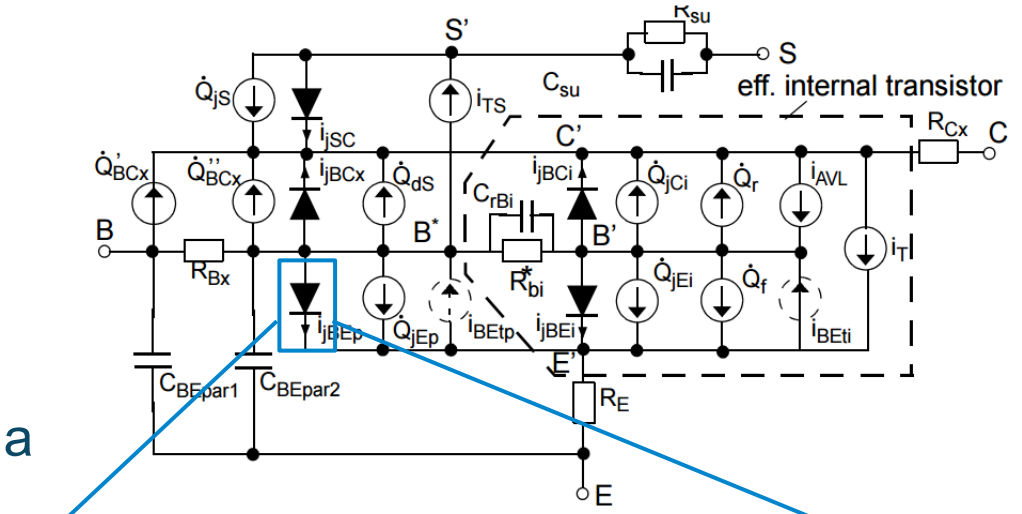
Trap density evolution

- At each stress time, extraction of trap density
- Evolution of trap density $N_T(t) = N_{Tfinal} - (N_{Tinit} - N_{Tfinal})\exp(-\frac{t}{\tau})$



Compact modeling

- HiCuM compact model L2
  - Version 2.33
- E-B junction periphery
  - Trap location
- I_{REpS} parameter converted as a new variable in HiCuM



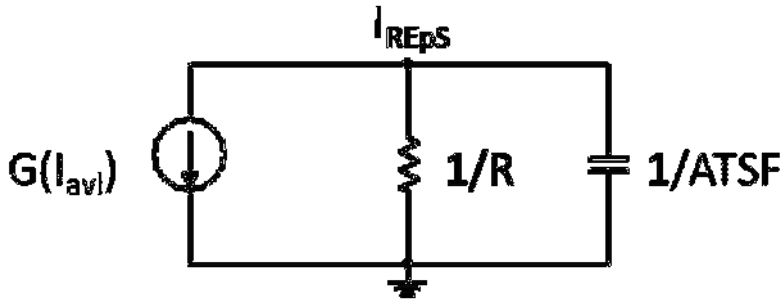
$$i_{jBEp} = I_{BEpS}\left[\exp\left(\frac{v_{BE}}{m_{BEp}V_T}\right)-1\right] + I_{REpS}\left[\exp\left(\frac{v_{BE}}{m_{REp}V_T}\right)-1\right]$$

$$I_{REpS} = I_{REpS,final} + (I_{REpS,initial} - I_{REpS,final})\exp(-\frac{t}{\tau})$$

Implementation in HiCuM Verilog A

- Evolution of I_{REpS}

$$\frac{dI_{REpS}}{dt} = ATSF \cdot (G - R \cdot I_{REpS})$$



- Constant recombination rate R

  $R = 3.7\text{x}10^{-6}\ s^{-1}$

- Generation rate G

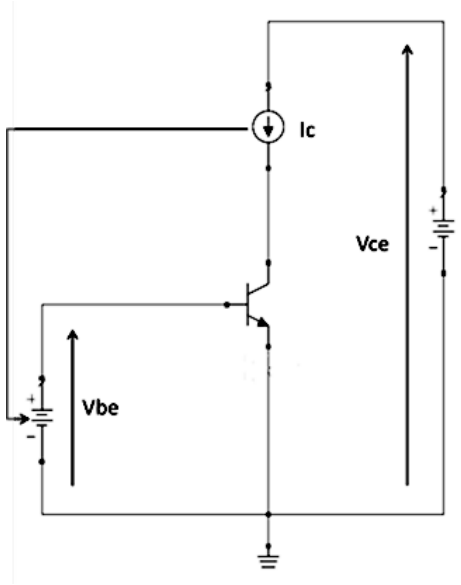
$$G(I_{avl}) = A \cdot I_{avl} + G_0$$

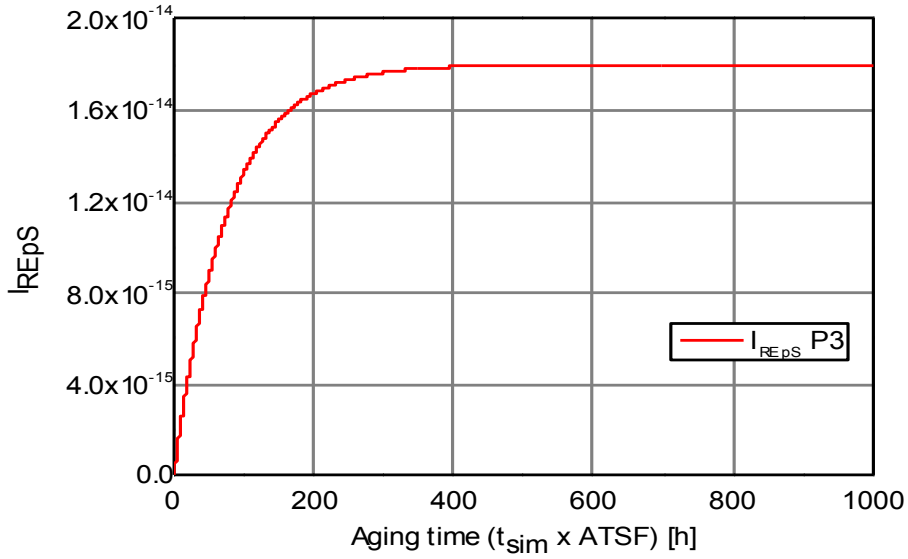
A=7.575x10^{-21} s^{-1}, G_0= 0.75e^{-20} A·s^{-1}

- Accelerating factor ATSF, Aging Time Scale Factor
  - ✓ Reduce simulation time for convenient time calculation
  - ✓ *ATSF*, fixed at 3.6x10^6 : 1000h (aging time) ↔ 1s (simulation time)

Simulation results

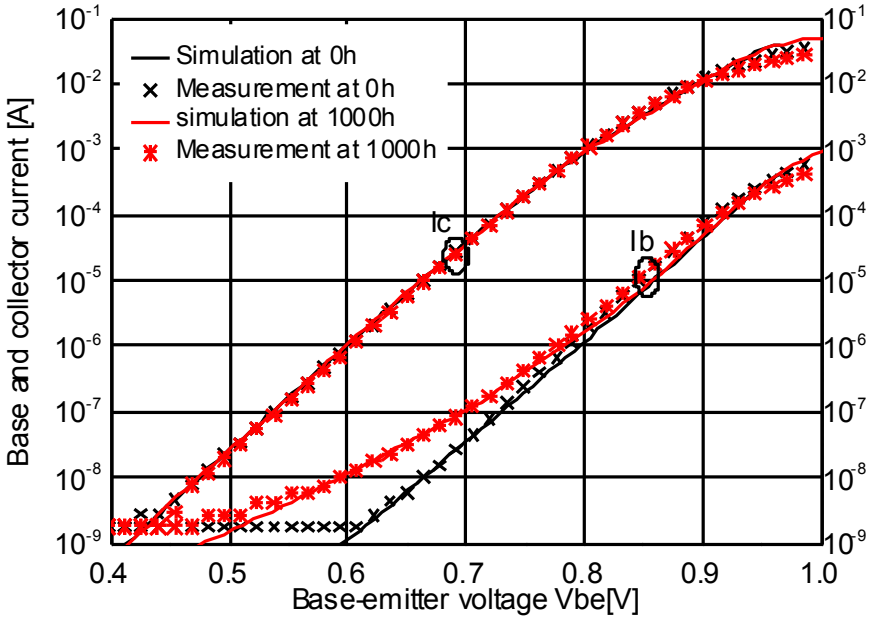
- Same conditions as P3 bias point





Comparison: aging tests vs simulation results

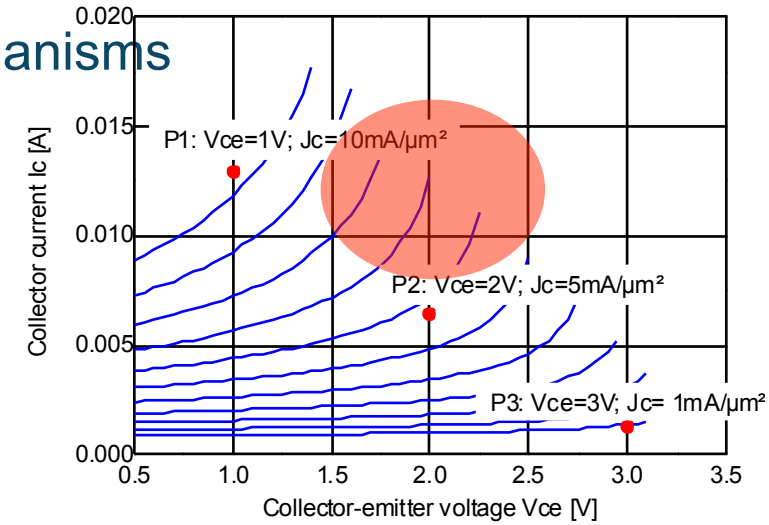
- Impact on performances
  - Excellent agreement
  - < 1% time increase compared with HiCuM without aging law



Jacquet et al., ''Reliability of high-speed SiGe:C HBT under electrical stress close to the SOA limit'', Microelectronics Reliability 55(9-10), pp. 1433-1437 (2015)

Reliability study at circuit level

- Validation of SiGe:C HBT compact model for reliability study at circuit level
  - ✓ Aging tests performed on single finger HBT
  - ✓ Analysis using 2D TCAD simulation (collaboration with UN)
  - ✓ Implantation of HBT failure laws into the compact model (HiCUM)
- Further investigations on HBT failure mechanisms
  - ➢ Self heating impact
- Targeted SiGe:C HBT Circuits
  - Power Amplifier (PA)
  - Low-Noise Amplifier (LNA)
  - Voltage Controlled Oscillator (VCO)



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