Reliability aware circuit design
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SiGe-THz devices:
Physics and reliability
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Outline

• Context:
  • Impact of dimensions shrinking on device operation margins
  • Impact of device operation margins on the device failure mechanisms
• From device to circuit reliability
  • Circuit aging simulation: Why?
  • Circuit aging simulation: How?
    • Conventional way of doing
    • IMS proposal for circuit aging simulation
• A study case: InP Bipolar Submicron devices for robust design of 112Gb/s optical transport network
• DOTSEVEN SiGe HBT technology
  • Operation
  • Aging tests results
  • Aging laws implementation in HiCUM model
  • Towards the evaluation of reliability at circuit level
SiGe HBT basics: device architecture

- $W_E \times L_E = 0.13 \times 2.69 \mu m^2$
- $f_T = 300$ GHz
- $f_{MAX} = 500$ GHz
- $J_C (\text{peak } f_T) = 17$ mA/$\mu m^2$
- $BV_{CEO} = 1.5$ V

DOTSEVEN SiGe HBTs: Performances

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>Infineon/IHP joint flow</th>
<th>IHP ref. *)</th>
<th>Infineon ref. **)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td></td>
<td>DPSA-SEG with EBL</td>
<td>DPSA-SEG without EBL</td>
<td></td>
</tr>
<tr>
<td>Layout</td>
<td></td>
<td>BEBC BEC</td>
<td>BEC</td>
<td>BEC</td>
</tr>
<tr>
<td>$W_e \times L_e$</td>
<td>$\mu m^2$</td>
<td>0.13x2.7</td>
<td>0.155x1.0</td>
<td>0.13x2.69</td>
</tr>
<tr>
<td>$f_T$</td>
<td>GHz</td>
<td>300 305</td>
<td>320</td>
<td>240</td>
</tr>
<tr>
<td>$f_{max}$</td>
<td>GHz</td>
<td>500 465</td>
<td>445</td>
<td>380</td>
</tr>
<tr>
<td>$j_c$ (peak $f_T$)</td>
<td>mA/$\mu m^2$</td>
<td>17</td>
<td>16</td>
<td>10</td>
</tr>
<tr>
<td>$BV_{CEO}$</td>
<td>V</td>
<td>1.5</td>
<td>1.75</td>
<td>1.5</td>
</tr>
<tr>
<td>$BV_{CEO}$</td>
<td>V</td>
<td>4.8</td>
<td>4.1</td>
<td>5.5</td>
</tr>
<tr>
<td>$BV_{CEO}$</td>
<td>V</td>
<td>1.5</td>
<td>1.35</td>
<td>2.3</td>
</tr>
<tr>
<td>($R_B + R_E$) $\times L_e$</td>
<td>$\Omega \times \mu m$</td>
<td>46 51</td>
<td>52 86</td>
<td></td>
</tr>
<tr>
<td>$C_{GB}/L_e$</td>
<td>fF/$\mu m$</td>
<td>1.45 1.4</td>
<td>2.2 1.3</td>
<td></td>
</tr>
<tr>
<td>$C_{BE}/L_e$</td>
<td>fF/$\mu m$</td>
<td>2.1 1.9</td>
<td>2.4 2.1</td>
<td></td>
</tr>
<tr>
<td>$R_{SBI}$</td>
<td>$K\Omega$</td>
<td>3.0</td>
<td>2.6 2.6</td>
<td></td>
</tr>
</tbody>
</table>

SiGe HBT basics: performances and scaling

- Device performance is improved through reduction in transit time and parasitic resistances and capacitances.
- $f_T$ improvement is achieved through improvement in each of the delay components, related to $f_T$ in the well-established approximation:

$$\frac{1}{2\pi f_T} = \tau_{EC} + \tau_E + \tau_C + \tau_B + \tau_{CSCL} \approx \frac{kT}{qI_C} C_{EB} + \left( \frac{kT}{qI_C} + R_C + R_E \right) C_{CB} + \frac{W_B^2}{\gamma D_n} + \frac{W_{CSCL}}{2v_{SAT}}$$

- $f_T$ is probably the most common figure of merit for an RF transistor. However, in many cases the $f_{MAX}$ figure of merit is more predictive for circuit performance.

$$f_{MAX} \approx \sqrt{\frac{f_T}{8\pi R_B C_{CB}}}$$
SiGe HBT basics: performances and scaling

Segmentation into stored minority charges and depletion charges:

- Minority holes in emitter:
  \[
  \frac{1}{2\pi f_T} = \tau_E + \tau_C + \tau_B + \tau_{BC} + \tau_{EB}
  \]
  \[
  \tau_E = q \int_{0}^{x_{mE}} \frac{\partial p}{\partial j_c} \, dx
  \]
  \[
  \tau_B = q \int_{x_{mC}}^{x_{mE}} \frac{\partial n}{\partial j_c} \, dx
  \]

- Minority electrons in base:
  \[
  \tau_C = q \int_{x_{mC}}^{L_z} \frac{\partial p}{\partial j_c} \, dx
  \]
  \[
  \tau_{EB} = q \int_{x_{mE}}^{x_{mC}} \frac{\partial (n - p)}{\partial j_c} \, dx
  \]

- Minority holes in collector:
  \[
  \tau_{BC} = q \int_{x_{mC}}^{L_z} \frac{\partial (n - p)}{\partial j_c} \, dx
  \]

- EB depletion charge:

SiGe HBT basics: device epitaxial structure

Measured doping profile of a first-generation SiGe HBT from IBM

Impact of dimensions shrinking on HBT structure

- SiGe HBT device scaling

<table>
<thead>
<tr>
<th></th>
<th>Emitter</th>
<th>Base</th>
<th>Collector</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Structure</strong></td>
<td>Replace Arsenic with Phos. Reduce interface layer</td>
<td>Narrow base Reduce base dose Increase Ge ramp Add Carbon Improve extrinsic structure</td>
<td>Increase concentration Improve extrinsic structure</td>
</tr>
<tr>
<td><strong>Electrical</strong></td>
<td>Lower $R_E$, Higher $I_B$</td>
<td>Lower $V_{BE}$ Reduce total $R_B$</td>
<td>Higher avalanche Higher peak $f_T$ Higher $C_{CB}$</td>
</tr>
</tbody>
</table>

Greg Freeman et al., "Reliability and performance scaling of very high speed SiGe HBTs", Microelectronics Reliability 44, pp397–410, 2004
Effect of collector design

- (a) peak $f_T$ current density
- (b) excess collector and base current from avalanche in the collector–base space-charge region.

Greg Freeman et al., "Reliability and performance scaling of very high speed SiGe HBTs", Microelectronics Reliability, 44, pp397–410, 2004
### Bipolar reliability overview and performance trend related issues

<table>
<thead>
<tr>
<th>Operation region</th>
<th>Stress condition $V_{BE}$ $V_{BC}$</th>
<th>Typical signature</th>
<th>Mechanism</th>
<th>Stress condition in typical circuit?</th>
<th>Trend with scaling</th>
<th>Remedy</th>
<th>Refs.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reverse</td>
<td>$-$</td>
<td>Low bias $I_B$ non-ideality</td>
<td>E-B oxide interface states</td>
<td>Limited</td>
<td>Neutral</td>
<td>Limit reverse voltage in design</td>
<td>[19–21]</td>
</tr>
<tr>
<td>Saturation</td>
<td>$+$</td>
<td>Low bias $I_B$ non-ideality</td>
<td>E-B oxide interface states</td>
<td>Limited</td>
<td>Neutral</td>
<td>Limit saturation voltage in design</td>
<td>[22]</td>
</tr>
<tr>
<td>Forward mode</td>
<td>$+$</td>
<td>Low bias $I_B$ non-ideality, parallel $I_B$ shift, $R_E$ shift, self-heating</td>
<td>E-B oxide interface states, poly-sc interface oxide, metal migration</td>
<td>Yes</td>
<td>Worse</td>
<td>Min. interface oxide, min. e-fields at surface, narrow $W_E$</td>
<td>[22–30]</td>
</tr>
<tr>
<td>Avalanche</td>
<td>$+$</td>
<td>Low bias $I_B$ non-ideality, self-heating</td>
<td>E-B oxide interface states</td>
<td>Yes</td>
<td>Worse</td>
<td>Design robust to $I_B$ variations, limit voltage in design</td>
<td>[33–35]</td>
</tr>
</tbody>
</table>

Avalanche effect on device operation

- (a) low $V_{CB}$
- (b) moderate avalanche
- (c) “pinch-in” resulting from high voltage drop across base resistance
Hot carrier generation from avalanche and trapping in dielectric layers

Avalanche generated base current degradation for 200 GHz SiGe HBT

- Emitter area: $0.12 \times 2.0 \, \mu m^2$.
- Stress conditions: $V_{CB}=2.5 \, V$, $I_E=1.92 \, mA$.
- Before aging and after 8.3 h under the stress

Greg Freeman et al., "Reliability and performance scaling of very high speed SiGe HBTs", Microelectronics Reliability, 44, pp397–410, 2004
Safe Operating Area : SOA

- Safe Operating Area
- High-performances HBT $f_T/f_{MAX} = 250/300$ GHz
- Common base configuration
- Forced $J_E$ output characteristics
- Breakdown voltages:
  - $BV_{CE0} = 1.7V$
  - $BV_{CB0} = 5.0V$

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From device to circuit reliability

- How to predict the circuit reliability during the design?
- Key points:
  - Taking into account mission profile (including signals)
  - Taking into account the circuit/transistor interaction
  - Relevance of electrical stress
- Device ageing test objective: wear out mechanisms
Aging circuit simulation: why?

Design time scale: weeks

Design | Validation (simulation) | Reliability simulation | Prototype | Electrical Tests | Reliability Tests | Production

Correction loop

Prototype time scale: months

Correction loop

Design For Reliability:

✓ Predict during the design phase the effect of transistors and architecture choices on the circuit reliability according to the application
Effect of circuit operation on each transistor stress

Operationnal amplifier

Vgs (V)

Vgs (V)

Vds (V)

V_{DD}=5V

V_T

100 years
10 years
1 year
1 month
1 week
1 day
6 hours
1 hour

Courtesy of François Marc (IMS)
Circuit reliability simulation

Simulations to predict the impact of transistor failure mechanisms on the circuit operation:

- life time
- electrical parameters
- outputs evolution

As a function of operating conditions:

- environment: temperature, pressure, radiations ...
- supply voltages
- Input signals

➤ Circuit Aging simulation
Conventional approach: Design in Reliability (DiR)

- **Model card Library**
  - Conditions: Bias, Temperature, Time, AC, DC, ...

  
  
  simulator ➔ Stress computation ➔ Aged model card library

- **DiR model flow highlights interactions between simulator, stress computation program and model cards.**

  S. Ighilahriz et al., "Reliability study under DC stress on mmW LNA, Mixer and VCO", IEEE International Reliability Physics Symposium (IRPS), 2012
Design in Reliability (DiR): an iterative method

2 software's associated through an iterative method

- A dedicated software has to be developed
Circuit aging simulation: IMS approach

A single simulator (with VHDL-AMS or Verilog-A)

- **Circuit netlist**
- **Ageing models**

**Simulator**
- **VHDL-AMS**
- **Outputs**
- **Modified parameters of transistors**

**Transistor aging model**
- Based on the transistor compact model
- Takes into account the aging models/laws/failure mechanisms (providing they are known)
- Need to access to model code
Requirements for circuit aging simulation

- Use VHDL-AMS or Verilog-A to build compact models including aging
  - Compact model code
  - Add physical quantities in the compact model
  - Implementation of the aging laws in the compact model
    - Physics of failure
    - Ageing tests @ transistor level
  - Change compact model parameters into (slowly) variable quantities
    - Parameters extraction of the failure laws

- Virtual acceleration of degradation mechanism to obtain electrical times (<1 second) and ageing time (> 1 week) in a same simulation

➤ Versatility and efficiency for ageing simulation
Benefits of a “real-time” dynamic aging model

- Directly integrated in CAD commercial software tools
  - in PDK to ease the circuit designer handling
  - can be realized easily in VerilogA language

- Use compact model with slowly varying parameters as a function of bias and temperature
  - under real circuit operating conditions

- Small performance penalty
  - compiled code
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A study case: InP Bipolar Submicron devices for robust design of 112 Gb/s optical transport network

This methodology is not process specific

- Alcatel Lucent
  - InP/InGaAs HBT technology

- Challenging applications
  - High speed optical communications systems working above 100 Gbit/s per channel

- Very high reliability requirements
  - e.g., submarine communication systems

- Accurate reliability modeling is mandatory

$$f_T$$ and $$f_{MAX}$$ are around 350 GHz

- 0.5x7 µm²

- InGaAs
- InP
InP HBT technologies

• In general, less complicated implementation than Si technologies
  ➢ Two metal levels
  ➢ Triple mesa process technology
  ➢ Mesa isolation

• Suffer from important self heating mechanism


Courtesy of Mohammed Zaknoune (IEMN)
**HiCuM compact model**

Why choosing HiCuM L2 v2.30 compact model?

- CMC labeled model (Available in most commercial simulators)
- VerilogA code available
- HiCuM accuracy + Specific improvements of version v2.30
- Modeling of advanced HBTs

➢ Parameter extraction for good initial model is already challenging
INITIAL parameter extraction: DC operation

Results for T7 ($W_E=0.5\mu m$ and $L_E=7\mu m$)
Initial parameter extraction: Dynamic operation

Results for T7 ($W_E=0.5\mu m$ and $L_E=7\mu m$)
Aging tests results

- Extensive aging tests campaign ($J_C$, $V_{CE}$, $T_J$)
- Moderate $I_C$ variation
  - increase @ low level injection
  - decrease @ high level injection
- Important $I_B$ increase
  - @ low level injection
Extensive 2D/3D Calibrated TCAD Hydrodynamic simulations

- Donor traps at E-B junction surroundings are responsible for the current variations
- Trap concentration increase linearly with stress time

Aging laws parameters

- Trap density is not a compact model parameter
  - need diode saturation currents

\[
i_{jBEi} = I_{BEiS} \left[ \exp\left( \frac{v_{BEi}'}{m_{BEi}V_T} \right) - 1 \right] + I_{REiS} \left[ \exp\left( \frac{v_{BEi}'}{m_{REi}V_T} \right) - 1 \right]
\]

\[
i_{Tf} = \frac{I_S}{Q_{p,T}/Q_{p0}} \left[ \exp\left( \frac{v_{BE}'}{V_T} \right) - \exp\left( \frac{v_{BC}'}{V_T} \right) \right]
\]

- \( I_S \) and \( I_{BEIS} \) are extracted from post stress measurements
- \( I_S \) and \( I_{BEIS} \) follow the same variation as traps density according to aging time
- \( I_S \) and \( I_{BEIS} \) can be used as variables of the aging model
Aging laws implementation

- Donor trap density can be modeled as a generation mechanism
  ✓ Same holds for $I_{\text{BEis}}$ and $I_S$

  \[
  \frac{dN_{\text{trap}}(t)}{dt} = G(T, J_C)
  \]

  \[
  \frac{dI_{\text{BEis}}(t)}{dt} = A_{\text{IBEIS}}(T, J_C)
  \]

  \[
  \frac{dI_S(t)}{dt} = A_{IS}(T, J_C)
  \]

- Constant increasing rates follow an Arrhenius law

  \[
  A_{\text{IBEIS}}(T, J_C) = B_{\text{IBEIS}} \left( \exp \left( \frac{-E_{\text{IBEIS}}}{k_B T} \right) \right) J_C^{\alpha_{\text{IBEIS}}}
  \]

  \[
  A_{IS}(T, J_C) = B_{IS} \left( \exp \left( \frac{-E_{IS}}{k_B T} \right) \right) J_C^{\alpha_{IS}}
  \]

- $B_{\text{IBEIS}}, E_{\text{IBEIS}}, B_{IS}, E_{IS}$ are new model parameters
Aging laws evolution

- Parameter extraction of $I_S$ and $I_{BEIS}$
  - @ different bias point P2, P3, P4
  - For the three HBT sizes: T5, T7, T10
- Extraction of generation rates
  - $A_{IS}$ and $A_{IBEIS}$
  - $A_{IS}$ and $A_{IBEIS}$ follow an Arrhenius law
    - $E_{IBEIS} = 1.34$ eV
    - $E_{IS} = 1.5$ eV
VerilogA implementation in HiCuM Model

\[ \frac{dI_{BEIS}(t)}{dt} = A_{IBEIS}(T, J_C) \]

[\( C=1 \)]

\[ \frac{dI_{S}(t)}{dt} = A_{IS}(T, J_C) \]

[\( C=1 \)]
Indepth into code description

module hic2_full_XDK (c,b,e,s,tnode, 
ibveis_out, is_out);
...
branch (ibeis_out) br_ibeisout 
branch (is_out) br_isout;

ibeis = V(br_ibeisout) +ibeis0;
ise = V(br_isout) +is0;

aibeis = bibeis*exp(-eibeis/(`P_K/`P_Q)*Tdev)) *pow( jc , alpha1);
ais = bis*exp(-eis/(`P_K/`P_Q)*Tdev)) *pow( jc , alpha2);

l(br_ibeisout) <+ -aibeis;
l(br_ibeisout) <+ ddt(V(br_ibeisout));
l(br_isout) <+ -ais;
l(br_isout) <+ ddt(V(br_isout));

New nodes and branch
Update model parameters: new nodes voltage represent degradation
Temp & Jc dependencies
Branch equations
Indepth into Code description

```verilog
module hic2_full_XDK (c,b,e,s,tnode, ibeis_out, is_out);
...
branch (ibeis_out) br_ibeisout
branch (is_out) br_isout;

ibeis = V(br_ibeisout) +ibeis0;
is = V(br_isout) +is0;

aibeis = bibeis*exp(-eibeis/(`P_K/`P_Q)*Tdev))
ais = bis*exp(-eis/(`P_K/`P_Q)*Tdev)) *pow( jc ,alpha1);  
     *pow( jc ,alpha2);

l(br_ibeisout) <= -atsf * aibeis;
l(br_ibeisout) <= ddt(V(br_ibeisout));
l(br_isout) <= -atsf * ais;
l(br_isout) <= ddt(V(br_isout));
```

Simulation of degradations is too slow: 10000 years of CPU time !!!

ATSF : Accelerating Time Scale Factor
new parameter

ATSF=3.6E13    100ns → 1000 h
ATSF=3.15E15 100ns → 10 years
Validation @ transistor level

- Verification on base current
  - monitored during ageing – 1000 h
- Transistor T7 (0.5x7µm²)
- Bias condition P4

➤ Compact model is accurate at transistor level
@ Circuit level: Transimpedance Amplifier (TIA)

- Featuring complex offset compensation loop

Diagram showing the circuit with labels for
- Transimpedance input stage
- Cherry-Hooper amplifier
- Differential amplifier
- 50-Ω output buffer
- Reference voltage
- External capacitor
- Low frequency (~DC) offset compensation amplifier
- Low pass filter
- Input and output nodes
- Peaking element
- V_TIA
- V_REF
- V_CC
- R_FB
- R_C

The diagram illustrates the circuit components and their connections at the circuit level.
TIA description

• 2 versions of the TIA available for aging tests
  ✓ TLIA (high DC gain – low cutoff frequency)
  ✓ TIA-HF (lower DC gain – Higher bandwidth)
• 22 circuits samples submitted to accelerated aging test for 1008 hours
• Chuck temperature = 70°C
• $T_j$ up 125°C
TLIA S parameters measured up to 65GHz

- Measurements versus simulations
- Perl scripting is used to automate ”aged” circuit simulation
- Software : Agilent ADS
  - Excellent initial model
  - Slightly pessimistic aging
  - But fairly accurate predictions

• ATSF=36x10^{12} (100\text{ns}=10\text{years})
• Temperature=100°C
• Dynamic observation of all circuit nodes
  ✓ Differential output voltage (S-Sb)
• Circuit instances can be extracted at any time step
Steady state @ selected time step: run AC simulation with aged parameters
Using a script to generate “alter” statements gathered in a include file

Alter:AGINGalter0 var="I182.I395.Q1.AGED_RE0" VarValue=1.051097526541248e+00
Alter:AGINGalter1 var="I182.I395.Q1.AGED_IS0" VarValue=2.296752299864880e-05
Alter:AGINGalter2 var="I182.I395.Q1.AGED_IBEIS0" VarValue=2.720339978065819e-02
Alter:AGINGalter4 var="I182.I414.Q1.AGED_IS0" VarValue=2.477855478244199e-03
Alter:AGINGalter5 var="I182.I414.Q1.AGED_IBEIS0" VarValue=1.822901099996015e+00
Alter:AGINGalter7 var="I182.I407.Q1.AGED_IS0" VarValue=1.003050582649662e-04
Alter:AGINGalter8 var="I182.I407.Q1.AGED_IBEIS0" VarValue=1.021350703026095e-01
Alter:AGINGalter10 var="I182.I408.Q1.AGED_IS0" VarValue=8.399430332061722e-05

TLIA Transient simulation
Circuit element parameter during simulated aging time

A transient simulations using Cadence SPECTRE
IBEIS [pA]

Input stage: Transimpedance input stage

Cherry-Hooper amplifier

Differential amplifier

50-Ω output buffer

Low frequency (~DC) offset compensation amplifier

Low pass filter

External capacitor

Reference voltage

V_{CC}

R_{FB}

R_C

L_{peaking}

Differential output

INPUT

OUTPUT

voltage

R_{C}

R_{FB}
Reliability aware design example

- No DC offset compensation loop

✓ VREF is constant over aging time
Reliability aware design example

- DC offset compensation loop with small gain

☑ VREF can’t follow VTIA over aging time
Reliability aware design example

- DC offset compensation loop with high gain

- VREF follows VTIA over aging time thanks to higher loop gain
Conclusion: Augmented compact model for reliability-aware circuit design

- New method for device dynamic reliability simulation
- Straightforward initial implementation in software design simulators (VerilogA): Available in a standard PDK (easy to adopt)
- Simulates complex interactions between stress conditions (bias/temperature) and device characteristics evolution
- Physics based methodology
- Validated at transistor level (InP/InGaAs HBT process)
- Validated at circuit level (24 transistors TIA – working above 100GHZ and using a complex offset compensation loops)
- Allows reliability aware circuit design
- Shortens circuit reliability improvement feedback loops
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Infineon SiGe:C HBT technology

- Test structure: GSG configuration
  - Emitter and substrate connected to ground pad

- CBEBC Configuration
  - Single emitter finger
  - Emitter size of 0.2x10µm²

- SiGe:C NPN transistor
  - $F_t/F_{max} = 240/380\text{GHz}$
  - $BV_{ceo} = 1.5\text{V}$
Device under test: DC characterization

- Measurement vs. HIC U.M.
- Current Gain ($\beta$)
- $A_{\text{area}} = 1 \times 0.11 \times 9.93 \, \mu\text{m}^2$
- $V_{\text{BE}} = 0.6 \, \text{to} \, 0.9 \, \text{V} \, (\text{in step of} \, 0.05 \, \text{V})$
- $I_{\text{B}} = 0.5 \, \text{to} \, 10 \, \mu\text{A} \, (\text{in step of} \, 0.95 \, \mu\text{A})$

- $I_C, I_B \, (A)$
- $V_{\text{BE}}, V_{\text{CE}} \, (V)$
Aging test campaigns

• Requirements: to identify wear out mechanisms
  • Slowly evolving with time
  • At the edge of the Safe Operating Area

• Long-time stress tests (i.e. 1000 h)
  • Stress tests and measurements realized using encapsulated devices
  • Samples biased in a common-emitter configuration at constant and controlled ambient temperature of 300K.

• Evolution characterization
  • DC characterization is performed at fixed time of 1h, 3h, 7h, 24h, 36h, 48h, 72h, 120h, 250h, 500h, 750h and 1000h.
  • At 300h, an additional point is added with 24h between the end of the stress test and the measurement ➔ Evaluation of recovery mechanism
  • Base-emitter junction characterization: forward Gummel plot at $V_{bc}=0V$
  • Base-collector junction characterization: Reverse Gummel plot at $V_{be}=0V$
### Aging test campaigns: Bias conditions

<table>
<thead>
<tr>
<th>Size</th>
<th>We (µm)</th>
<th>Le (µm)</th>
<th>P1</th>
<th>P2</th>
<th>P3</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Vce= 1V</td>
<td>Vce= 2V</td>
<td>Vce= 3V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Jc=10mA/µm²</td>
<td>Jc=5mA/µm²</td>
<td>Jc=1mA/µm²</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>Ic (mA)</td>
<td>Ic (mA)</td>
<td>Ic (mA)</td>
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<tr>
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<td>1</td>
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<td>0.6</td>
<td>0.29</td>
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<tr>
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<td>2.8</td>
<td>3.55</td>
<td>1.75</td>
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</tr>
<tr>
<td>Size 3</td>
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<td>10</td>
<td>12.91</td>
<td>6.46</td>
<td>1.29</td>
</tr>
</tbody>
</table>
Aging tests description

- Emitter common configuration
  - Vce fixed
  - Ic forward control
  - Ib monitoring

- Bias conditions:
  - Wear out mechanisms
  - SOA edge
    - 1 bias point below BVceo
    - 2 bias points above BVceo
    - 6 HBT per bias conditions

- Aging time up to 1000h

![Graph showing Collector current Ic vs Collector-emitter voltage Vce](image)
Test bench description
Aging tests results

Base and collector current $[A]$ vs. Base-emitter voltage $V_{be} [V]$
Aging tests results analysis @P1

P1: Vce=1V; Jc=10mA/µm²

\[ \Delta I_b(t) = I_b(t) - I_b(0) \]

Collector current Ic [A]

Collector-emitter voltage Vce [V]

P1: Vce=1V; Jc=10mA/µm²
P2: Vce=2V; Jc=5mA/µm²
P3: Vce=3V; Jc=1mA/µm²
Aging tests results analysis @P2

P2: Vce=2V; Jc=5mA/µm²

\[ \Delta I_b(t) = I_b(t) - I_b(0) \]

Aging time [h]

\[ \Delta I_b(t) @ V_{be}=0.65V \]

Collector-emitter voltage Vce [V]

Collector current Ic [A]

P1: Vce=1V; Jc=10mA/µm²

P2: Vce=2V; Jc=5mA/µm²

P3: Vce=3V; Jc=1mA/µm²
Aging tests results analysis @P3

P3: V_{ce}=3\,V; J_{c}=1\,mA/\mu m^2

\Delta I_b(t) @ V_{be}=0.65\,V

\Delta I_b(t) = I_b(t) - I_b(0)

Aging time [h]

Collector current I_c [A]

Collector-emitter voltage V_{ce} [V]

P1: V_{ce}=1\,V; J_{c}=10\,mA/\mu m^2

P2: V_{ce}=2\,V; J_{c}=5\,mA/\mu m^2

P3: V_{ce}=3\,V; J_{c}=1\,mA/\mu m^2
Aging mechanism analysis

- High Vce (>BVceo)
- Electrons accelerate in BC space region
- Creation of electron-hole pairs (Impact ionization)
- Hot carriers injected in E-B spacer
- Carriers break dangling bond *
- Increase of trap density

Trap density simulation

- Uniform acceptor type trap density
  - Trap energy level: $E_T - E_V = 0.6 \text{ eV}$

Si$_3$ $\equiv$ SiH $+ h^+$ $\rightarrow$ Si $\equiv$ Si $\cdot$ $+H^+$

Si$_3$ $\equiv$ SiOH $+ h^+$ $\rightarrow$ Si $\equiv$ SiO $\cdot$ $+H^+$

Schroder et al., “Negative bias temperature instability: Road to cross in deep submicron silicon semiconductor manufacturing”, J. Appl. Phys. 94(1), 2003
At each stress time, extraction of trap density

Evolution of trap density

\[ N_T(t) = N_{T_{\text{final}}} - (N_{T_{\text{init}}} - N_{T_{\text{final}}}) \exp\left(-\frac{t}{\tau}\right) \]
Compact modeling

- HiCuM compact model L2
  - Version 2.33

- E-B junction periphery
  - Trap location

- $I_{REpS}$ parameter converted as a new variable in HiCuM

$$i_{jBEp} = I_{BEpS} \left[ \exp \left( \frac{v_{BE}}{m_{BEp} V_T} \right) - 1 \right] + I_{REpS} \left[ \exp \left( \frac{v_{BE}}{m_{REp} V_T} \right) - 1 \right]$$

$$I_{REpS} = I_{REpS, final} + (I_{REpS, initial} - I_{REpS, final}) \exp \left( -\frac{t}{\tau} \right)$$
Evolution of $I_{REpS}$

$$\frac{dI_{REpS}}{dt} = ATSF \cdot (G - R \cdot I_{REpS})$$

- Constant recombination rate $R$
  $$R = 3.7 \times 10^{-6} \text{ s}^{-1}$$
- Generation rate $G$
  $$G(I_{avl}) = A \cdot I_{avl} + G_0$$
  
  $A = 7.575 \times 10^{-21} \text{ s}^{-1}$, 
  $$G_0 = 0.75e^{-20} \text{ A} \cdot \text{s}^{-1}$$

- Accelerating factor ATSF, Aging Time Scale Factor
  - Reduce simulation time for convenient time calculation
  - $ATSF$, fixed at $3.6 \times 10^6 : 1000\text{h (aging time)} \leftrightarrow 1\text{s (simulation time)}$
Simulation results

• Same conditions as P3 bias point
Comparison: aging tests vs simulation results

- Impact on performances
  - Excellent agreement
  - < 1% time increase compared with HiCuM without aging law

Reliability study at circuit level

- Validation of SiGe:C HBT compact model for reliability study at circuit level
  - Aging tests performed on single finger HBT
  - Analysis using 2D TCAD simulation (collaboration with UN)
  - Implantation of HBT failure laws into the compact model (HiCUM)

- Further investigations on HBT failure mechanisms
  - Self heating impact

- Targeted SiGe:C HBT Circuits
  - Power Amplifier (PA)
  - Low-Noise Amplifier (LNA)
  - Voltage Controlled Oscillator (VCO)

![Graph showing collector current and collector-emitter voltage relationship.]

- P1: $V_{ce}=1V, J_c=10\text{mA/\mu m}^2$
- P2: $V_{ce}=2V, J_c=5\text{mA/\mu m}^2$
- P3: $V_{ce}=3V, J_c=1\text{mA/\mu m}^2$
Acknowledgement

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